Course on CMOS Data Converters for Communications

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A Sigma-Delta modulator design example: From specs to measurements

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MIXMODEST

Mixed-Signal Design Cluster

OUTLINE

- Solution of a design exercise and practical considerations on the selection of:
  - **Architecture**
  - **Reference voltages**
  - **Integrator weights**
  - **Oversampling ratio**
  - **Sampling capacitors**
  - **Opamp DC-gain**
  - **Comparator hysteresis**
  - **Integrator and comparator dynamics**
  - **Switches**
  - **Component non-linearity**
- Simulating ΣΔ modulators
- Circuit-level design
- Layout for mixed-signal performance
- From layout to measurements
- Measurements

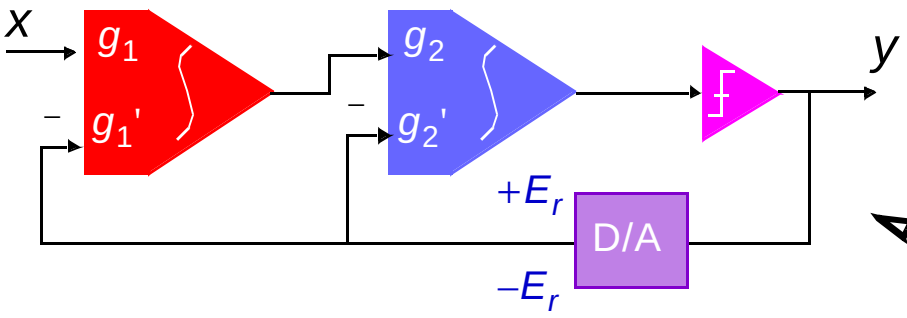
- **Modulator specifications:**
  - **Effective resolution: 17bit**
  - **Signal Bandwidth: 4.8kHz**
  - **Maximum input signal: 2Vpp**
  - **Minimum power consumption**

$$FOM = \frac{\text{Power(W)}}{2^{\text{resolution(bit)}} \times DOR(\text{S/s})} \times 10^{12}\text{pJ}$$

[Goodenough ED'96]

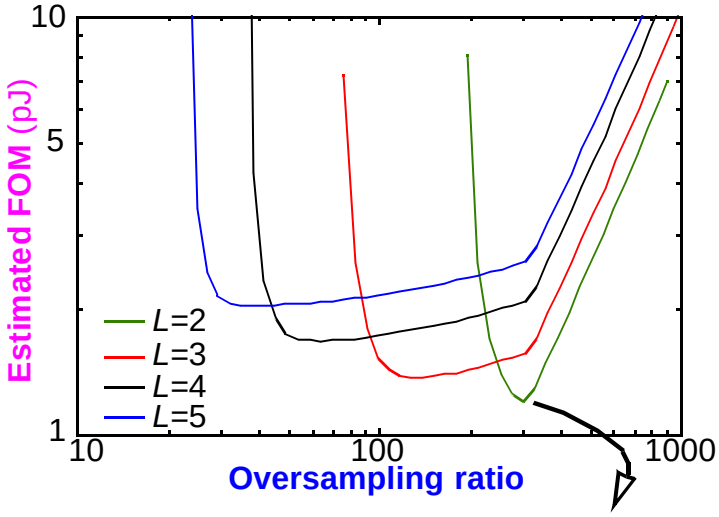
Intended technology: 5-V 0.7μm CMOS

2nd-order ΣΔ Modulator



[Candy, Trans. Comm. 85]

Architecture selection *[Medeiro, Kluwer98]*



Minimum: 2nd-order ΔΣM with *M* ~ 300

- **When resolution is high**
  - **In-band error power dominated by other error sources than quantization (for instance, thermal noise)**
  - **Asume that $P_{error} = P_Q + P_{th}$**

X_{FS} = modulator full scale L = modulator order

$$P_Q = \frac{X_{FS}^2}{12} \cdot \frac{\pi^{2L}}{(2L+1)M^{(2L+1)}}$$

M = oversampling ratio

$$P_{th} \cong kT/(MC_s)$$

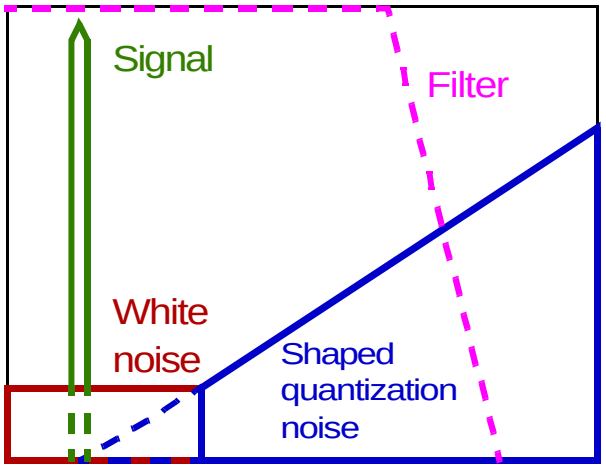
C_s = sampling cap.

$$DR(X_{FS}, L, M, C_s) \cong \frac{(X_{FS}/2)^2/2}{\frac{X_{FS}^2}{12} \cdot \frac{\pi^{2L}}{(2L+1)M^{(2L+1)}} + kT/(MC_s)}$$

$$N_{eff} = \frac{DR|_{dB} - 1.76}{6.02} \text{ in bits}$$

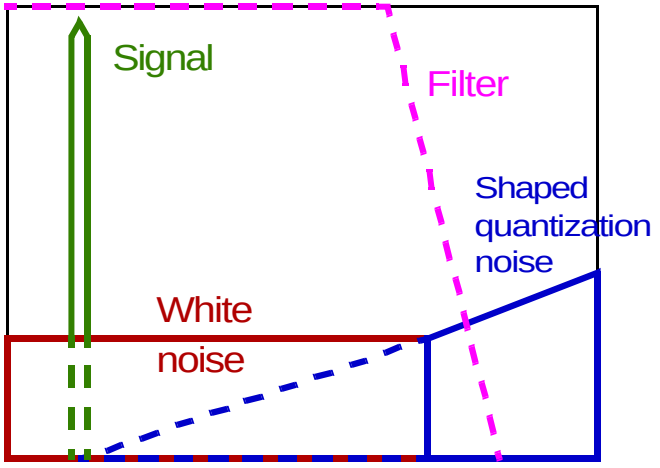
- The larger X_{FS}, the better, but it is limited by output swing and dynamic requirements

- **If quantization error dominates**



$$DR \cong DR(X_{FS}, L, M, C_s)$$

- **If white noise dominates**



$$DR \cong DR(X_{FS}, M, C_s)$$

***DR* does not depend on modulator order**

$$P_Q = \frac{X_{FS}^2}{12} \cdot \frac{\pi^4}{5M^5}$$

$$\Delta P_Q(A_V) = \frac{X_{FS}^2}{12} \cdot \frac{(g_1 + g_2 + g_2')^2}{A_v^2} \cdot \frac{\pi^2}{3M^3}$$

$$\Delta P_Q(h) = 4h^2 \cdot \frac{\pi^4}{5M^5}$$

} → Quantization error power

$$P_{samp} = \frac{X_{FS}^2}{9M}\left(1 + \frac{C_p}{C_o}\right)^2\left(\frac{C_{I_1}}{C_{eq,1}}\right)^2 \exp\left(-\frac{g_m}{C_{eq,1}}\frac{1}{f_S}\right)$$

$$P_{int} = \frac{X_{FS}^2}{9M}\left(1 + \frac{C_p}{C_s}\right)^2\left(\frac{C_s}{C_{eq,2}}\right)^2\left(1 + \frac{C_{I_2}}{C_o}\right)^2 \exp\left(-\frac{g_m}{C_{eq,2}}\frac{1}{f_S}\right)$$

$$P_{sw} = \frac{X_{FS}^2}{9M}\left(\frac{C_s}{C_o}\right)^2 \exp\left(-\frac{1}{2r_{on}C_s f_S}\right)$$

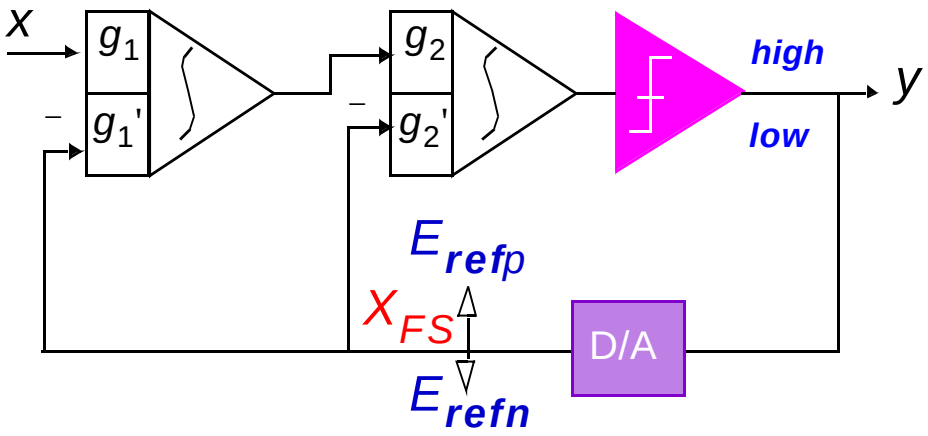
} → Settling error power

$$P_{th} = \frac{kT}{2MC_s} + \frac{kT}{M(C_s + C_p)}\left(\frac{1}{3} + g_m r_{on}\right)$$

→ Thermal noise power

• • • → Distortion, jitter noise ...

⇨ ***How to select the reference voltages?***



⇨ ***Input Full-Scale,*** $X_{FS} = E_{refp} - E_{refn}$

$(X_{FS} = 2E_{ref})$ ***for symmetrical references***

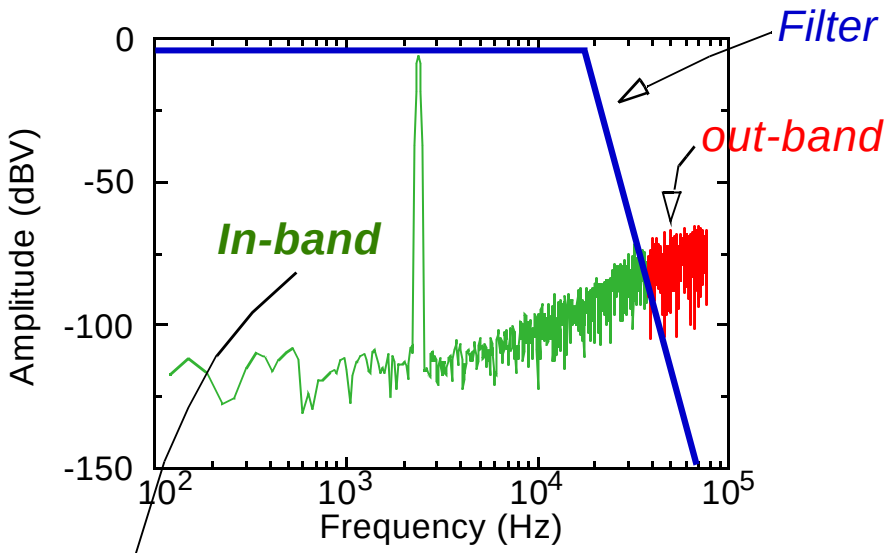
⇨ ***Specification: Max. signal = 2Vpp***

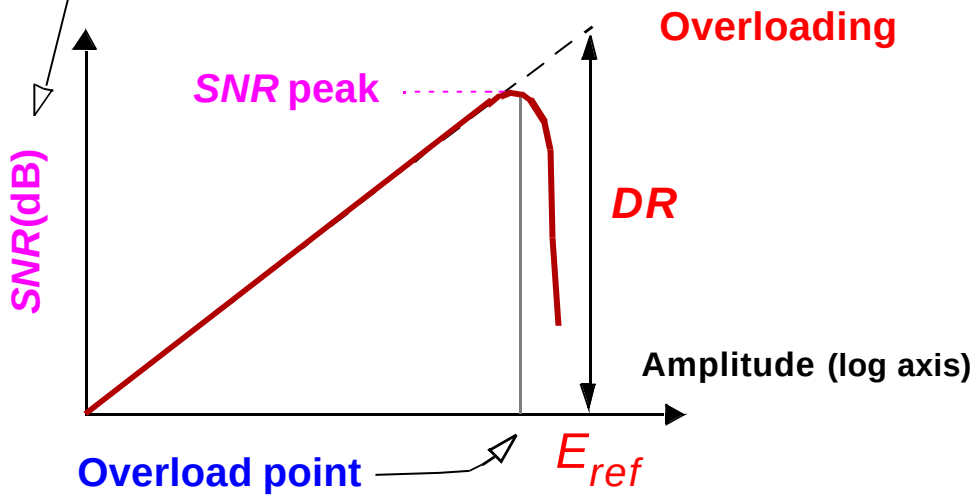
If

$E_{ref} = 1.5V,\ X_{FS} = 3V$

OK

Max. input signal = **80% X_{FS} = 2.4Vpp**

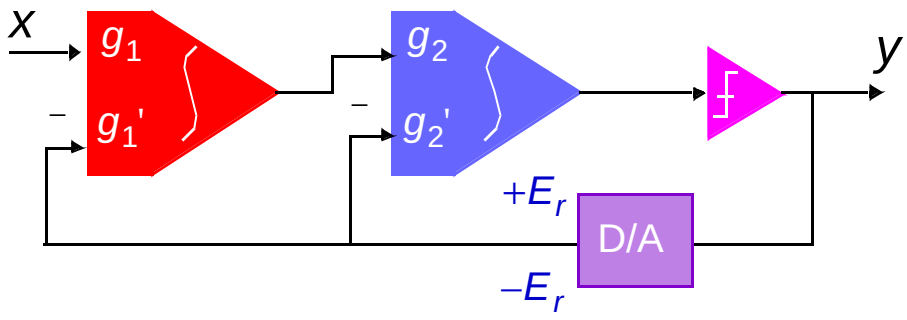




@ **80% E_{ref} for a 2nd-order ΔΣM**

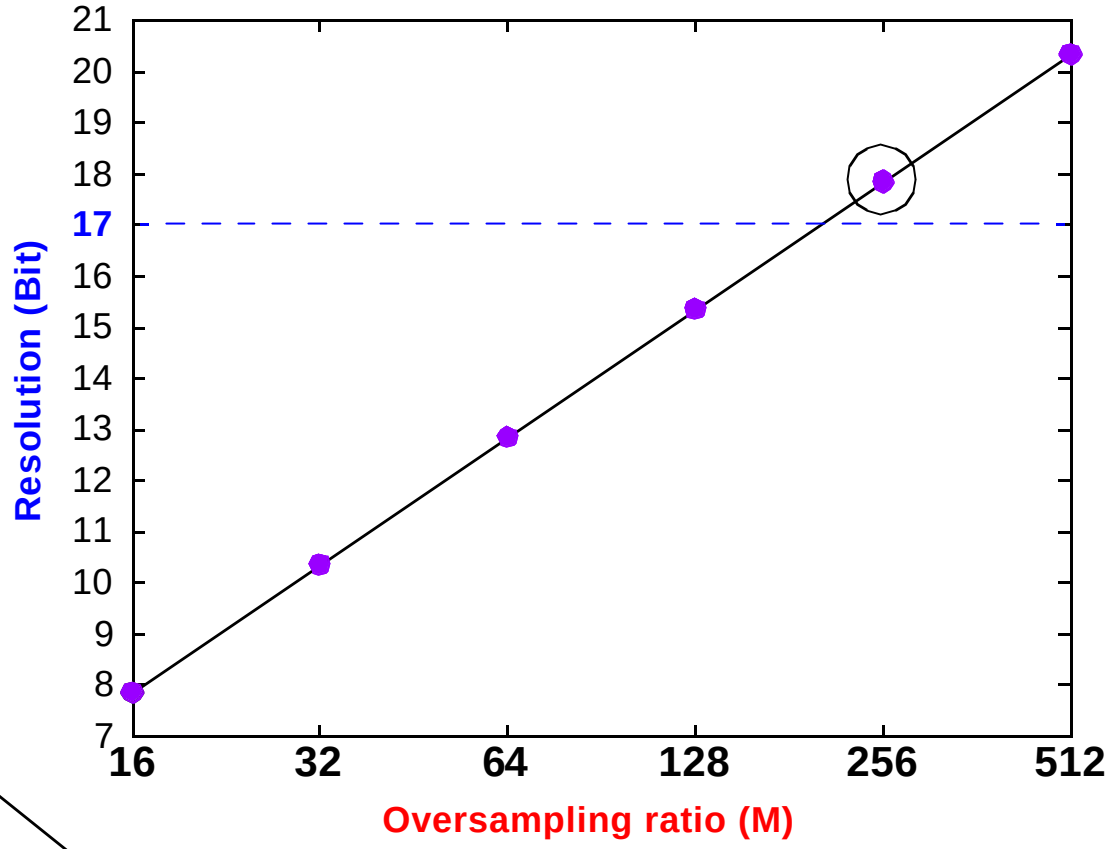
⇨ *Take into account:*

- **Stability of the loop:** $g_2'/(g_1 g_2) > 1.25$
- **Maximum *SNR* peak:**
  - Available integrator output swing
  - Required integrator dynamic
  - SC implementation: size and number of capacitors
  - ...



Weight	Bosse,88	Yin,94	Marques, 97	Medeiro, 98
g_1, g_1'	0.5	0.25	1/3	0.25
g_2	0.5	0.5	0.6	1
g_2'	0.5	0.25	0.4	0.5
Total int. OS / E_{ref}	3.5	2	2.4	2
# unitary caps.	6	10	12	9

- ***For an ideal ΔΣM (Quantization error only)*** → $N_{eff} = \frac{1}{2}\log_2[(2^N - 1)^2 (2L + 1) M^{2L+1} / (\pi^{2L})]$
- ***In our case,*** $N = 1$ $L = 2$
- ***So, M?***
  - **For $M = 128$, $N_{eff} = 15.3$bit**
  - **For $M = 256$, $N_{eff} = 17.8$bit, OK**



$M = 256$

- ***Thus,***

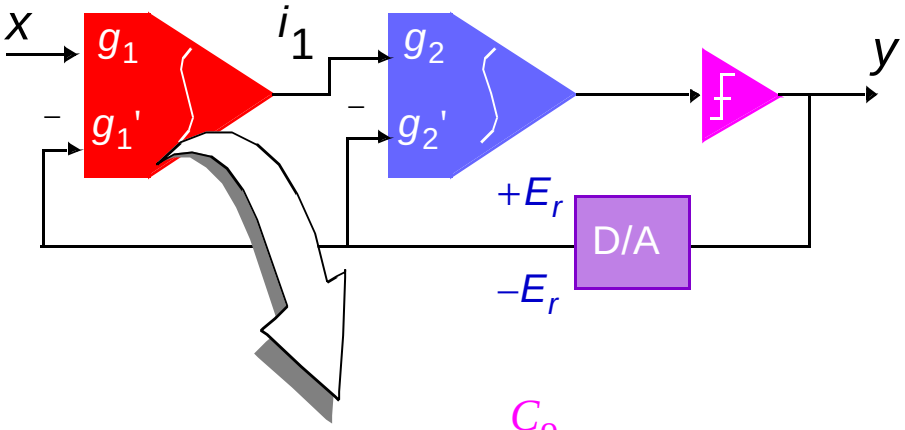
$$P_Q = \frac{X_{FS}^2}{12} \cdot \frac{\pi^4}{5M^5} = -108.8\text{dB}$$

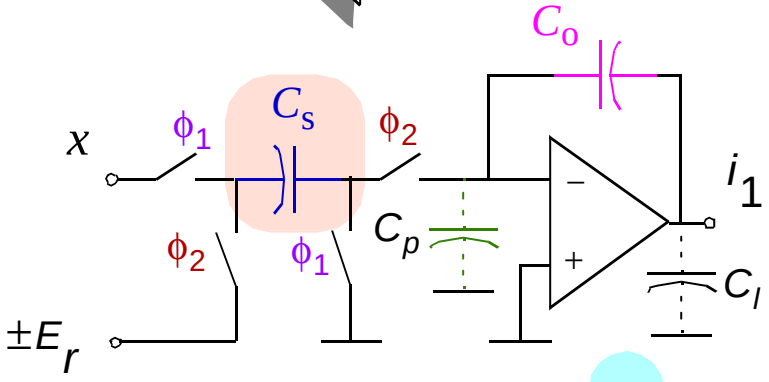
$$DR = \frac{E_{ref}^2/2}{P_Q} = 109.2\text{dB}$$

$$N_{eff} = \frac{DR(\text{dB}) - 1.76}{6.02} = 17.8\text{bit}$$

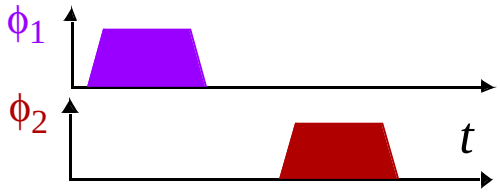
$f_S = 2f_B M = 2.4576$MHz

4.8kHz





$$i_{1,n} = i_{1,n-1} + \frac{C_s}{C_o}(x_{n-1} \pm E_r)$$

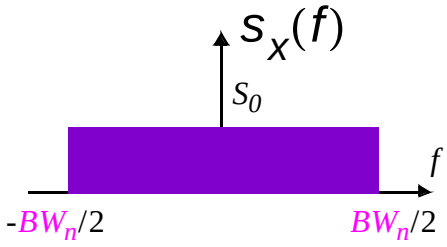


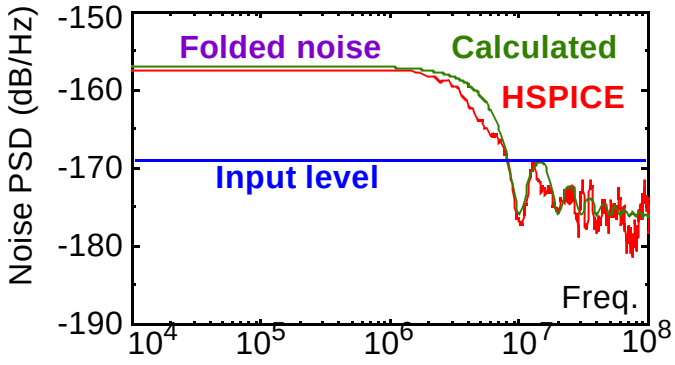
$$g_1 = g_1' = \frac{C_s}{C_o}$$

⇨ ***The choice of C_s is mainly related to:***

- **Thermal noise**
- **Integrator dynamics**

Folded-back noise in a SH circuit





$$P_{th} = \frac{kT}{2MC_s} + \frac{kT}{M(C_s + C_p)}\left(\frac{1}{3} + g_m r_{on}\right)$$

$$\boldsymbol{P_{th} @ kT/(MC_s)}$$

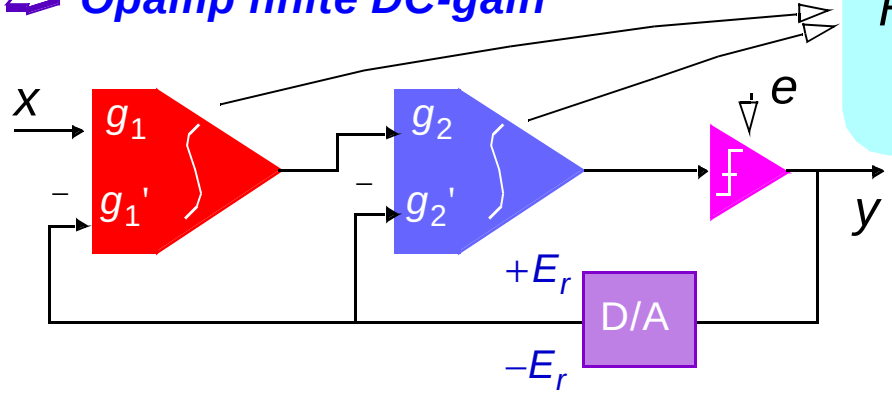
$C_s = 1\text{pF}$

$$DR = \frac{E_{ref}^2/2}{(P_Q + P_{th})} \longrightarrow \textbf{17.3bit} \quad \textbf{OK}$$

-107.9dB

$$C_o = C_s/g_1 = 4\text{pF}$$

Opamp finite DC-gain



$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

Implies infinite DC-gain!

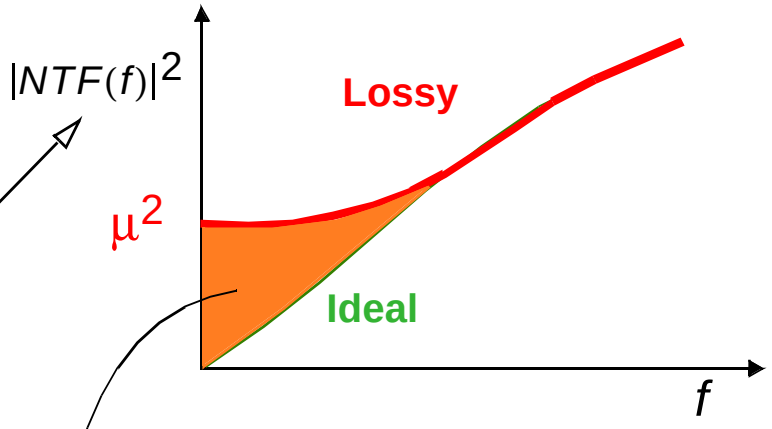
$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z)$$

Not possible in practice

In practice: *"Lossy" integrator*

$$H(z) \overset{A_V \gg 1}{=} \frac{g_1 z^{-1}}{1 - (1 - \mu)z^{-1}} \qquad \mu \approx \frac{1}{A_V}$$

$$Y(z) \cong z^{-2}X(z) + (1 - z^{-1} + \mu z^{-1})^2 E(z)$$

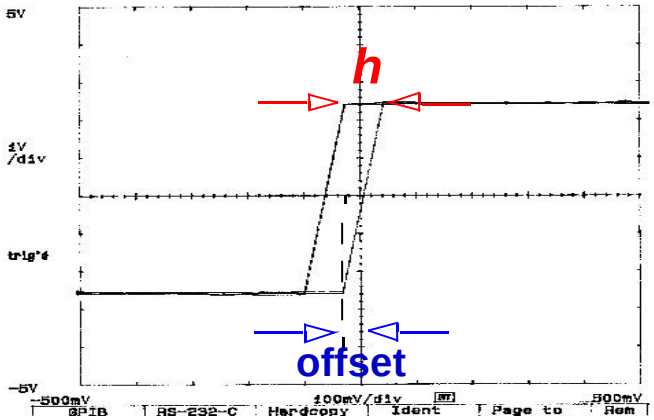


$$\Delta P_Q(A_v) = \frac{X_{FS}^2}{12} \cdot \frac{(g_1 + g_2 + g_2')^2}{A_v^2} \cdot \frac{\pi^2}{3M^3}$$

Quite insensitive to the finite opamp DC-gain

Comparator hysteresis

Hysteresis and offset



Offset

Attenuated by the integrator DC-gain

Hysteresis

$$\Delta P_Q(h) = 4h^2 \cdot \frac{\pi^4}{5M^5}$$

Quite insensitive to hysteresis

We do not need precise comparators

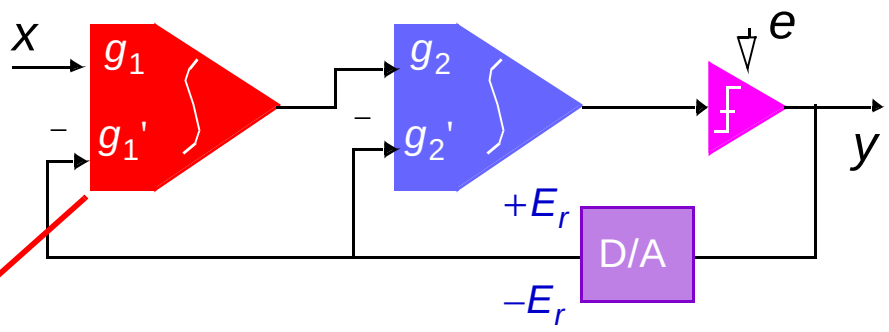
If we set $A_V = 500$ $h = 50\text{mV}$

$$DR = \frac{E_{ref}^2/2}{(P_Q + \Delta P_Q(A_v) + \Delta P_Q(h) + P_{th})} \longrightarrow \textbf{17.2bit OK}$$

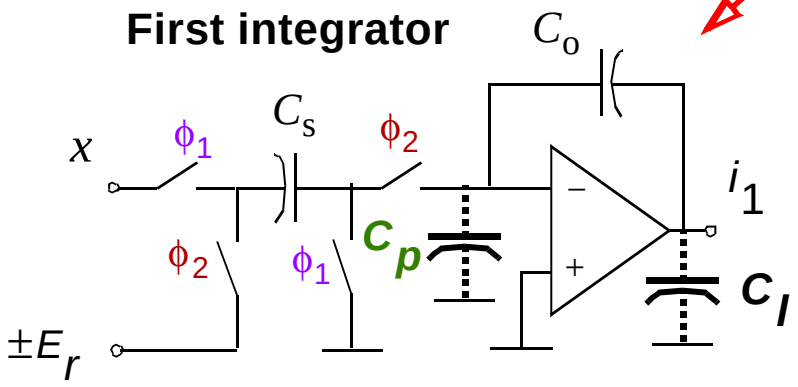
-128.3dB -127.5dB

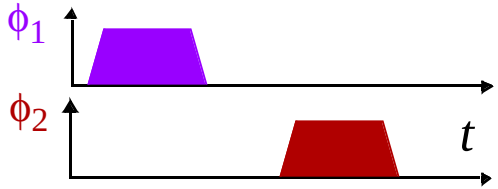
We already set

$C_s = 1pF \quad C_o = 4pF$



First integrator





C_p ?

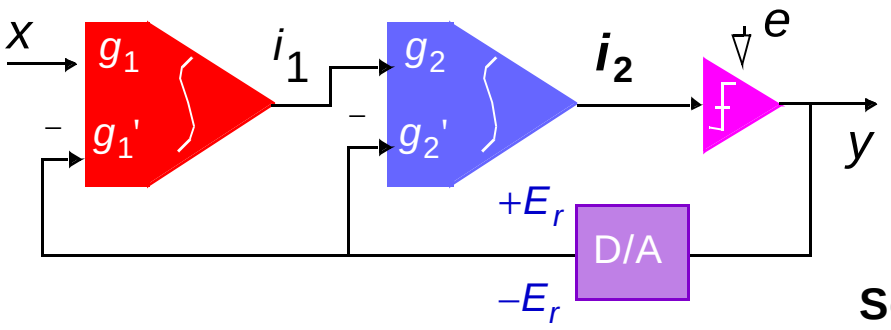
Opamp input parasitic

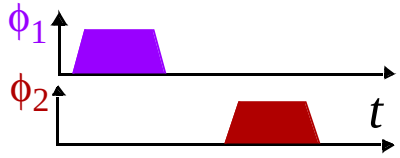
+

$C_p \cong$ Small capacitance (Interconnection, switches)

Depends on the opamp design

An estimation: $C_p = 0.5pF$





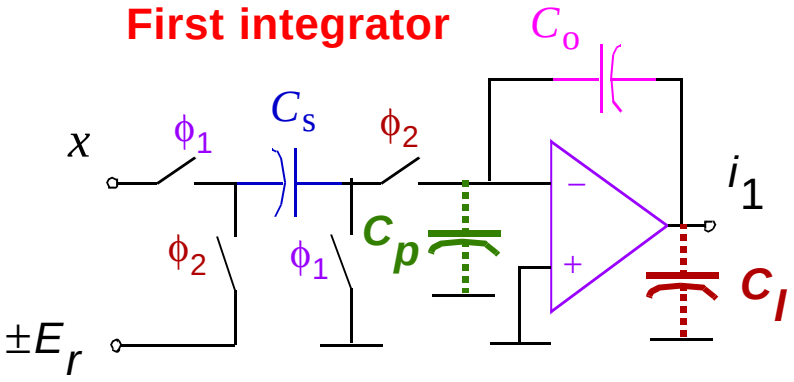
$$C_{s2} = C_{s2}' = 0.5\text{pF}$$

$$C_{o2} = 2\text{pF}$$

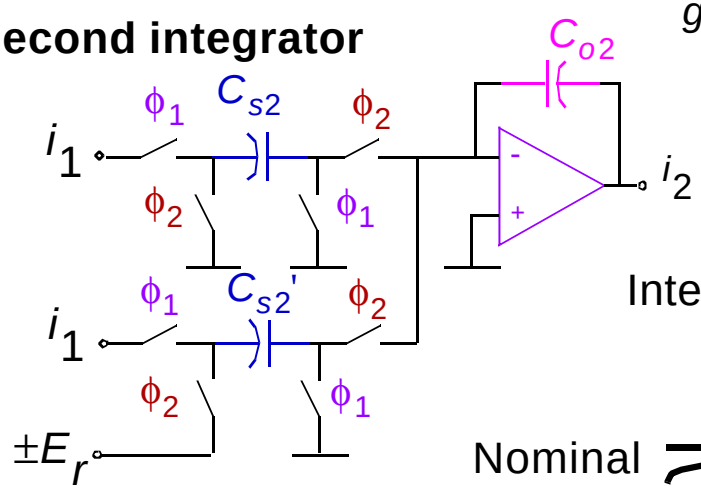
$$g_2 = \frac{C_{s2}}{C_{o2}} + \frac{C_{s2}'}{C_{o2}} = 0.5$$

$$g_2' = \frac{C_{s2}'}{C_{o2}} = 0.25$$

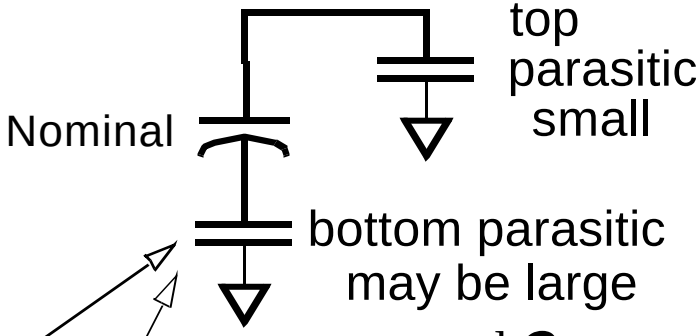
First integrator



Second integrator



Integrated capacitors



ϕ_2

Opamp output parasitic

\+

Bottom parasitic of C_o

⇨ C_I

ϕ_1

Opamp output parasitic

\+

Bottom parasitic of C_o

\+

Next integrator sampling capacitors C_{s2} C_{s2}'

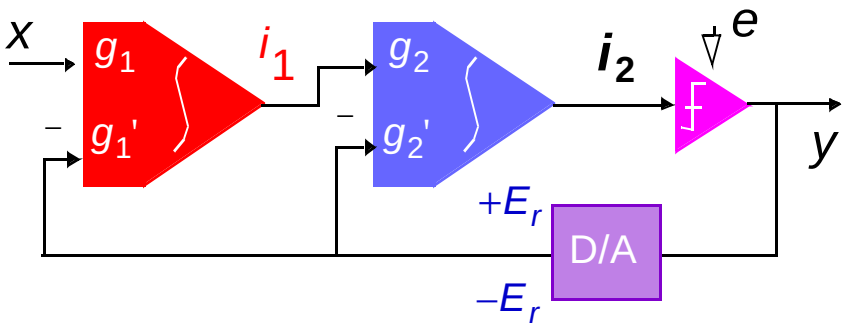
\+

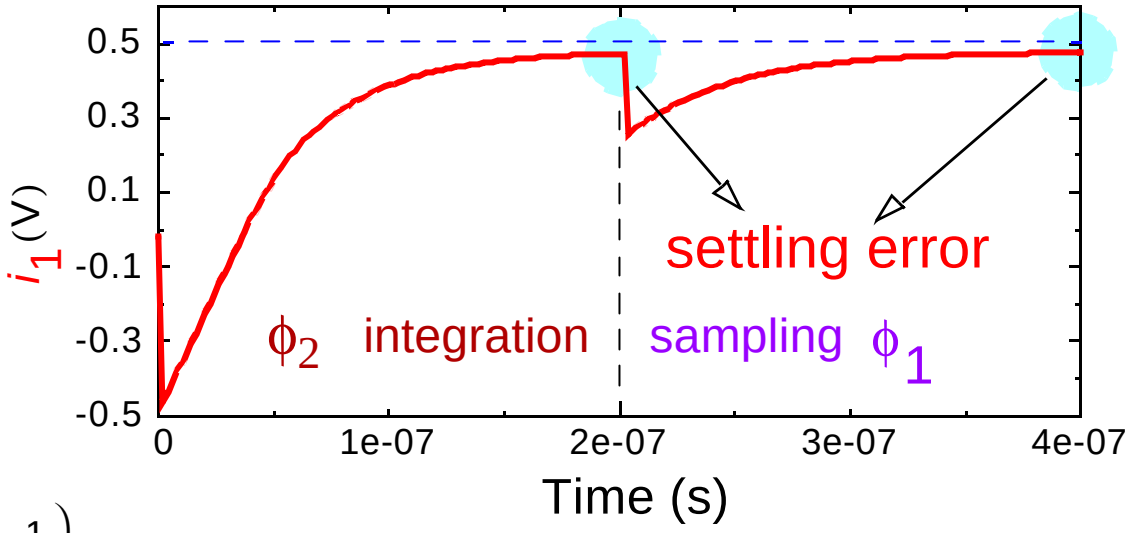
Bottom parasitic of C_{s2} C_{s2}'

C_I

$C_{I1} = 3.5\text{pF}$

$C_{I2} = 2\text{pF}$





$$P_{samp} = \frac{X_{FS}^2}{9M}\left(1+\frac{C_p}{C_o}\right)^2\left(\frac{C_{I_1}}{C_{eq,1}}\right)^2 \exp\left(-\frac{g_m}{C_{eq,1}}\frac{1}{f_S}\right)$$

$$P_{int} = \frac{X_{FS}^2}{9M}\left(1+\frac{C_p}{C_s}\right)^2\left(\frac{C_s}{C_{eq,2}}\right)^2\left(1+\frac{C_{I_2}}{C_o}\right)^2 \exp\left(-\frac{g_m}{C_{eq,2}}\frac{1}{f_S}\right)$$

Valid for linear (no slew-rate) settling, or non-linear (slew-rate) if

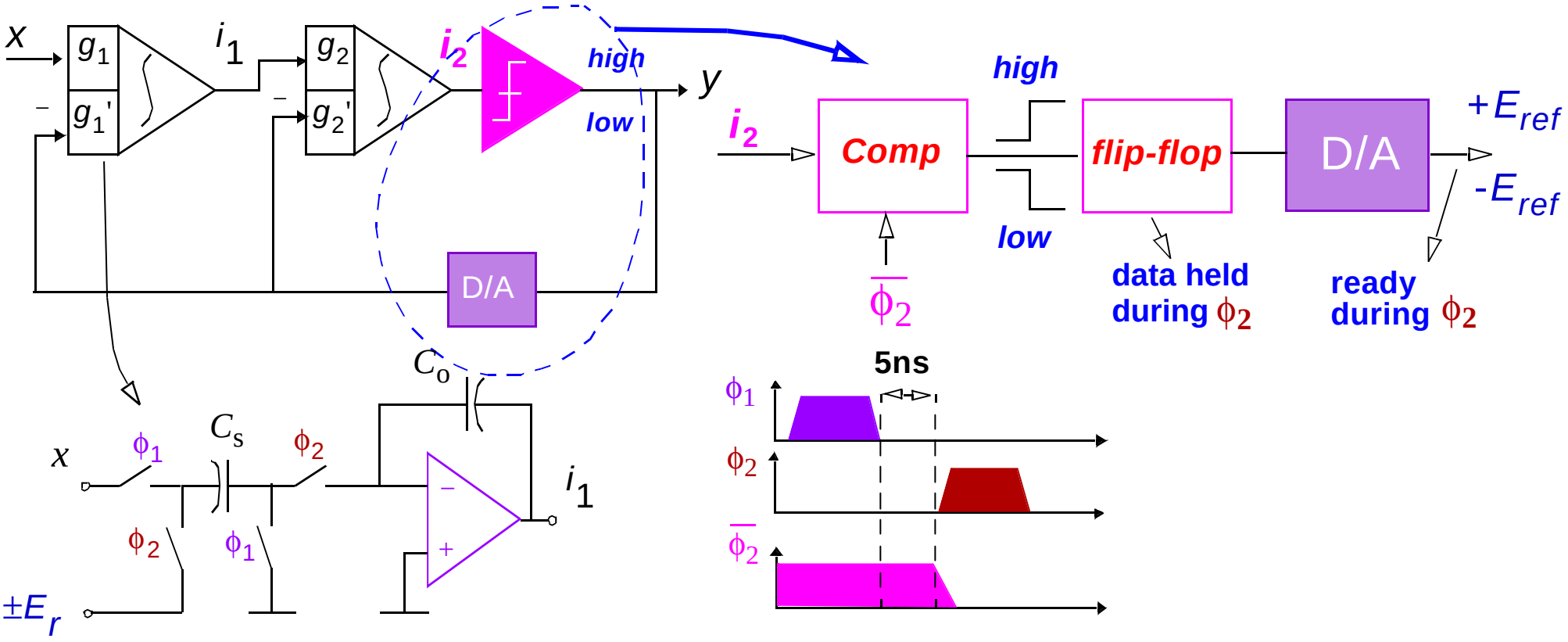
$$I_o = g_m(C_s/C_{eq,2})(1+C_{I_2}/C_o)(X_{FS}/4)$$

$$C_{eq,1} = C_p + C_{I_1}(1+C_p/C_o) = 4.4375\text{pF}$$

$$C_{eq,2} = C_s + C_p + C_{I_2}[1+(C_s+C_p)/C_o] = 4.25\text{pF}$$

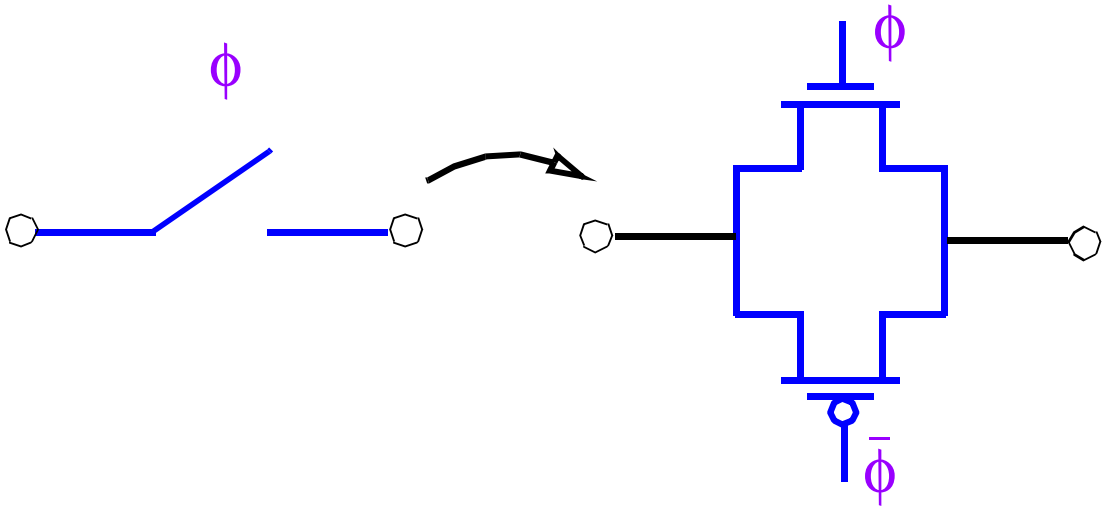
$g_m = 220\mu\text{A/V} \Rightarrow I_o = 58\mu\text{A}$

$$DR = \frac{E_{ref}^2/2}{(P_Q^* + P_{th} + \boldsymbol{P_{samp}} + \boldsymbol{P_{int}})} \rightarrow \textbf{17.1bit} \quad \textbf{OK}$$



- ***The comparator does not have to be very precise (50mV is OK), but it must be fast enough***
- ***Usual choice: to make the comparator resolve in 1/8 of the clock period = 50ns***

Use a latched comparator



ON State

r_{on} 1 0

Thermal noise **Incorrect sampling**

⇨ **Thermal noise**

$$P_{th} = \frac{kT}{2MC_s} + \frac{kT}{M(C_s + C_p)}\left(\frac{1}{3} + g_m r_{on}\right)$$

$r_{on} = 2k\Omega$

$P_{th} = -107.8dB$

Previously, we estimated

$P_{th} = -107.9dB$

⇨ **Incorrect sampling error**

$$P_{sw} = \frac{X_{FS}^2}{9M}\left(\frac{C_s}{C_o}\right)^2 \exp\left(-\frac{1}{2r_{on}C_s f_S}\right)$$

$P_{sw} = -478dB$

$2r_{on}$ x C_s

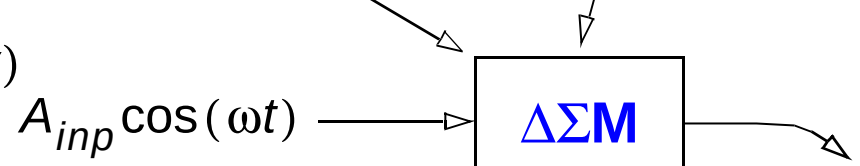
OK

Non-linear capacitors

$$C(v) = C\exp(k_v v) \cong C(1 + k_v v)$$

Voltage coefficient

Weak non-linearity $k_v \ll 1$

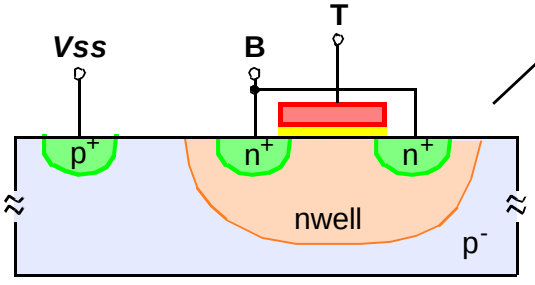


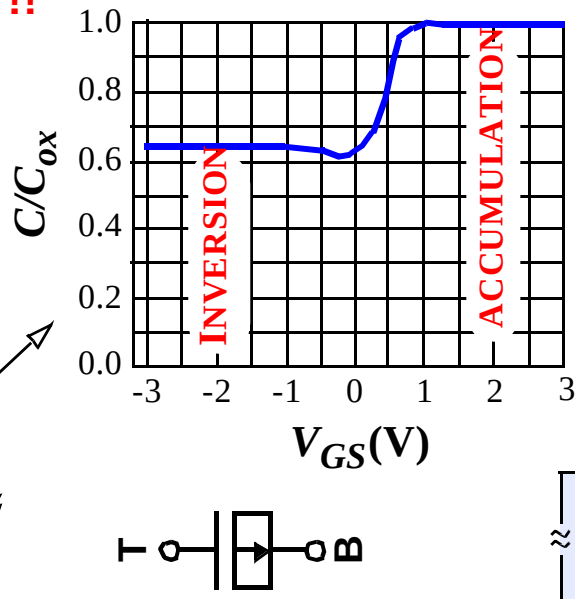
$$P_{cnl} \cong \begin{cases} \frac{1}{8}k_v^2 A_{inp}^4 & \text{Singled-end circuitry} \\ 0 & \text{Fully-differential circuitry} \end{cases}$$

$$+\frac{1}{2}k_v A_{inp}^2 \cos(2\omega t + \varphi_2)$$

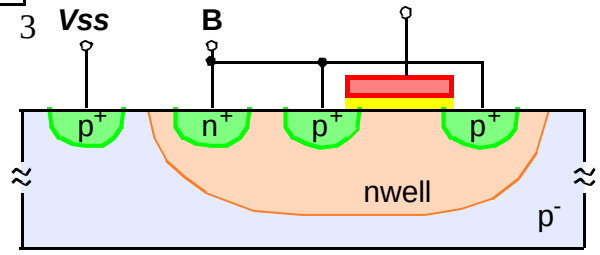
- **Some integrated capacitor are not weakly non-linear!!**

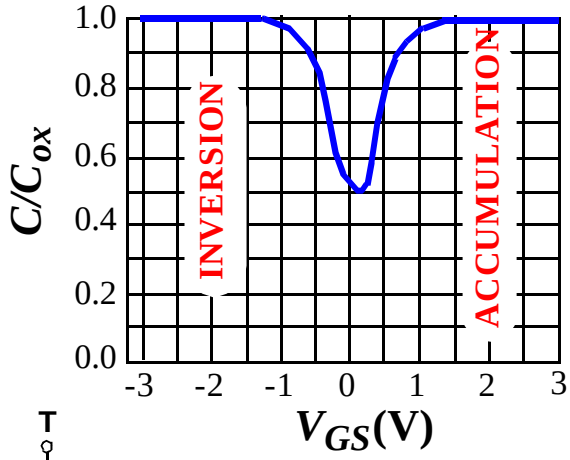
NMOS in NWELL



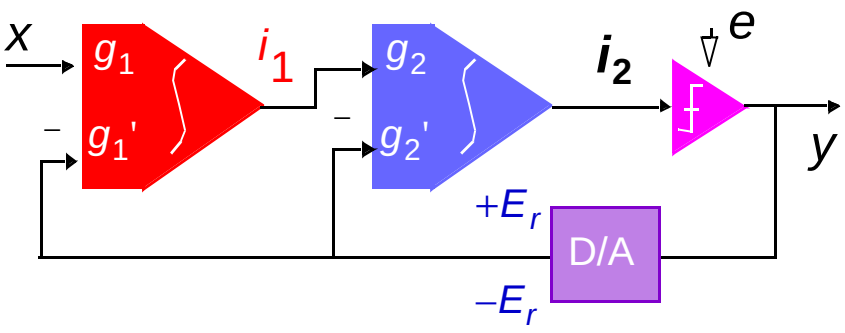


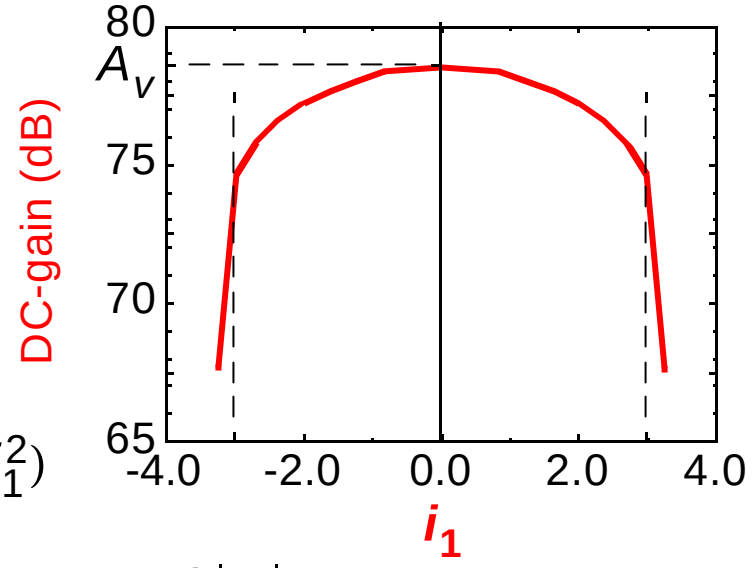
PMOS





Non-linear opamp DC-gain





$$A(i_1) = A_v(1 + \gamma_1 i_1 + \gamma_2 i_1^2)$$

$$A_{inp}\cos(\omega t) \longrightarrow \boxed{\Delta\Sigma M} \longrightarrow \cong A_{inp}\cos(\omega t + \varphi_1) + \frac{2|\gamma_1|}{A_v} g_1^2 A_{inp}^2 \cos(2\omega t + \varphi_2)$$

$$+ \frac{2|\gamma_2|}{A_v} g_1^3 A_{inp}^3 \cos(3\omega t + \varphi_2)$$

- *In fully-differential mode,* $\gamma_1 \ll 1$
- *Remember that* $A_v = 500 \longrightarrow \gamma_2 \leq 5\%$ *to keep resolution above* **17bit**

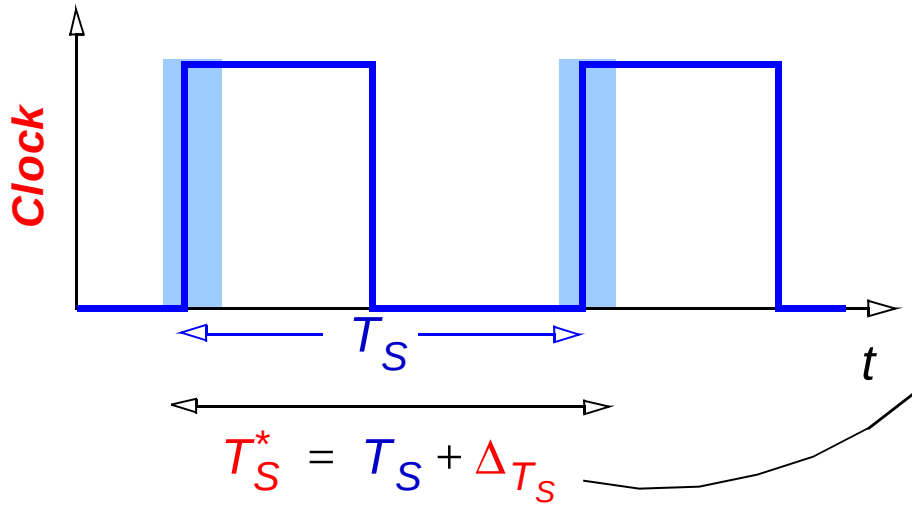
Very demanding !

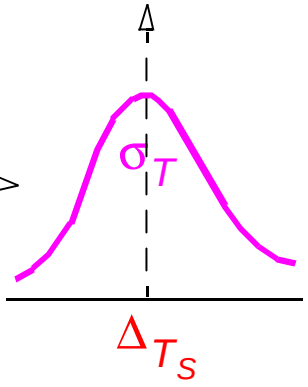
- ***Solution:*** **increase DC-gain**

$A_v = 1000 \longrightarrow \gamma_1 = 1\%,\ \gamma_2 = 10\%$ **OK**

Non-uniform sampling

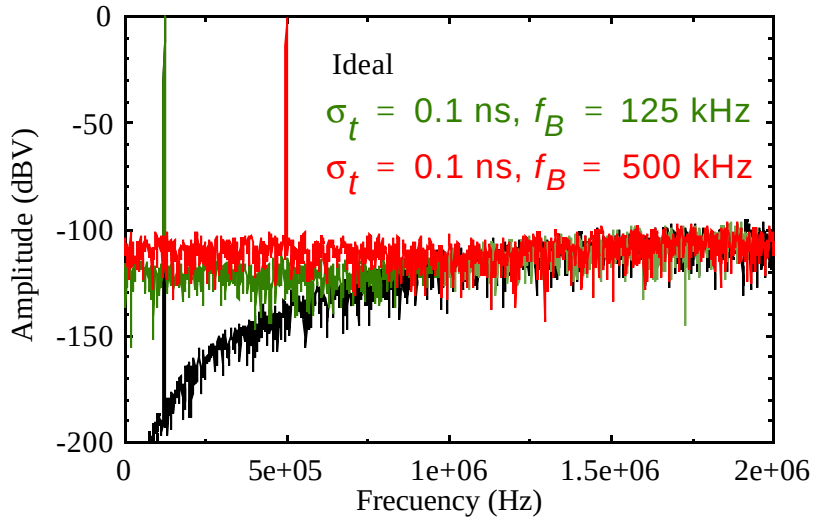
$$T_S = 1/f_S$$





nearly gaussian

$$P_j = \frac{A_{inp}^2}{2}\frac{(2\pi f_B \sigma_T)^2}{M}$$



Example for high-frequency application

$\sigma_T \leq 1$ns

17bit OK

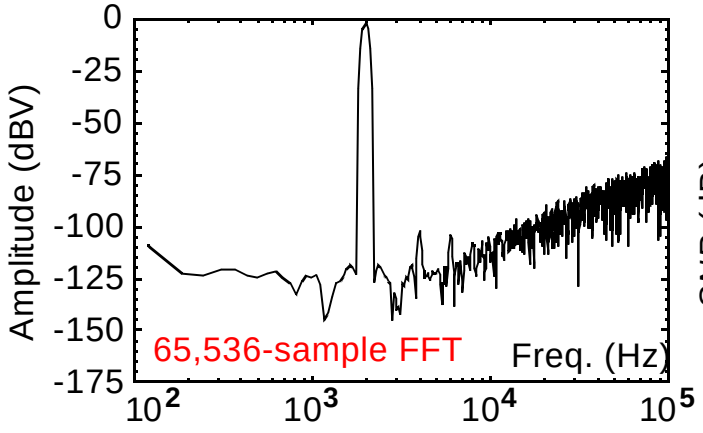
$$DR = \frac{E_{ref}^2/2}{(P_Q^* + P_{th} + \boldsymbol{P_{samp}} + \boldsymbol{P_{int}} + P_{HD} + P_j)}$$

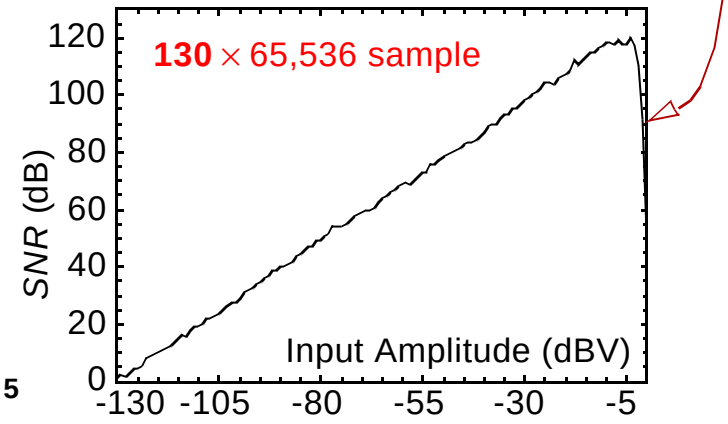
Simulating ΣΔ modulators...

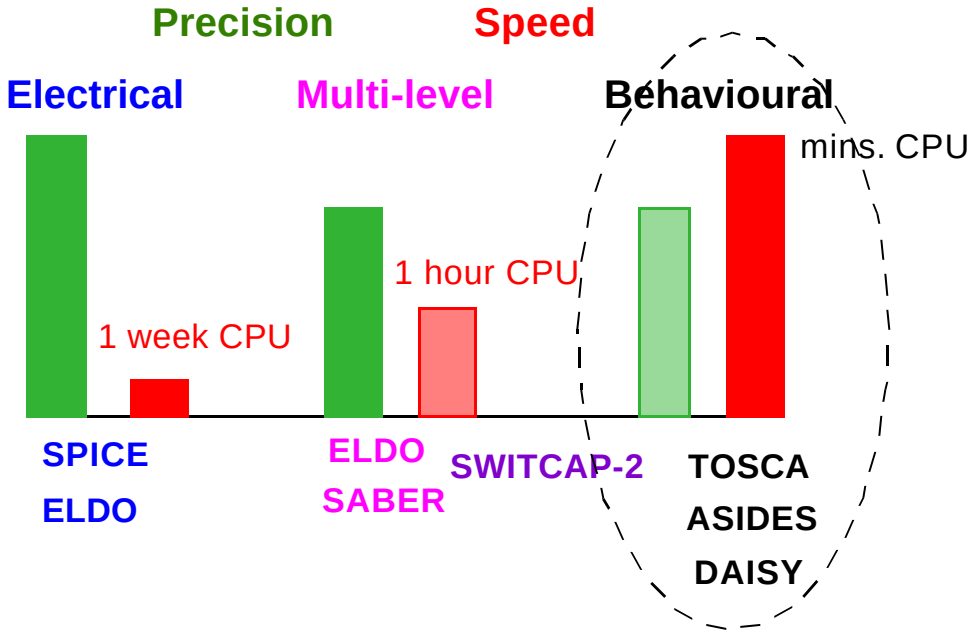
Non-linear operation

Need for time-domain simulation

Lots of samples required



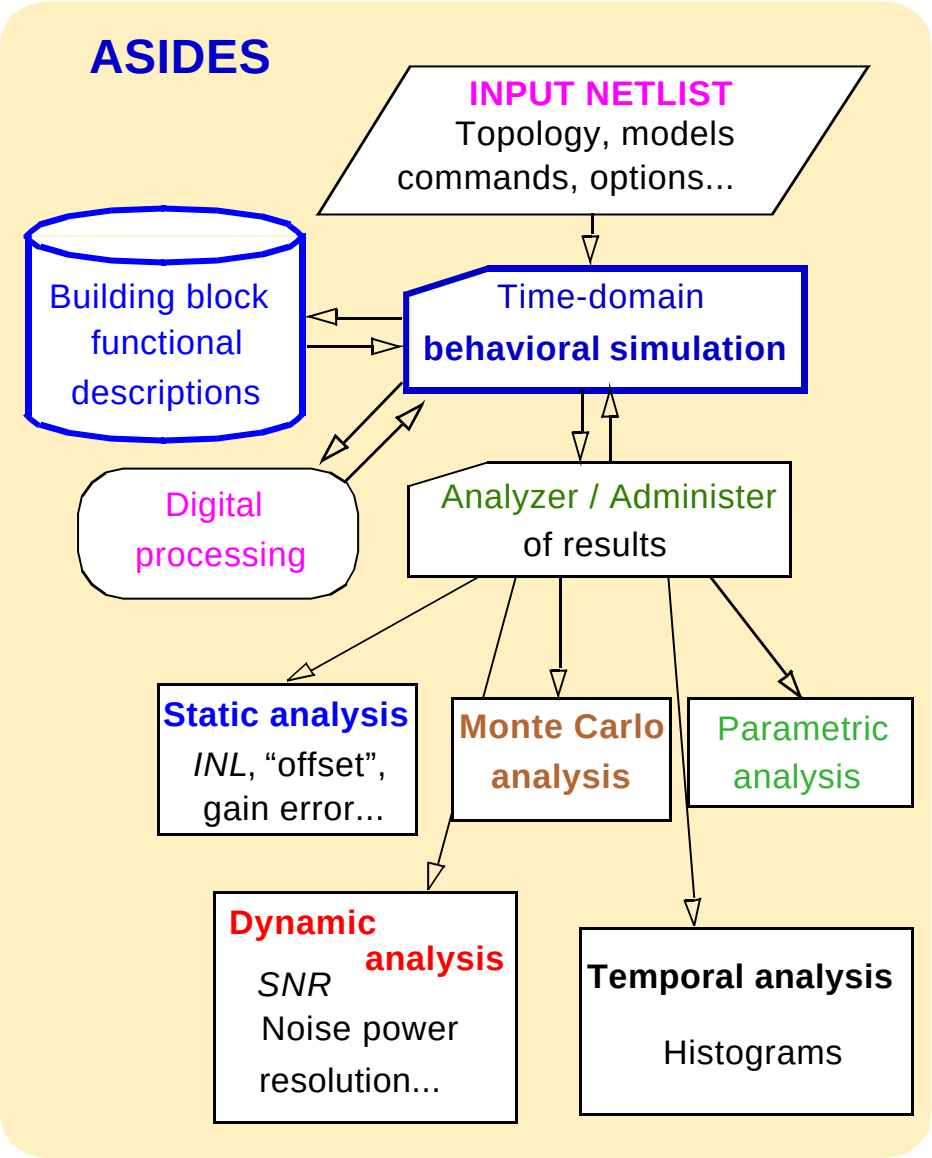




Use behavioural simulation but, it must precise:

- **Non-ideal simulation**
- **Practice-founded behavioural models**
- **IC-oriented**

Dedicated behavioural simulators

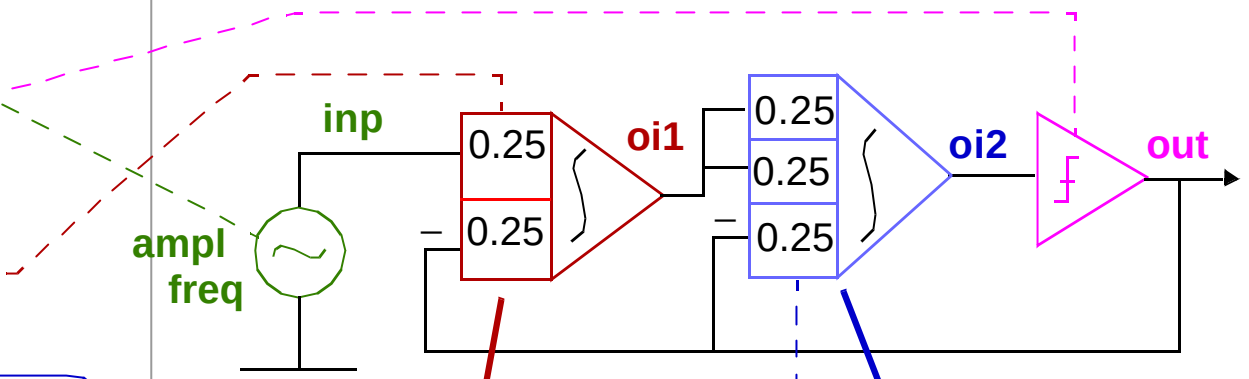


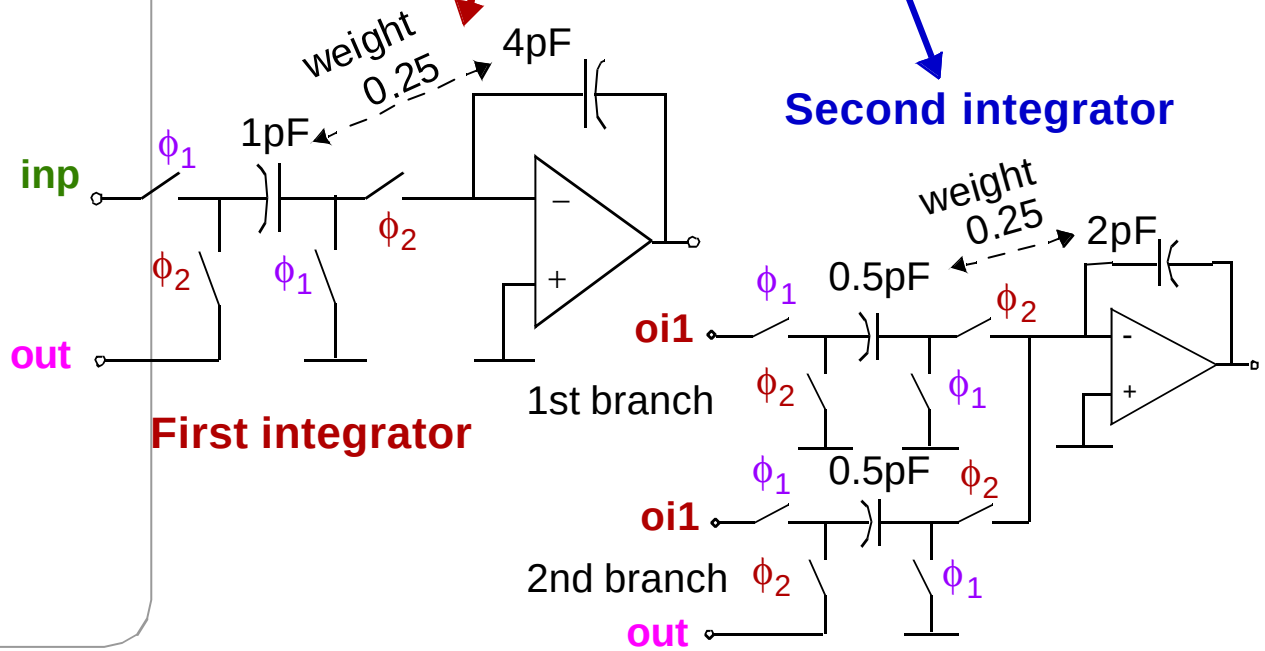
Covered non-idealities

Building Blocks		Non-idealities	Consequences
Integrators	Opamps	DC-gain, finite and non-linear	Increased quantization error, harmonic distortion.
		Dynamic limitations	Settling error, harmonic distortion.
		Output range	Overloading.
		Thermal noise	White noise.
	Switches	ON-resistance, thermal noise	Settling error, white noise.
	Capacitors	Non-linearity, mismatch	Increased quantization error, harmonic distortion.
	Clock	Jitter	Jitter Noise.
	Comparators	Hysteresis, offset	Increased quantization error.
	Multi-bit ADC, DAC	Non-linearity, gain error, offset	Increased quantization error. Harmonic distortion.

```
Vin inp ampl=0.5 freq=1.2k;
Comp1 out (oi2) real cm;
I1 oi1 (inp,out*0.25) real im1;
I2 oi2 (oi1,0*0.25  oi1,out*0.25) real im2;
```

```
.output spc(out);
.clock freq=2.4576x jitter=1n;
.oversamp 256;
.nsamp 65536;
.options fullydiff;
...
```





```
Vin inp ampl=0.5 freq=2.4k;

Comp1 out (oi2) real cm;
I1 oi1 (inp,out*0.25) real im1;
I2 oi2 (oi1,0*0.25 oi1,out*0.25) real im2;

.output spc(out);
.clock freq=2.4576x jitter=1n;
.oversamp 256;
.nsamp 65536;
.options fullydiff;


.model cm Comparator
          vhigh=1.5      vlow=-1.5      hys=50m;
.model im1 Integrator
          cfb=4p         ron=2k         cload=0.5p
          dcgain=60d     dcgnl1=1       dcgnl1=-10
          gm=220u        imax=58u       btpar=0.5
          osp=1.5        osn=-1.5       cpa=0.5p;
.model im2 Integrator
          cfb=4p         ron=2k         cload=0.5p
          dcgain=60d     dcgnl1=1       dcgnl1=-10
          gm=220u        imax=58u       btpar=0.5
          osp=1.5        osn=-1.5       cpa=0.5p;
```

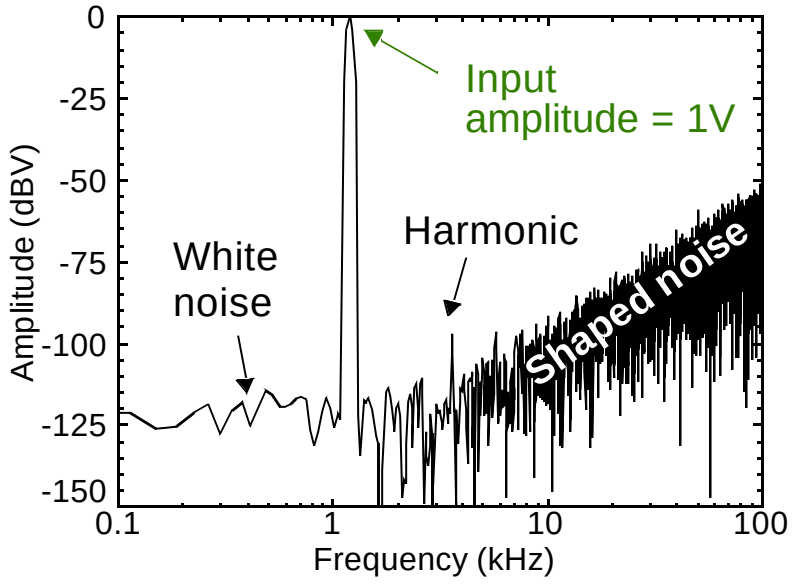
Manual sizing results

Topology	2nd-order	Modulator
Sampling frequency	2.4576MHz	
Oversampling ratio	256	
DAC output high, Low	±1.5V	Quantizer
Hysteresis	< 50mV	
g_1, g_1', g_2, g_2'	0.25, 0.25, 0.5, 0.25	Integrators
Integration capacitor (1st int.)	4pF	
Integration capacitor (2nd int.)	2pF	
MOS switch-ON resistance	2kΩ	
Maximum clock jitter	< 1ns	
DC-gain	> 60dB	Opamps
DC-gain non-linearity	< $1\%V^{-1}$, $10\%V^{-2}$	
Transconductance	> 220mA/V	
Maximum output current	> 58mA	
Total output swing	> 3V	
Parasitic input capacitor	< 0.5pF	

- "cload" must include **only**:
  - opamp output parasitic
  - input parasitic of a possible quantizer
- Remaining contributions to C_{I1} and C_{I2} are automatically estimated by ASIDES, through "**btpar**" -> relative bottom parasitic

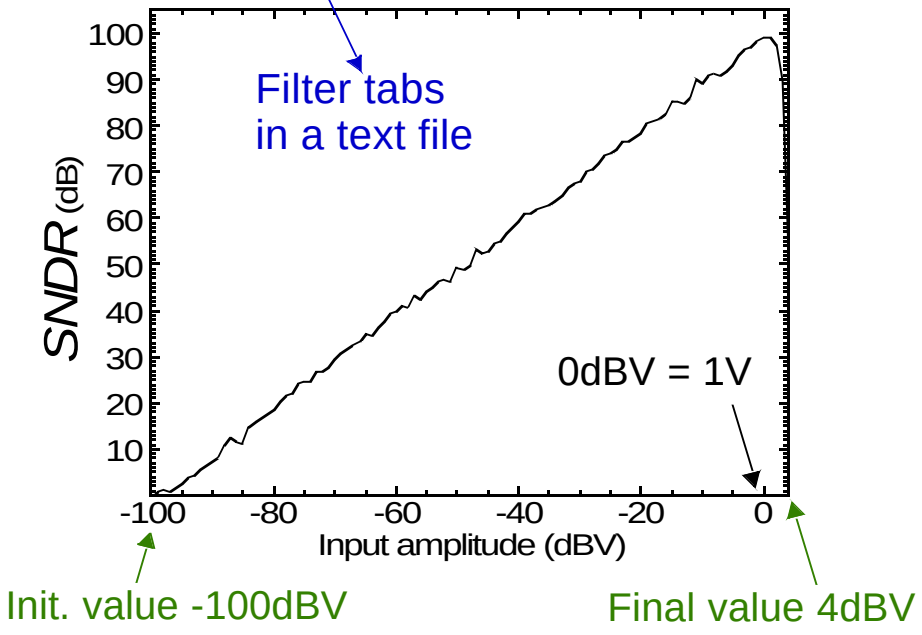
Output spectrum

```
Vin inp ampl=1 freq=1.2k;

Comp1 out (oi2) real cm;
I1 oi1 (inp,out*0.25) real im1;
I2 oi2 (oi1,0*0.25 oi1,out*0.25) real im2;

.clock freq=2.4576x jitter=1n;
.options fullydiff;    # Using differential circuitry

.nsamp 65536;          # Number of samples
.output spc(out);      # Amplitude spectrum
```



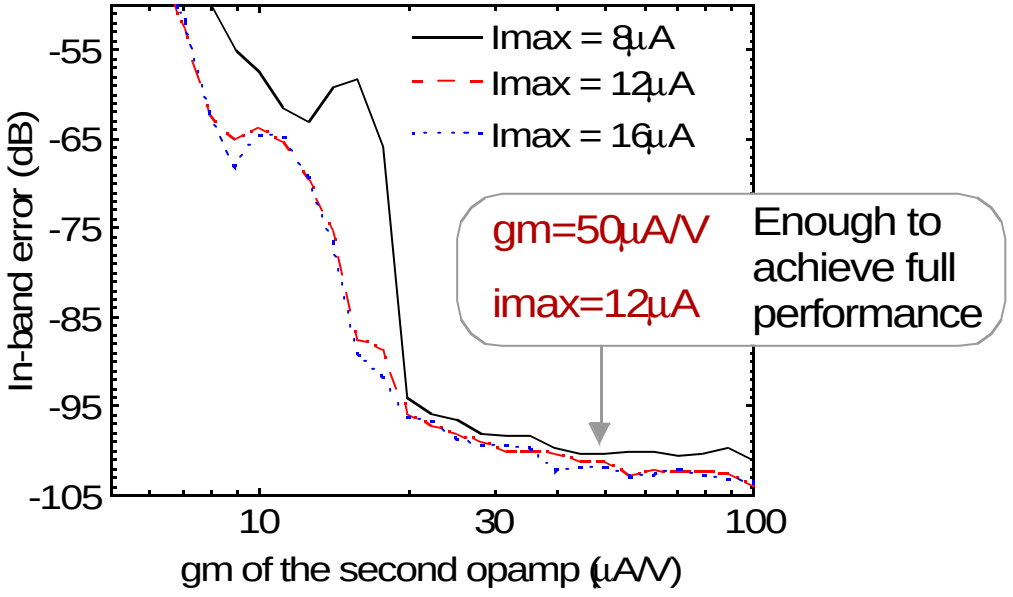
Signal-to-noise vs. input amplitude

```
Vin inp ampl=(-100 4 2) freq=1.2k;
Comp1 out (oi2) real cm;
I1 oi1 (inp,out*0.25) real im1;
I2 oi2 (oi1,0*0.25 oi1,out*0.25) real im2;
.clock freq=2.4576x jitter=1n;
.options fullydiff;      # Using differential circuitry
.nsamp 65536;            # Number of samples

.output snr(out);        # Signal-to-noise
.oversamp 256;           # Oversampling ratio
.filtfile file=f256_1024 type=fir    # FIR filter
```



Relaxing 2nd integrator dynamics

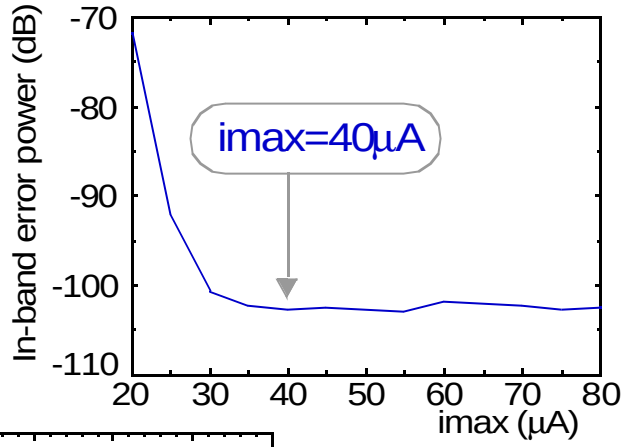
```
.output ibn(out);      # In-band error power

.option nother fullydiff; # disables thermal noise

.model im1 Integrator
            gm=220u      imax=58u
            ...
.model im2 Integrator
            gm=gm2       imax=58u
            ...
.param gm2=sweep(dec 20 5u 100u)
```

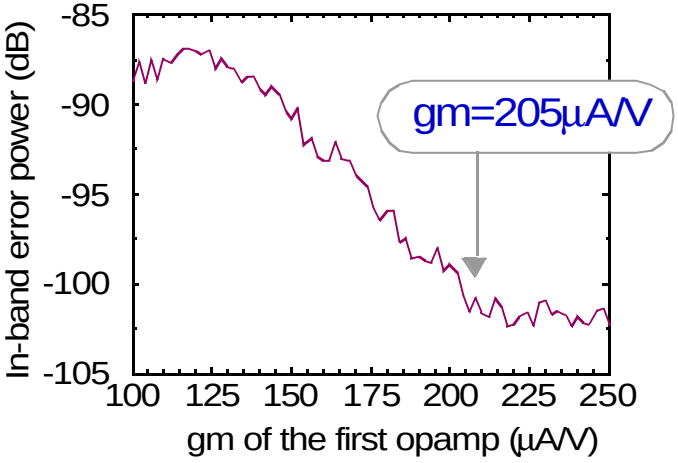


Fine-tuning 1st integrator dynamics

```
.model im1 Integrator
            gm=220u      imax=io1
.param io1=sweep(lin 20u 80u 5u)
```

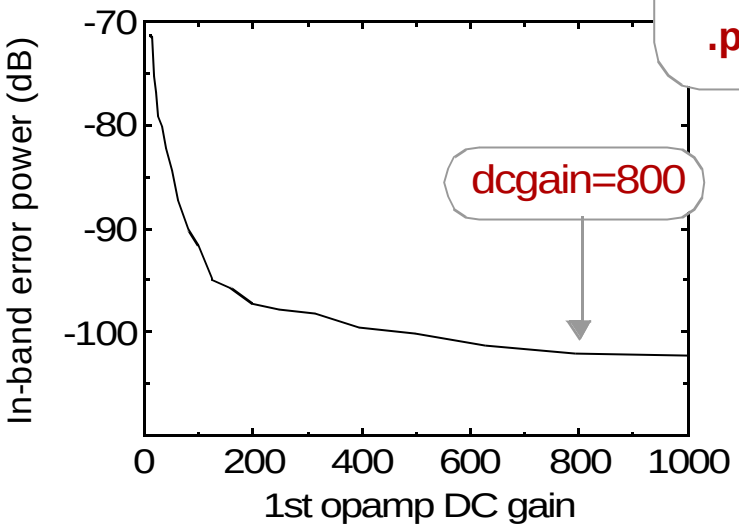
```
.model im1 Integrator
            gm=gm1       imax=40u
.param gm1=sweep(lin 100u 250u 2u)
```

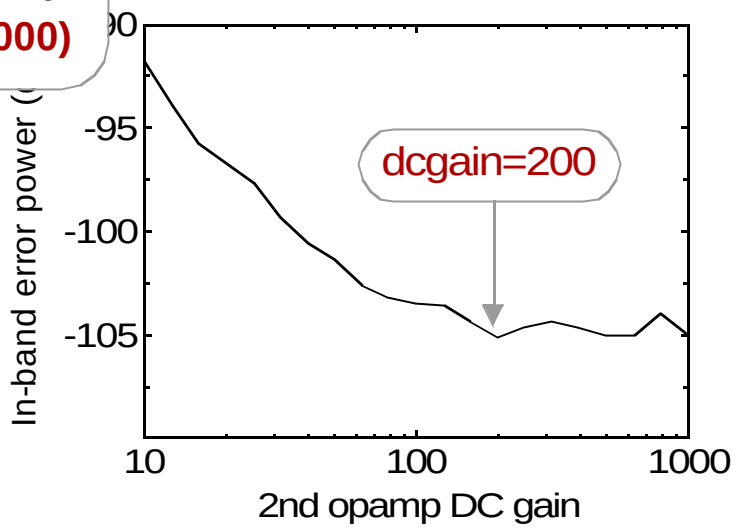


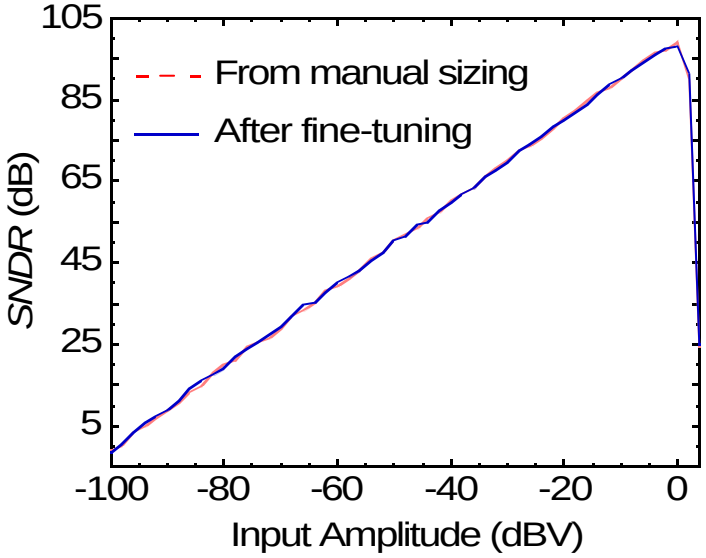


Fine-tuning DC gain

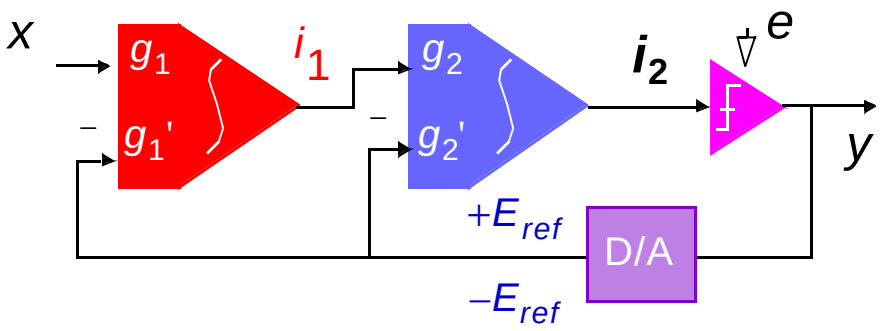
```
.model im1 Integrator
      dcgain=dcg dcgnl1=1 dcgnl2=10
.param dcg=sweep(dec 10 10 1000)
```







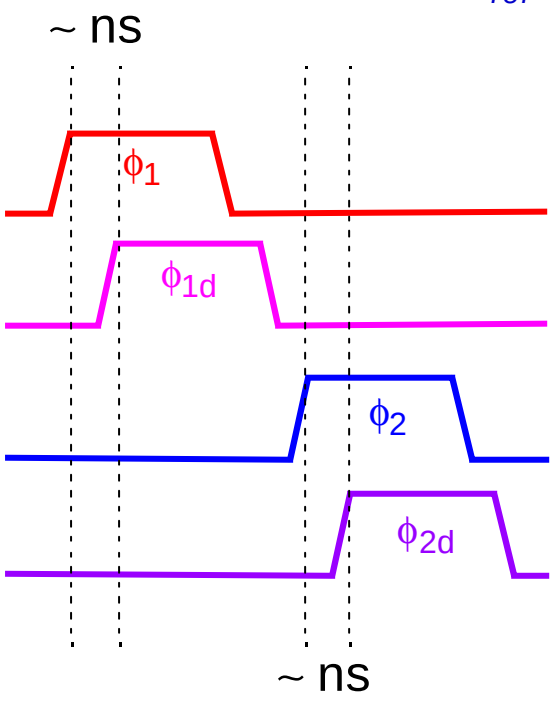
	1st opamp		2nd opamp	
	Before	After	Before	After
gm	220µA/V	205µA/V	200µA/V	50µA/V
imax	58µA	40µA	58µA	12µA
dcgain	1000	800	1000	200

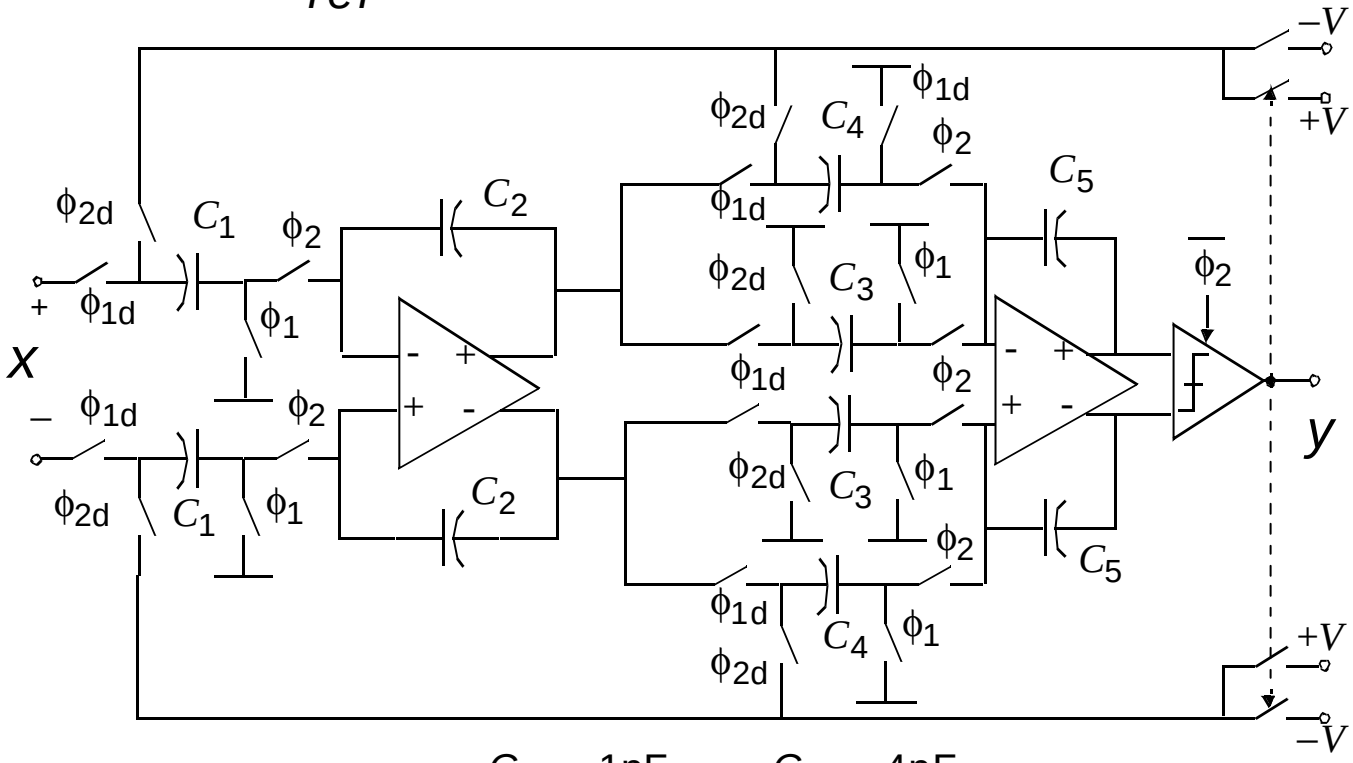


Fully-differential SC schematic

- Large common-mode rejection
- 3dB increase in *SNR*

$$+E_{ref} = +V-(-V) = 2V$$
$$-E_{ref} = -V-(+V) = -2V$$
$$\longrightarrow \quad V = \frac{E_{ref}}{2}$$





$C_1 = 1\text{pF}$ $C_2 = 4\text{pF}$

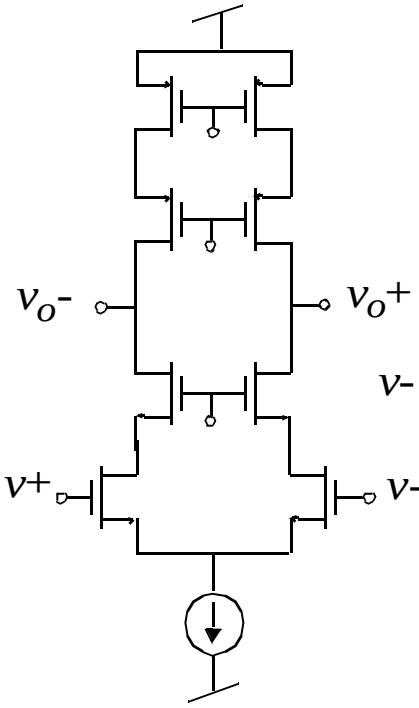
$C_3 = 1\text{pF}$ $C_4 = 1\text{pF}$ $C_5 = 1\text{pF}$

⇨ *Opamp topology selection must primarily consider:*

- **Output swing requirement**
  - **Remember:** it critically depends on the integrator weight
  - Cascode techniques may not be valid
- **Open-loop DC gain requirement**
  - Single, non-cascode stages may not be enough
  - Cascode, and/or multi-stage topologies may be required
- **Dynamic requirements**
  - Obtaining correct transient behaviour is harder in multi-stage topologies
- **Power dissipation and simplicity**

⇨ *In our case*

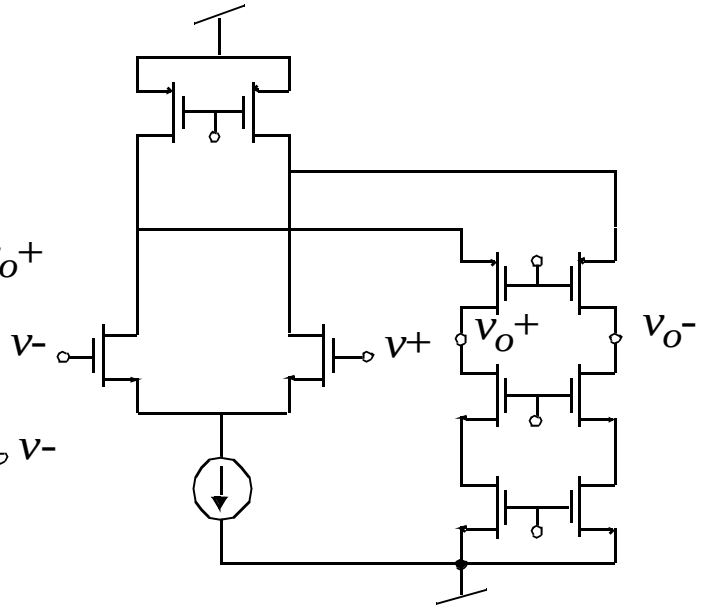
- **Technology is 5-V Supply, O.S. = 3V differential => not tight**
- **Cascode techniques appropriate to obtain required DC gain**



Telescopic cascode

Best speed-power figure

CM output voltage different from input

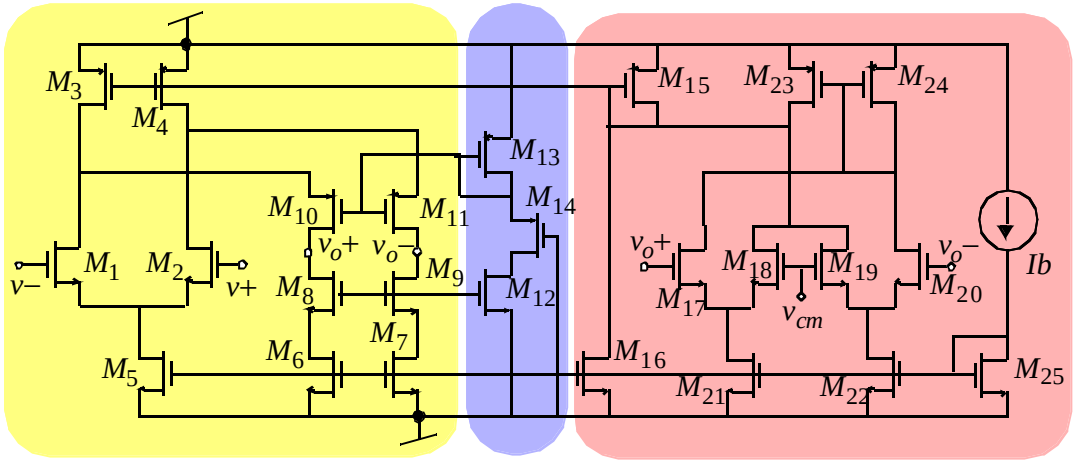


Folded cascode

Good speed-power figure

CM output = CM input

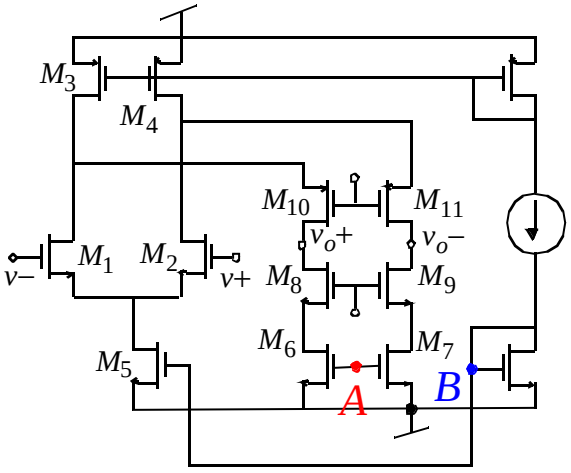
Fully-differential folded-cascode OTA

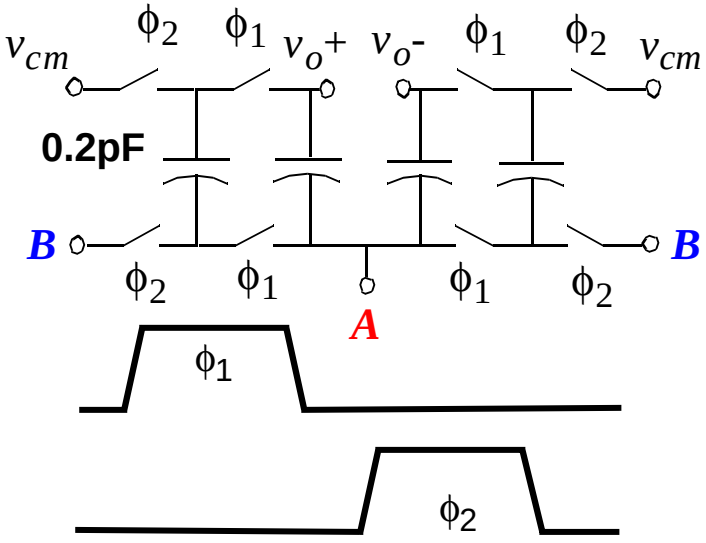


OTA core *Biasing* ***Static Common-mode feed-back net***

Up to approx. 3V supply voltage

- **Good trade-off performance/ power consumption**
- **Relatively easy to design**
  - **Single-stage amplifier**
- **Good supply rejection ratio figures**

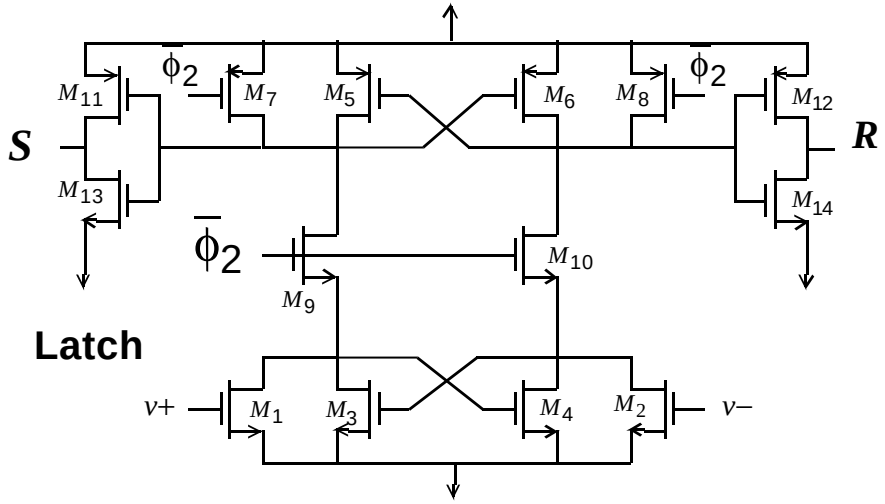




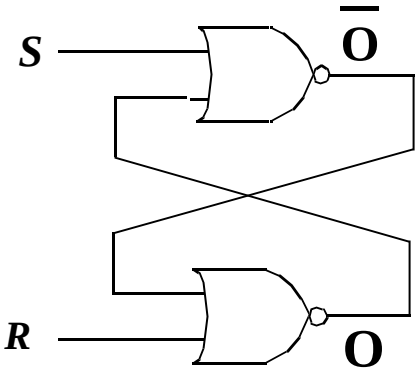
Dynamic Common-mode feed-back net

- **Lower power consumption**
  - **CMFB net practically does not consume**
- **but,**
  - **Larger difficulties in the test**

1-bit Quantizer, latched comparator

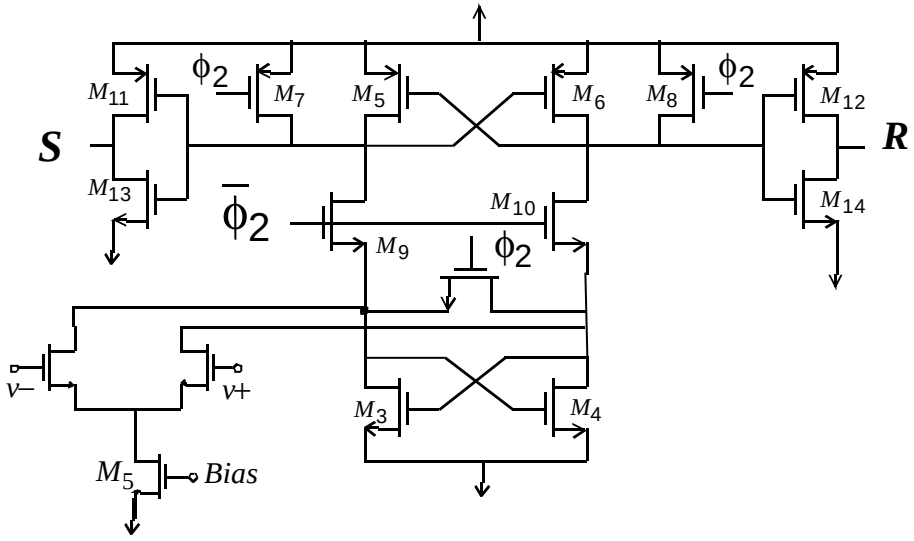


resolution around 50mV

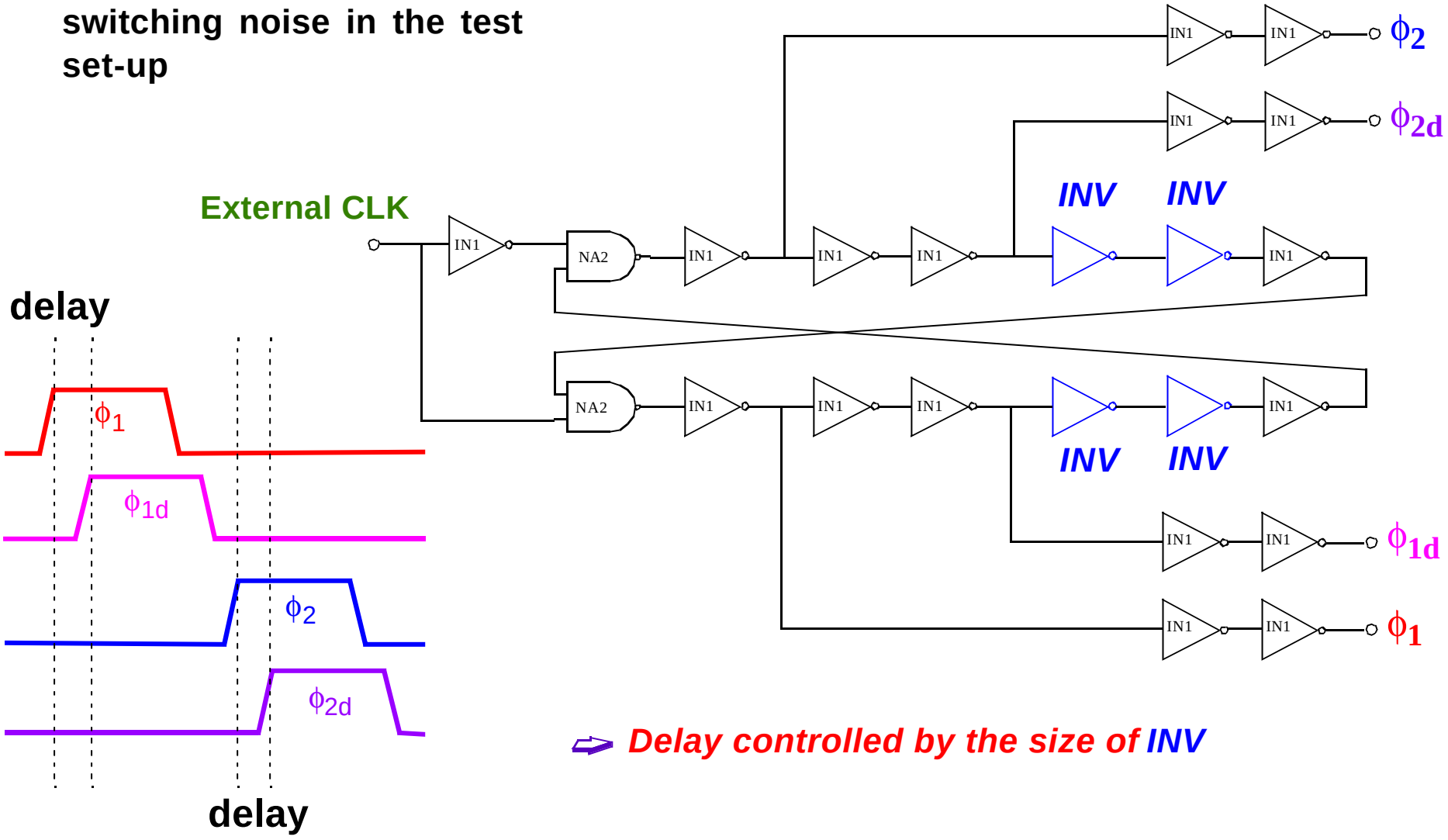


SR flip-flop

If a larger resolution is needed, use a differential pair as input transconductor

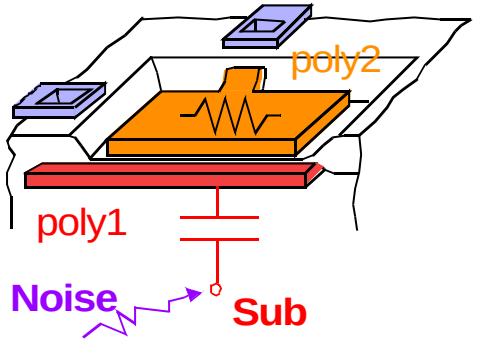


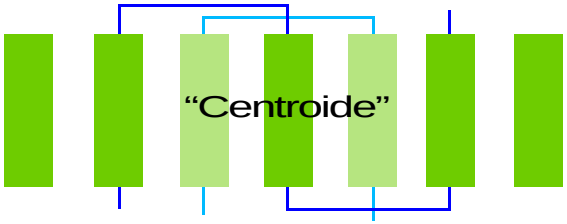
- **Always on-chip to reduce switching noise in the test set-up**

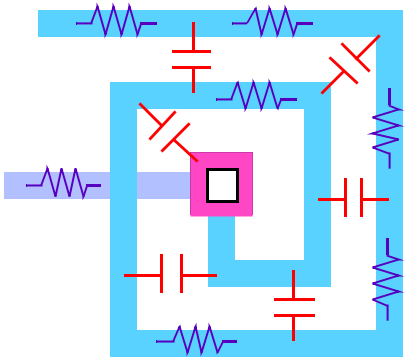


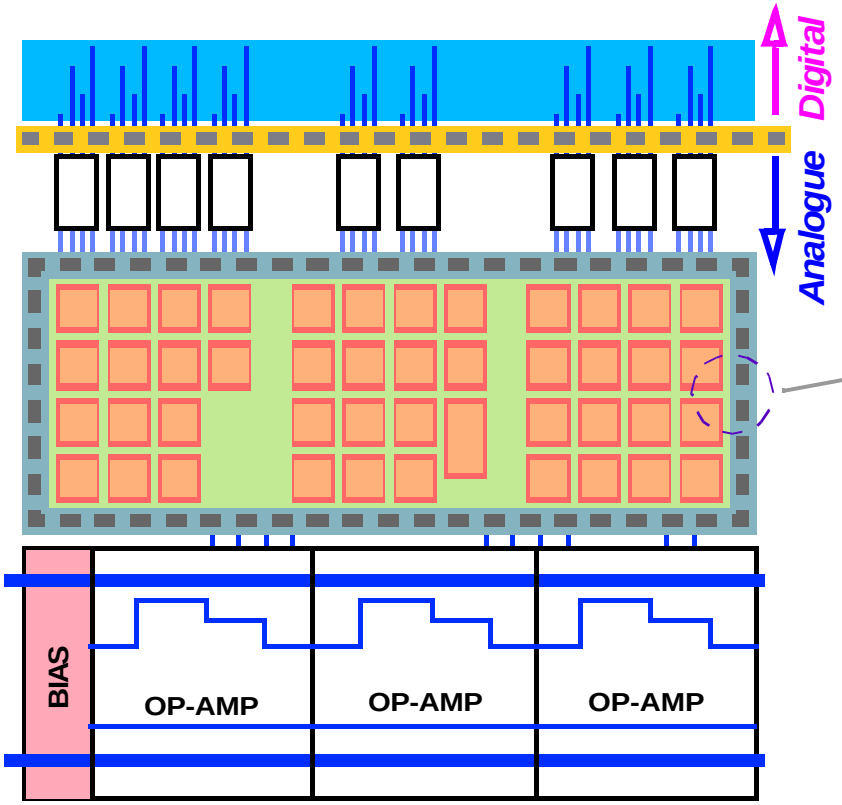
⇨ ***Delay controlled by the size of INV***

- A good layout must
  - **Protect against interferences**
  - **Ensure good matching / typical performance**
  - **Reduce parasitics**

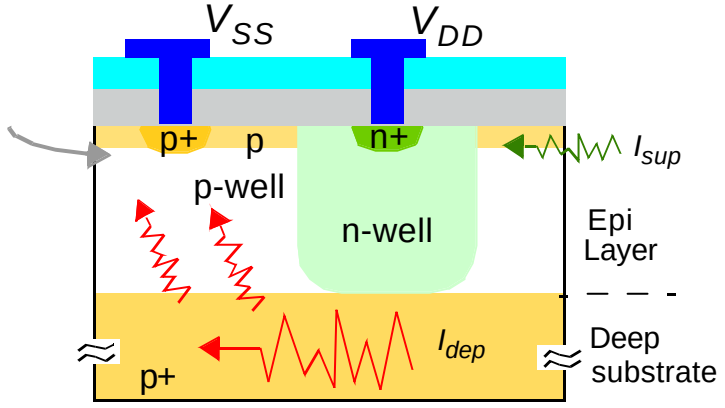






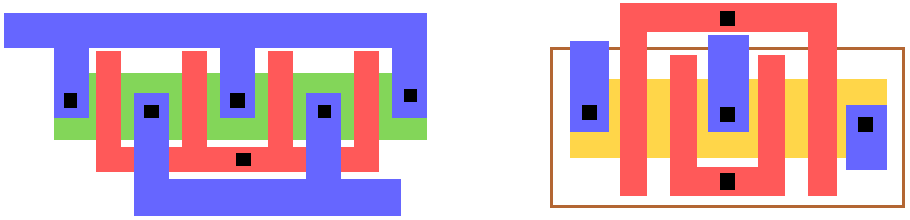


- **p/p+ substrate**

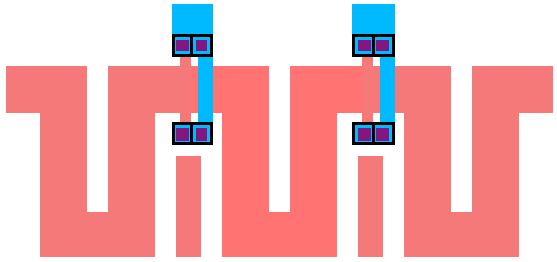


? **Revision of substrate noise coupling techniques**

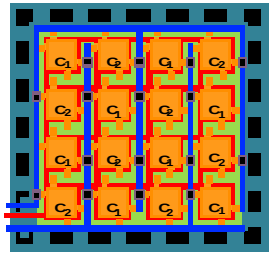
- **MOS transistors**



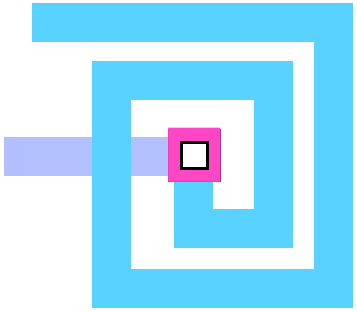
- **Resistors**



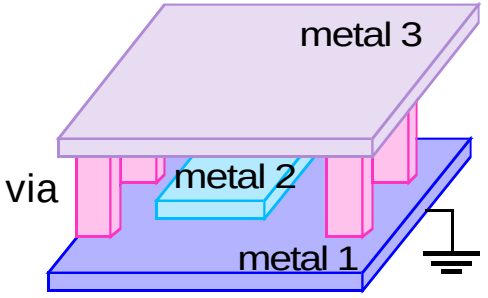
- **Capacitors**



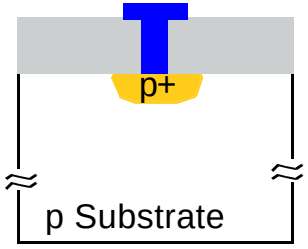
- **Inductors**



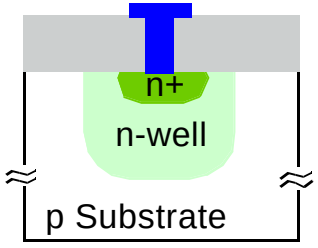
- **Interconnects**



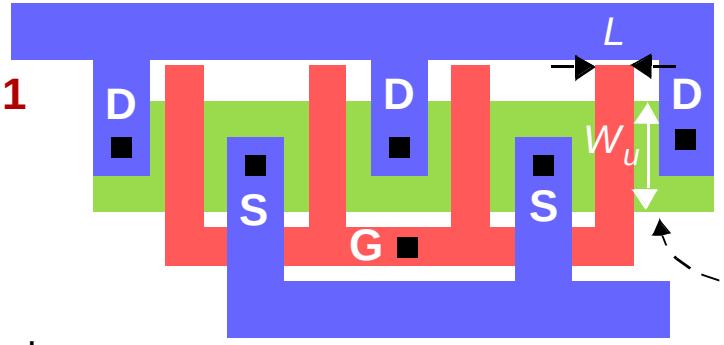
- **Substrate contacts (p+ guard ring)**

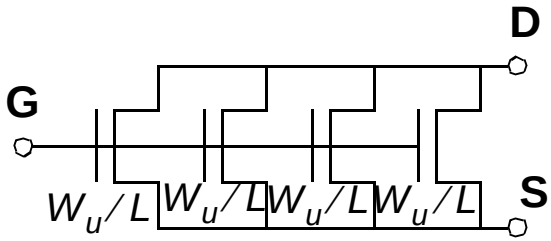


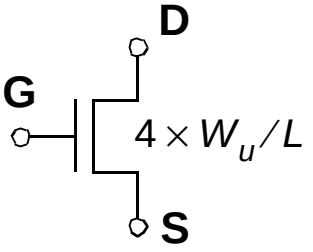
- **n+ in n-well guard ring**



⇨ **W/L >> 1**



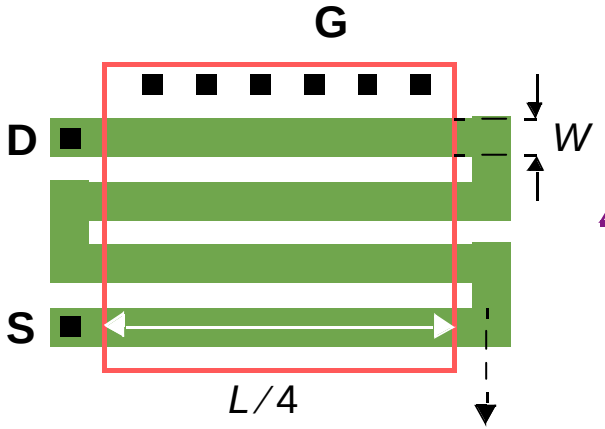




$$\frac{W_u}{L} R_{\square\,\text{poly}} < \frac{1}{g_{m,\,\text{unitary}}} \Rightarrow \text{Th. noise}_{\text{poly}} < \text{Th. noise}_{\text{MOS}}$$

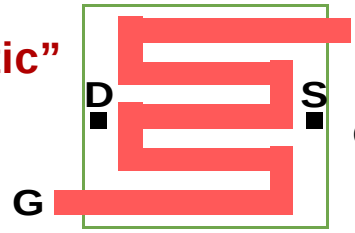
- Reduced area
- Reduced bottom junction capacitance (drain and source areas shared)
- Reduced side-wall junction capacitance (avoids contacting active area and channel-stop p implant)
- Usually well characterised except for parasitics

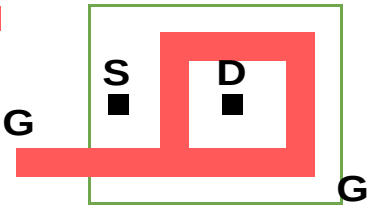
⇨ **W/L << 1**



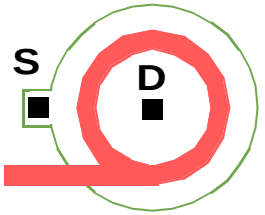
Salicide reduces inter-channel resistance

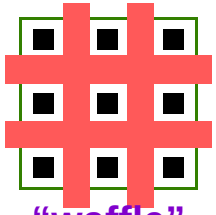
⇨ **"Exotic"**





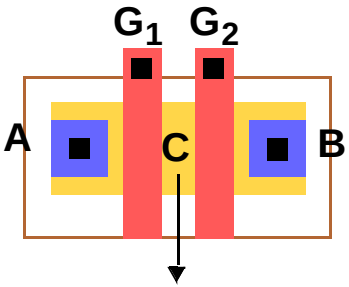
Poor modelling



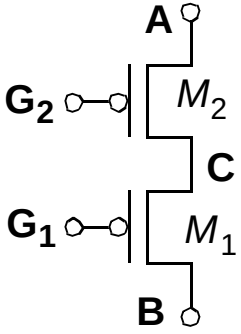


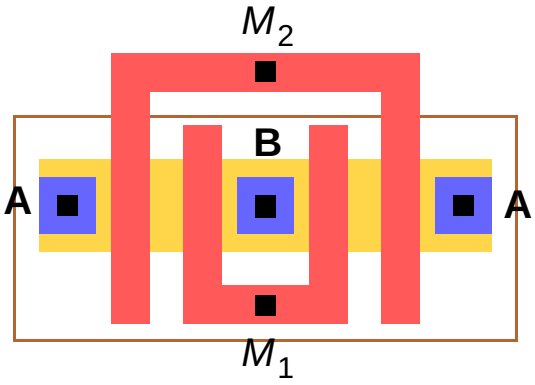
"waffle"

⇨ **Speficic**



Reduced parasitic at the cascode node

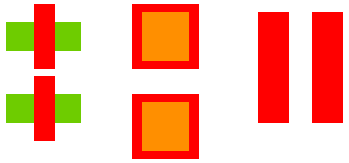




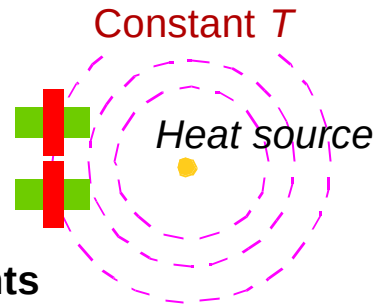
- **Preserving symmetry helps a lot**
  - Even order non-linearity is suppressed
  - Common-mode interferences are largely attenuated

⇨ ***Two devices are actually "equal" if***

✓ **Same structure**



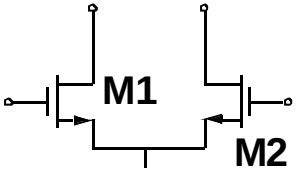
✓ **Same temperature**

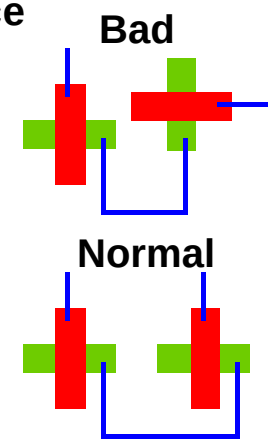


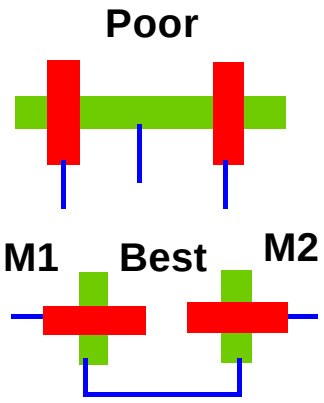
✓ **Same shape and size**

✓ **Minimum Distance**

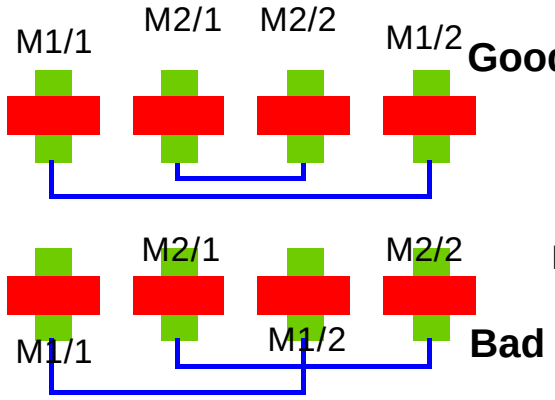
✓ **Same Orientation**

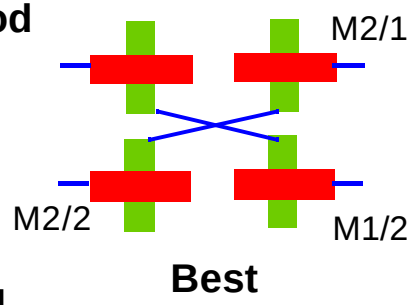




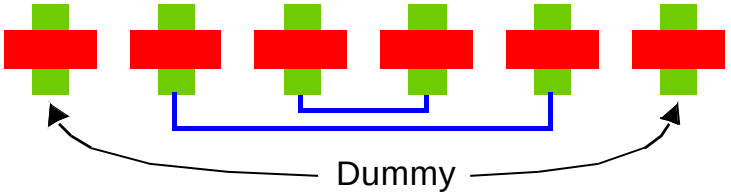


✓ **Cancell linear gradients**





✓ **Same Surrounding**

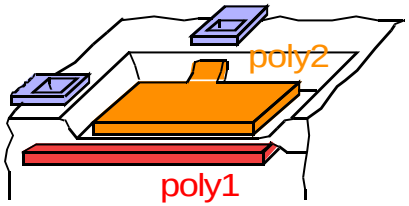


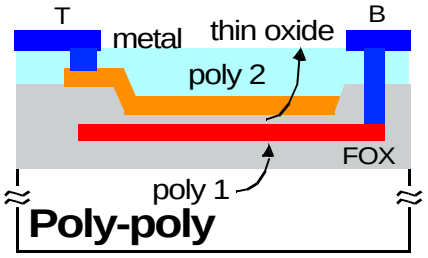
- **There are still differences due to local errors**
  - Errors are inverse function of device size

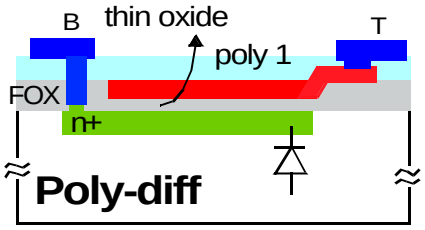
$$\frac{\sigma_p^2}{p^2} \approx \frac{A_p^2}{WL} + \frac{B_p^2}{W^2L} + \frac{C_p^2}{WL^2}$$

  - Use statistic models to estimate minimum dimensions

Thin oxide capacitor ("analog" CMOS)

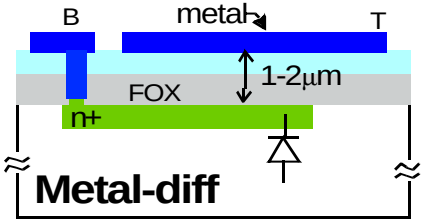


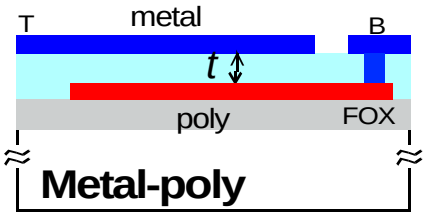


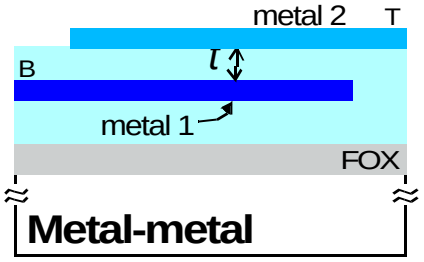


Density	■■■■■
Linearity	■■■■■
Temperature	■
Parasitics	■■■
Matching	■■■■

Digital CMOS compatible

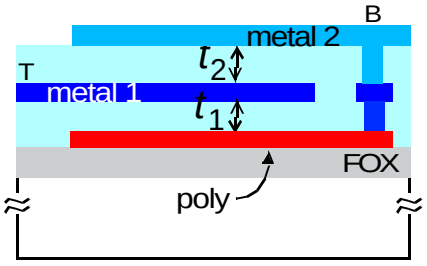




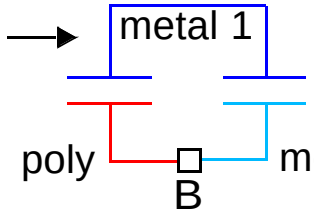


Density	■■
Linearity	■■■■■
Temperature	■
Parasitics	■■■
Matching	■■

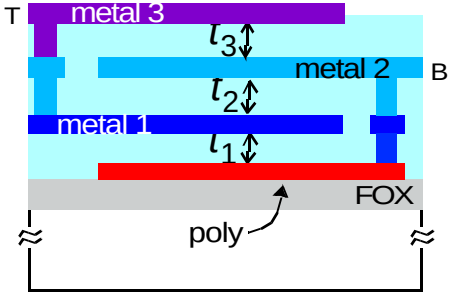
- Multi-layer



cap. density X 2

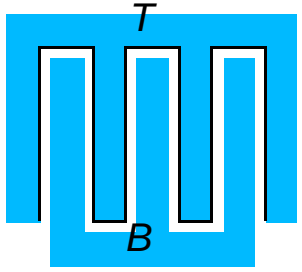


cap. density X 3



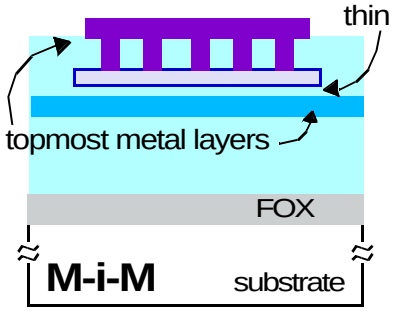
- Polishing after dielectric deposition improves mathing
- Lack of models

- Lateral capacitors



- Lage density (combination with multi-layer)
- Lack of models (value? variations? ...)

Best choice!



Density	■■■■■
Linearity	■■■■■
Temperature	■
Parasitics	■
Matching	■■■■■

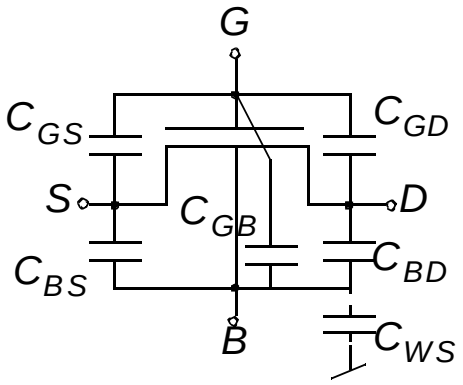
- MOS capacitors

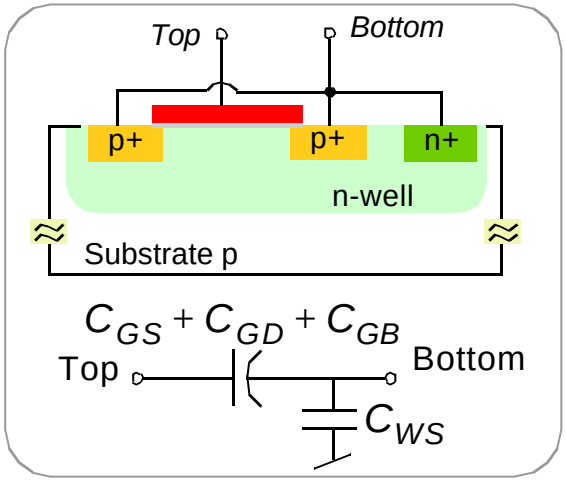
Density	■■■■■	Temperature	■□□□□
Linearity	■□□□□	Parasitics	■■■■□
			Matching ■■■■■

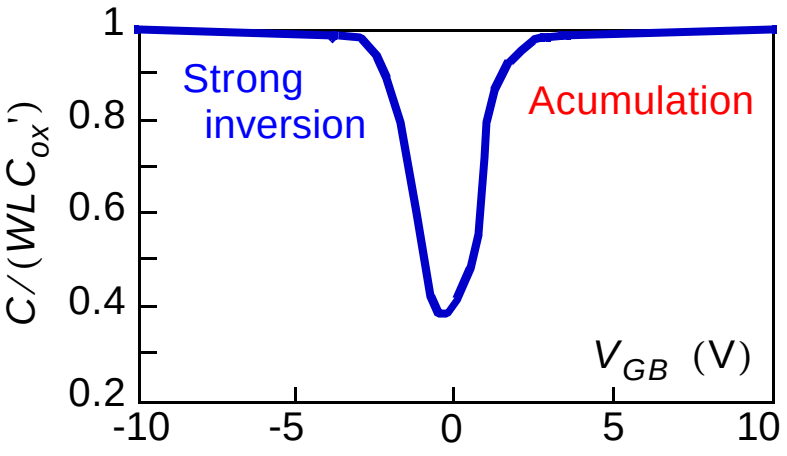
Maximum density

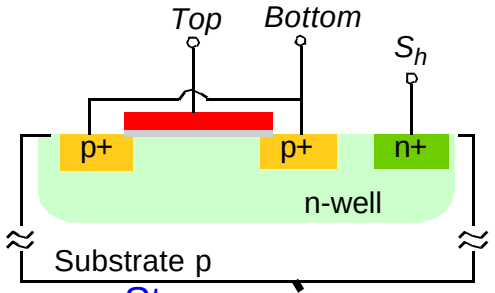
Good matching

Very poor linearity

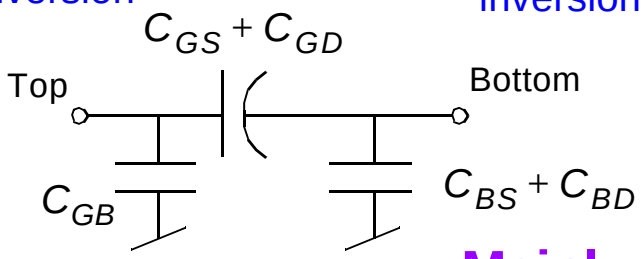


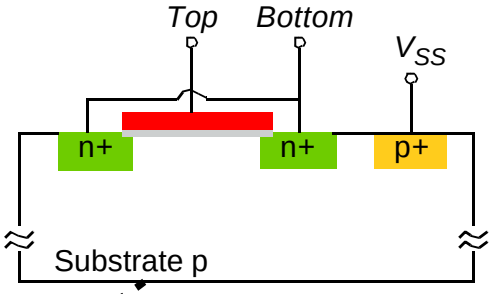




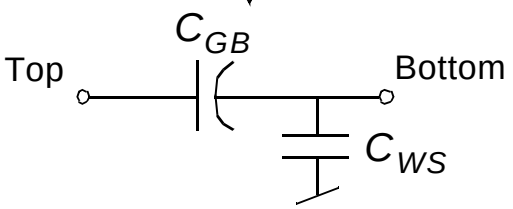


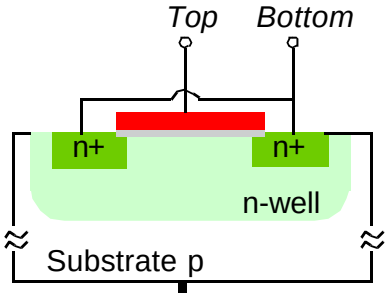
Strong inversion



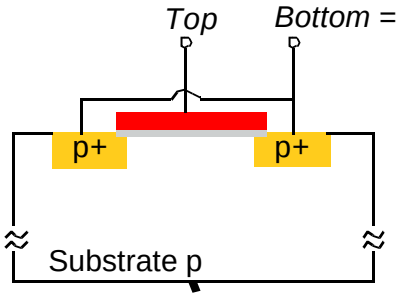


Strong inversion

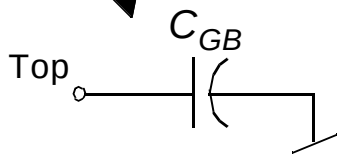




Acumulation



Acumulation



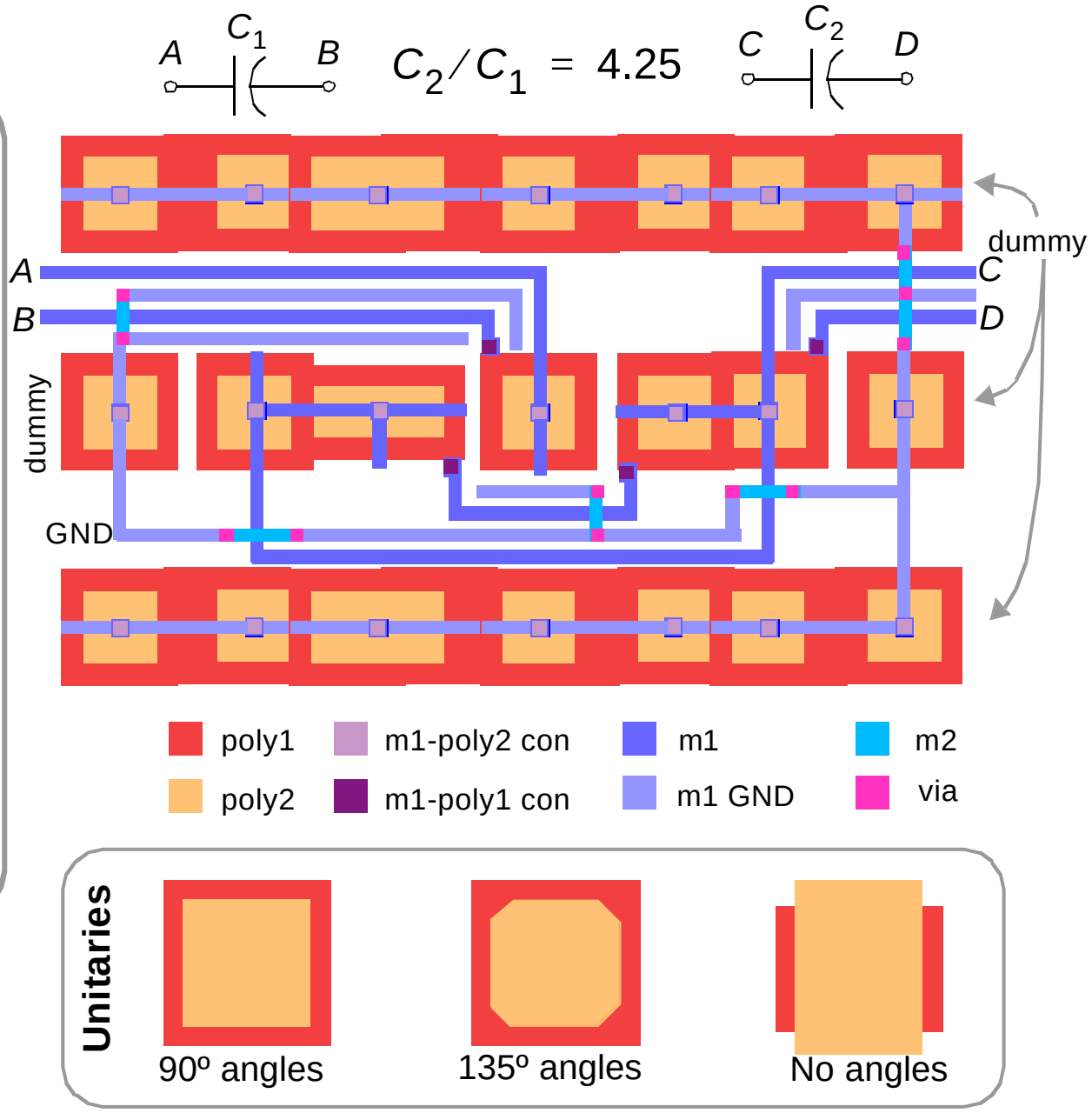
Non floating V_{SS}

Mainly used for decoupling

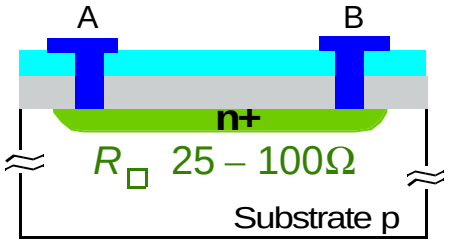
- Double-poly capacitors:

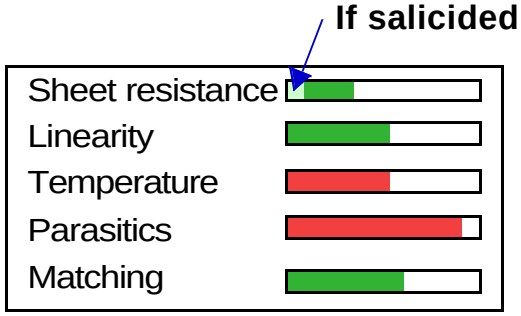
- Use **centroid** structure with **equally sized** unitary cap. or with the **same A/P** and locate then over an isotherm
- In non-integer ratios the non-unitary cap. must contribute to the largest capacitance and its value should be as close as possible to the unitary
- **Same surroundings** up to 50µm
- Make **interconnect capacitance** keep the same ratio as nominal
- Place grounded **decoupling lines** between interconnets
- If possible**,** place a **grounded metal** plane over the structure and a **well** below it connected to a “clean” voltage

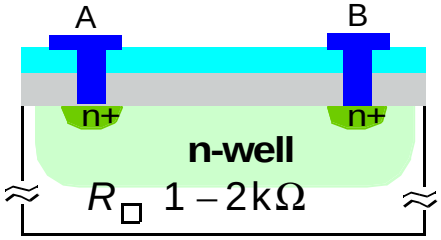
? **Largely dependent on the proccess and capacitor type**

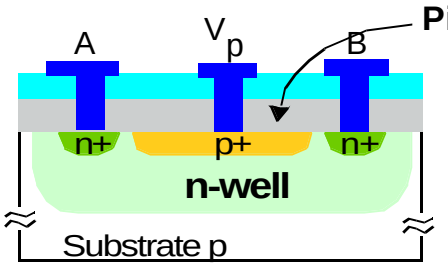


- Diffused resistors





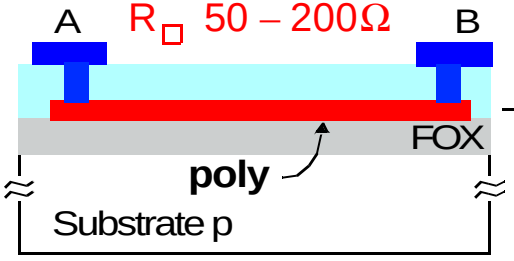


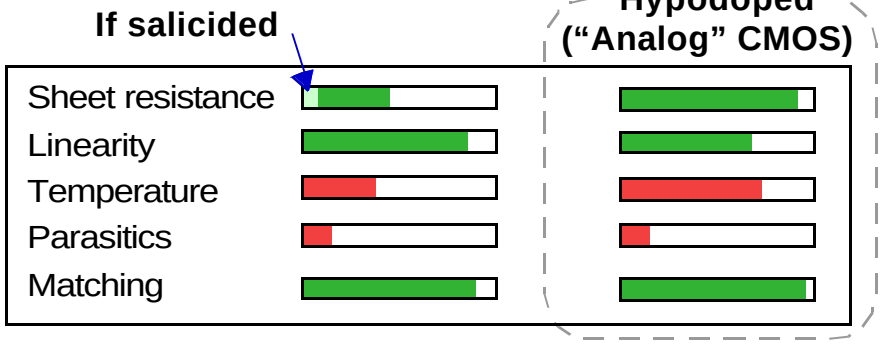


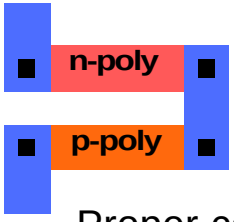
▶ **Less doping**

- ▶ $R_\square$ larger (1-2 kΩ)
- ▶ Smaller parasitic cap
- ▶ Worse linearity
  Larger temperature coeff

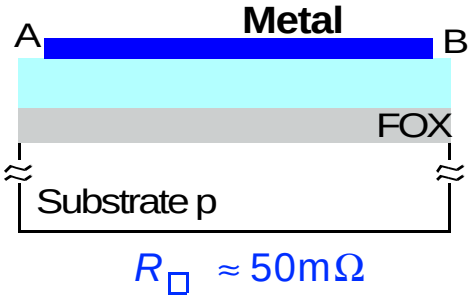
- Deposited resistors

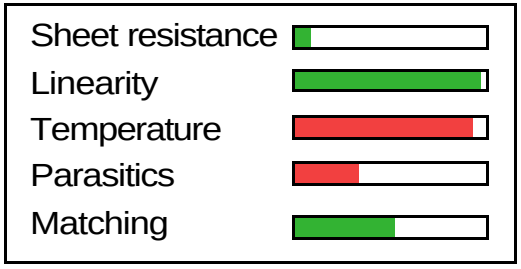






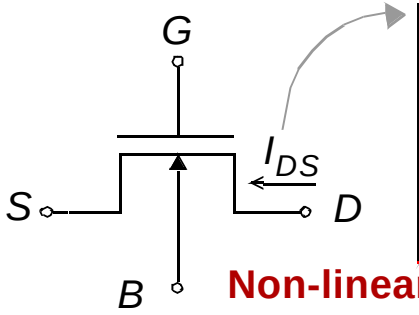
Proper combination of n- and p-poly may improve linearity and tempemparture dependence

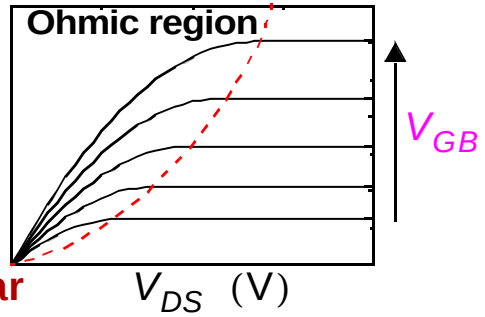




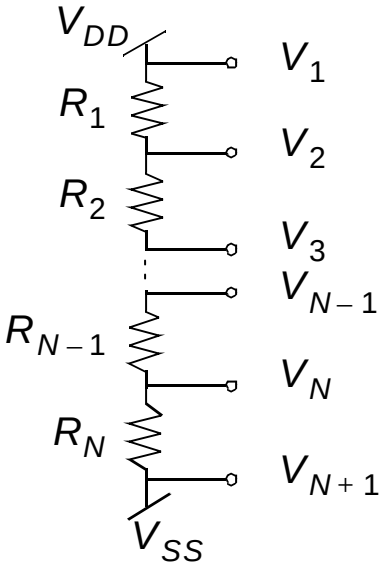
☹ **Large temperature dependence**

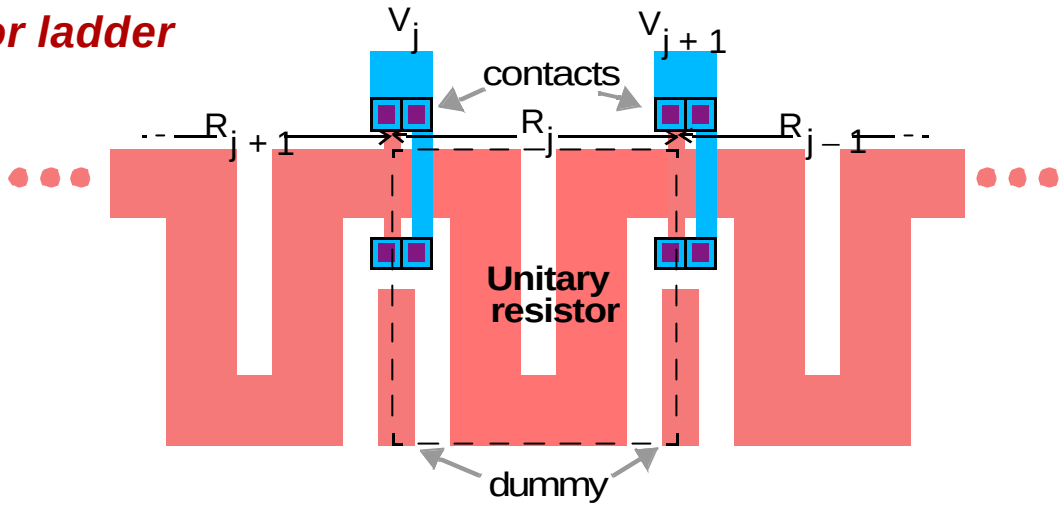
- Channel resistors





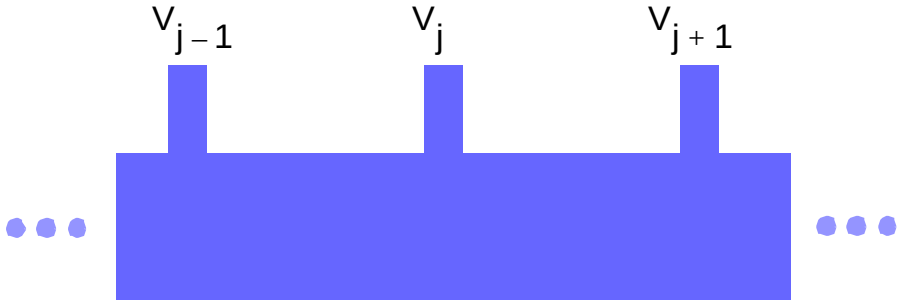
High-precision resistor ladder





- **Folded structure** (if required) to reduce gradient effects
- **Contacts outside the resistive string**
- **Two contacts per tab** to compensate for mask displacement

High-speed resistor ladder



Top-most metal

- **Small sheet resistance**
- **Small parasitic capacitance to substrate**
- **Good linearity**

but...

- **Good matching requires large width**
- **Large temperature coefficient**

Crosstalk

- **Capacitive and/or inductive coupling between interconnects**

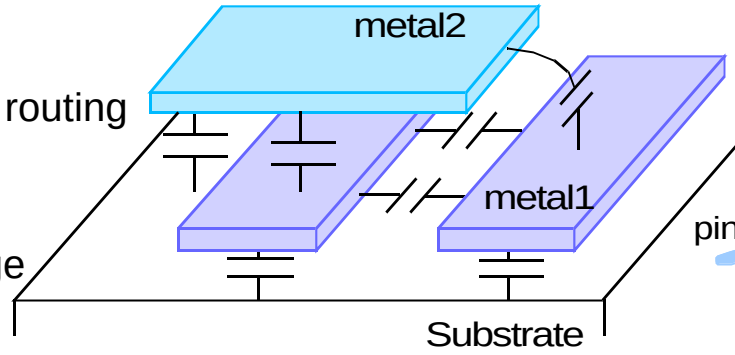
Substrate noise

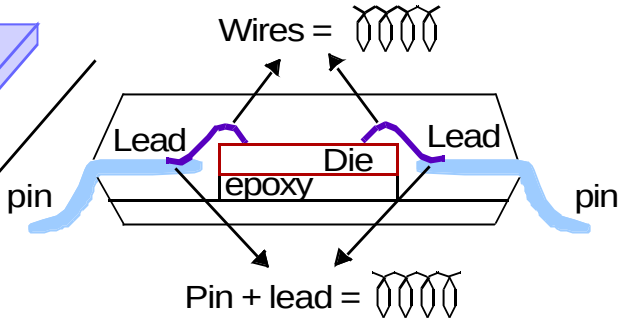
- **Coupled and propagated through the common substrate**

Power and ground supply bounce

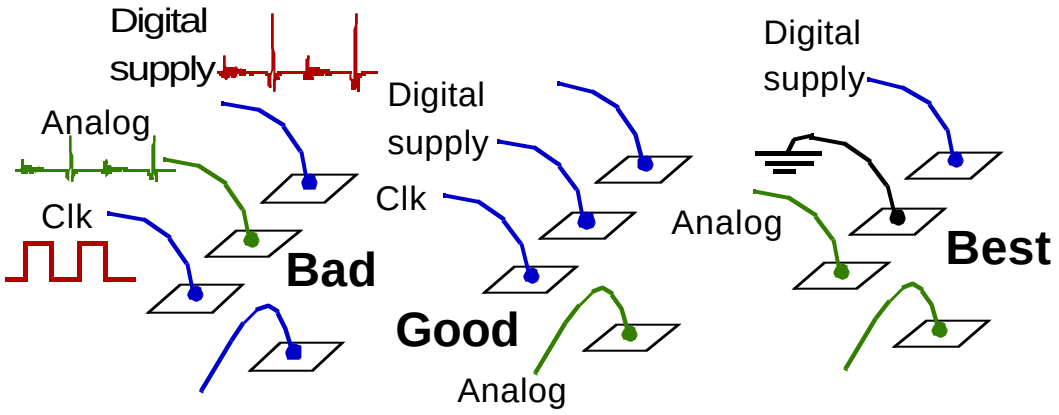
- **Coupled and propagated through power and ground distribution**

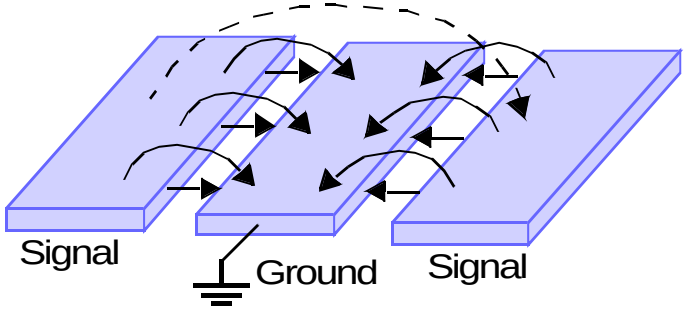
- **Causes**
  - Capacitive coupling between routing lines
  - Capacitive coupling to substrate
  - Inductive coupling through package



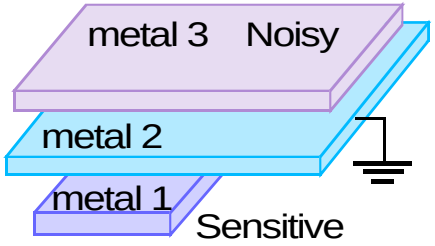


- **Solutions**
  - Increase distance between pads/pins for noisy and sensitive signals
  - Increase distance between noisy and sensitive lines
  - Add shied between closely spaced lines
  - Avoid crossing of noisy and sensitive lines
  - Add shield to unavoidable crossings
  - Use differential circuits and clocks

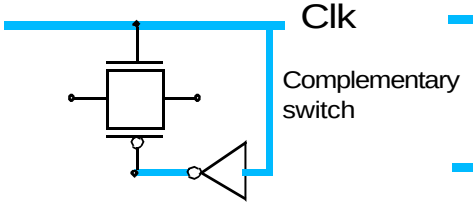


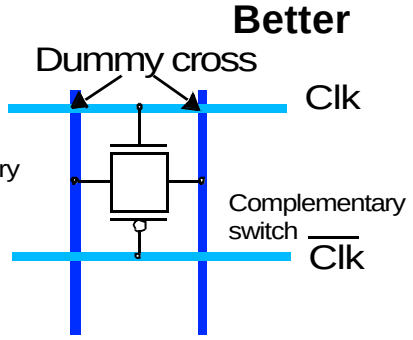


Reducing capacitive coupling



Crossing shielding

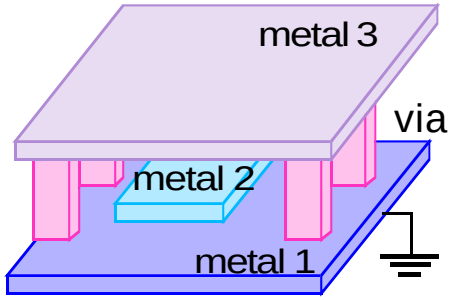




Shielding metal lines

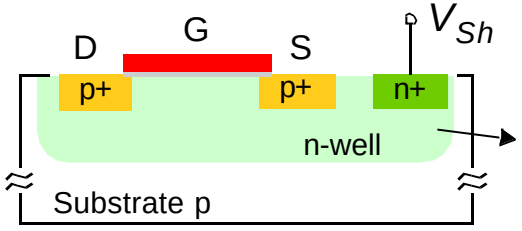
Example:

Decoupling analog supply from a noisy substrate



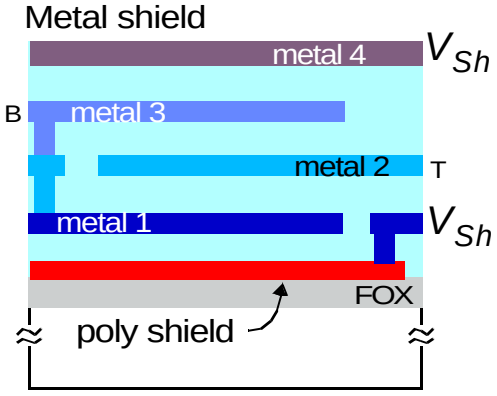
- Attenuates on-chiff and off-chiff interferences
- Reduces capacitive coupling to substrate
- May increase capacitive loading
- **Requires a "clean" voltage**
  Low-impedance path to ground

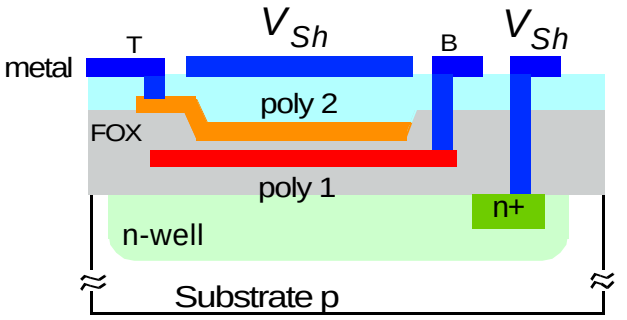
Shielding MOS transistors



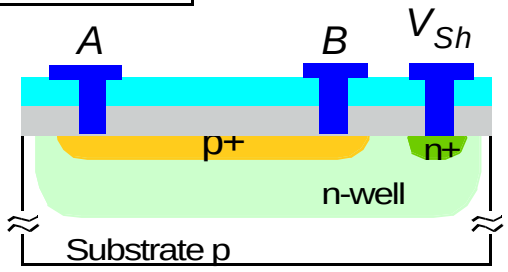
n-well is not a good shield due to its high resistivity → Place contacts surrounding the device

Shielding passive devices

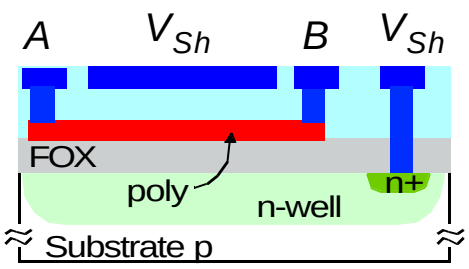


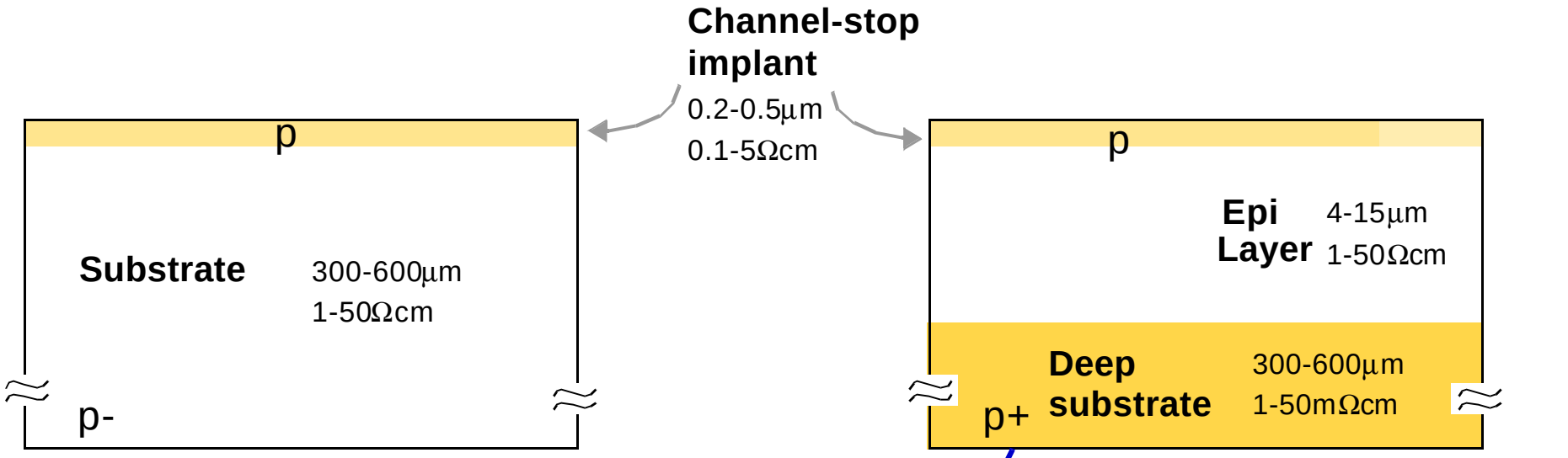


Capacitors



Resistors

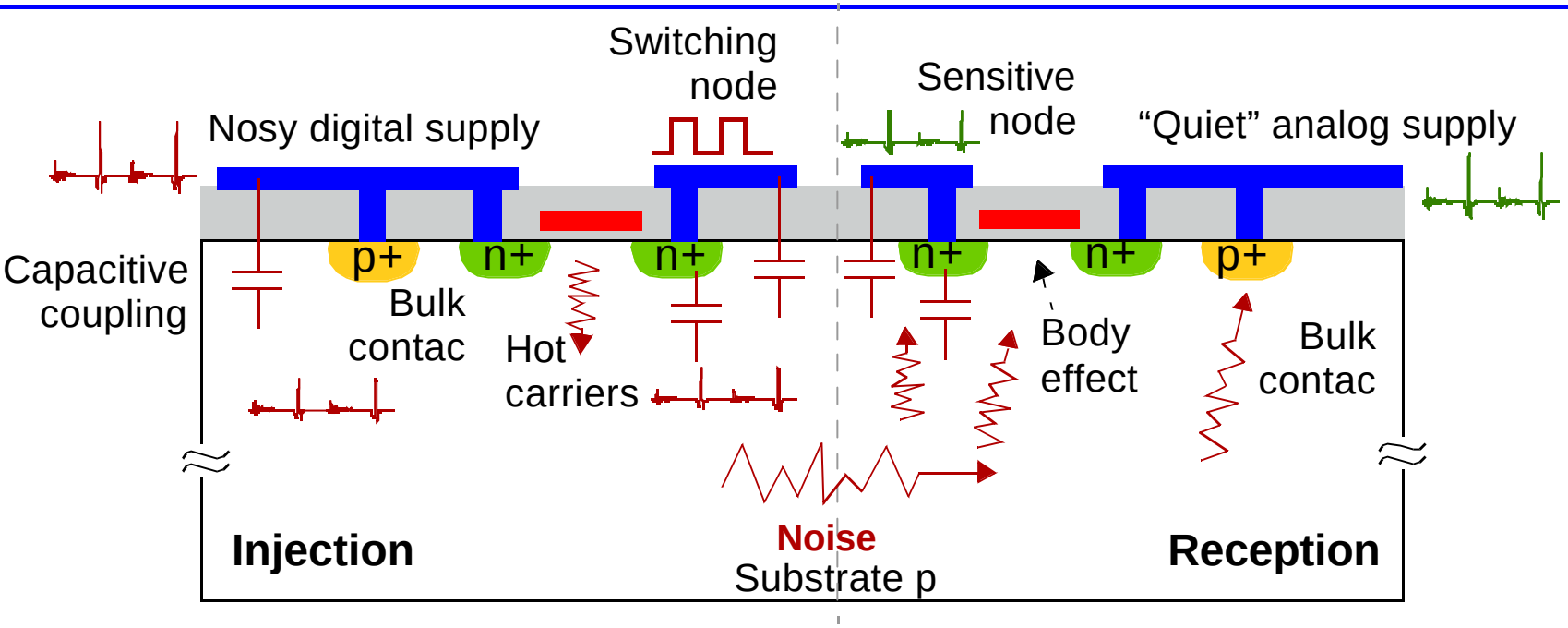




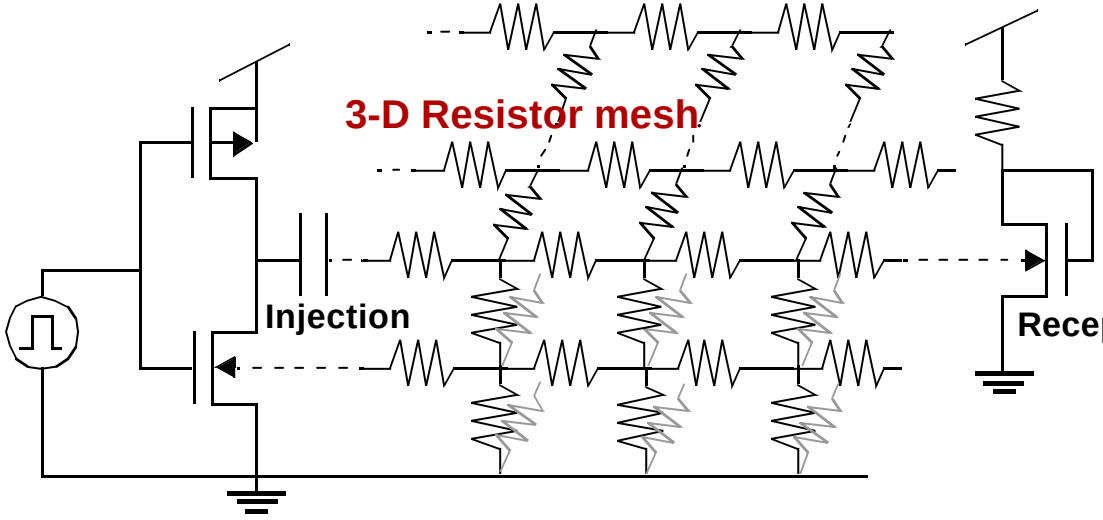
Lightly-doped low-conductive / high-resistive p- substrate

Heavily-doped high-conductive / low-resistive p+ substrate

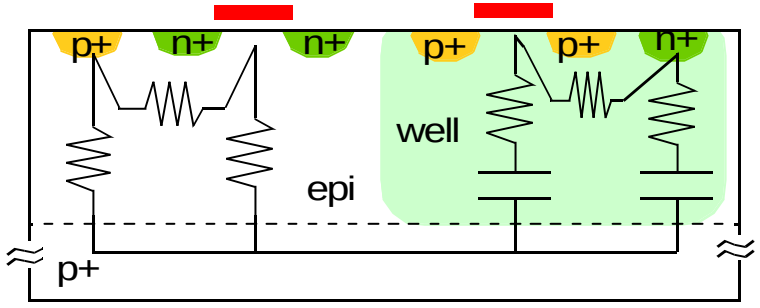
Back contact to ground allowed



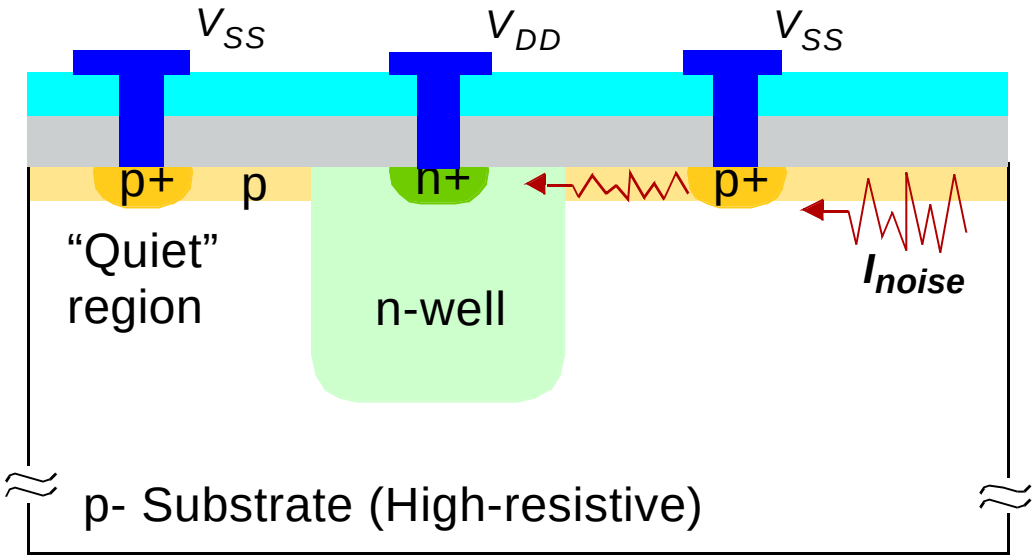
⇨ ***Substrate models*** [Verg95]



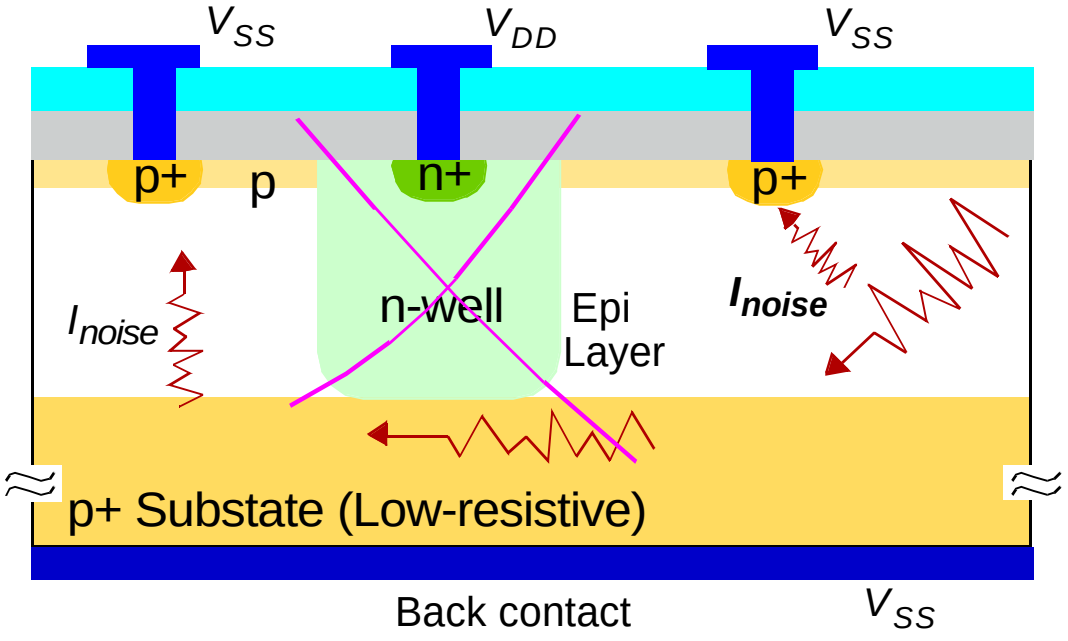
Accurate model up to 5GHz **Slow and difficult to extract**



Simplified 2-D model for p+ wafers



- **Noise current flows near surface** by a resistive material
  - Increase distance between noisy and sensitive
  - Provide a low impedance path to "drain" noise
- **Guard rings... (assume ideal pins)**
  - effectiveness depends on path impedance vs. substrate impedance. Place enough contacts.
  - position affects performance. Place p+ rings close to the noisy area. Place n+ and p+ rings surrounding sensitive area



- **Noise current flows in deep substrate,** a highly conductive material
  - Noise almost the same everywhere
- **Guard rings...(assume ideal pins)**
  - n+ rings are useless. p+ rings may help if placed very close to the noisy/sensitive area. (farther than epi thickness => useless)
  - position does not affects performance. Only number of contacts (impedance) is important.
- **Back contact...**
  - provides a low-impedance path to noise
  - But in practice (skin effect, pin parasitics) may be useless

Noise... Because...

- **increases as device area increases** — larger devices => larger junction caps.
  - Use **adjusted sizes** for every application
  - Area reduction is also a matter of noise
- **largely increases as rise/fall time decreases** — larger dV/dt => larger capacitive coupling
  - Use logic as **slow** as possible
- **in p- bulk decreases with distance** — => larger resistance in the noise path
  - **Maximise distance** between noisy and sensitive nodes
  - In practice, **not true in p+ subs**
- **sensitivity varies with transistor design**

Transconductace — Junction cap — Body effect coeff.

$$\frac{\text{substrate noise gain}}{\text{signal gain}} \approx \sqrt{\left(\frac{2\pi f C_j}{g_m}\right)^2 + \frac{\gamma^2}{4(V_{SB}+\phi_B)}}$$

Capacitive coupling term

Body effect term

- If $V_{SB} = 0V$

$$\frac{\text{substrate noise gain}}{\text{signal gain}} \approx \frac{2\pi f C_j}{g_m}$$

- Sensitivity decreases if source and bulk are at the same effective voltage; e.g. short-circuit pMOS source and n-well

[Arag99]

- Digital substrate → Digital VSS
  Analog substrate → Dedicated pin

Best

- Digital substrate → Dedicated pin
  Analog substrate → Analog VSS
- Digital substrate → Dedicated pin
  Analog substrate → Another pin
- Digital substrate → Digital VSS
  Analog substrate → Analog VSS

Normal

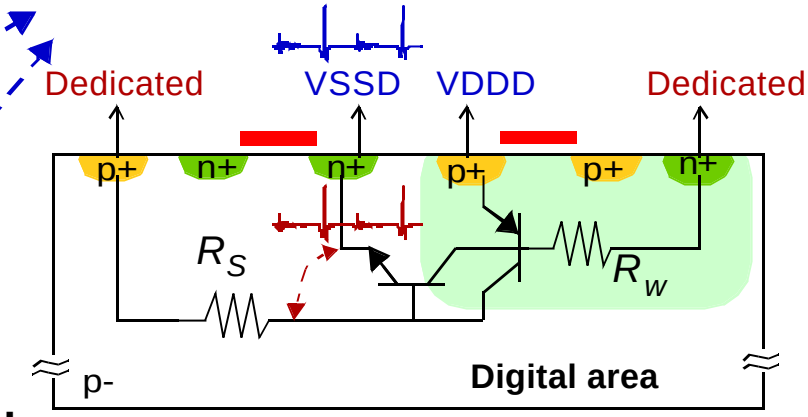
- Digital substrate → Digital VSS
  Analog substrate → Digital VSS

Bad

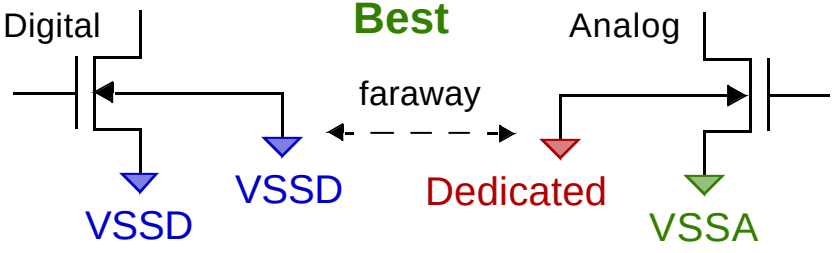
- Digital substrate → Analog VSS
  Analog substrate → Analog VSS

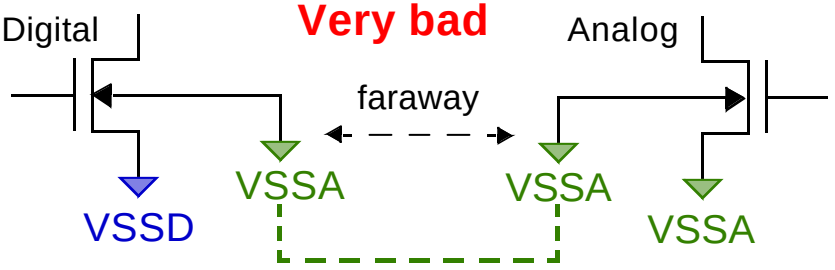
Very bad

- **May produce latch-up in digital part**

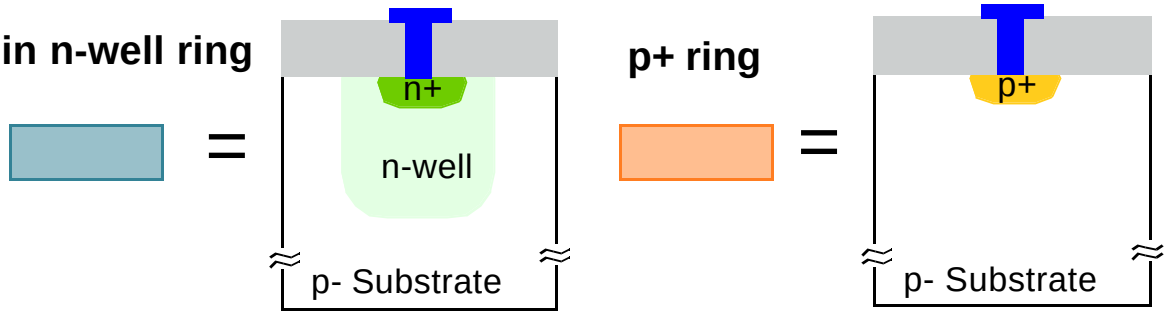


- **Never bias a p- substrate with a single source**
  - It puts in contact noisy and quiet substrate areas, thus ruining substrate provided resistive isolation

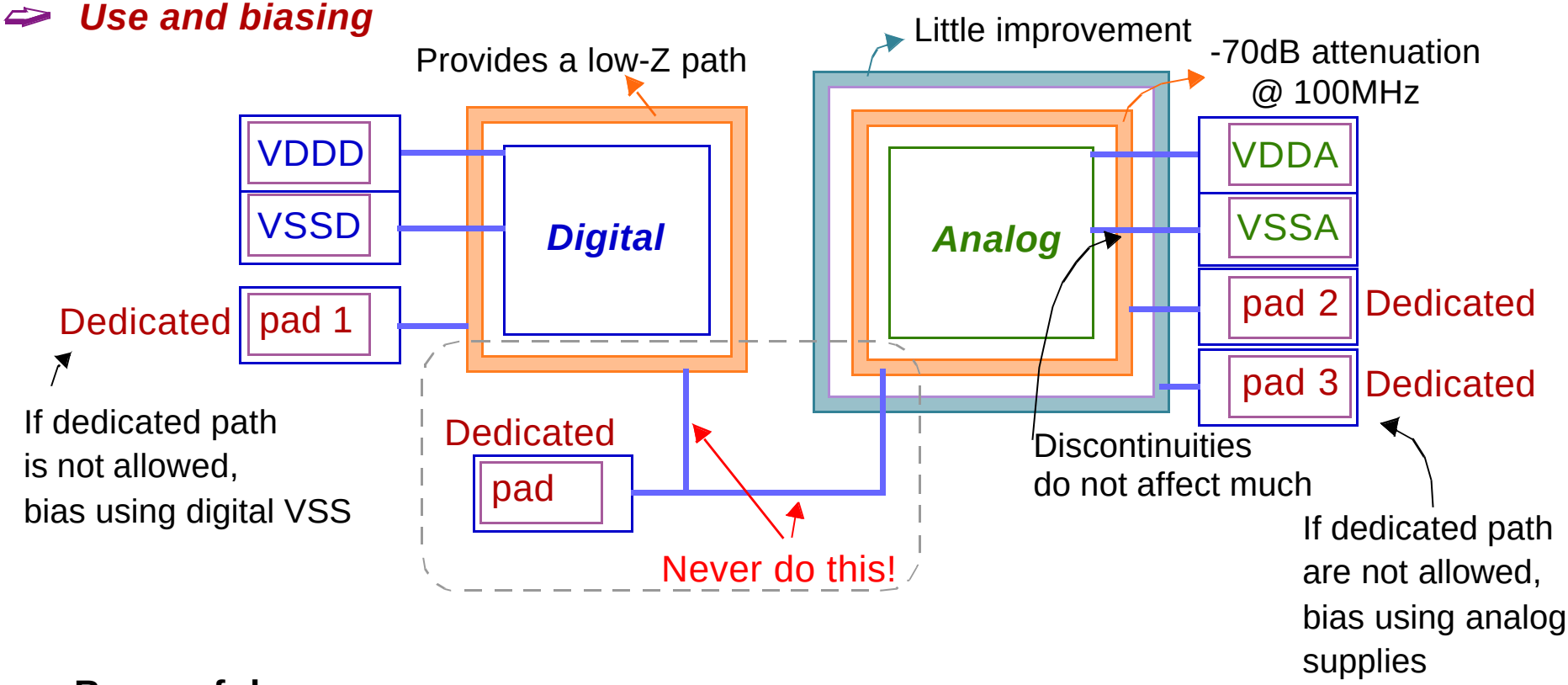




Types

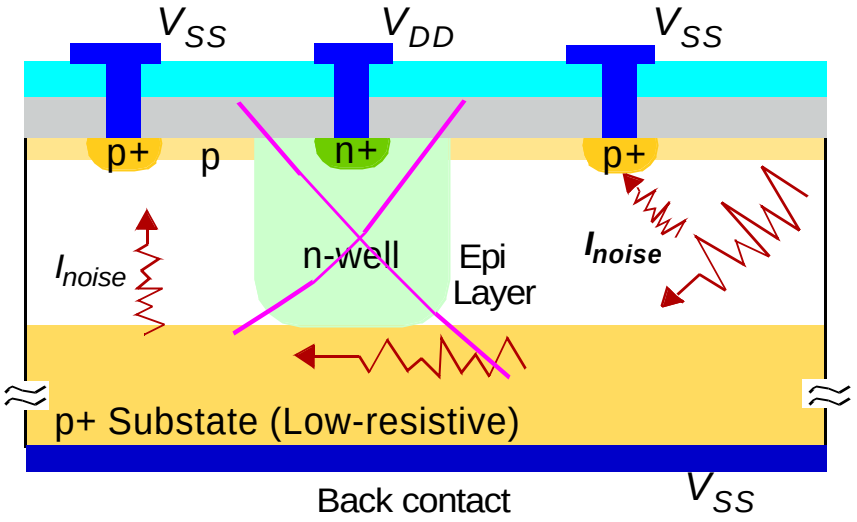


Use and biasing



- **Be careful**
  - This works only if (routing + pad + wirebond + lead + external interconnects) = **low-impedance path**

- **Noise is everywhere along the chip (through the high-conductive p+ substrate)**
  - Don't contact VSS analog to substrate! It will be quickly contaminated. Use a dedicated pad.
  - Minimize parasitic caps between analog supply and substrate: Shield
  - Even if this is avoided at the core level, the pad ring will do it!
  - Different biasing strategies show little difference
  - Back contact does not help much because of parasitics

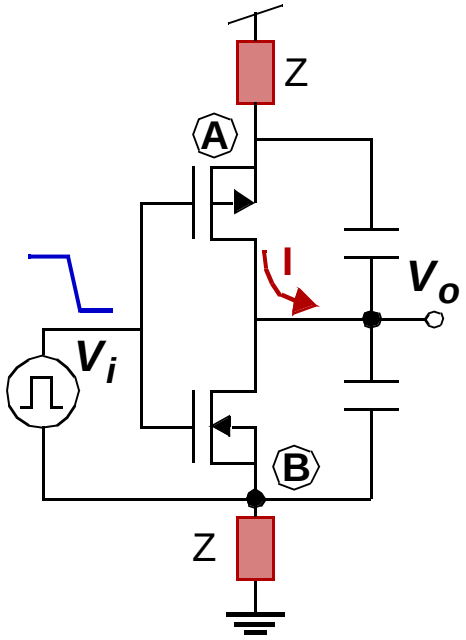


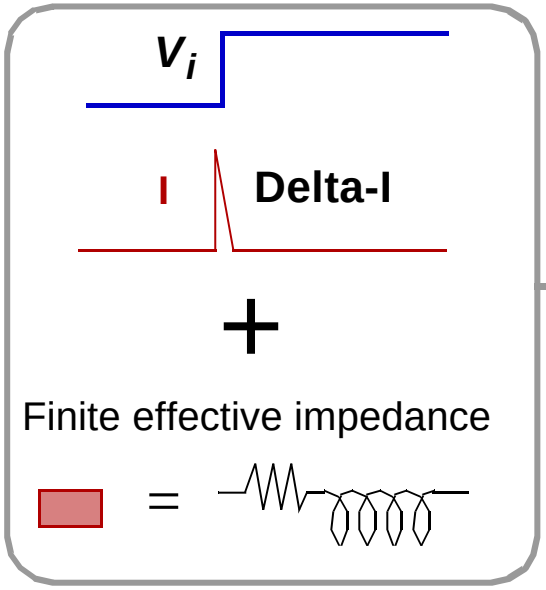
Non-general rules, They may change a lot depending on size of the digital and analog part, application, technology, etc.

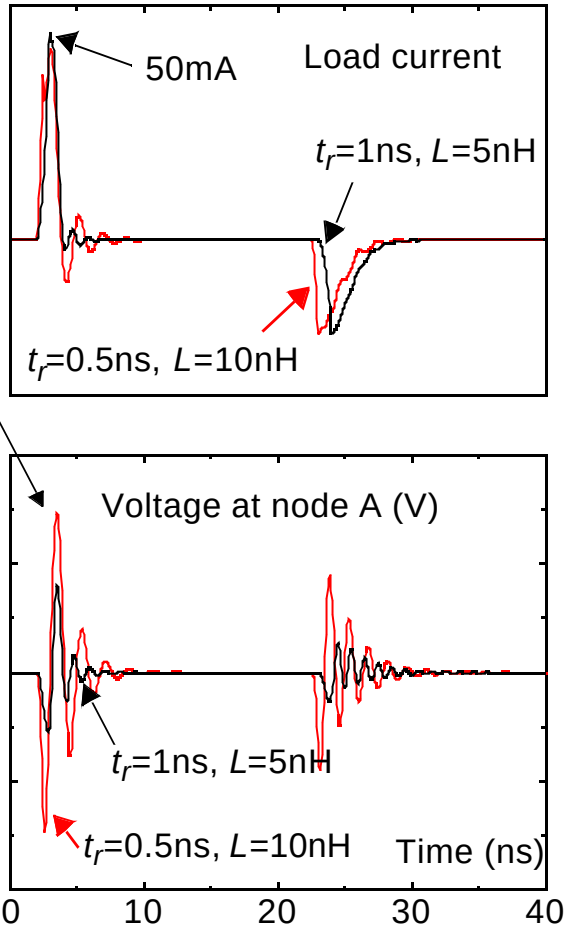
- **Guard rings?**
  - n+ in n-well rings are useless
  - p+ guard rings **surrounding** an analog block, not necessary. Only number of contacts and distance (impedance) are important.
  - If impedance is dominated by pad+package parasitics, then p+ guard rings are useless

- **In p+ substrates, noise is critically dependent on package inductance**
  - Not too much to do at the layout level
  - Solutions are at the package + board level
  - Use of circuit solutions as
    low-noise logic, trapezoidal digital buffers...
  - and on-chip decoupling devices may help

Supply bounce or Delta-I noise
Simultaneous switching noise (**SSN**)







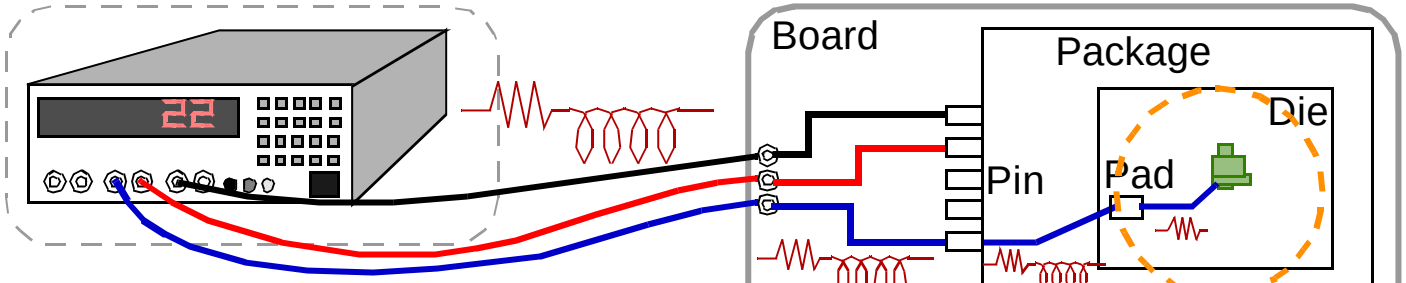
- The larger the impedance, the larger the noise

Try to minimize inductance + resistance

- The larger the current peak, the larger the noise
- The shorter the rise (fall) time, the larger the noise

Most SSN produced by I/O buffers
Use separate supply for them
(Dedicated pin + pad + routing)

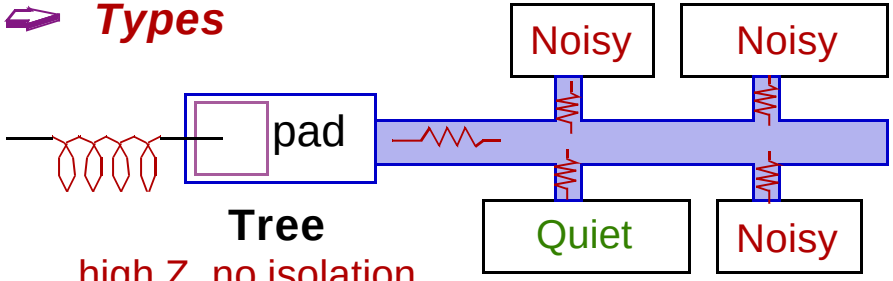
Supply distribution



Typical supply distribution system

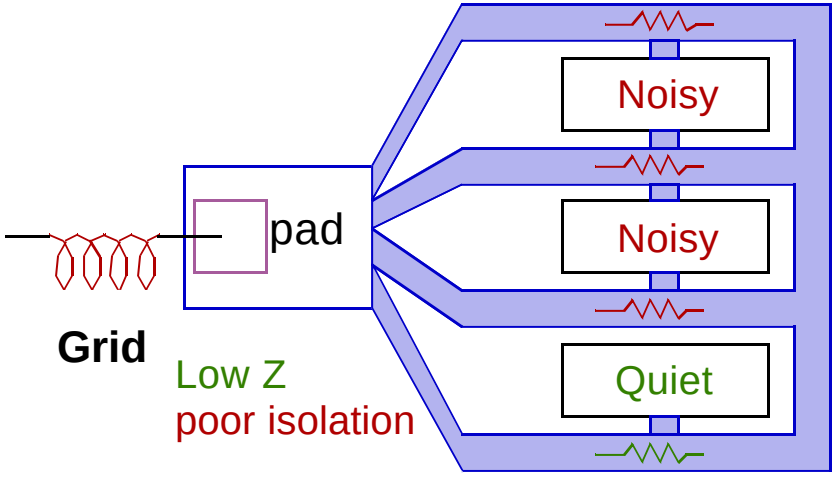
- **Once in the power and ground supplies, SSN...**
  - is transmitted to any circuit connected to the same supply
  - is coupled to substrate, other signal and/or biasing lines

Types



Tree

high Z, no isolation



Grid

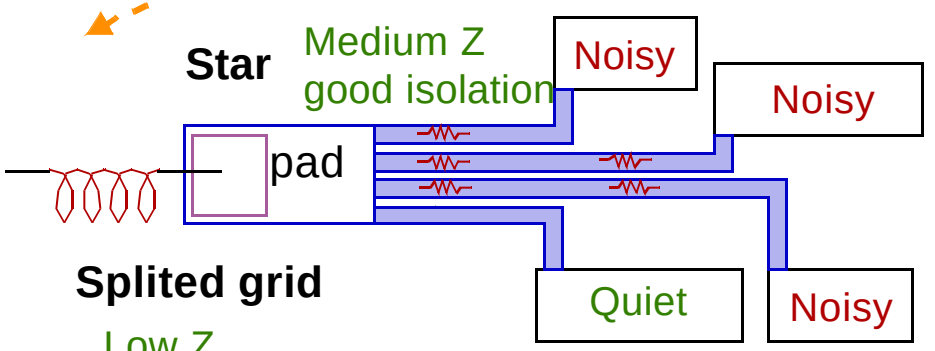
Low Z

poor isolation

Star

Medium Z

good isolation

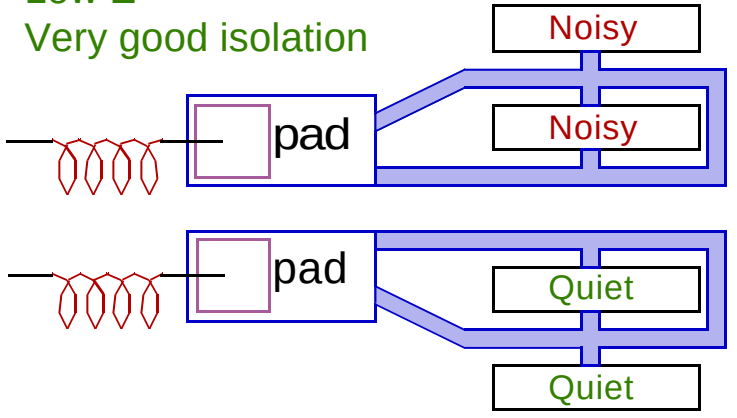


Splited grid

Low Z

Very good isolation

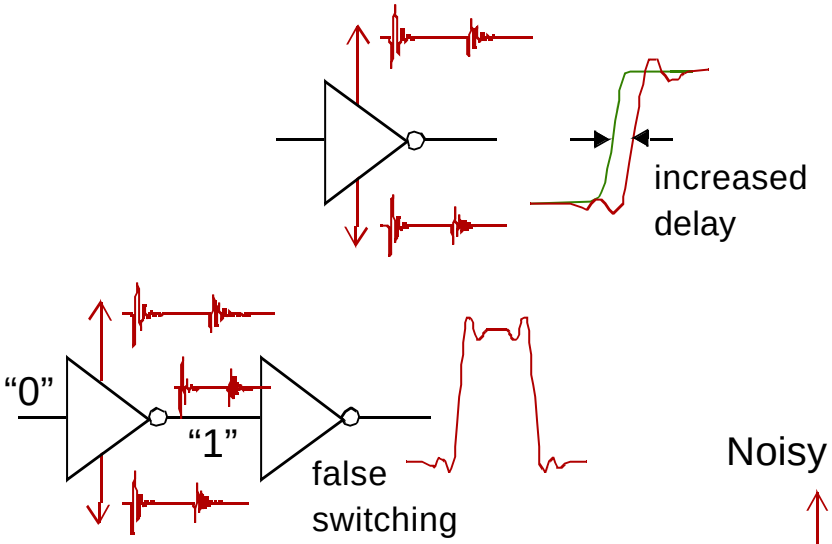
[Verg95]



- **Substrate (p+) is an excellent path for SSN**

Digital circuits

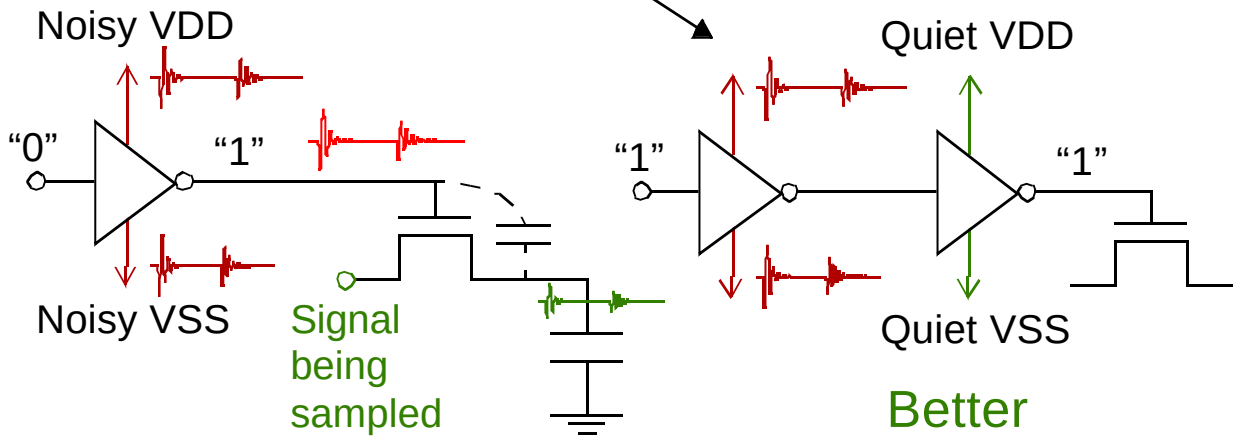
- **SSN causes...**
  - delay to increase, through variation on current due to supply bounce
  - false switching, due to changes in voltage driving a non-switching gate



Analog and mixed-signal circuits

- **SSN causes...**
  - Distortion and phase errors in linear circuits (Amplifiers, Filters, etc.)
  - **Dynamic range reduction** in ADCs and DACs

- **Be careful with digital/analog interface points**
  - Clock phases controlling analog switches
  - Supplying the last inverter with a clean voltage helps



⇨ ***SSN reduction techniques***

- **Proper synthesis of the digital circuitry**
- **Control of the digital buffer transition**
- **Use of constant-current logic**

Trying to minimize SSN injection

- **Proper selection of packages and pin assignment**
- **On chip decoupling**

Trying to attenuate SSN impact

⇨ ***Proper synthesis of digital circuitry*** [Arag99]

- **Reduce the number of gates switching simultaneously**
  - SSN is proportional to the number of gates switching
  - Keep digital blocks quiet when not used
- **Adjust timing to the application requirement**
  - SSN is inversely proportional to the rise (fall) time of the switching signal
  - Do not use oversized logic gates
  - Pay special attention to the transition at the input of the output buffers

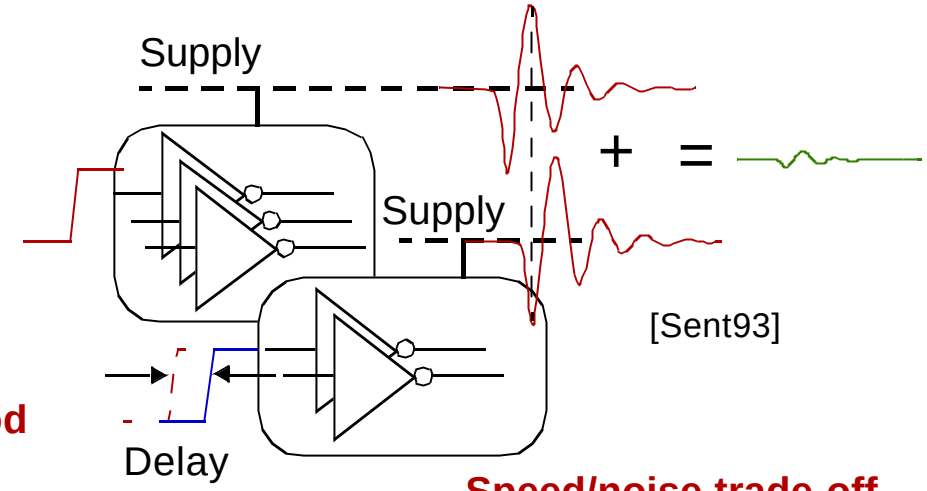
- **Set the minimum cost (minimum area) option when synthesizing from VDHL**

- **Manually size critical blocks**

⇨ *Control of the digital buffer transition*

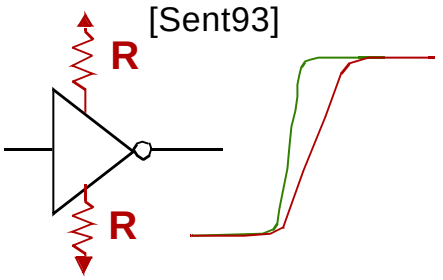
- **Skewing**
  - ♦ Delay switching of a part of the output buffers with respect to the other part
  - ♦ If the period of the ringing is know, delay can be adjusted to reduce overall ringing

The value of the ringing period must be known a priori



Speed/noise trade-off

- **Controlling slew-rate**
  - ♦ Reduces the clock edge slope or changes it during the transition
  - ♦ e.g.: resistor added in the switching current path to limit its peak value

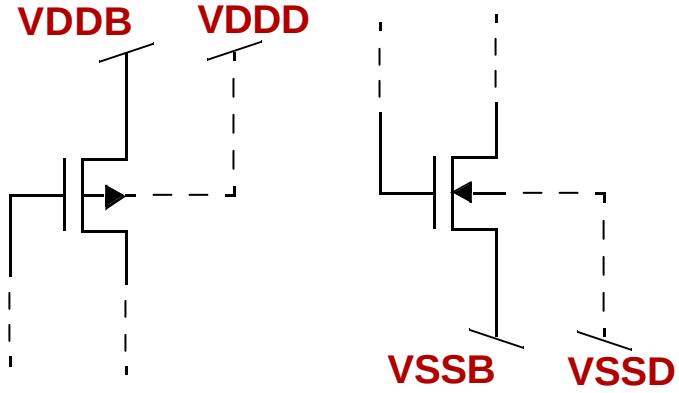


- **Damping resistor R,**
  - ♦ must be large to attenuate ringing
  - ♦ must be small to keep speed

- **Reducing supply voltages (in prototyping)**
  - ♦ Reduces current peak => largely reduces SSN power
  - ♦ Separately supply digitally buffers and reduce its voltage

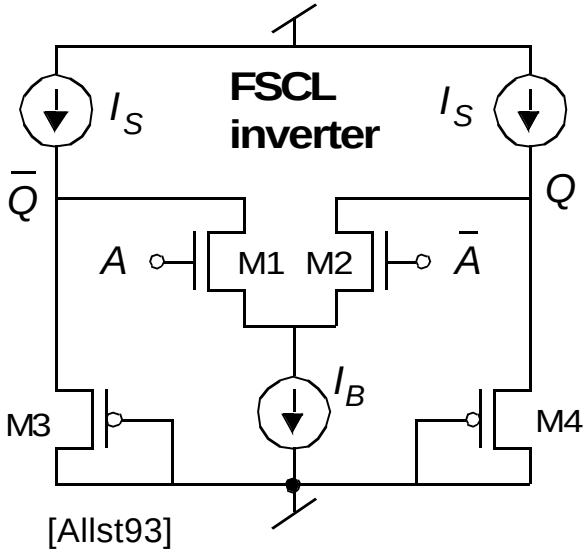
Be careful with latch-up!

External timing and high/low levels must be readjusted

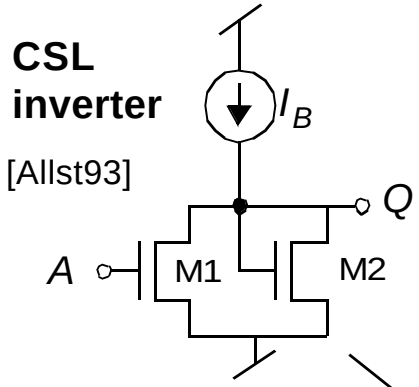


Use of constant-current logic

- Ideally, there are no current peaks => no SSN
- Used as a complement of the CMOS logic for high-speed digital blocks, I/O buffers



[Allst93]



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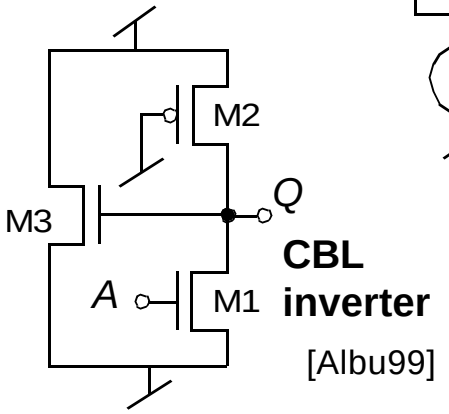
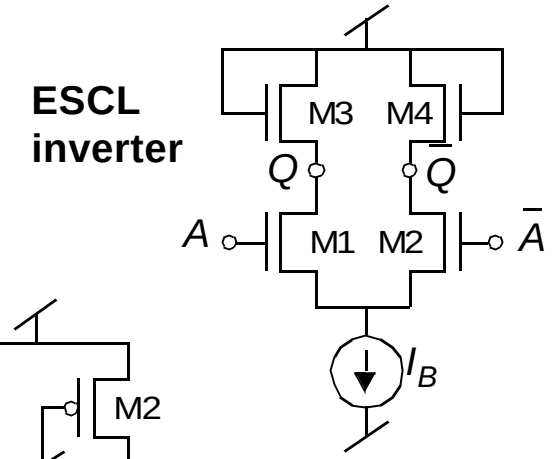
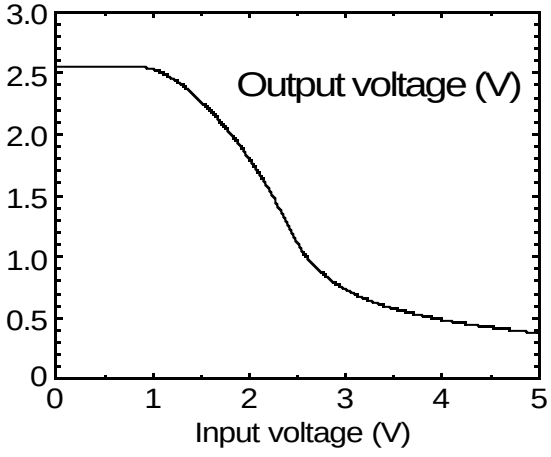


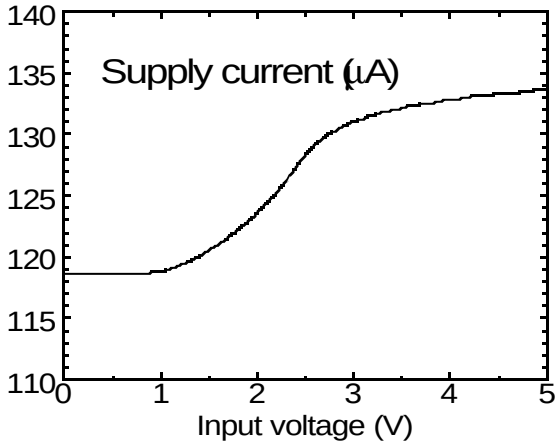
CBL inverter

[Albu99]



- SSN two order of magnitude smaller than that of conventional CMOS
- Reduced output voltage swing
- Static power dissipation

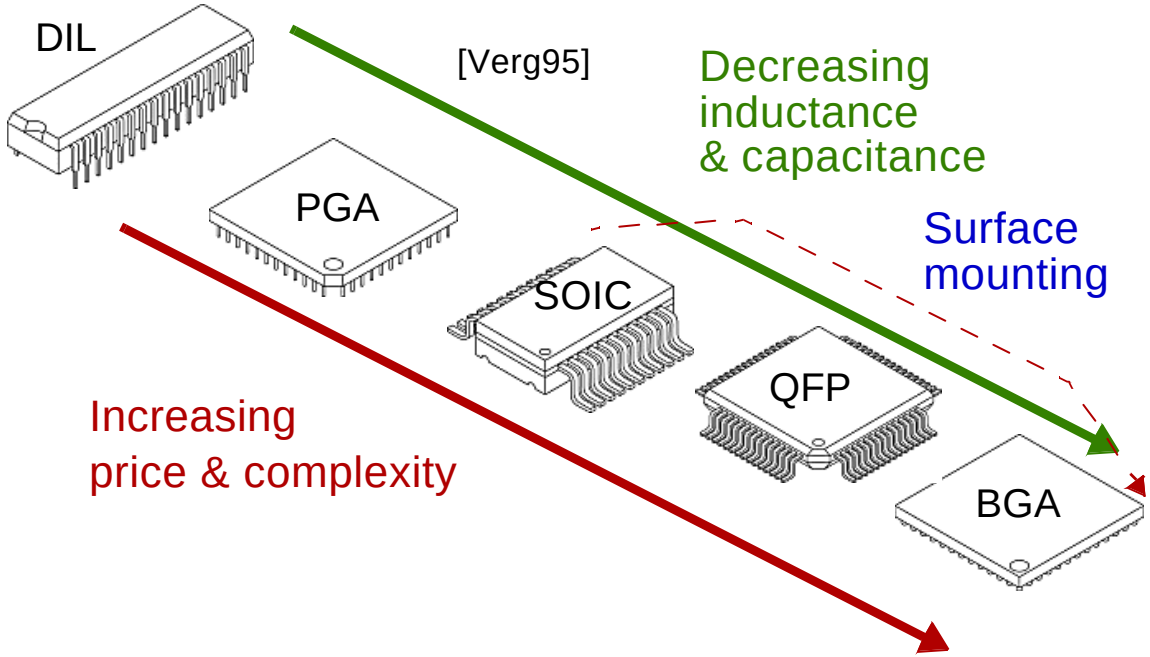


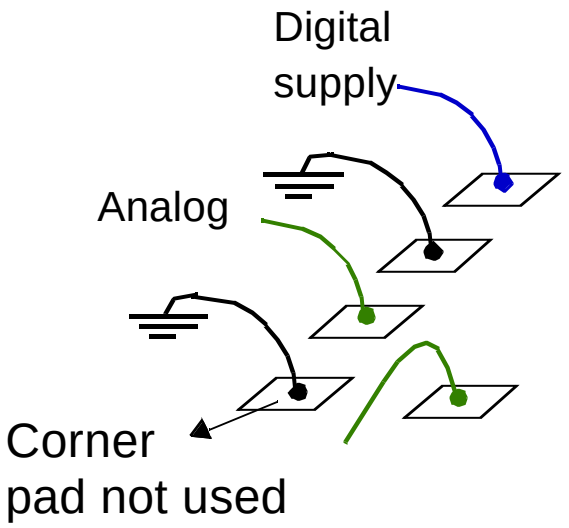


Proper selection of packages and pin assignment

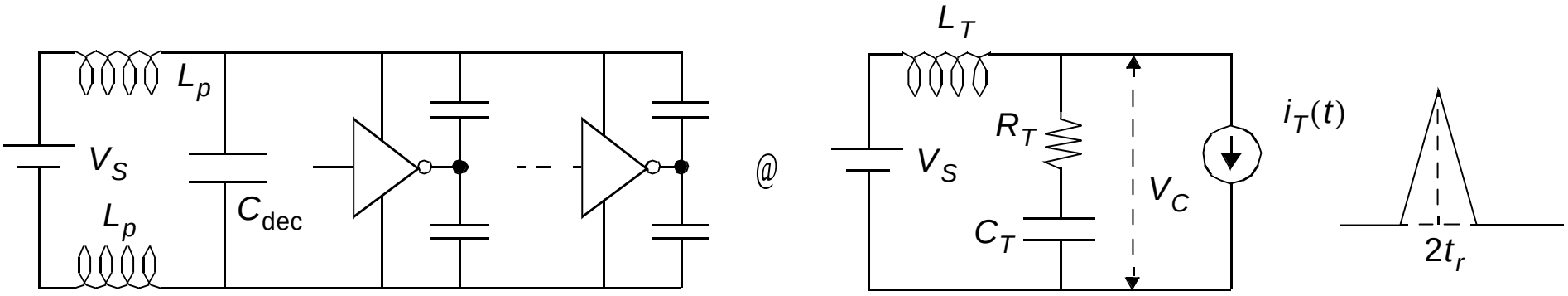
- **Target: minimum inductance**
  - **Use surface mounting packages** (SMT, SOIC, QFP, L~3-7nH)
  - The larger the pin count, the larger the inductance
  - Be careful with **DIL** or large **PGA** (typical L ~ 20nH)
  - **Assign power and ground to centre pins** (corner pins have ~ 40% more inductance) [Will96]
  - **Assign several pins and pads** to the critical voltages (supply, references, ...)
  - Place a **grounded pin** between each pair of used pins
  - If possible, **solder the die directly on PCB** (L < 1nH)

Sockets largely increases inductance!



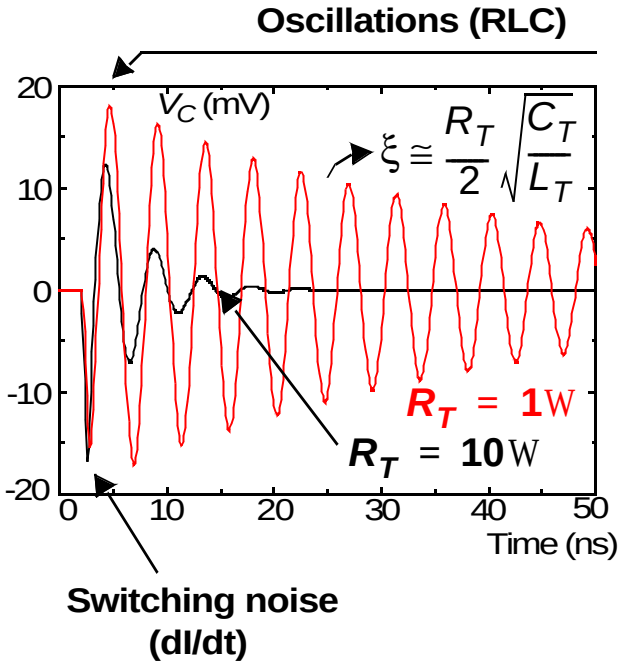


On-chip decoupling

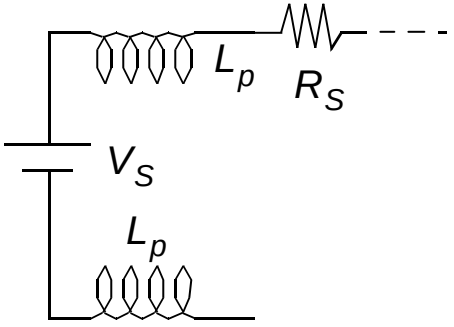


$$\omega_0 \cong 1/(\sqrt{L_T C_T})$$

- **Problem: R_T usually small => low damping factor**
  - Ringing even more harmful than SSN itself
  - If any of the clock harmonics coincides with the resonant frequency, constructive SSN largely amplifies the effect

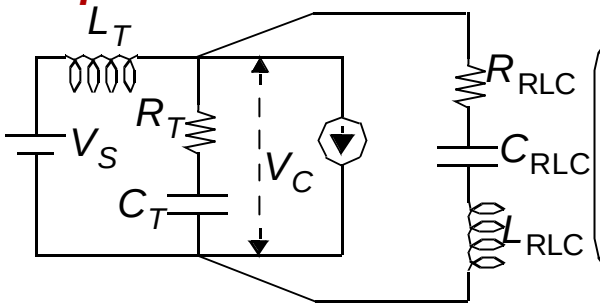


- **Simplest solution: increase R_T**
  - Add a resistor in series with the supply inductance, but then
    - Resistive switching noise is increased
    - Power dissipation is increased



⇨ *More sophisticated on-chip decoupling techniques*

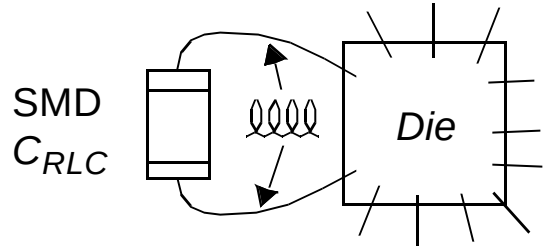
- **RCL decoupling method** [Inge97]
  - Connecting a properly sized RLC net in parallel to the on-chip decoupling capacitor prevents oscillations
  - L_{RLC} can be implemented using wire parasitic inductance. C_{RLC} as an "in"-chip SDM cap.

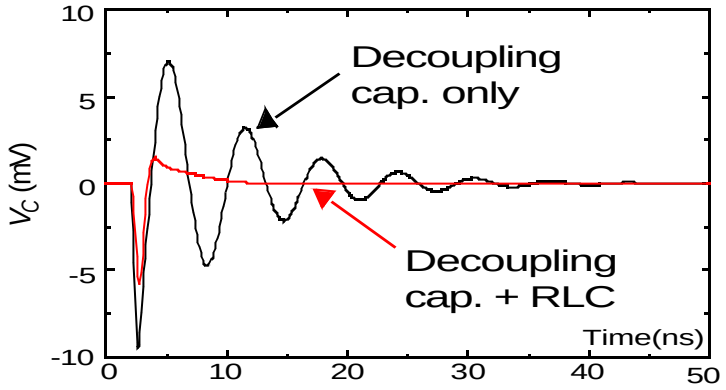


L and C choice

$L_{RCL}C_{RLC} \cong L_T C_T$

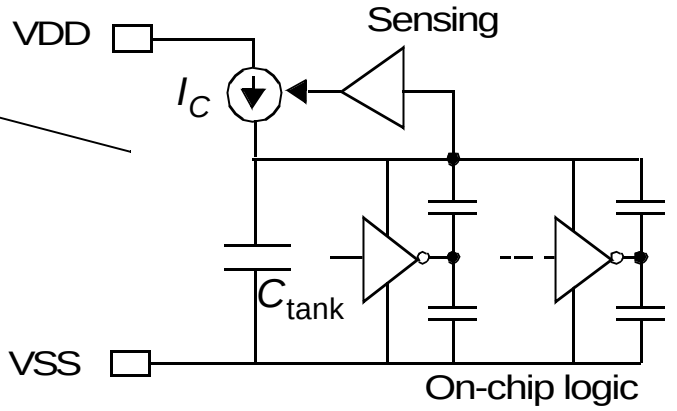
The larger C_{RLC}/C_T, the better





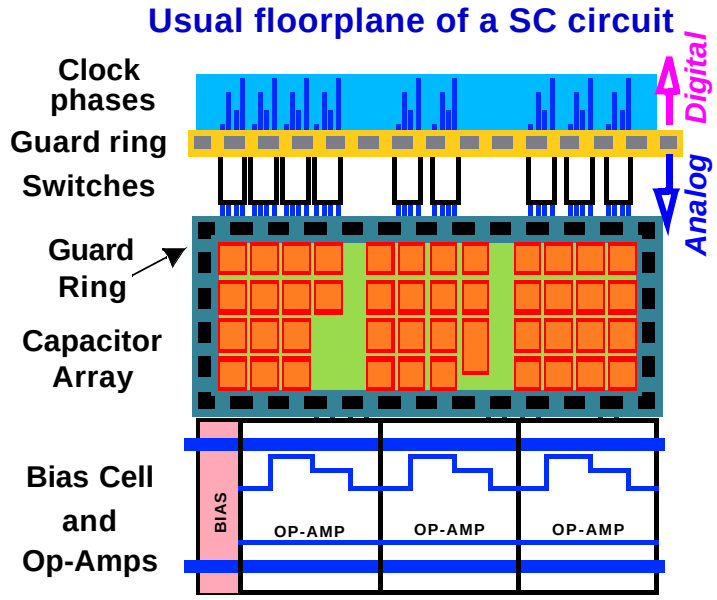
- **Tank CMOS method** [Arag99]
  - On-chip logic isolated from external supply and supplied directly by a tank capacitor
  - Voltage across C_{tank} is kept by a controlled current source. *IC* is connected only when V_{tank} drops below certain level

70% reduction on SSN has been reported



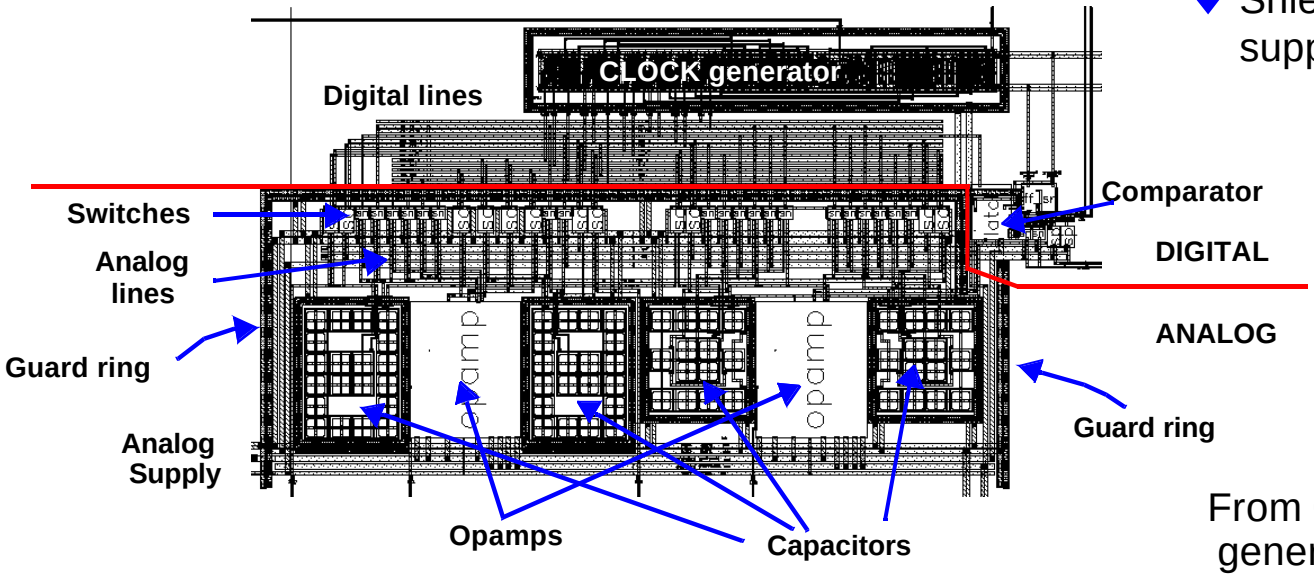
⇨ *Final recommendation*

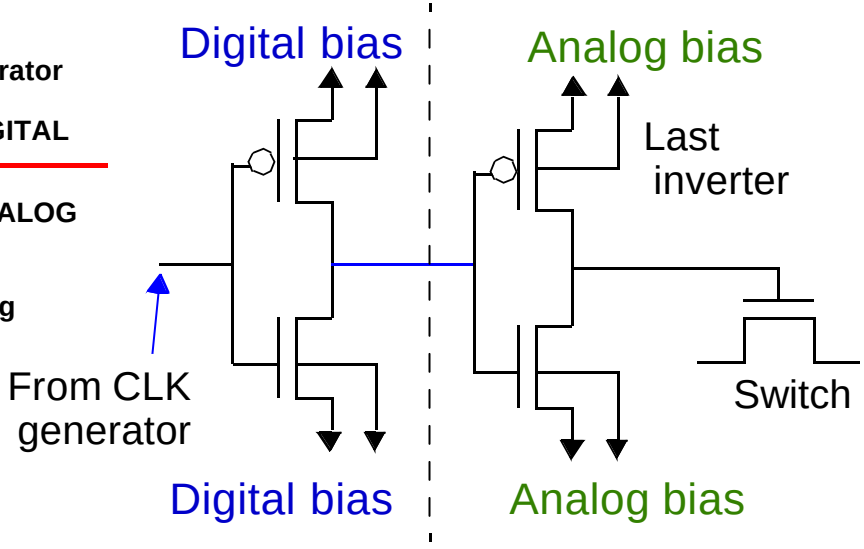
Avoid synchronizing critical analog operations with the clock edge



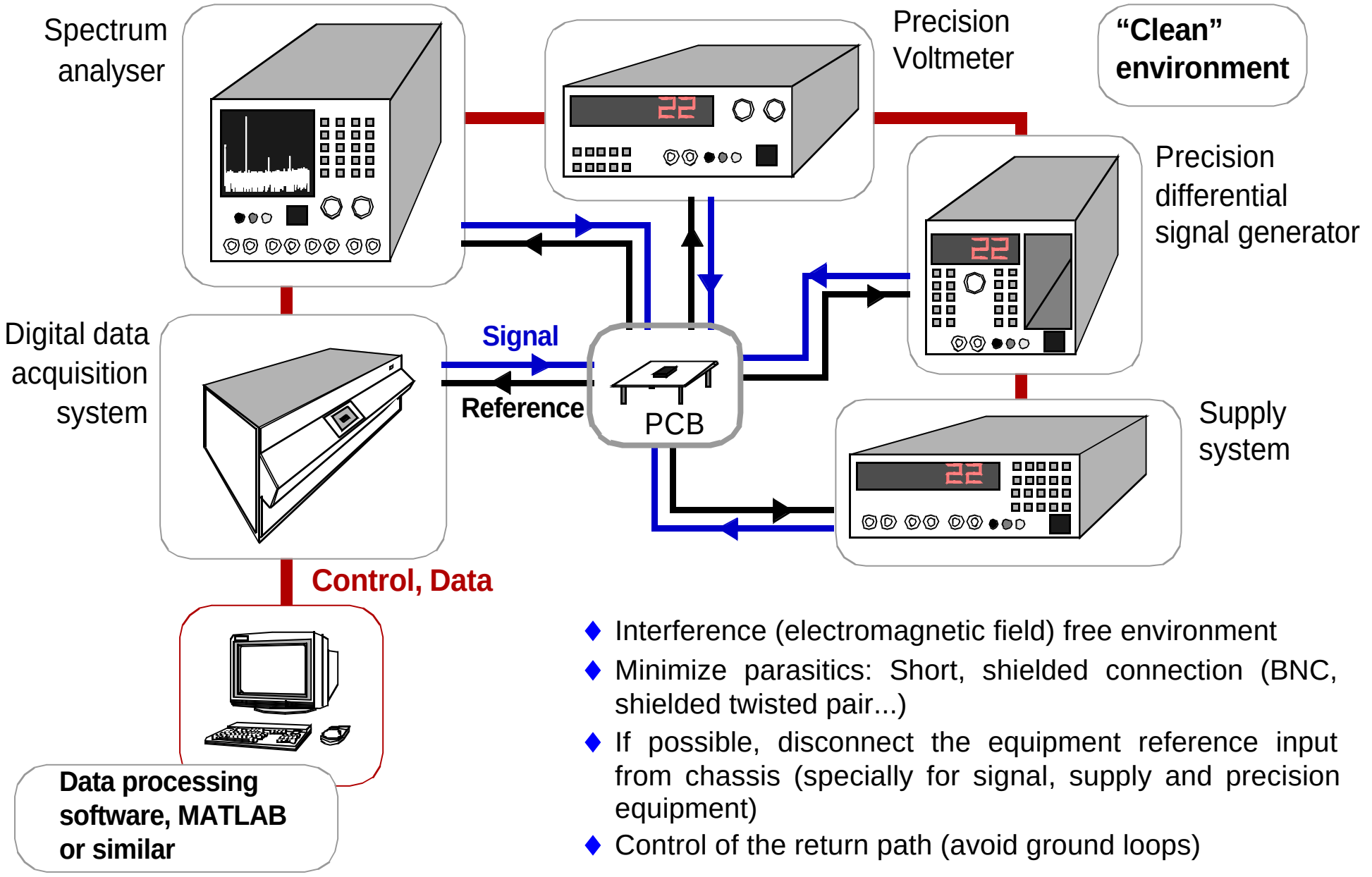
- **Multiple supply**
  - VDDa, VSSa: Analog block supply
  - VDDs, VSSs: Analog substrate and n-well biasing
  - VDDd, VSSd: Digital core supply and substrate biasing
  - VDDb, VSSb: Digital buffer supply and substrate

- **Analog blocks**
  - Common-centroide techniques in opamp and latch transistors, and in capacitors
  - Symmetrical routing
  - Shielded capacitors and analog supply distribution



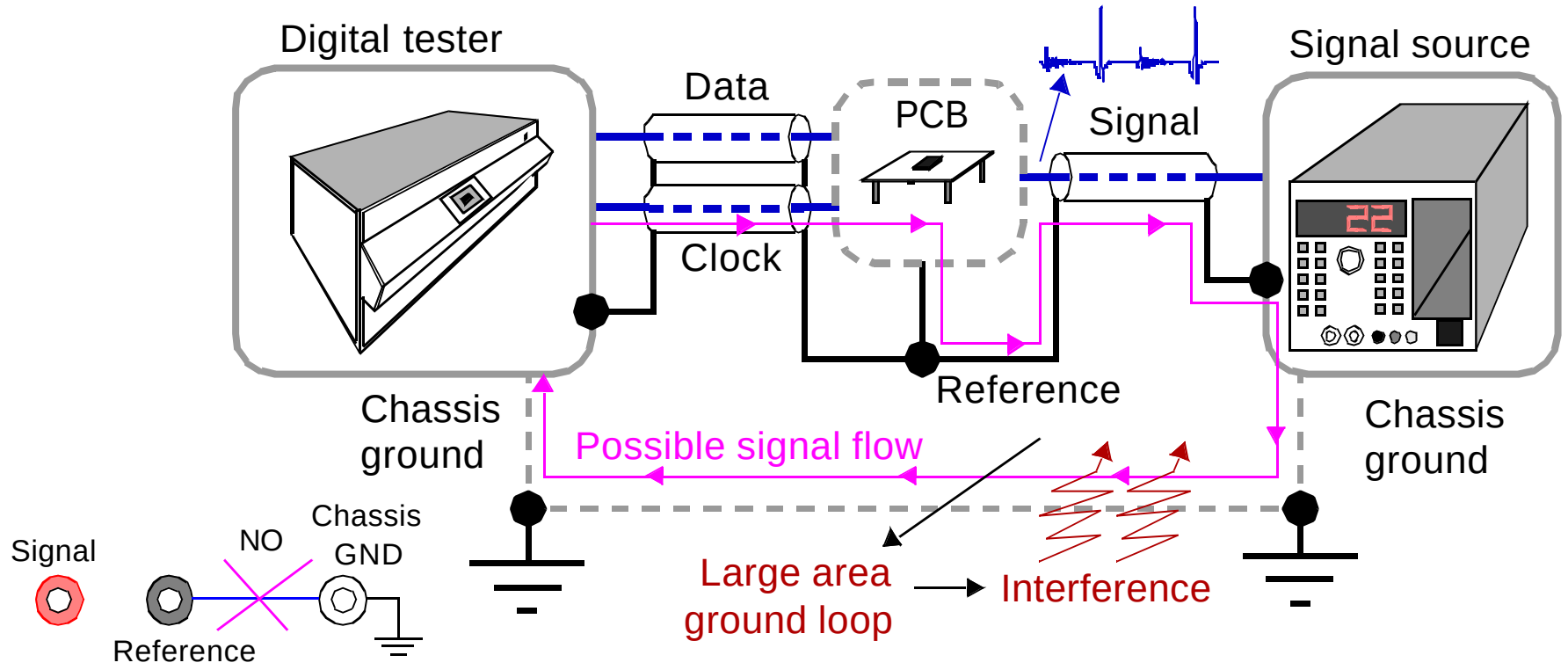


0.7μm CMOS poly-diff caps 2-metal (p- substrate)
0.42mm^2



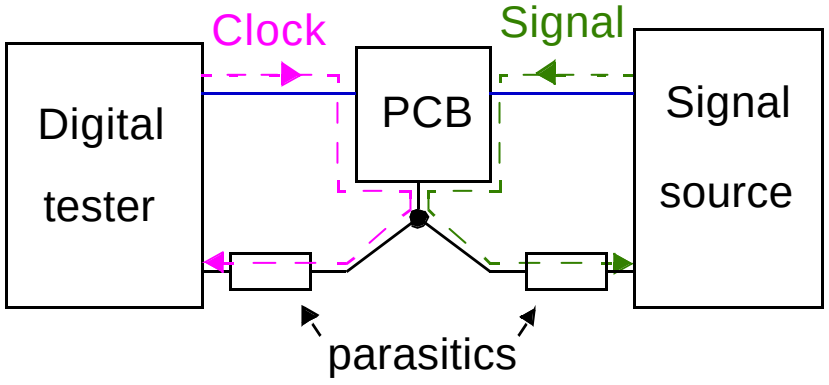
- Interference (electromagnetic field) free environment
- Minimize parasitics: Short, shielded connection (BNC, shielded twisted pair...)
- If possible, disconnect the equipment reference input from chassis (specially for signal, supply and precision equipment)
- Control of the return path (avoid ground loops)

Ground loop effects



How to avoid a ground loop? Open it

- Use floating input signal and supply sources (Do not connect signal reference to chassis)
- Make return path shared by noisy and sensitive signals as short as possible (a single point, ideally)



ADC and DAC testing

Static

Clock → max. rate

Signal → DC or low frequency

DC Accuracy

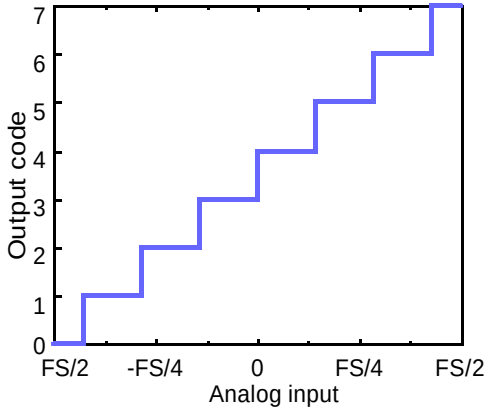
Offset

Gain error

Non-linearity INL, DNL

missing codes

non-monotonicity



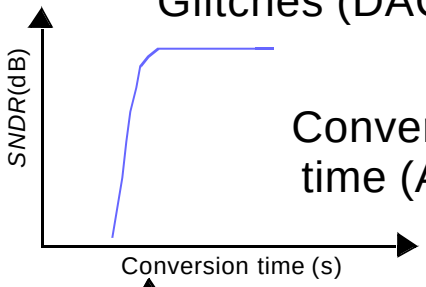
Dynamic

Clock → max. rate

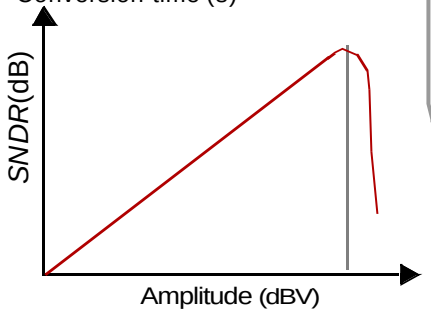
Signal → variable freq. & amplitude

Dynamic non-linearity test

Settling time, Glitches (DAC)



Conversion time (ADC)



Noise

Signal-to-noise ratio

SNDR (SINAD)

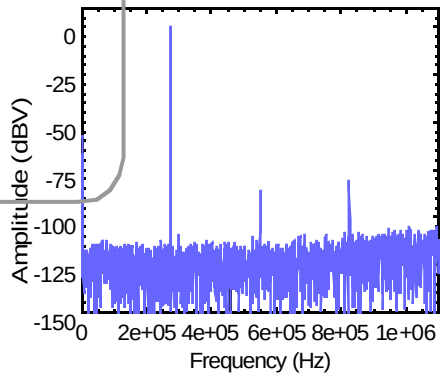
Dynamic Range, ENOB

Distortion

THD

IP3

SFDR



Using MATLAB

- **Windowing the signal...**

```
>> Np = # points;
>> W = hanning(Np);
>> xw=W.*x;
```

- **FFT...**

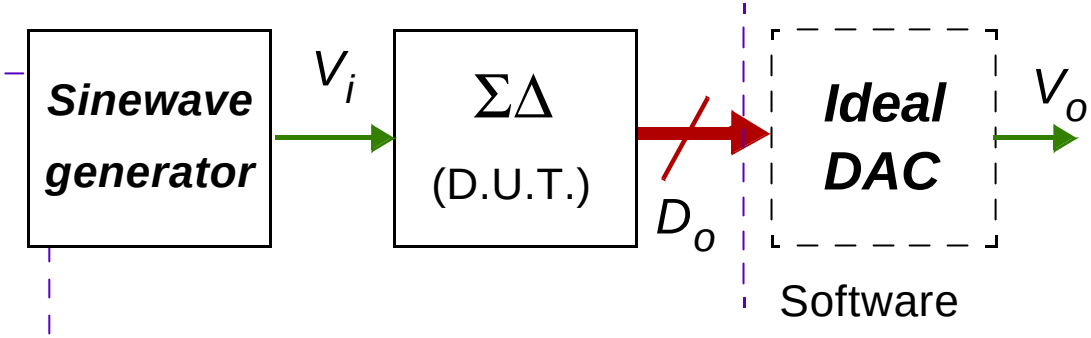
```
>> pxx = abs(fft(xw/sqrt(Np))).^2;
>> pxx = 2*pxx/norm(W)^2; % factor 2 because
   only half of the spectrum is plotted
```

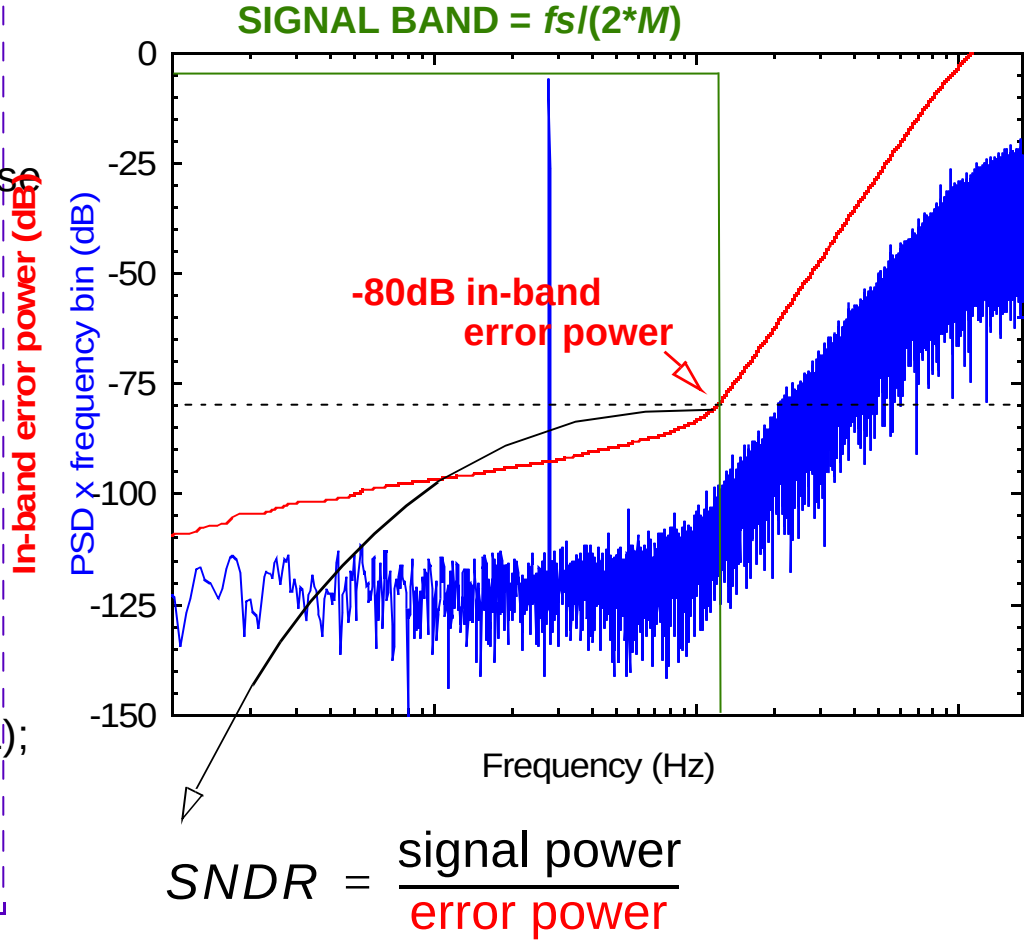
- **Plotting...**

```
>> f=(1:ceil(Np/2))*fs/Np;
>> pxx=pxx(1:ceil(Np/2));
>> semilogx(f,10*log10(pxx))
```

- **SNDR estimation**

```
>> [pxxm,index]=max(pxx(BAND));
>> SIGNAL=index-:index+5;
>> noise=sum(pxx(BAND))-sum(pxx(SIGNAL);
>> psignal=sum(pxx(SIGNAL));
>> SNDR=10*log10(psignal/pnoise)
```

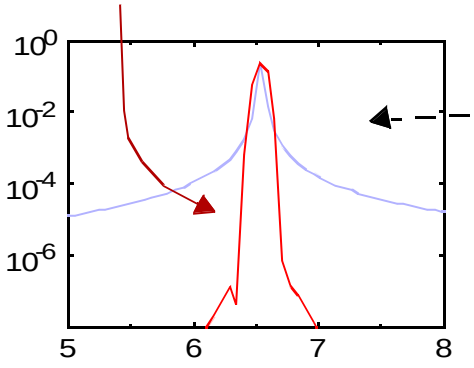


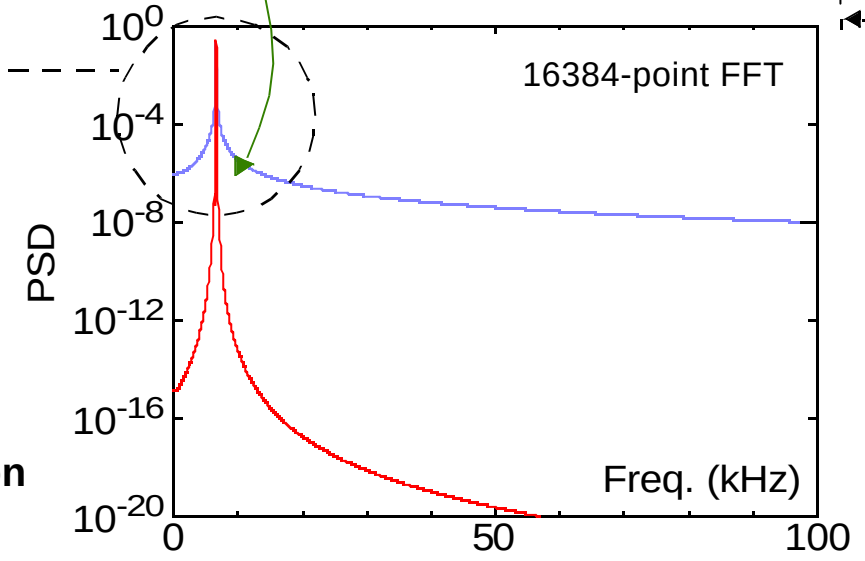


$$SNDR = \frac{\text{signal power}}{\text{error power}}$$

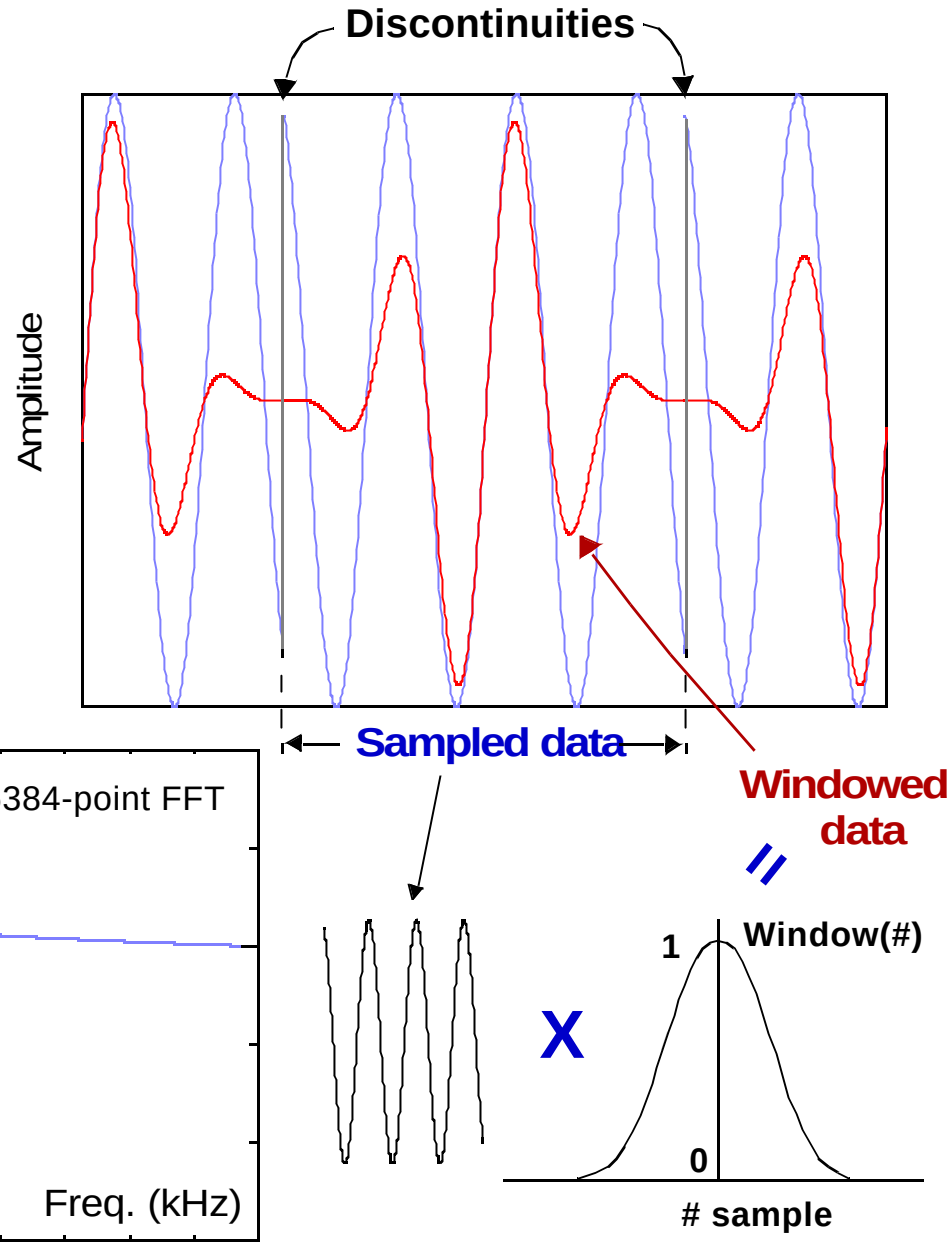
Data windowing

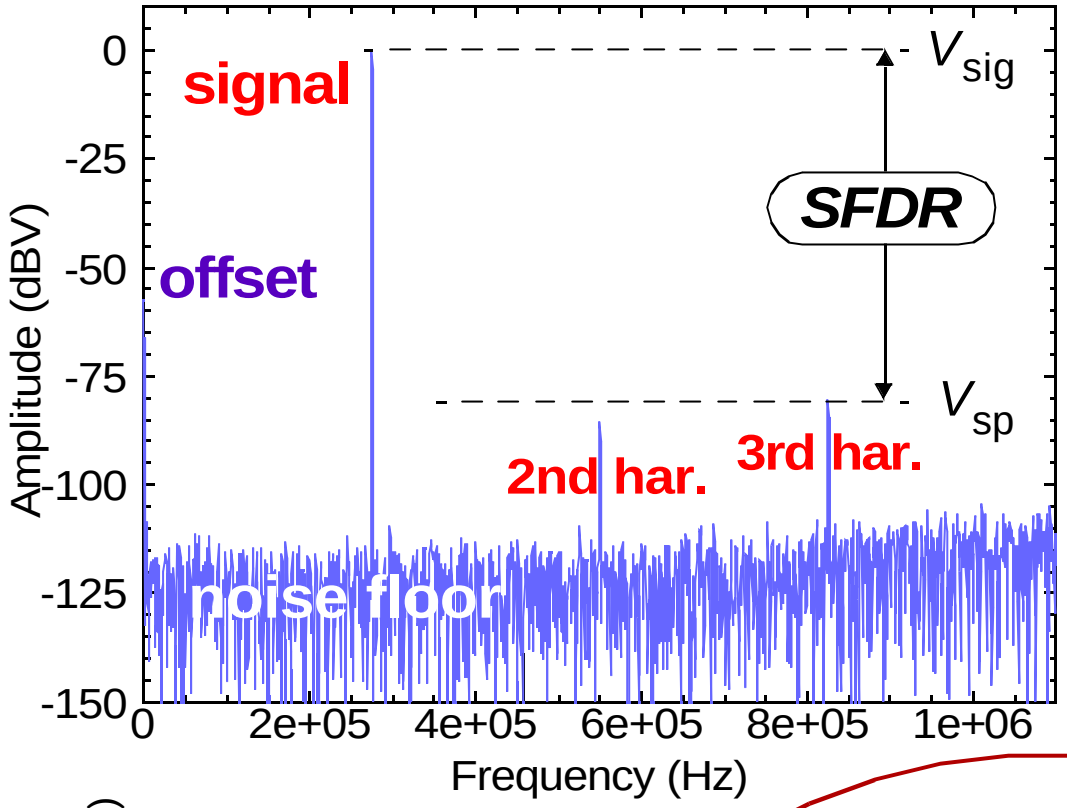
- **Required when sampled data do not contain an integer number of signal periods**
  - FFT assumes that sampled data are periodic with period equal to the sampled time slot
  - Such periodicity may require a “jump”, thus corrupting the results
  - Windowing alter start and end data to avoid discontinuities
- **Windowing reduces sidelobes but also reduces frequency resolution**





- **Compromise between sidelobe suppression and frequency resolution**





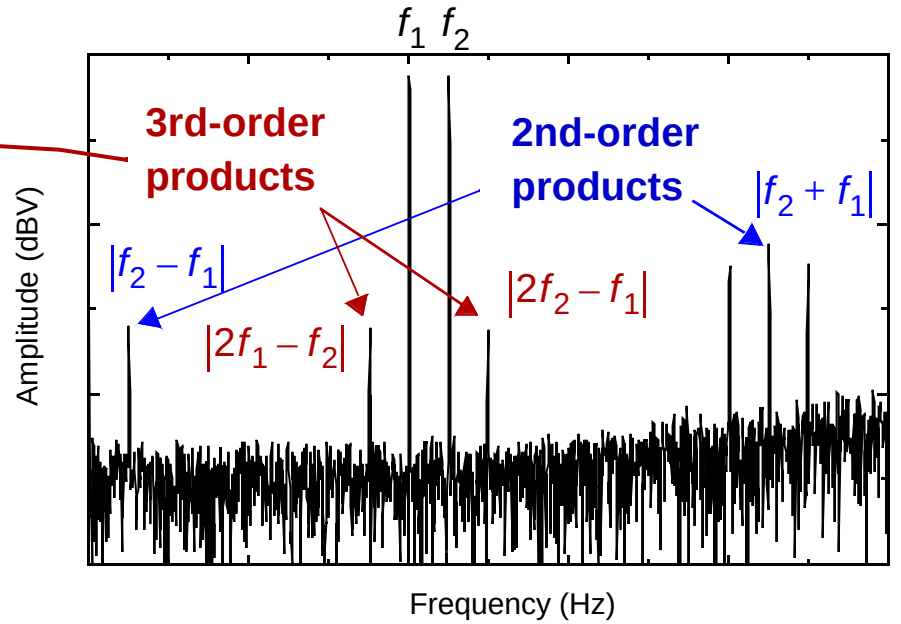
⇨ ***Total harmonic distortion (dB)***

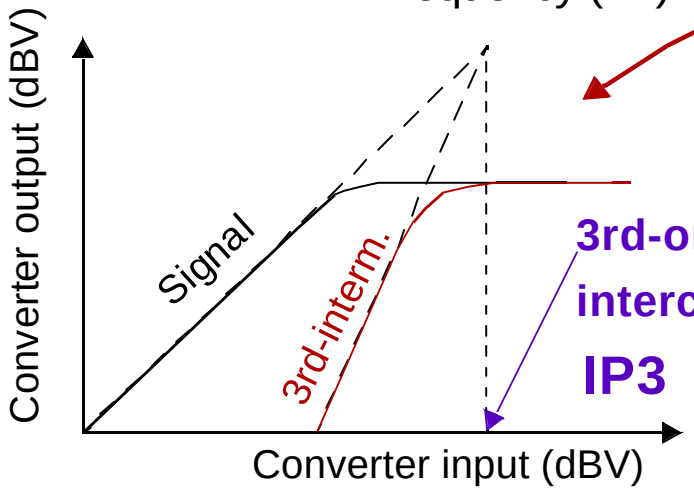
$$THD|_{dB} = 10\log_{10}\frac{\sum V_{harj}^2}{V_{sig}^2}$$

⇨ ***Spurious-free dynamic range (dB)***

$$SFDR|_{dB} = 20\log|_{10}(V_{sig}/V_{sp})$$

2-tone input





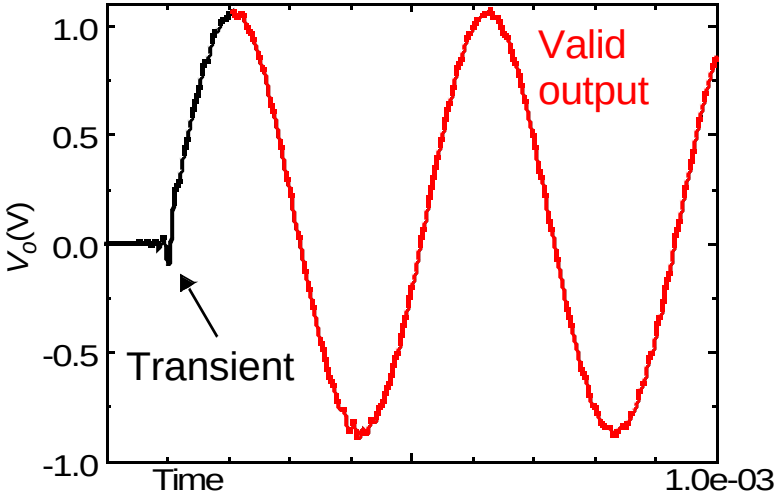
Difficult to remove when $f_1 \approx f_2$

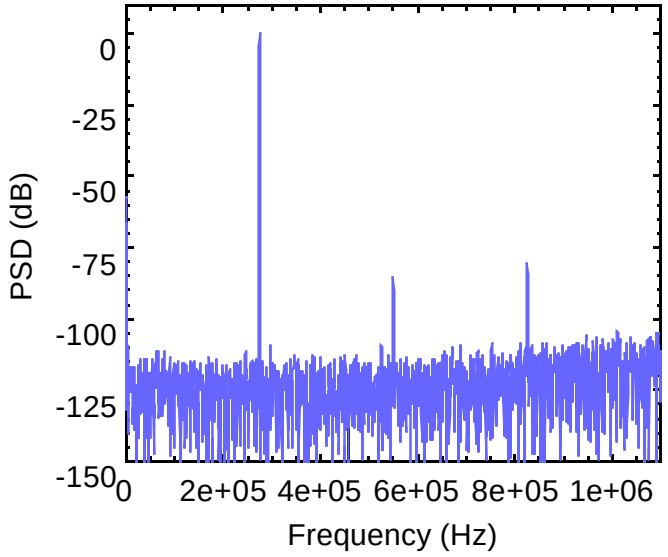
3rd-order intercept point

IP3

⇨ *Minimum Sinusoidal Error (MSE) method*

- **Basis:**
  - **Apply a sinusoidal input**
  - **Fit the converter output to a sinewave of the same frequency + offset + some harmonics**
  - **The fitting coefficients are offset and harmonic amplitudes**
  - **The fitting error is noise**





$$V_{fit} = V_{off} + \sum A_i \sin\left(2\pi j \frac{f_x}{f_s} + \phi_j\right)$$

V_{off} = 85.4mV
A_1 = 960mV
A_2 = 9.5mV
A_2 = 3.2mV
Noise = 0.1mV_{rms}

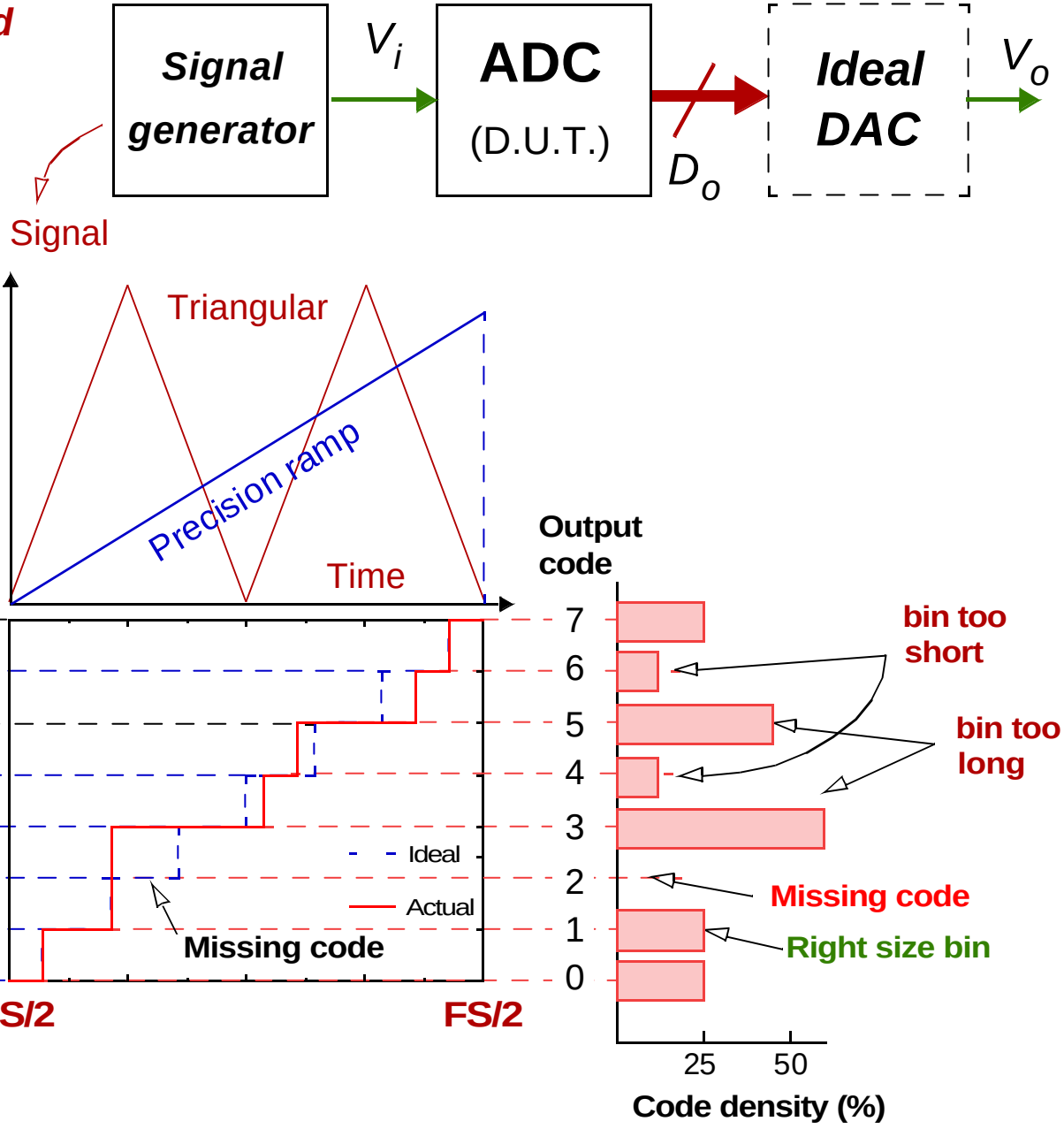
SNR = 37dB
THD = –40dB

Pros/Cons

- No FFT required
- Requires a reconstruction filter
- Slow for large number of harmonics
- Non-convergence for very corrupted data

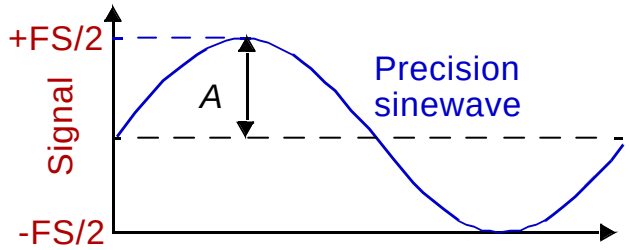
Code density (histogram) method

- Apply an accurately known signal
- Histogram of the output codes
- Bin size can be obtained from the histogram data
  - If signal = ramp, bin size is proportional to code density.



Code density method with sinewaves

- Peak-peak signal slightly above full-scale
- Signal frequency $f_x = \frac{P}{M} f_S$
  - *fs* = sampling frequency
  - *P* = number of signal period (odd, prime number: 1,3,5,7...)
  - *M* = total number of samples taken
- If sinewave generator is not precise enough, divide ADC FS in sections



n -> *n*+1 code transition point:

$$v_n = A \sin\left[\pi \frac{n_{Cn}}{n_{total}} + \sin^{-1}\left(\frac{V_{n-1}}{A}\right)\right]$$

$$v_0 = A \sin\left[\pi\left(\frac{n_{C0}}{n_{total}} - 1\right)\right]$$

n_{Cn} = number of occurrences of code *n*

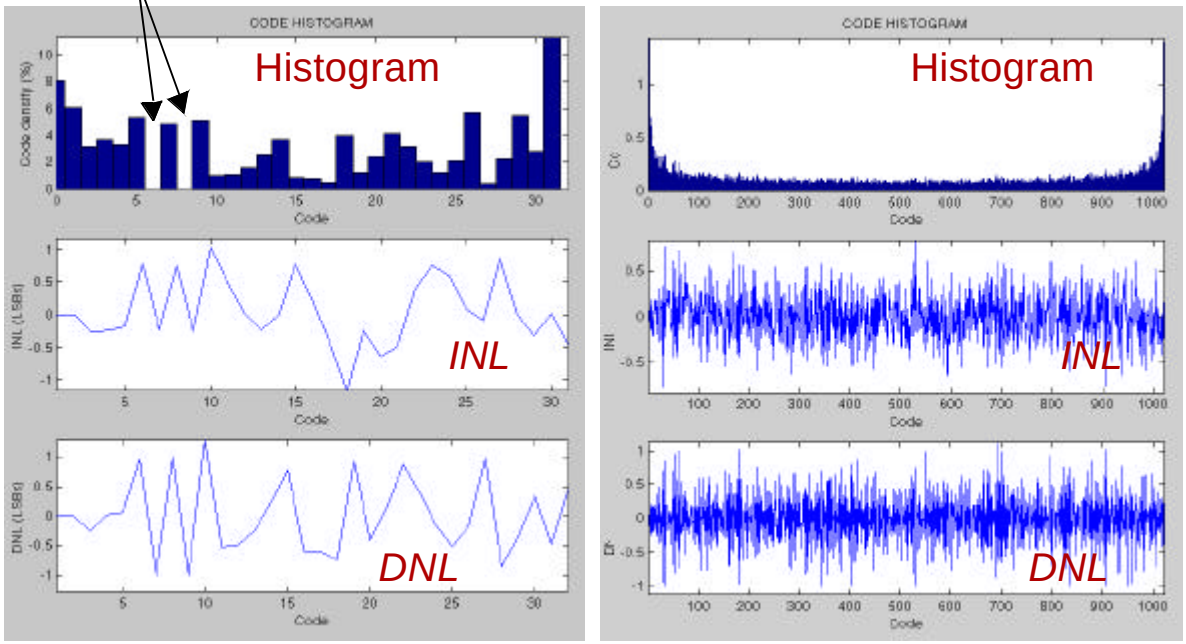
n_{total} = total number of samples

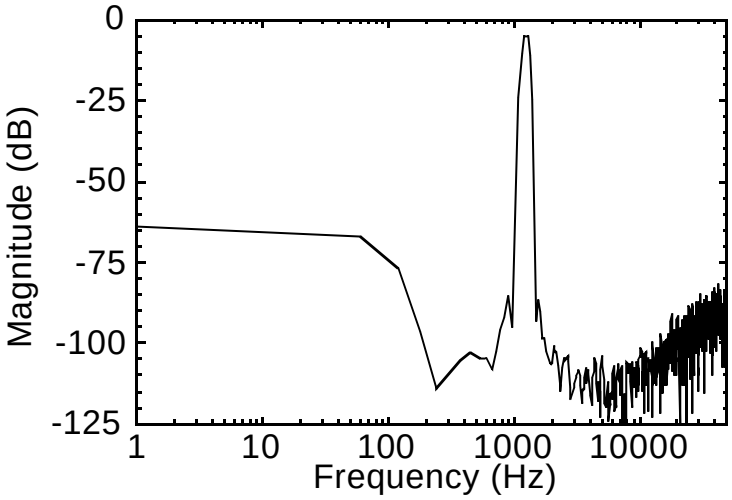
Pros/Cons

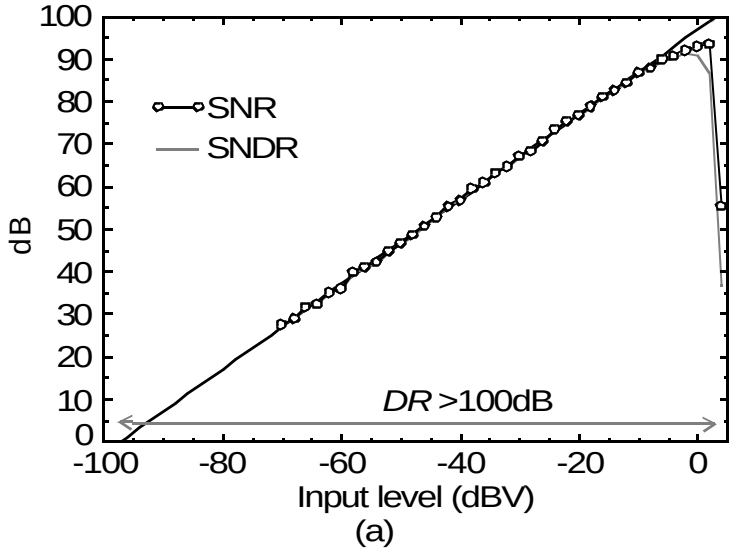
- Allows evaluation of the accuracy of high-frequency converters
- Requires synchronisation for high resolution
- Otherwise, the number of samples needed may be prohibitive: 40Msamples for 16bit!, within 0.1LSB
- Slow for high resolution

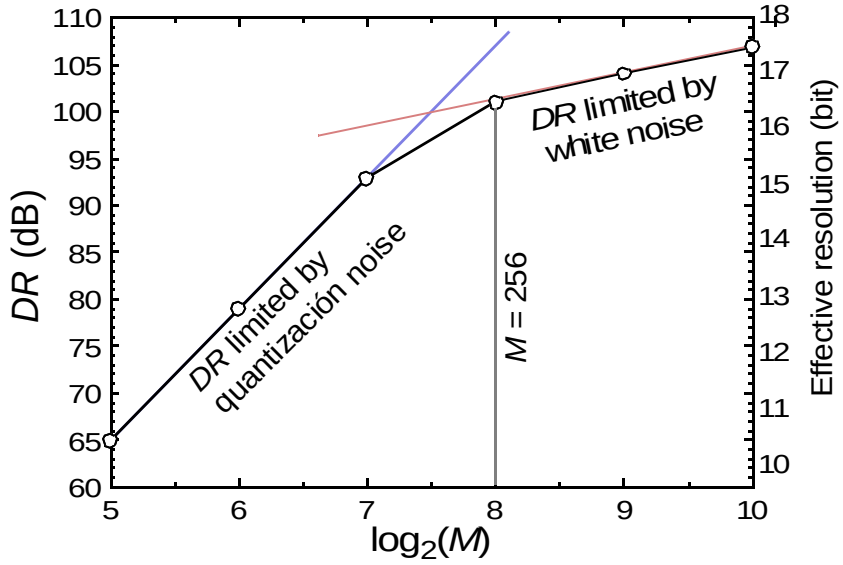
Missing codes

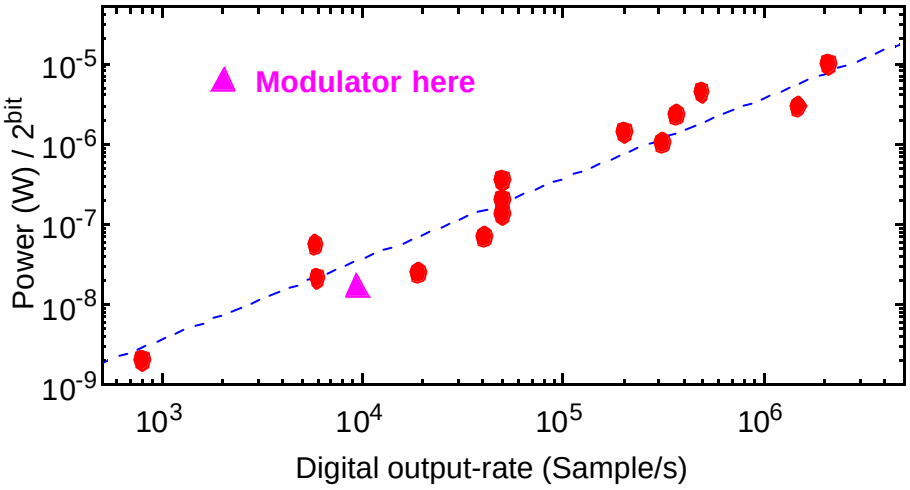
5-bit ADC **10-bit ADC**











- **Design on the border of the quantization noise limited and the white noise limited regions**

→ **Efficient design**

References

[ALBU99] E. ALBUQUERQUE, M. SILVA: "A NEW LOW-NOISE LOGIC FAMILY FOR MIXED-SIGNAL INTEGRATED CIRCUITS," *IEEE TRANS. ON CIRCUITS AND SYSTEMS - I*, VOL. 46, PP. 1498-1500, DECEMBER 1999.

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