A Compact High-Efficiency Broadband Rectifier With a Wide Dynamic Range of Input Power for Energy Harvesting

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***Abstract*— In this letter, a compact high-efficiency broadband microwave rectifier with an extended range of input power is proposed for energy harvesting. In the proposed structure, a novel broadband impedance-matching network is employed to reach high radio frequency (RF) to dc conversion efficiency. The reduction in mismatching loss over a wide bandwidth and input power range is achieved by impedance transformation from three segments of microstrip lines, which leads to a compact design to realize broadband impedance matching. A theoretical analysis and simulations of the proposed rectifier are presented. For validation, a broadband rectifier operating between 2.1 and 3.3 GHz is implemented and tested. The proposed rectifier shows a bandwidth of 44.4% for efficiency over 70% at an input power of 14 dBm. The measured efficiency remains above 50% from 2 to 3.3 GHz with an input power from 4 to 16 dBm. Moreover, the proposed rectifier has a compact size of 31 mm × 18 mm.**

***Index Terms*— Broadband, energy harvesting (EH), high efficiency, rectifier, wide input power range.**

I. Introduction

ENERGY harvesting (EH) technology recycles environmental electromagnetic energy for charging electronic devices where it is hard to access wired power, such as in pipes and remote areas [1]. Microwave rectifiers are a key component in an EH system for converting radio frequency (RF) power into dc power [2]–[6]. Tan and Liu [4] and Shen and Yang [5] successfully realized multiband microwave rectifying with wide dynamic ranges. High RF to dc conversion efficiency is the main demand for a rectifier, which is closely related to system performance. The available energy sources in EH systems, e.g., WiFi, cellular, AM/FM, and TV, [7], are in a wide frequency band. The power densities of ambient electromagnetic energy span an extended power range [8]. A high-efficiency broadband rectifier with wide input power range is required.

However, it is challenging to design a high-efficiency rectifier with broadband and extended input power range because the input impedance of a rectifying diode varies nonlinearly with the operating frequency and input power level. Impedance mismatching will greatly decrease the rectifying efficiency. To address this problem, several research groups have presented some efficient design methods to improve the performance of the rectifier over a wide bandwidth and input power ranges, such as different impedance-matching networks [9]–[12], introducing broadband transmission lines [13], and presenting multirectifying cells [14]. Zhang *et al.* [9] proposed a rectifier with wide bandwidth and input power range based on a branchline coupler. High conversion efficiencies were achieved successfully. The rectifier was a little large because of the couplers before two subrectifiers. Wu *et al.* [10] employed a multistage transmission line with three segments to achieve impedance matching over a broadband spanning from 2 to 3 GHz. Sakaki and Nishikawa [11] demonstrated an impedance-matching network to maximize the quality of input circuits in a wideband rectifier with an operating bandwidth of 300 MHz for efficiency over 81%. Mansour and Kanaya [12] proposed two L-section stages (a high-pass type L-section for lower band and an inductive L-section for higher band) for widening the rectifier bandwidth. The system achieves an operating bandwidth from 870 MHz to 2.5 GHz and shows reduction in robustness and increase in cost for introducing several surface-mounted devices (SMDs) in the design. Kimionis *et al.* [13] showed a novel nonuniform transmission line used in wideband impedance matching, which was applied in two broadband rectifiers to reach an octave bandwidth of 470–860 MHz and decade bandwidth of 250 MHz to 3 GHz. Wu *et al.* [14] presented a rectifier with one octave bandwidth using a frequency-selective topology with a diode array. The proposed rectifier shows a high efficiency of 70% from 1.75 to 3.55 GHz.

In this letter, we propose a high-efficiency rectifier with wide bandwidth and input power range for EH. Three transmission line stubs were employed to achieve broadband impedance matching. With the broadband-matching network, an uncomplicated circuit structure was achieved, which leads to a reduction in the complexity of matching circuits, insertion loss, and physical size. The fabricated rectifier retains an operating wideband of 2.1–3.3 GHz with a conversion efficiency $>70\%$. It also maintains an efficiency of $>50\%$ from -1 to 17 dBm at 2.1 GHz.

II. Design Methodology and Simulation

Fig. 1 shows the schematic of the proposed rectifier with wide bandwidth and input power range. It consists of a dc block, a broadband-matching network, a diode HSMS286, a dc

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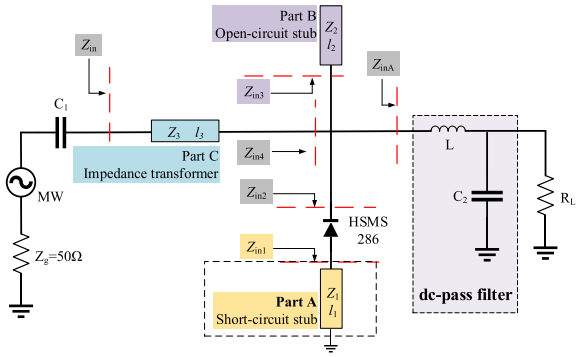

Fig. 1. Proposed rectifier with a wide bandwidth and input power range.

pass filter, and a dc load, from left to right. In the matching network, Part A is presented to reduce the imaginary part of the diode impedance and meanwhile maintain the real part constant. Part B is proposed to minimize the range of variation on the imaginary part of Z_{in4} and maintain the real part near 50 Ω. Part C is an impedance transformer for matching Z_{in4} to 50 Ω.

A. Part a Design

Part A is a short-circuit stub with a characteristic impedance of Z_1 and a length of l_1. From the transmission theory, the input impedance of Part A can be written as $Z_{\text{in1}} = jZ_1\tan(\beta l_1)$. $Z_{\text{inA}} = \infty$ at all frequencies of interest. Therefore, Z_{in2} can be obtained as follows:

$$Z_{\text{in2}} = Z_{\text{d}} + jZ_1\tan(\beta l_1) \tag{1}$$

where Z_{d} is the input impedance of the diode. Z_{d} and Z_{in2} vary nonlinearly with operating frequency and input power level. Part A is designed to reduce the imaginary part of Z_{d} from f_1 to f_2. $Z_{\text{in2}}(f_1)$ to $Z_{\text{in2}}(f_2)$ is symmetric along the axis on a Smith chart. At a given input power, the parameters of Part A can, therefore, be determined by calculating the equation below

$$\text{Im}(Z_{\text{in2}}(f_1)) = -\text{Im}(Z_{\text{in2}}(f_2)). \tag{2}$$

In the design, an Avago HSMS286 diode was chosen for the proposed rectifier. Z_1 and l_1 were calculated based on (2) and the diode model. The input impedance of the HSMS286 diode with Part A over different frequencies and input power was simulated based on the SPICE model. As shown in Fig. 2(a), the imaginary part of Z_{in2} is nearly oddly symmetrical at 14 dBm and the real part is around 100 Ω. When the input power decreases from 14 to 10 dBm or 7 dBm, Z_{in2} varies similarly with respect to frequency in the Smith Chart. Thus, we can design a broadband rectifier with impedance matching over certain input power range.

B. Part B Design

Z_{in2} is capacitive and inductive at low and high frequencies, respectively. When introducing a shunt open circuit stub, Z_{in4} is at the equal conductivity circle of Z_{in2} and rotates clockwise. The short-circuit (Part A) and open-circuit (Part B) stubs own reverse characteristics with respect to frequency variation, which limits the impedance variation of Z_{in4}. Z_{in4} is compressed into a small area on the Smith chart.

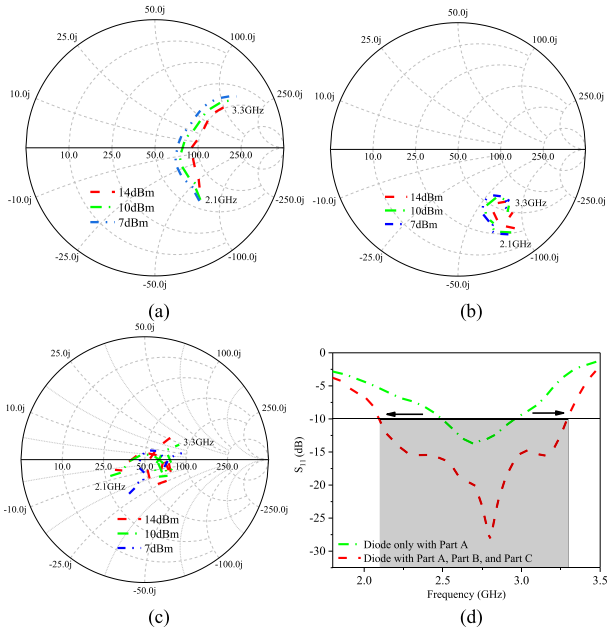

Fig. 2. (a) Z_{in2}, (b) Z_{in4}, and (c) Z_{in} from 2.1 to 3.3 GHz at different input power levels. (d) $|S_{11}|$ of the diode with Part A or Parts A, B, and C at 14 dBm.

Part B is an open-circuit stub having a characteristic impedance of Z_2 and a length of l_2. The input impedance of Part B can be written as $Z_{\text{in3}} = -jZ_2/\tan(\beta l_2)$. Mathematically, Z_{in2} and Z_{in4} are linked as follows:

$$Z_{\text{in4}}(f_i) = \frac{Z_2 \times Z_{\text{in2}}(f_i)}{Z_2 + jZ_{in2}(f_i)\tan\theta_2(f_i)}, \quad i = 1, 2 \tag{3}$$

where $\theta_2(f_1)$ and $\theta_2(f_2)$ are the electrical length of the open-circuit stub in Part B at f_1 and f_2, respectively. $\theta_2(f_2)$ can be denoted as $\theta_2(f_2) = k\theta_2(f_1)$, and k is the frequency ratio.

Based on circuit simulation and optimization, $Z_{\text{in4}}(f_i) = 50-\text{j}75\ \Omega$ presents the best performance in a wide frequency range and input power range. Z_2 and $\theta_2(f_1)$ were calculated from $Z_{\text{in4}}(f_i) = 50-\text{j}75\ \Omega$. With the characteristic impedance of 50 Ω and the electrical length of 0.05 λ at f_1, the diode with Parts A and B was simulated and Z_{in4} was obtained. Fig. 2(b) shows the simulated Z_{in4} versus the frequency of interest at different input power levels. As can be seen with the open-circuit stub, the three curves were nearly compressed to a small area on the Smith chart, which indicates a great reduction in the range of variation of the imaginary part of the input impedance. The real part is near Z_{g}. The imaginary part of the input impedance was reduced to a limited range of $-75 \pm 20\ \Omega$, indicating that the rate of its variation was $\pm 27\%$. The range of variation of $\text{Im}(Z_{\text{in4}})$ was much less than that of $\text{Im}(Z_{\text{in2}})$.

C. Part C Design

Part C is an impedance transformer having a characteristic impedance of Z_3 and a length of l_3. On the Smith chart, Z_{in4} can clearly be transformed into 50 Ω through a transmission line with high characteristic impedance because $Z_{\text{in4}}(f)$ gathers in a small area and $\text{Re}(Z_{\text{in4}}(f))$ was about 50 Ω. The input impedance of the proposed rectifier can be obtained as

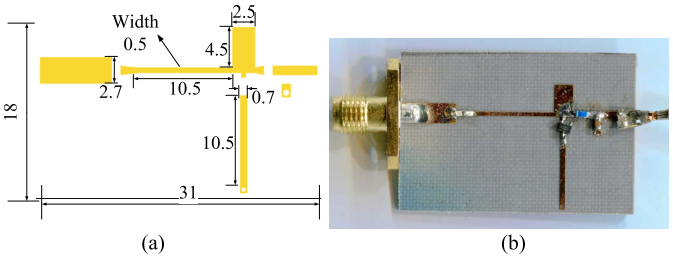

Fig. 3. (a) Layout of the proposed rectifier. (b) Fabricated rectifier.

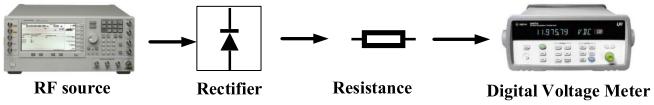

Fig. 4. Diagram of the tested system.

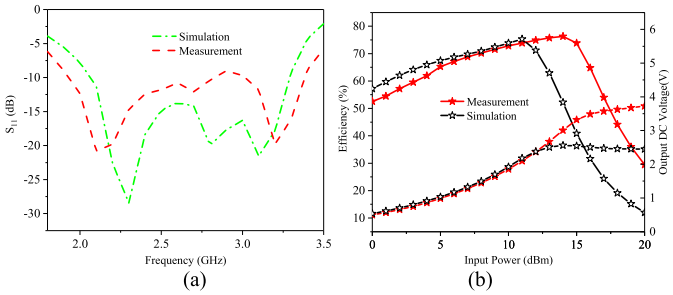

Fig. 5. (a) Reflection coefficient $|S_{11}|$ versus frequency at 10 dBm. (b) Efficiency of simulation and measurement versus input power at 2.1 GHz.

follows:

$$Z_{\text{in}}(f_i) = Z_3 \frac{Z_{\text{in4}}(f_i) + jZ_3 \tan\theta_3(f_i)}{Z_3 + jZ_{\text{in4}}(f_i)\tan\theta_3(f_i)}, \quad i = 1, 2 \qquad (4)$$

where $\theta_3(f_1)$ and $\theta_3(f_2)$ are the electrical lengths of the impedance transformer in Part C at f_1 and f_2, respectively. The rate of frequency k was used to link $\theta_3(f_2)$ and $\theta_3(f_1)$: $\theta_3(f_2) = k\theta_3(f_1)$. Z_3 and $\theta_3(f_1)$ were calculated by pushing $\text{Re}(Z_{\text{in}}(f_i)) \approx 50\ \Omega$ and $\text{Im}(Z_{\text{in}}(f_i)) \approx 0\ \Omega$. The simulation was conducted with a characteristic impedance of 110 Ω and an electrical length of 0.1 λ at f_1.

As shown in Fig. 2(c), three curves indicating three input power levels were close to 50 Ω over a wide bandwidth on the Smith chart. Fig. 2(d) shows the input reflection coefficient $|S_{11}|$ of two rectifiers. One is a rectifier only with Part A and the other one is the proposed broadband rectifier. The bandwidth for $|S_{11}| < -10$ dB was clearly significantly widened with the proposed Parts A, B, and C.

III. Implementation and Measurement

The frequencies f_1 and f_2 were set to be 2.1 and 3.3 GHz, respectively. The proposed rectifier was implemented and measured. The substrate used in the design was F4B with a thickness of 1 mm, a relative dielectric constant of 2.65, and a loss tangent of 0.002. The layout of the proposed rectifier is shown in Fig. 3(a) with detailed dimensions and the fabricated rectifier is shown in Fig. 3(b). A capacitor C_1 (22 pF) was used as a dc clock, and the dc-pass filter includes an inductor L (10 nH) and a capacitor C_2 (10 pF).

Fig. 4 shows the test system. A microwave source (E8730C; Agilent) was used to generate microwave power, a standard resistance box was employed as the dc load, and a digital meter was applied to measure the output dc voltage.

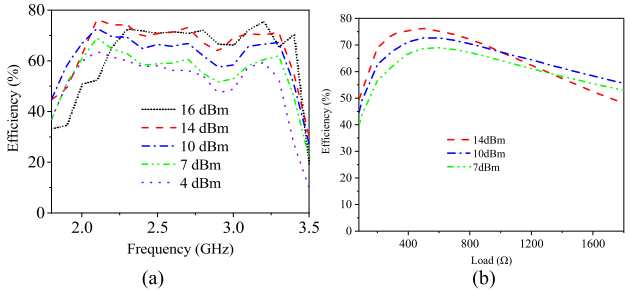

Fig. 6. (a) Measured efficiency versus frequency and (b) dc load.

TABLE I
Comparison With Some Prior Rectifiers

Ref.	Efficiency over operating band				Max efficiency	Size (mm^2)
	RF-to-dc efficiency	Frequency (GHz)	Measured Bandwidth	Input power		
[9]	>70%	2.08–2.58	21.5%	15.5 dBm	80.8%	126×68
[10]	>70%	2.0–3.05	41.5%	10 dBm	75.8%	36×35
[11]	>70%	1.47–1.77	18.5%	10 dBm	80%	71×20
[12]	>30%	0.87–2.5	91%	0 dBm	63%	18×6
This work	>70%	2.1-3.3	44.4%	14 dBm	76.3%	31×18

The simulated and measured $|S_{11}|$ at 10 dBm are shown in Fig. 5(a). It reaches a good performance from 2 to 3.3 GHz. Fig. 5(b) draws the measured efficiency versus input power at 2.1 GHz. The measurement result shows a wide dynamic input power range from −1 to 17 dBm (18 dB) for a conversion efficiency of >50%. To show the performance of the rectifier operating at different frequencies and dc loads, the fabricated rectifier was tested versus frequency and dc load with different input power. Fig. 6(a) shows that the conversion efficiency was over 70% from 2.1 to 3.3 GHz, featuring a broadband of 44.4%. The rectifier remains high efficiency above 50% from 2 to 3.3 GHz when the input power varies from 4 to 16 dBm. Fig. 6(b) shows the efficiency as a function of dc load at 2.1 GHz. As observed, the efficiency was >50% from 80 to 1700 Ω at 14 dBm. Table I gives the comparison between the proposed rectifier and some prior works. The proposed rectifier presents the widest bandwidth (efficiency >70%) of 44.4% among all designs under comparison with a compact size of 31 × 18 mm^2.

IV. Conclusion

A high-efficiency broadband rectifier with a wide input power range was presented by employing an impedance-matching network. In such a matching network, three transmission line stubs were chosen to achieve impedance matching in a wide bandwidth. With the proposed structure, an uncomplicated circuit structure was achieved, leading to a reduction in the complexity of matching circuits, the insertion loss, and the physical size. A rectifier operating at 2.1–3.3 GHz was fabricated and measured to test the design. The measurement results show a wide bandwidth of 44.4% when the efficiency was >70%. The efficiency remains over 50% with a broadband of 2–3.3 GHz when the input power varies from 4 to 16 dBm. Moreover, the proposed design method with wide bandwidth can be applied to other RF circuit designs.

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