A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2

Chi-Hung Lin and Klaas Bult

***Abstract*— A 10-b current steering CMOS digital-to-analog converter (DAC) is described, with optimized performance for frequency domain applications. For sampling frequencies up to 200 MSample/s, the spurious free dynamic range (SFDR) is better than 60 dB for signals from dc to Nyquist. For sampling frequencies up to 400 MSample/s, the SFDR is better than 55 dB for signals from dc to Nyquist.**

The measured differential nonlinearity and integral nonlinearity are 0.1 least significant bit (LSB) and 0.2 LSB, respectively. The circuit is fabricated in a 0.35-μm, single-poly, four-metal, 3.3-V, standard digital CMOS process and occupies 0.6 mm^2. When operating at 500 MSample/s, it dissipates 125 mW from a 3.3-V power supply. This DAC is optimized for embedded applications with large amounts of digital circuitry.

***Index Terms*—CMOS analog integrated circuits, digital–analog conversion, matching, mixed analog–digital integrated circuits.**

I. Introduction

THE pressure to reduce cost in mass market communication devices such as cable modems and digital cable set-top boxes has created a need for embedded high-speed high-resolution digital-to-analog converters (DAC's). With the ability to integrate analog circuits with memory and digital signal processing (DSP) circuits on the same die, CMOS technology is poised to meet that challenge. In the past 20 years, much research has been devoted to DAC's [1]–[8] optimized for time domain applications, such as high-resolution displays for computer graphics and high definition television (HDTV). These DAC's were mainly focused on dc linearity, settling behavior, and glitch energy performance. When used to synthesize sinewaves in frequency-domain applications, however, their spurious free dynamic range (SFDR) performance is typically not sufficient for broad-band applications.

As an example, a simplified architecture of a cable modem headend transmitter is shown in Fig. 1. The cable modem system consists of multiple channels, where each channel contains a digital modulator and a DAC. The channels can have different digital modulation schemes, for example, quadrature amplitude modulation (QAM) or quadrature phase-shift keying (QPSK). Without a high-speed, high-resolution DAC, these modulation functions must be implemented in the analog domain, which generally results in relatively poor quality signals.

When multiple channels are combined simultaneously, it is very important that the DAC's meet a minimum SFDR, or signals in one channel will be corrupted by spurious components from other channels. Therefore, the major challenge for designing DAC's for frequency domain applications is to obtain large *wideband* SFDR. Fig. 2 shows an example of a 16-QAM spectrum for cable modem upstream signals. The transmitted signal frequencies range from 5–65 MHz. The specification of the multimedia cable network system (MCNS) requires the (aliased) harmonics to be at least 47 dB below the fundamental signal. Experimental results have shown that this number translates into an SFDR of more than 52 dB for a single tone sinewave. That is a difficult requirement to meet for DAC's operating at high signal frequencies.

The goal of the DAC reported here is to obtain true 10-bit performance (SFDR $>$ 60 dB) for signals from dc to Nyquist, for sampling speeds up to 200 MSample/s. For embedded applications, use of standard digital CMOS processes and a small chip area is a must. The chip area of this DAC is 0.6 mm^2 in a 0.35 μm, single-poly, four-metal, 3.3 V, standard digital CMOS process.

Sections II and III discuss the advantages and shortcomings of binary-weighted DAC's and thermometer-coded DAC's, respectively. Section IV compares the area requirement for these binary-weighted and thermometer-coded DAC's. Section V deals with the optimization of the architecture for minimum area. Section VI shows circuit implementation and layout issues. Section VII presents results from measurements, and Section VIII summarizes the conclusions.

II. Binary Weighted DAC

Fig. 3(a) shows a conceptual circuit of a 10-bit binary-weighted DAC. The digital inputs directly control the switches. The current sources associated with the switches are binary weighted. The advantage of such a binary-weighted DAC is its simplicity, as no decoding logic is required. There are several major drawbacks, however, which are all associated with major bit transitions. At the mid-code transition (0 111 111 111 $\rightarrow$ 1 000 000 000), the most significant bit (MSB) current source needs to be matched to the sum of all the other current sources to within 0.5 LSB's (least significant bits). This is difficult to achieve. Because of statistical spread, such matching can never be guaranteed. Therefore this architecture is not guaranteed monotonic. Matching is an issue for all bit transitions, but the severity of the problem is proportional to the weight of the bit, resulting in a typical differential nonlinearity (DNL) plot as shown in Fig. 3(b). In addition, the errors caused by the dynamic behavior of the switches (such as charge-injection and clock-feedthrough) result in glitches in the output signal as shown in Fig. 3(c). This problem is most severe at the midcode transition, as all switches are switching simultaneously. Such a midcode glitch contains

Manuscript received June 25, 1998; revised August 19, 1998.

The authors are with the Broadcom Corporation, Irvine, CA 92618 USA (e-mail: chlin@broadcom.com, bult@broadcom.com).

Publisher Item Identifier S 0018-9200(98)08566-7.

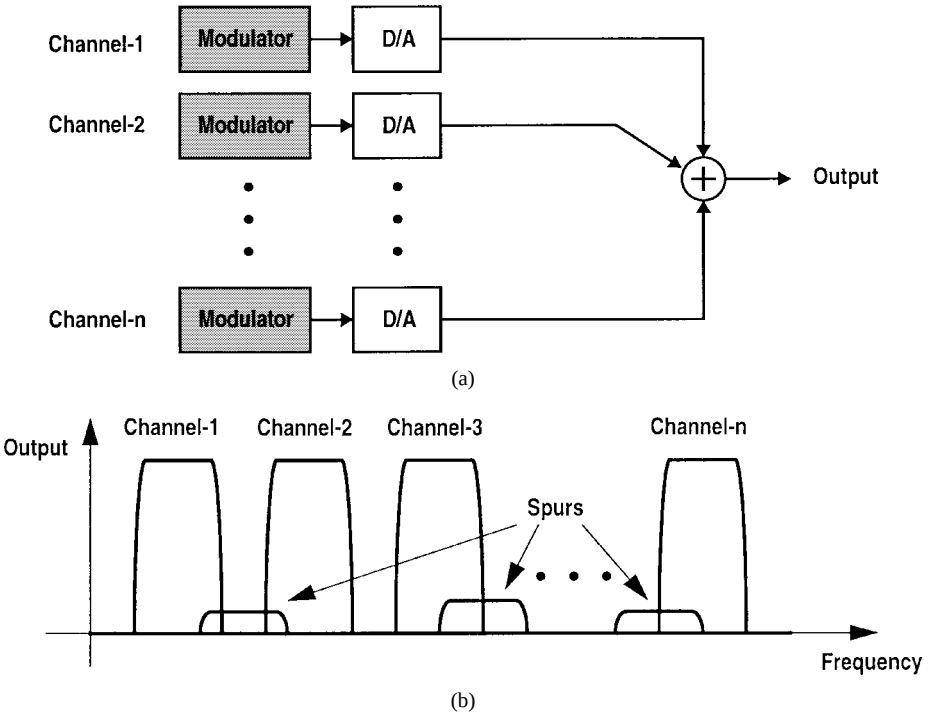


Fig. 1. DAC's for cable modem applications.

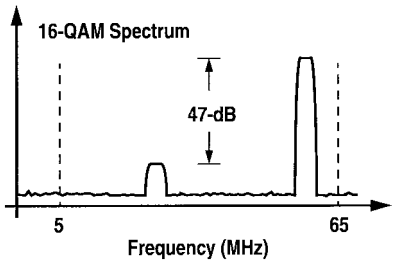


Fig. 2. 16-QAM spectrum including an aliased harmonics 47 dB below the fundamental.

highly nonlinear signal components, even for small output signals and will manifest itself as spurs in the frequency domain.

III. Thermometer Coded DAC

Fig. 4(a) shows an example of a 10-bit thermometer-coded DAC. There are $2^{10} = 1024$ unit current sources. Each unit current source is connected to a switch controlled by the signal coming from the binary-to-thermometer decoder. When the digital input increases by 1 LSB, one more current source is switched from the negative to the positive side. Assuming positive-only current sources, the analog output is always increasing as the digital input increases. Hence, monotonicity is guaranteed using this architecture.

In addition, there are several other advantages for a thermometer-coded DAC compared to its binary-weighted counterpart. First, the matching requirement is much relaxed: 50% matching of the unit current source is good enough for DNL $<$ 0.5 LSB, as shown in Fig. 4(b). At the midcode, a 1-LSB transition (0 111 111 111 $\rightarrow$ 1 000 000 000), causes

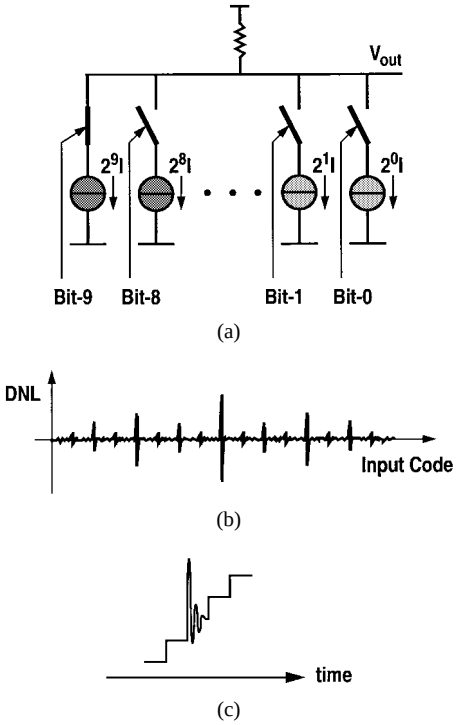


Fig. 3. Matching and glitch problems of a binary-weighted DAC.

only one current source to switch as the digital input only increases by one. This greatly reduces the glitch problem.

On top of that, glitches hardly contribute to nonlinearity in the thermometer-coded architectures. This is because the magnitude of a glitch is proportional to the number of switches that are actually switching. So for small steps, the glitch is small, and for a large step, the glitch is large. Since the number of switches that switch is proportional to the signal

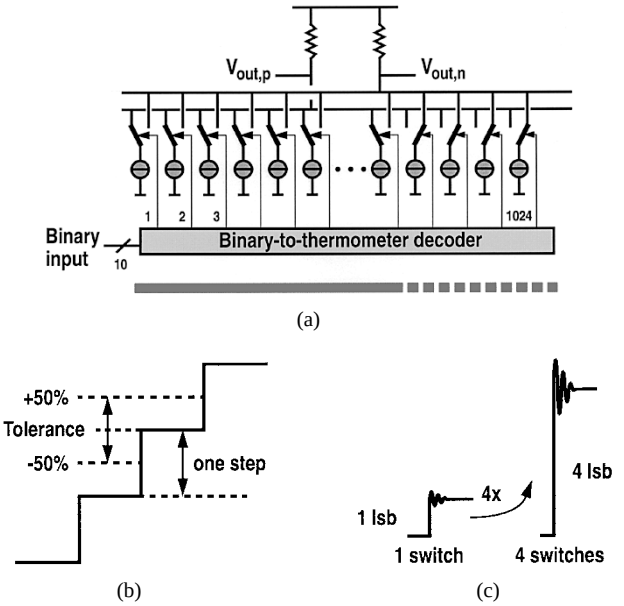


Fig. 4. Matching and glitch advantages of a thermometer-coded DAC.

step between two consecutive clock cycles, the magnitude of the glitch is directly proportional to the amplitude of the signal step. As an example, Fig. 4(c) shows that the glitch in the output signal of a step of 4 LSB's has exactly the same shape and duration as the glitch in the output signal for a 1 LSB step and it is exactly 4× larger in amplitude. If the glitch is strictly proportional to the signal step, it will not cause any nonlinearity in the DAC output signal.

To discuss this point in further detail, consider Fig. 5. A sinewave signal is shown, where $x(n)$ is the digital input at sample n and $y(n)$ is the analog output at sample n. For each sample n, $y(n)$ consists of two parts.

1) The nonshaded part is nonswitching, defined by the current sources that have already been on during the previous sample $(n-1)$. The value of the nonswitching part is equal to $a*x(n-1)$, where "a" is the nonswitching unit current source and $x(n-1)$ is the value of the digital input signal in the previous clock cycle.
2) The shaded part is switching, equal to $b*[x(n)-x(n-1)]$, where "b" is the switching unit current source and $[x(n)-x(n-1)]$ is the difference between the current and the previous values of the digital input signal. For a thermometer-coded approach, both "a" and "b" are constant and independent of the signal step. Therefore the total analog output function $y(n)$, which is equal to the sum of the nonswitching part and the switching part, can be expressed as follows:

$$y(n) = a \cdot x(n-1) + b \cdot [x(n) - x(n-1)]. \quad (1)$$

With "a" and "b" constant and independent of $x(n)$, $y(n)$ is only linearly dependent on $x(n)$ and although it produces slight filtering of the signal, distortion due to glitches is reduced to zero.

One major drawback of the thermometer-coded DAC is area, since for every LSB this architecture needs a current source, a switch, and a decoding circuit, as well as the binary to thermometer decoder.

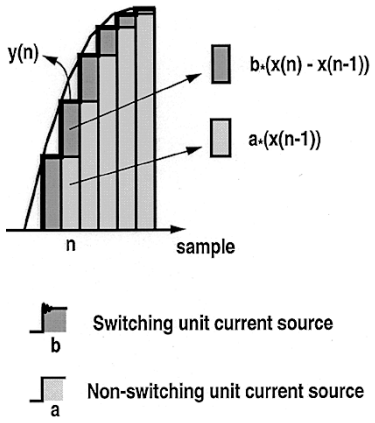
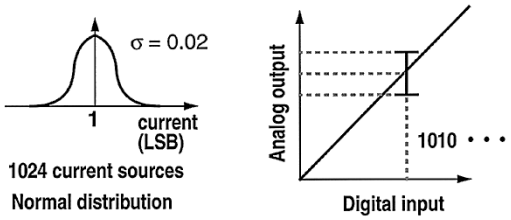


Fig. 5. Linear output function for a thermometer-coded DAC.



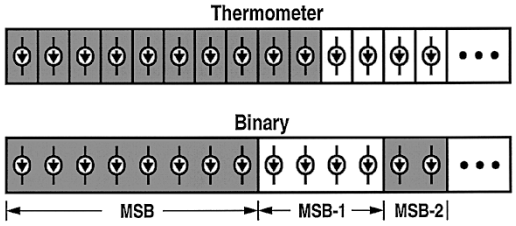


Fig. 6. MATLAB simulations for thermometer-coded versus binary-weighted DAC.

IV. Area Comparison

To compare the area requirements of binary-weighted and thermometer-coded architectures, a MATLAB simulation was performed. First, 1024 normally distributed unit current sources were generated, with a mean of 1 LSB and a standard deviation of 0.02 LSB's. The same current sources were used for simulating the binary-weighted as well as the thermometer-coded architecture as shown in Fig. 6. For the thermometer-coded approach, 1024 cells were generated, with each cell containing one current source. For the binary-weighted design, ten cells were generated. The first 512 current sources were grouped into the MSB cell, then the next 256 current sources into the (MSB-1) cell, the next 128 current sources into the (MSB-2) cell, etc. To obtain insight into the DNL and integreal nonlinearity (INL) performance of these two architectures, 100 MATLAB simulations were performed and DNL and INL were computed for each run for both cases. Fig. 7 shows the 100 MATLAB simulation results for

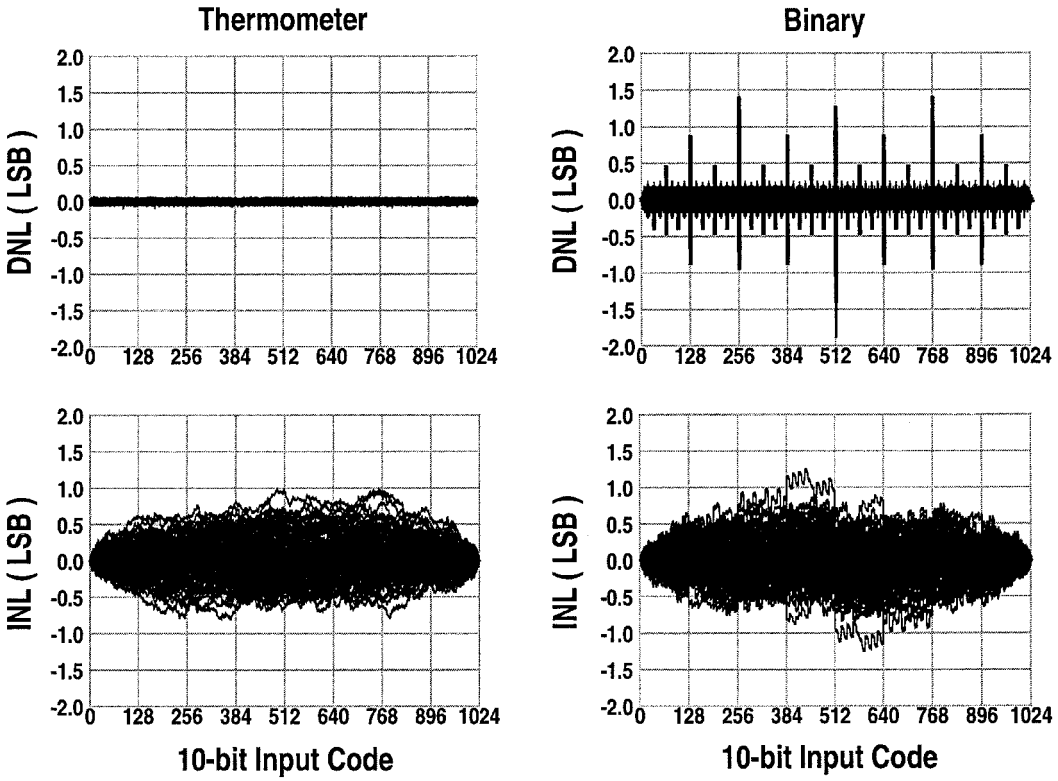


Fig. 7. One hundred MATLAB simulation results for thermometer-coded versus binary-weighted DAC.

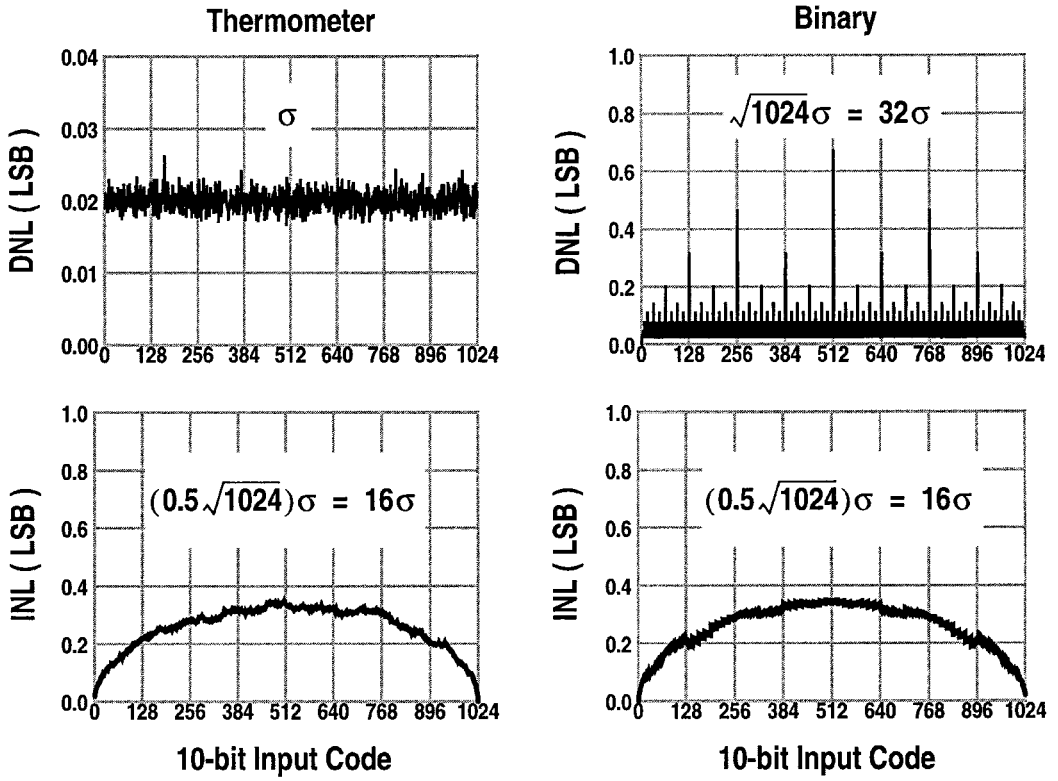


Fig. 8. RMS of 100 MATLAB simulation results for thermometer-coded versus binary-weighted DAC.

both cases. It is clear that the INL behavior is very similar for both cases. However, their DNL behavior differs greatly, especially at midcode.

To get a better view of these results, Fig. 8 shows the root mean square (rms) of these 100 simulation results. The INL values are virtually identical and the peak values are very

TABLE I
AREA REQUIREMENT FOR BINARY-WEIGHTED AND THERMOMETER-CODED DAC

Requirement	Binary Weighted	Thermometer Coded
INL	16σ	16σ
DNL	32σ	σ
Area(INL=0.5-lsb)	$256*A_{unit}$	$256*A_{unit}$
Area(INL=1-lsb)	$64*A_{unit}$	$64*A_{unit}$
Area(DNL=0.5-lsb)	$1024*A_{unit}$	A_{unit}

close to the theoretical values of $16\sigma = 0.5 * \sqrt{1024}\sigma$, where the factor 0.5 comes from the fact that the INL curve was fit to zero at both ends of the curve. With $\sigma = 0.02$-LSB, this results in an INL of 0.32-LSB. The DNL value for the thermometer-coded approach is very close to the σ value of 0.02-LSB's as expected. However, the DNL value for the binary-weighted design shows a dramatic difference compared to its thermometer-coded counterpart. The midcode DNL value for the binary-weighted design is as high as 0.64-LSB or 32σ, which again matches very well with the theoretical value of $\sqrt{1024} * \sigma$.

From Fig. 8 we can clearly see that, with the same analog area, the rms INL for both cases are very similar and close to 16σ, while the DNL for the thermometer-coded approach is equal to σ and the DNL for the binary-weighted design is equal to 32σ. These results are summarized in Table I.

The above results are being used to make area estimates for both architectures, based on equal INL and DNL performance. As a first-order approximation, the relationship between area and σ is given by [9]

$$\text{Area} \propto \frac{1}{\sigma^2}. \tag{2}$$

So, if A_{unit} is the minimum required area to obtain a DNL $= 0.5 -$ LSB for the thermometer-coded architecture, the required analog area for the binary-weighted design would be $1024 * A_{\text{unit}}$. With respect to INL, both architectures require the same area. For an INL requirement of INL $= 0.5 -$ LSB, the total required analog area would be $256 * A_{\text{unit}}$. These requirements are also summarized in Table I.

V. SEGMENTATION

Usually, to leverage the clear advantages of the thermometer-coded architecture and to obtain a small area simultaneously, a compromise is found by using segmentation. The DAC is divided into two sub-DAC's, one for the MSB's and one for the LSB's. Thermometer coding is used in the MSB where the accuracy is needed most. Because of the reduced number of bits in this section, the size is considerably smaller than a true thermometer-coded design. The LSB section can either be done using the binary-weighted or the thermometer-coded approach. We will refer to a fully binary-weighted design as 0% segmented, whereas a fully thermometer-coded design is referred to as 100% segmented. This section discusses the minimization of chip area, under the constraints of true 10-bit dc performance, while simultaneously trying to optimize the frequency domain performance. To this extent the optimum amount of segmentation is investigated.

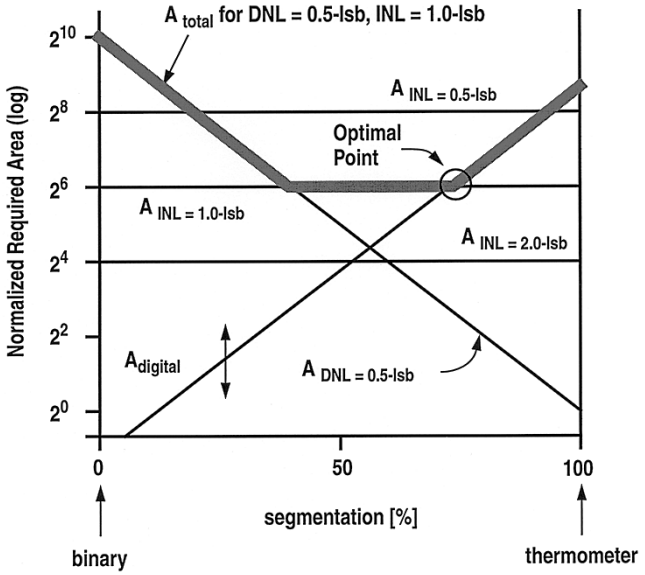


Fig. 9. Normalized required area versus percentage of segmentation.

Fig. 9 shows the normalized required area versus percentage of segmentation. Based on DNL performance only, the minimum analog area for 100% segmentation is A_{unit} and the minimum analog area for 0% segmentation is $1024 * A_{\text{unit}}$ (see Table I). On a logarithmic scale, the minimum analog area requirement as a function of segmentation will form a straight line connecting the above mentioned points, as shown in Fig. 9. Since the INL behavior (Fig. 8) is dependent only on the total analog area, it is independent of the amount of segmentation and shows up as a horizontal line in Fig. 9.

So far, we focused on analog area only. As discussed in Section III, the thermometer-coded section requires decoding logic for each current source. If A_{decode} is the required area for the digital decoding logic per current source, the total digital area equals $2^M * A_{\text{decode}}$, where M is the number of bits in the MSB section. On a logarithmic scale, the area of decoding logic as a function of segmentation is a straight line as shown in Fig. 9. The relative position of this line with respect to the analog area requirements is dependent on circuit implementation and technology.

As we increase the percentage of segmentation, the required total area is first dominated by the DNL requirement, then by the INL requirement, and finally by the decoding logic. Often, the system requirements for INL are more relaxed than for DNL. If the INL requirement were to be relaxed by a factor of 2, the required analog area will be reduced by a factor of 4. This is an important fact that needs to be taken advantage of when designing the DAC. So, if the system requirement is DNL $= 0.5 -$ LSB and INL $= 1.0 -$ LSB, the required analog area versus percentage of segmentation is as indicated by the shaded line in Fig. 9. For minimum area, the flat part of this curve would be optimum and the total area would be determined by the INL requirement.

Without other criteria, any point along the flat part of the curve would be equally good for area and INL. Going

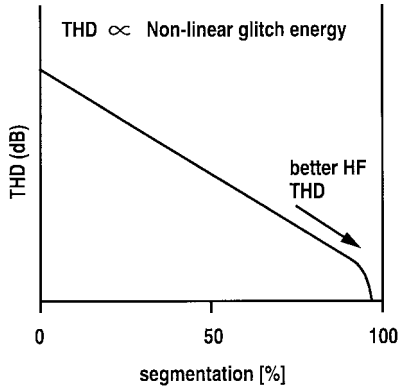


Fig. 10. THD versus percentage of segmentation.

toward more segmentation, however, would improve the DNL performance. As discussed in Section III, thermometer coding has additional advantages with respect to glitch performance. As soon as the segmentation is less than 100%, glitches will contribute to distortion, particularly at higher frequencies. Every additional bit in the LSB section will increase the distortion by $2\times$, as is shown in Fig. 10. Combining the results of Figs. 9 and 10, we can conclude that under the condition of minimum area, the best total harmonic distortion (THD) performance would be obtained at the "optimal point" in Fig. 9. At that point, area is still minimum, INL performance is according to the specification and DNL is even better. The THD is reduced to the minimum possible under these constraints. If needed, the THD can be further improved, but only at the cost of extra area. As we can see from Fig. 9, at the optimal point, the total analog area is equal to the total digital area.

This macro-level observation can actually be extended to the cell level. At the optimal point, the total area is dominated by the thermometer-coded MSB section. So in first-order approximation, the number of decoding circuits is equal to the number of current sources. This means that also at the cell level, the analog area equals to the digital area.

VI. Architectural Choices and Circuit Design

A. Unit Current Cell

Fig. 11 shows the circuit of one unit current cell. It consists of an analog part and a digital part. The analog part consists of a differential switch and a cascoded current source. The digital part consists of a decoding logic and a latch. The decoding logic is equivalent to an AND–OR gate function and the latch is essential for timing synchronization, as all the current cells should switch at the same time.

B. Optimum Segmentation

To optimize the design of the DAC to the optimal point as indicated in Fig. 9, the following steps where used in the design process.

1) The digital decoding logic is designed and laid out first.
2) The analog part of the cell is designed and matched in size to the digital part.

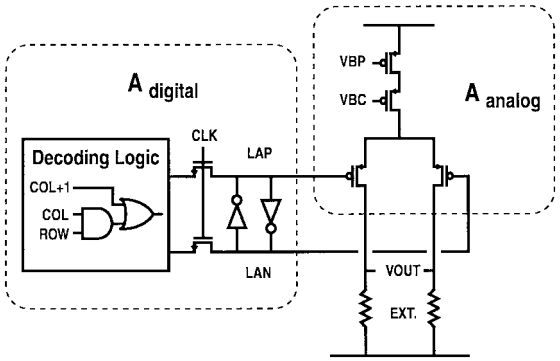


Fig. 11. Current cell.

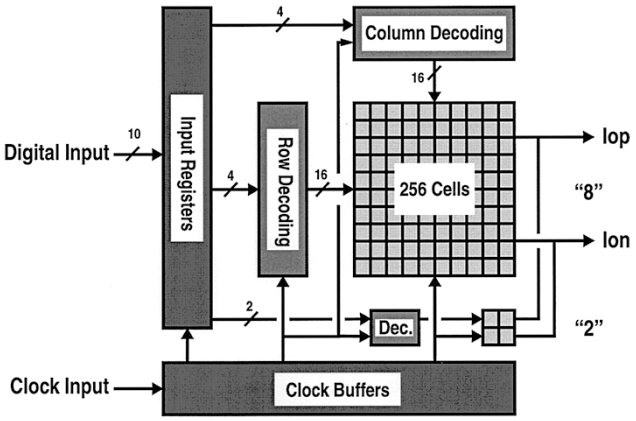


Fig. 12. Block diagram: "$8 + 2$" segmentation.

3) Based on the area of the transistors in the current source, the matching accuracy is estimated using data well described in the literature [9].
4) Using the matching estimates and the yield requirements, the maximum number of bits in the LSB section is determined.

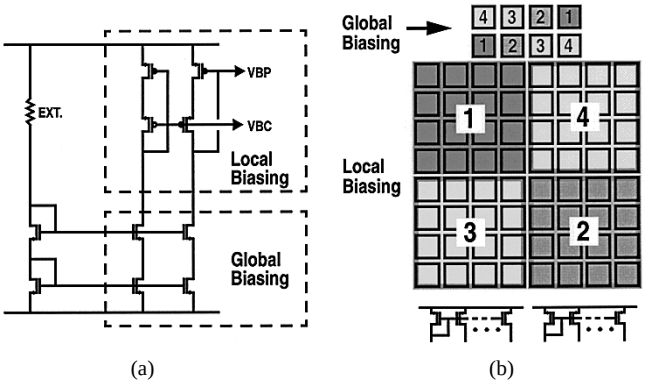
Using the design procedure outlined above, we determined that the maximum number of bits in the LSB section is two and therefore, the number of bits in the MSB section equals eight.

C. Block Diagram

Fig. 12 shows the block diagram for the "$8 + 2$" segmentation. The digital inputs are first clocked into input registers. Then the first four MSB's are column decoded, the next four bits are row decoded, and the final two bits are sent to the decoding logic for the 2-bit LSB section. The LSB section is also implemented fully segmented. There are 256 cells in the main matrix and four cells in the small matrix. As the segmentation is implemented as "$8 + 2$," the current source value in the main matrix is equal to 4 LSB's while the current source value in the small matrix is equal to 1 LSB.

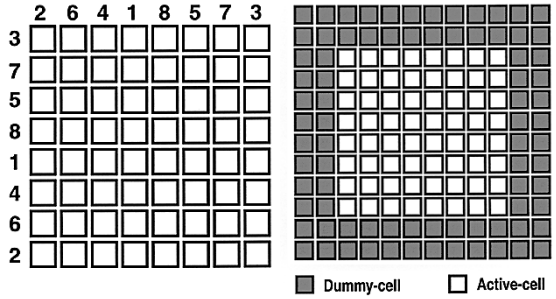
D. Biasing Scheme

Fig. 13 shows the biasing scheme for the cascoded current sources. An external resistor is used to generate the reference current. The NMOS sections of the biasing circuits are labeled



(a) (b)

Fig. 13. Biasing scheme.



(a) (b)

Fig. 14. Randomization and dummies.

as "global biasing" while the PMOS sections are labeled as "local biasing." In the actual implementation, the global biasing is realized using a common-centroid layout to reduce effects of gradients. The local biasing is separated into four quadrants. There is no direct connection between any two quadrants as shown in Fig. 13(b). This will improve both DNL as well as INL performance as explained later in Section VII-B.

E. Randomization and Dummies

Although breaking up the biasing of the main matrix into four quadrants is very helpful, the gradients within each quadrant still could effect the INL behavior. To solve this problem, the order of the columns and rows were shuffled, as shown in Fig. 14(a). Two layers of dummy cells surrounding the active cells were added as shown in Fig. 14(b) to avoid any boundary effects. This was done to make sure all the active cells experience exactly the same environment.

VII. Measurement Results

A. Chip Micrograph

Fig. 15 shows the chip micrograph. Two direct digital frequency synthesizers (DDFS's) are integrated onto the same die with the DAC. In this way, either single tone or two-tone test can be performed. The technology used is a 0.35 μm, single-poly four-metal, 3.3 V, standard digital CMOS process. The active area of the DAC, as shown in Fig. 15, is 0.6-mm^2.

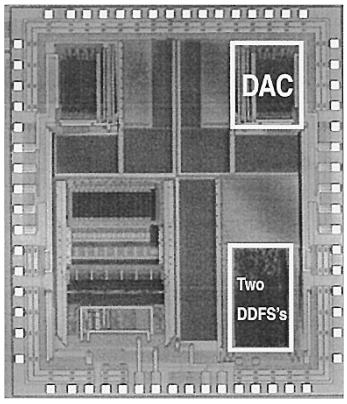


Fig. 15. Chip micrograph.

B. Measured Current Source Values

Fig. 16(a) shows a three-dimensional plot of the measured current source values at their actual location in the layout. As the main matrix is generating the 8 MSB's, the value of each unit current source is equal to 4 LSB's. As the plot shows, the measured values are very close to 4.0 LSB's and the fluctuation around that value is small (<0.1 LSB). A gradient from rows 1–8 can be clearly recognized, however, along with a sudden jump between rows 8 and 9. This jump is caused by the way the biasing was split up into four quadrants, basically causing row 9 to be realigned with row 1. The importance of that is shown in Fig. 16(b). This figure shows measurements taken from a second chip, in which the biasing was not split up into four quadrants. The same gradient can be observed as in Fig. 16(a), but no realignment is found between rows 8 and 9. The result is that the gradient has an effect twice as strong, causing the DNL to be 0.2 LSB's instead of 0.1 LSB's as it is in Fig. 16(a).

C. Measured DNL and INL

The measured DNL and INL data are shown in Fig. 17. The measured DNL value is 0.1 LSB, and the measured INL value is 0.2 LSB. This clearly shows the advantage of the row and column randomization and the splitting of the biasing into four quadrants.

D. Sinewave Spectra

The most important performance aspect for the applications mentioned in the introduction is spectral purity. A measured sinewave spectrum for $F_s = 100$ MSample/s and $F_{sig} = 8$ MHz is shown in Fig. 18. The SFDR is 73 dB. The sinewave spectrum for $F_s = 300$ MSample/s and $F_{sig} = 100$ MHz is shown in Fig. 19. The measured SFDR is 60 dB. The sinewave spectrum for $F_s = 500$ MSample/s and $F_{sig} = 240$ MHz (almost Nyquist) is shown in Fig. 20. The SFDR is still better than 51 dB.

E. Sinewave Performance Summary

Many measurements like those of Figs. 18–20 have been performed. These measurements are summarized in Fig. 21, where the measured SFDR is plotted versus the normalized

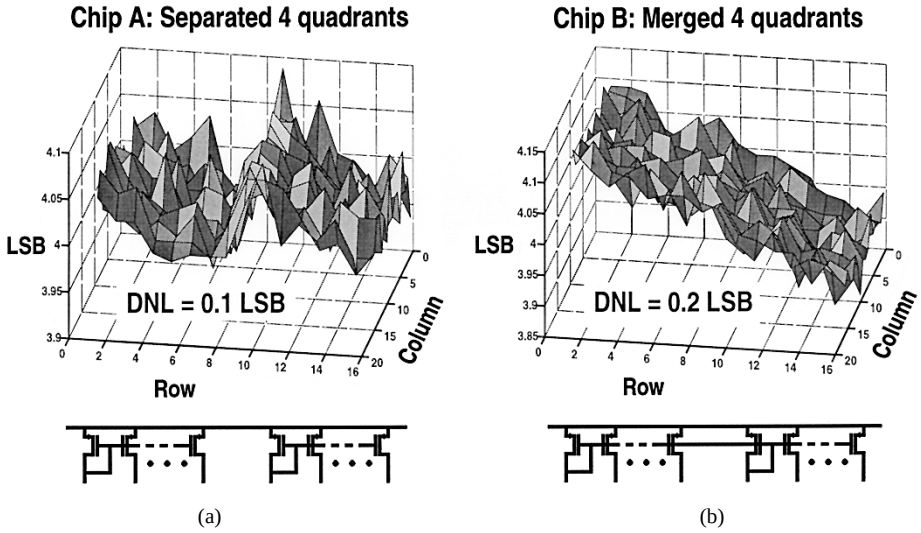


Fig. 16. Measured current source values.

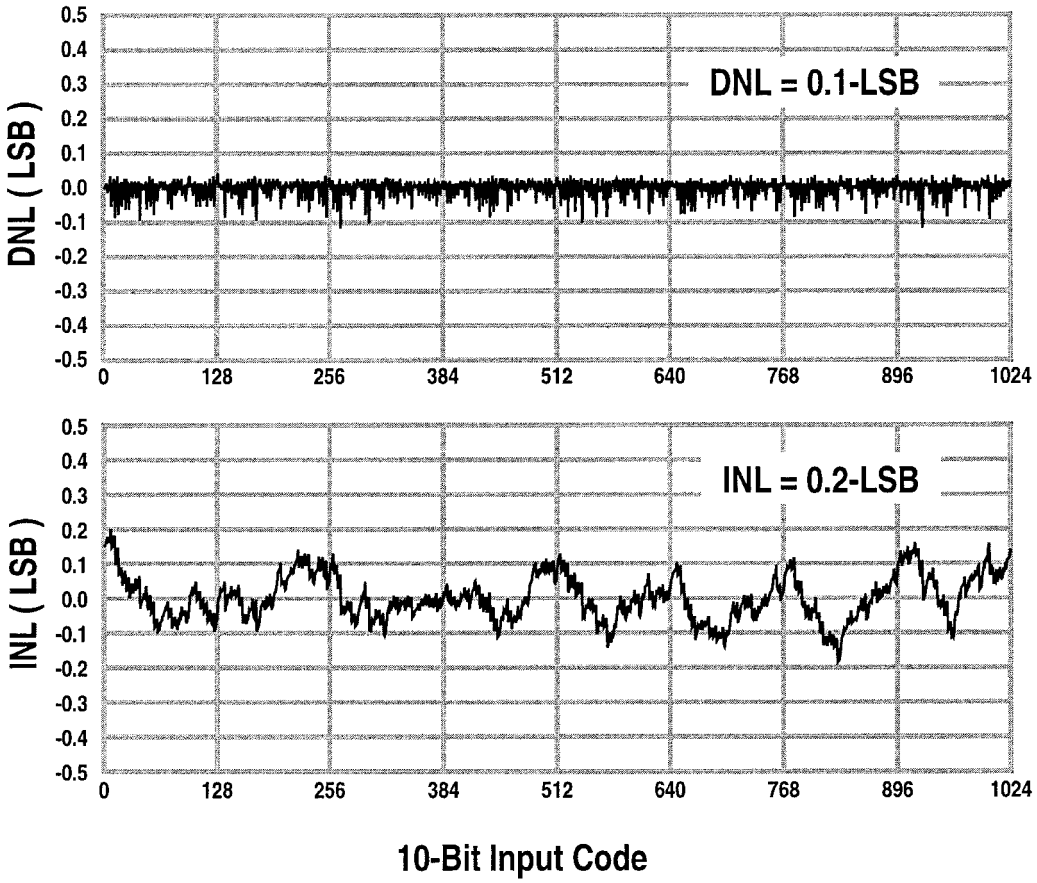


Fig. 17. Measured DNL and INL.

signal frequency, F_{sig}/F_s. In the graph, $F_{sig}/F_s = 0.5$ is the Nyquist frequency. For $F_s = 50$ MSample/s, this value is 25 MHz, and for $F_s = 500$ MSample/s, it is 250 MHz. As is shown, for sampling frequencies up to 200 MSample/s and signals from dc to Nyquist, the measured SFDR is better than 60 dB. For sampling frequencies up to 400 MSample/s and signals from dc to Nyquist, the measured SFDR is better than 55-dB.

F. AGC Function: Measured SFDR Versus I_{bias}

Cable modem applications require an automatic gain control (AGC) function to be added to the DAC output signal. This was obtained by varying the input bias current, I_{bias}, of the DAC. A measurement of SFDR as a function of I_{bias} was performed at $F_s = 125$ MSample/s and $F_{sig} = 40$ MHz with fixed loading resistance. The results are shown in

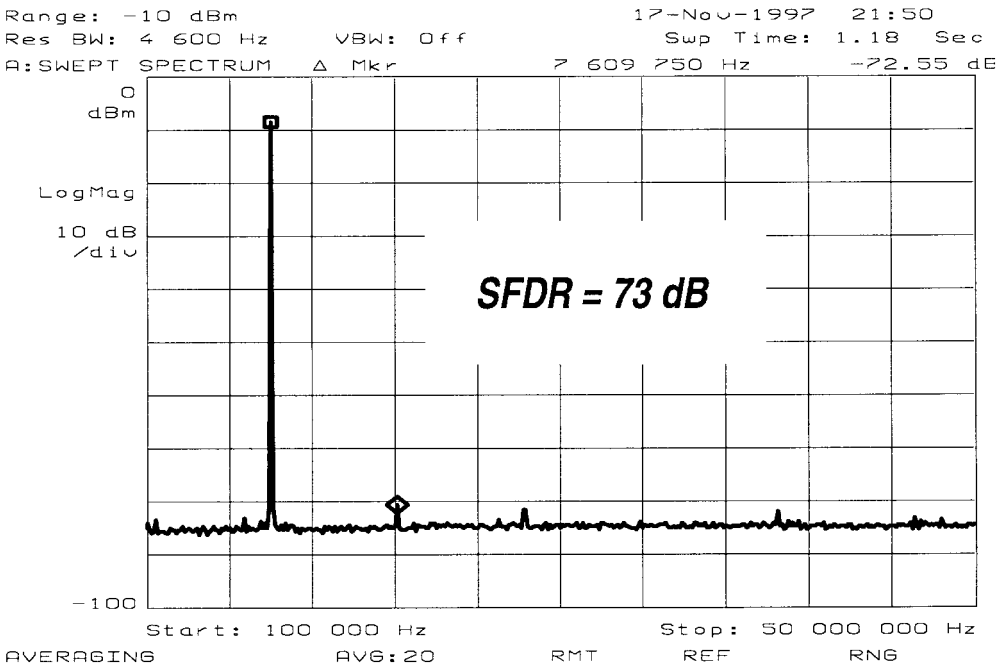


Fig. 18. Sinewave spectrum for $F_s = 100$ MSample/s, $F_{sig} = 8$ MHz.

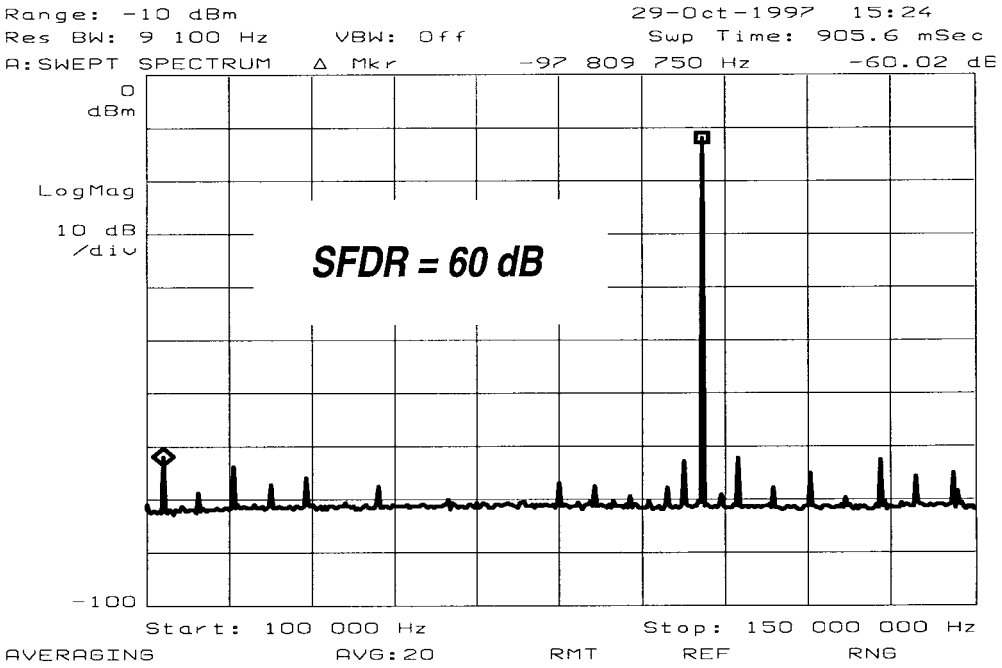


Fig. 19. Sinewave spectrum for $F_s = 300$ MSample/s, $F_{sig} = 100$ MHz.

Fig. 22. The circuit was designed for a bias current of 400 μA, in the middle of the curve. Decreasing the bias current decreases the SFDR because the effective gate-source voltage ($V_{gs} - V_{th}$) decreases and threshold voltage mismatch becomes more dominant. Increasing the bias current will also decrease the SFDR since the output compliance will be reached due to the increasing output swing. As is shown in Fig. 22, the flat spot is more than an octave wide and could be used without any degradation of the SFDR. If an SFDR of 60-dB can be tolerated, however, an AGC range of over 20-dB may be obtained in this way.

G. Measurement Summary

All measurements are summarized in Table II. The maximum sampling frequency is 500 MSample/s. The output swing is 2 V_{pp}, differential into a 75 Ω load. At 500 MSample/s, the analog part and the digital part draw 18 mA and 20 mA, respectively, from a 3.3 V power supply.

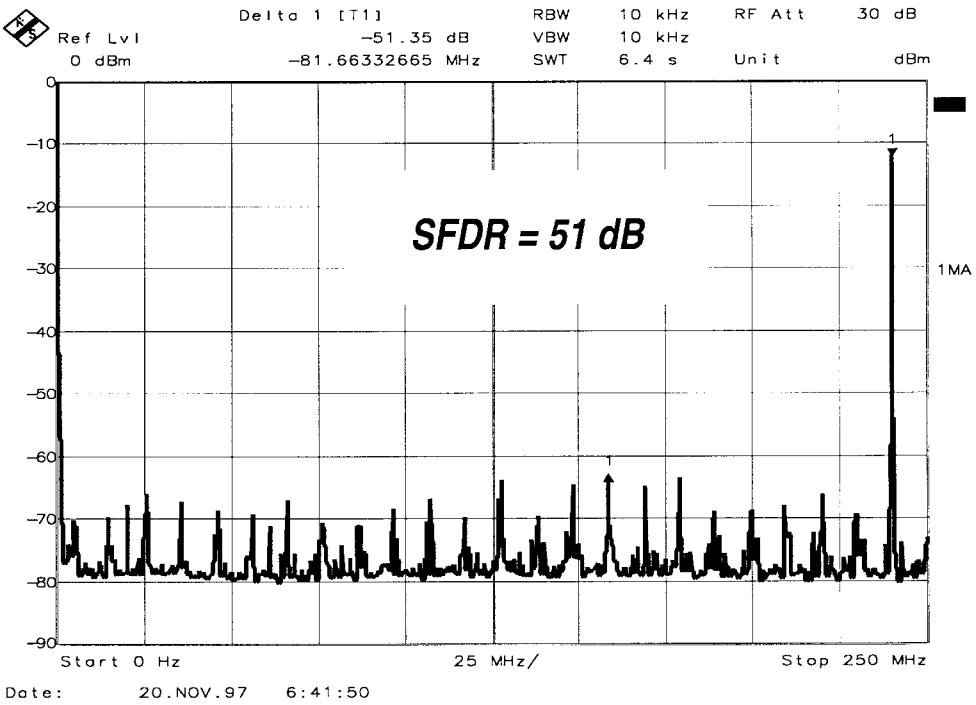


Fig. 20. Sinewave spectrum for $F_s = 500$ MSample/s, $F_{sig} = 240$ MHz.

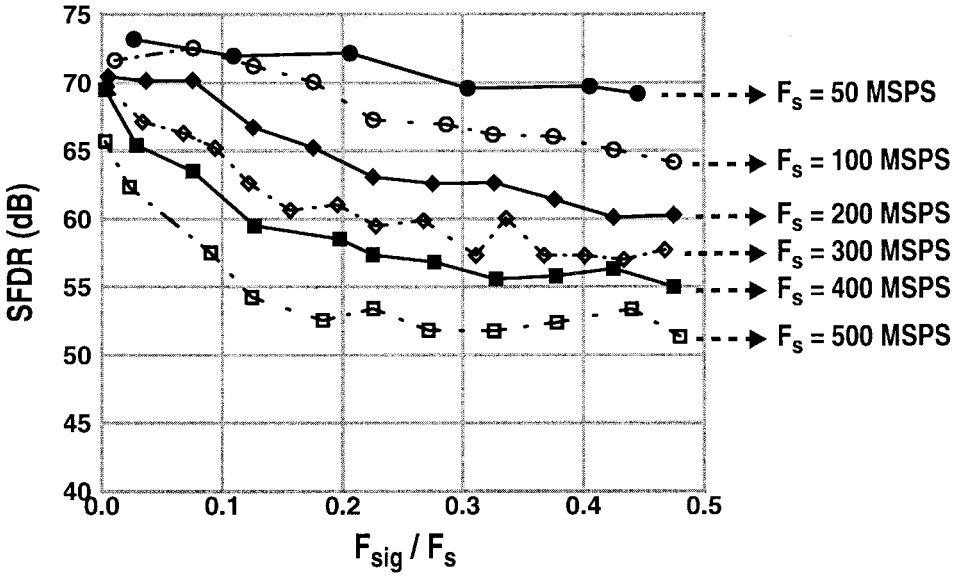


Fig. 21. Sinewave performance summary.

VIII. Conclusions

The thermometer-coded architecture is shown to have superior spectral purity at high sampling speeds, especially for output frequencies approaching the Nyquist frequency. It has also been shown that, based on area minimization only, a very flat minimum exists allowing for a high degree of segmentation. The optimum segmentation found in this design used eight thermometer-coded bits in the MSB section and 2 bits in the LSB section. It was shown that a tradeoff exists between good SFDR performance at high frequencies and area.

A 10-bit DAC was implemented in a 0.35 μm, single-poly, four-metal, 3.3 V, standard digital CMOS process, occupying 0.6-mm^2. For $F_s \leq 400$ MSample/s, this design shows an SFDR better than 55-dB, even for signals close to Nyquist.

Acknowledgment

The authors wish to thank S. Tsubota for designing the 12-b 500-MSample/s CMOS two-tone DDFS and the following colleagues at Broadcom Corp. for contributions to this project: Dr. F. Lu, Dr. K. Chan, D. Reynolds, D. Cheung, Dr. A. Buchwald, Dr. H.-C. Liu, K. Hublitz, and D. Nguyen.

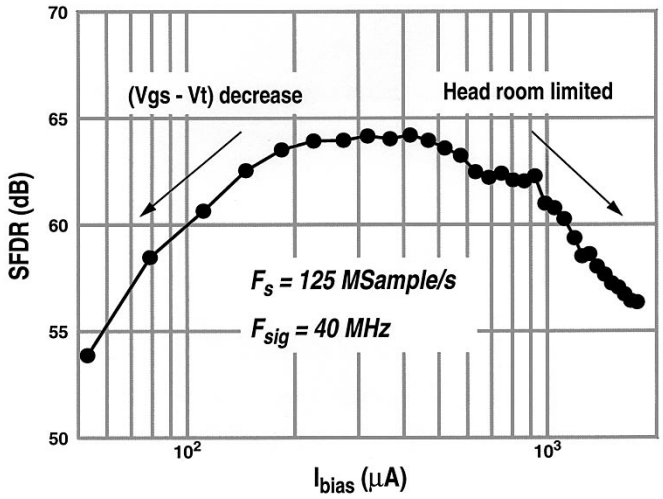


Fig. 22. AGC function: measured SFDR versus I_{bias}.

TABLE II
MEASURED PERFORMANCE

Technology	0.35μm (1P4M) pure digital CMOS
Area	0.6mm^2
Sampling Frequency	500 MSample/s
Ouput Swing (into 75Ω load)	2V$_{pp}$ (differential)
Power Disspation (at 500 MSample/s)	18mA (analog)
	20mA (digital)
	from 3.3V supply

REFERENCES

[1] T.-Y. Wu, C.-T. Jih, J.-C. Chen, and C.-Y. Wu, "A low glitch 10-bit 75-MHz CMOS video D/A converter," *IEEE J. Solid-State Circuits,* vol. 30, pp. 68–72, Jan. 1995.

[2] S.-Y. Chin and C.-Y. Wu, "A 10-b 125-MHz CMOS digital-to-analog converter (DAC) with threshold-voltage compensated current sources," *IEEE J. Solid-State Circuits,* vol. 29, pp. 1374–1380, Nov. 1994.

[3] B. G. Henriques and J. E. Franca, "A high-speed programmable CMOS interface system combining D/A conversion and FIR filtering," *IEEE J. Solid-State Circuits,* vol. 29, pp. 972–977, Aug. 1994.

[4] S. Brigati, G. Caiulo, F. Maloberti, and G. Torelli, "Active compensation of parasitic capacitances in a 10 bit 50 MHz CMOS D/A converter," in *CICC Dig. Tech. Papers,* May 1994, pp. 507–510.

[5] D. Draxelmayr, "A CMOS triple 9-Bit 180 MHz DAC for HDTV applications," in *CICC Dig. Tech. Papers,* May 1993, pp. 28.3.1–28.3.4.

[6] J. M. Fournier and P. Senn, "A 130-MHz 8-b CMOS video DAC for HDTV applications," *IEEE J. Solid-State Circuits,* vol. 26, pp. 1073–1077, July 1991.

[7] A. W. Vogt and I. J. Dedic, "A 10-bit high speed CMOS DAC macrocell," in *CICC Dig. Tech. Papers,* May 1989, pp. 6.7.1–6.7.4.

[8] A. Abrial, J. Bouvier, J.-M. Fournier, P. Senn, and M. Veillard, "A 27-MHz digital-to-analog video processor," *IEEE J. Solid-State Circuits,* vol. 23, pp. 1358–1369, Dec. 1988.

[9] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits,* vol. 24, pp. 1433–1440, Oct. 1989.

Chi-Hung Lin was born in Keelung, Taiwan, R.O.C., in 1967. He received the B.S. degree in electrical engineering from National Taiwan University in 1989 and the M.S. and Ph.D. degrees in electrical engineering from University of California, Los Angeles, in 1994 and 1998, respectively.

From 1989–1991, he served in the Chinese Army Missile Corps as a Maintenance Officer and was granted the Best Personnel Award in 1991. From 1991–1994, he was involved in the study of CMOS device physics and reliability. In 1994, he joined Broadcom Corporation, Irvine, CA, where he became a Staff Scientist in charge of the research and development of high speed data converters.

Klaas Bult was born in Marienberg, The Netherlands, in 1959. He received the M.S. degree in electrical engineering in 1988 and the Ph.D. degree, also in 1988, from the University of Twente, Enschede, The Netherlands.

In 1988, he joined Philips Research Laboratories, where he worked on basic analog CMOS circuits, predominantly for consumer applications in audio and video. In 1993, he was a part-time Professor at the University of Twente. In 1994, he became an Associate Professor at the University of California, Los Angeles, where he taught analog and digital circuit design and conducted research in the area of high speed digital-to-analog and analog-to-digital conversion and RF CMOS circuits. In 1996, he joined Broadcom Corporation, Irvine, CA, where he became Director of Analog and RF Microelectronics Technology. His work focuses on high-speed CMOS analog and mixed-signal processing.

Dr. Bult was a corecipient of the Lewis Winner Award for outstanding conference paper of ISSCC 1990, ISSCC 1992, and ISSCC 1997.