A Single-Phase Photovoltaic Inverter Topology With a Series-Connected Energy Buffer

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***Abstract*—Module integrated converters (MICs) have been under rapid development for single-phase grid-tied photovoltaic applications. The capacitive energy storage implementation for the double-line-frequency power variation represents a differentiating factor among existing designs. This paper introduces a new topology that places the energy storage block in a series-connected path with the line interface block. This design provides independent control over the capacitor voltage, soft-switching for all semiconductor devices, and the full four-quadrant operation with the grid. The proposed approach is analyzed and experimentally demonstrated.**

***Index Terms*—AC module, bidirectional power transfer, cycloconverter, dc-ac power converters, distributed power generation, double line-frequency ripple, grid-connected PV systems, high-frequency ac-link, module integrated converter (MIC), multiport circuit, photovoltaic (PV) inverter, photovoltaic power systems, resonant power converters, single-phase energy storage, single-phase inverters, single-stage inverters, switching circuits, zero voltage switching.**

I. Introduction

GRID-TIED inverters for photovoltaic systems represent a rapidly developing area. Module-integrated converters (MICs), sometimes known as microinverters, are designed to interface a single, low-voltage (25–40 V, typically) panel to the ac grid [1]–[5]. Such converters provide a number of benefits: ease of installation, system redundancy, and increased energy capture in partially shaded conditions [6].

MICs typically target single-phase electrical systems [7] (e.g., at 240 V), and are typically restricted to the unity power factor operation [8]. Therefore, the converter must deliver average power plus a time-varying power component at twice the line frequency, while drawing a constant power from the PV module. Fig. 1 illustrates the power transfer versus time for the grid and the PV module, with the shaded area between the curves indicating the temporal energy storage required for the inverter. To model this transfer of energy through the converter, a generalized three-port system can be used. The constant power source

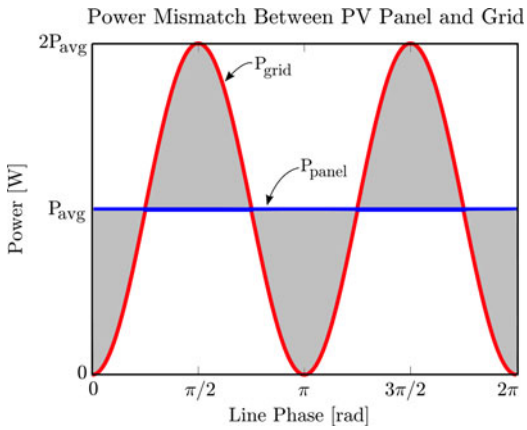

Fig. 1. Power flow mismatch between the grid and a constant power source results in the shaded area, representing the required energy storage.

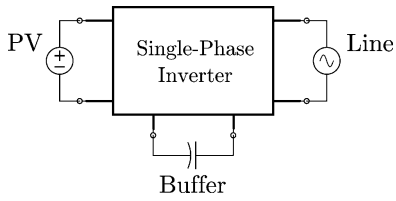

Fig. 2. Generalized grid-connected power converter, visualized as a three-port system.

of the PV and the sinusoidal power load of the grid are illustrated in Fig. 2, and can be written as

$$P_{\mathrm{PV}} = P_{\mathrm{avg}} \tag{1}$$

$$P_{\mathrm{Line}} = -P_{\mathrm{avg}}(1 - \cos(2\omega_l t)) \tag{2}$$

when no reactive power is transferred. The energy storage buffer must absorb and deliver the difference in power between these two ports, specifically

$$P_{\mathrm{Buf}} = -P_{\mathrm{avg}} \cos(2\omega_l t). \tag{3}$$

Inverters investigated in the past (see the literature reviews [4], [5]) can be classified by the location and the operation of the energy storage buffer within the converter. Most single-stage topologies, such as flyback and ac-link converters, place capacitance in parallel with the PV panel [9], [10]. This is an effective low-complexity implementation, but to avoid interfering with the maximum peak-power tracking (MPPT) efficiency, substantial energy storage is required to limit the voltage ripple across the panel. A second common method involves two complete cascaded conversion stages, providing energy storage at an intermediate dc bus. This arrangement can be implemented with less energy storage than the previous method, as a larger voltage fluctuation on the intermediate bus can be tolerated

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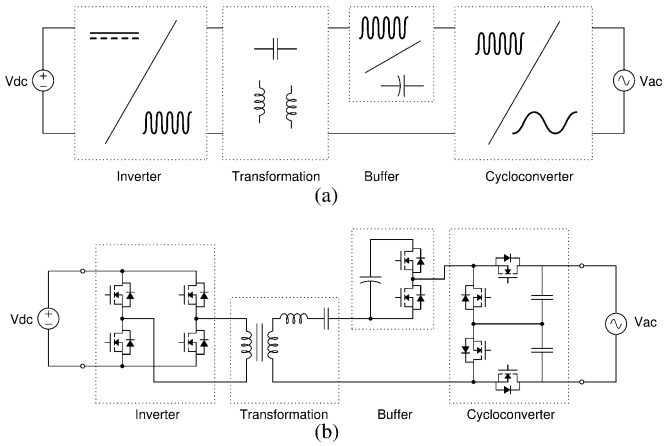

Fig. 3. Proposed photovoltaic module-integrated converter: (a) block diagram and (b) schematic.

without impacting the MPPT operation. The removal of the energy storage from the input also improves the transient response for peak-power tracking, as the PV module voltage can be controlled with a much higher bandwidth.

One drawback common to both of the energy storage methods described previously involves the typical use of electrolytic capacitors for the dc energy storage. Electrolytic capacitors are traditionally selected due to their high energy density, but suffer from the stigma of long-term failure rates. As MICs are typically mounted on the frame or backsheet of the PV module assembly, the high temperatures can accelerate aging processes for many of the internal components. To address this, focus is placed on improving converter efficiency (i.e., reduction in thermal output) and transitioning to the use of higher-reliability capacitors. Recent developments in converter topologies have included "third-port" systems [11], [12], providing active control of the energy storage stage, independent of the input and output voltages. This reduces the required energy storage, and provides the opportunity for less energy-dense film capacitors to be used.

The power converter presented in this paper implements a new type of third-port topology, where the energy storage (buffer) block is placed "in series" with the line voltage interface. The topology achieves high efficiencies with its continuous constant-power operation, zero-voltage switching (ZVS) capability for all devices, and reduced volt-seconds applied to the high-frequency transformer.

II. Proposed Solution

The block diagram and schematic in Fig. 3 illustrate the four functional blocks of the converter: the high-frequency resonant inverter, transformation stage, energy buffer, and cycloconverter. Each is connected electrically in series, with a common high-frequency resonant current linking them together.

At first glance, this series-connected configuration would seem to impose a heavy conduction-loss penalty. However, scaling up device sizes appropriately can reduce this impact, and the switching losses associated with large MOSFET devices can be greatly reduced through soft-switching techniques [13]. Additionally, the resistive channel structure allows current to flow both directions through the device, allowing for bidirectional power flow in each block of the converter. This is in contrast with devices such as IGBTs, SCRs, and diodes which allow current flow in a single direction and impose a fixed on-state voltage drop. Additionally, the figure-of-merit for MOSFETs has improved steadily since their introduction, particularly with the recent charge-compensation principles. This has allowed high-voltage silicon MOSFETs to surpass the "silicon limit" [14]–[16] and become viable for voltage ranges once relegated to low-frequency IGBTs. Additionally, the emergence of wide-bandgap FET-based device structures, implemented in SiC and GaN, have the potential to meet these same voltage levels while dramatically reducing the on-state resistance and undesirable device parasitics [17], [18]. This historical semiconductor device progress, combined with these and other anticipated future developments, are a motivating factor in the elimination of p-n junction devices in the topology. This study shows that this approach provides high efficiency with presently available devices, and is anticipated to scale with the improvements in device technology. Even with the departure from traditional converter design, the well-known methods and algorithms for MPPT [19], grid synchronization [20], and islanding detection [21] can continue to be used.

To place the series-buffer topology in context, a comparative listing of both commercial and academic work is presented in Table I. At the expense of slightly higher complexity, the proposed converter provides a number of additional capabilities while achieving an *unoptimized* efficiency that matches presently available designs.

III. Topology Operation and Analysis

At a very high level, the converter operation is closely related to the ac-link family of topologies. Here, the switching waveforms of all three series-connected blocks are responsible for generating the intermediate high-frequency current waveform. This can be seen in Fig. 4, where each active switching block is replaced with an idealized square-wave voltage source, and connected in series with the resonant circuit. To modulate power flow through the converter, each block uses the resulting series current as a reference, to which it readjusts its switching waveform appropriately.

The interdependence of the resonant current and switching behavior of the three blocks presents a challenge for directly evaluating the full converter operation. To ease this, the analysis is performed with two simplifying approximations: 1) the quality factor of the series resonant circuit is sufficiently high to approximate it as a sinusoidal current source operating at the switching frequency; and 2) the voltage at each terminal of the converter (PV, buffer, and line) changes slowly enough, relative to the switching frequency, that they can be approximated as constant over a switching cycle. With these, the converter can then be decoupled into the the two circuits in Fig. 5, separated such that the dc-connected inverter and transformation blocks are grouped into the *primary* side, and the buffer and cycloconverter are grouped into the *secondary* side. This permits the two

TABLE I
PERFORMANCE COMPARISON WITH EXISTING MICROINVERTERS

	This Work	(1)	[10]	[22]	[23]	(2)	(3)	[9]	[11]
Topology	Series-Buffer	Flyback + Unfolder			Boost + ac-Bridge			Ac-Link	Parallel-Buffer
Energy Storage	Independent	Input			Intermediate DC			Input	Independent
Input Voltage (V)	25–40	22–36	25–50	25–45	20–40	25–37	30–50	25–40	—
Rated Power (W)	200	215	200	215	250	250	250	175	200
CEC Efficiency [24] (%)	95.5	96	~93	~93.5	95	95	96	95.9	—
Reactive Power	Yes	No	No	No	Yes	Yes	Yes	Yes	Yes
Complexity	High	Low			Medium			Medium	High

All units are specified with a nominal 230–240V, 50–60 Hz mains interface.
(1) Enphase Energy, M215-60-2LL.
(2) SolarBridge Pantheon II, P250LV-240.
(3) Power-One, MICRO-0.25-I-OUTD-US-208/240.

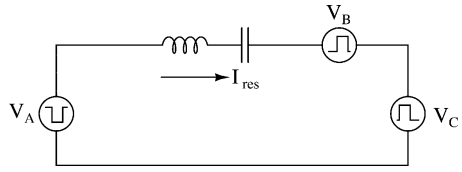

Fig. 4. Proposed topology of Fig. 3, where each active switching block is replaced with a square-wave voltage source. The applied voltage of all three blocks results in a high-frequency series current which links each block together.

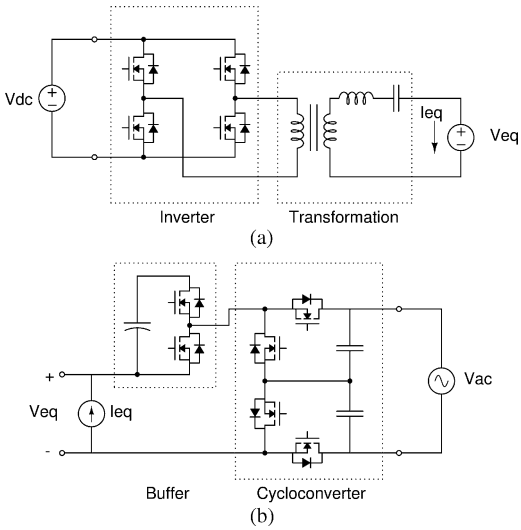

Fig. 5. Equivalent circuits representing the (a) primary and (b) secondary sides, decoupled by approximating the output of the transformation stage as a current source.

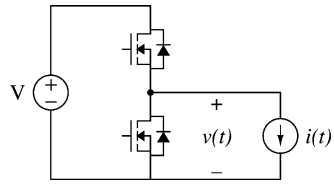

Fig. 6. Constituent subcircuit of the buffer and cycloconverter blocks from Fig. 5(b).

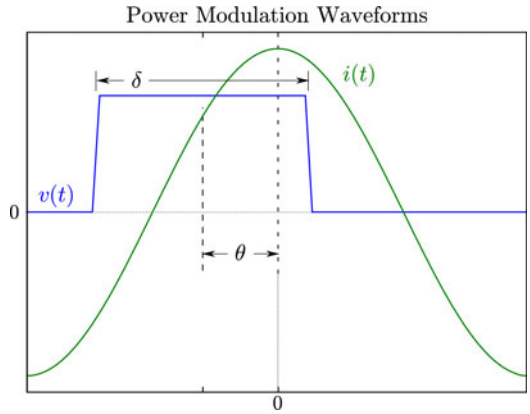

Fig. 7. Current and voltage operating waveforms of the constituent subcircuit in Fig. 6, illustrating the control parameters δ and θ.

circuits to be analyzed separately, which motivates the design process outlined in this section.

A. Switch Modulation

Both the primary and secondary sides of the converter are constructed from a number of canonical totem-pole structures. The buffer is composed of one such block, where the energy storage voltage is represented as unipolar, while the line-interfaced cycloconverter is composed of two such blocks, in a common-source layout (each providing operation under opposite voltage polarities).

The modulation of power through the simple circuit in Fig. 6 is accomplished by controlling the switching of the voltage waveform $v(t)$ relative to the series resonant current $i(t)$. This is shown in in Fig. 7 where the resonant current and switching-voltage waveform are illustrated with the variables δ and θ, corresponding to duty-cycle and phase-shift parameters, respectively. The average power delivery over a switching cycle can then be expressed as a function of these components through

$$\begin{aligned}\langle P \rangle &= \frac{1}{T}\int_0^T i(t)v(t)\mathrm{d}t \\ &= \frac{VI}{\pi}\cos(\theta)\sin(\delta/2) \end{aligned} \tag{4}$$

where δ and θ are expressed in radians. This same result can also be reached by representing the voltage and current waveforms as phasor quantities (at the switching frequency). It is important to note that for a given voltage, current, and power requirements, a continuum of solutions exist for the control variables, providing the flexibility to implement additional constraints, such as soft-switching transitions.

B. Resonant Current Magnitude

In addition to the switching parameters, the resonant current magnitude in (4) remains as an additional parameter for

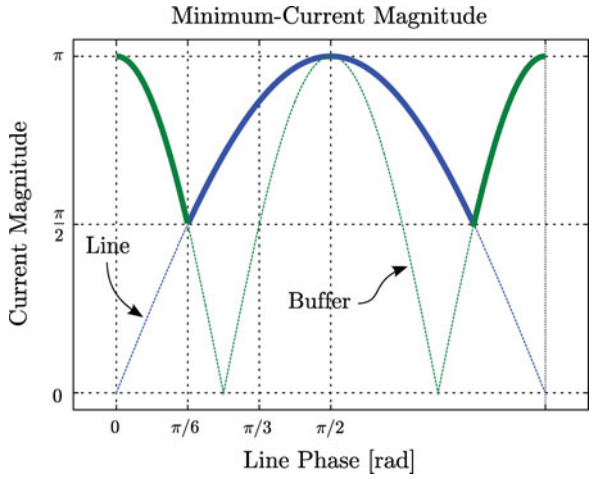

Fig. 8. Minimum resonant current magnitude requirements for the buffer block and cycloconverter, including the bold line indicating the envelope of current that meets both constraints.

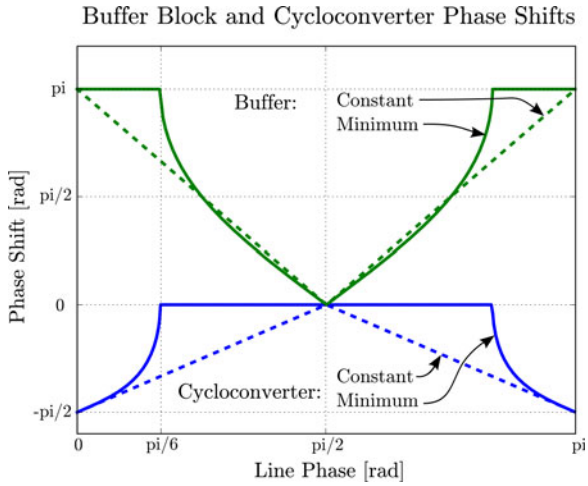

Fig. 9. Phase-modulation control parameters for the cycloconverter and buffer blocks, when operated under constant-current and minimum-current modes.

modulating the power transfer through the converter. For each block, a lower bound exists on the required magnitude of current needed to achieve a desired power transfer. As the terminal voltages V and resonant current magnitude I of the canonical circuit in Fig. 6 vary slowly over a line cycle, the defined power flow requirements in (1)–(3) result in the minimum current profiles shown in Fig. 8. For this case, the buffer-block voltage is assumed to be constant, such that the peak current requirements of I_B and I_C are equal.

Operating with the minimum resonant current may be desirable to limit conduction losses; however, the selection of current magnitude directly impacts the resulting converter control parameters. When operating with a fixed duty cycle, and implementing simple phase-shift control, the required phase-angle for each block can be derived from (4), such that

$$\theta_C(t) = \pm\cos^{-1}\left(\frac{\pi I_C \sin(\omega_l t)}{I_r(t)}\right) \tag{5}$$

$$\theta_B(t) = \pm\cos^{-1}\left(\frac{\pi I_B \cos(2\omega_l t)}{I_r(t)}\right) \tag{6}$$

where θ_C and θ_B are the phase angle parameters for the cycloconverter and buffer blocks, respectively, I_C and I_B are the corresponding peak current requirements, and $I_r(t)$ is the resonant current amplitude. Each phase expression is symmetric and contains two valid solutions, allowing a choice based on an external constraint or preference (e.g., ZVS).

The phase solutions when operating with minimum current are dependent on the waveform segments in Fig. 8. The block with the largest current requirement maintains a constant phase, whereas the remaining will vary. With the buffer and cycloconverter having the same peak current requirements as before, then

$$\theta_C(t) = \begin{cases} \pm\cos^{-1}\left(\dfrac{\pi\sin(\omega_l t)}{\cos(2\omega_l t)}\right) & \text{if } \omega_l t \in \left[0, \dfrac{\pi}{6}\right] \\ \pm\cos^{-1}(1), & \text{if } \omega_l t \in \left[\dfrac{\pi}{6}, \dfrac{\pi}{2}\right] \end{cases} \tag{7}$$

and

$$\theta_B(t) = \begin{cases} \pm\cos^{-1}(-1), & \text{if } \omega_l t \in \left[0, \dfrac{\pi}{6}\right] \\ \pm\cos^{-1}\left(\dfrac{\pi\cos(2\omega_l t)}{\sin(\omega_l t)}\right) & \text{if } \omega_l t \in \left[\dfrac{\pi}{6}, \dfrac{\pi}{2}\right] \end{cases} \tag{8}$$

where each of these solutions contain even symmetry at intervals of $\pi/2$.

As a comparison, if the resonant current amplitude is held constant over a line cycle, where $I_r(t)/\pi = I_C = I_B$, the resulting phase-angle control parameters can be compactly written as

$$\theta_C(t) = \pm\cos^{-1}(\sin(\omega_l t)) \tag{9}$$

$$\theta_B(t) = \pm\cos^{-1}(\cos(2\omega_l t)) \tag{10}$$

which contain the same symmetry as those for the minimum-current mode. The resulting control angles of (7)–(10) are plotted over a half-line cycle in Fig. 9, with only the ZVS solutions shown.

C. Transformation and Inverter Design

With an understanding of the behavior of the secondary side of the converter, the primary-side circuit in Fig. 5(a) can be considered with the objective of obtaining an inverter and transformation combination capable of synthesizing the required resonant current, as defined in the preceding section. The transformation stage is designed to provide an impedance appropriate for the primary side driving circuit, in this case it is desired to present a positive reactance at the switching frequency for the bridge converter to achieve the desired ZVS conditions. Additionally, the magnitude of the impedance must be managed such that the inverter is capable of operating over the full required voltage and power range.

The varying control and behavior of the secondary half of the converter results in a dynamic load over a line cycle. Using phasors, the secondary-side circuit can be approximated as a complex impedance at the switching frequency, as shown in

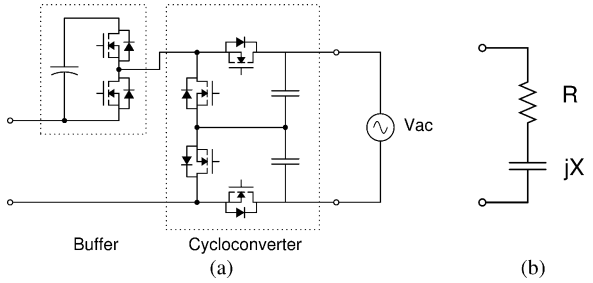

Fig. 10. (a) Buffer block and cycloconverter can be approximated as (b) the complex load impedance.

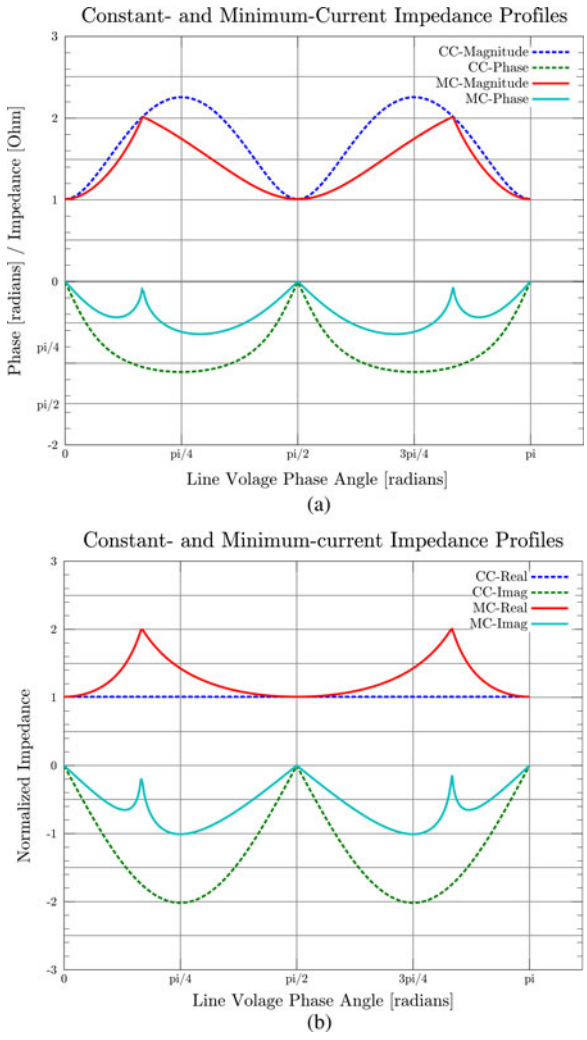

Fig. 11. Complex impedance of the buffer-block and cycloconverter are shown to vary over a line cycle based on the constant- or minimum-current drive method. Both the (a) magnitude/phase and (b) real/reactive relationships are presented.

Fig. 10. The equivalent impedance

$$\bar{Z} = \frac{\bar{V}_C + \bar{V}_B}{\bar{I}} \tag{11}$$

of this stage is calculated and shown in Fig. 11 for both the constant and minimum-current envelopes considered previously.

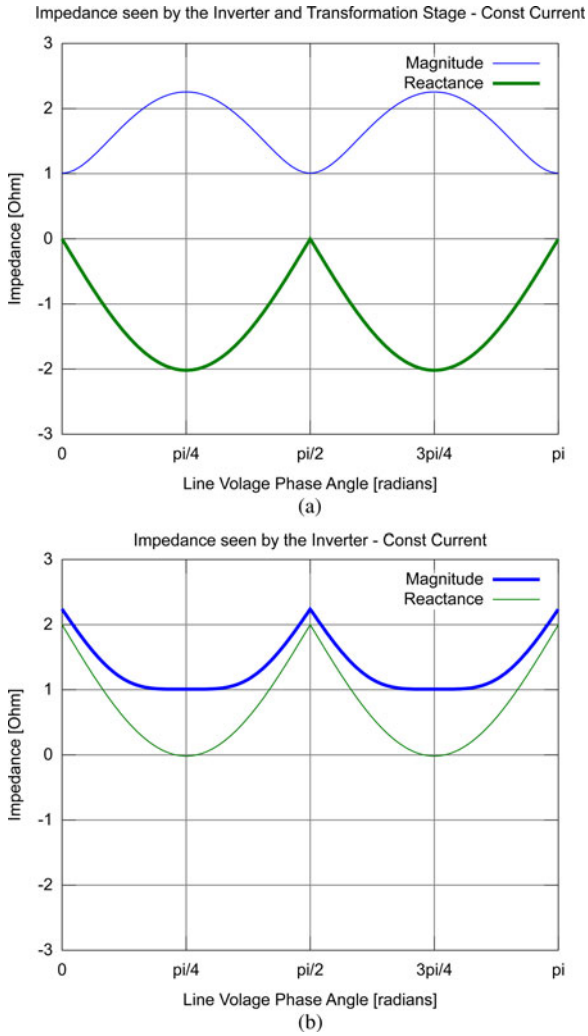

Fig. 12. Normalized load impedance, at the switching frequency, presented to the full-bridge inverter by (a) buffer-block, and cycloconverter stages, and (b) including the series-resonant tank. Without the inductance of the resonant tank, the reactance presented to the inverter prevents zero-voltage switching.

The lower reactive impedance for the minimum current envelope can be understood by the length of time the blocks' phase deviate from alignment with the resonant current (0 or π). The minimum-current operation always maintains one block in phase with the current, maximizing the power factor of the resonant tank, while the constant-current method results in higher reactance.

In the transformation block, the negative reactance of the secondary side is offset by selecting the components of the series-resonant tank to compensate. The resulting impedance changes, as shown Fig. 12, where the minimal required positive compensating reactance is provided. In this case, the peak magnitude remains the same; however, its overall shape has changed.

To drive this compensated load, the inverter is operated as a phase-shift full-bridge, where its applied voltage is defined in phasor form as

$$\bar{V} = 2\frac{V}{\pi}\sin(\delta/4)e^{j\theta} \tag{12}$$

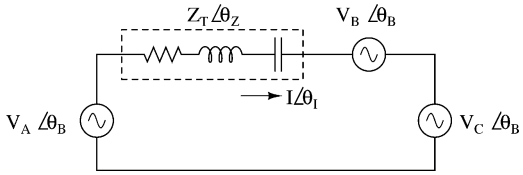

Fig. 13. Phasor equivalent of the circuit shown in Fig. 4, which approximates the operation of each active block as a sinusoidal voltage source.

where δ represents the duty cycle and θ is the phase of the voltage relative to the resonant current waveform. With control of this driving voltage, and the flexibility in selecting the transformer turns ratio and the resonant tank component values, a transformation stage and inverter can be created which is capable of synthesizing the required resonant current.

D. Control Parameter Solutions

With the control parameters for each block defined, the interdependence between them can be investigated by considering the operation of all blocks together. To simplify the analysis, the equivalent circuit in Fig. 13 illustrates the converter in phasor form, with the voltages normalized to allow the transformation stage to be lumped into a single-series element $z_T = R + jX_T$, implicitly dependent on the switching frequency ($f_{\rm sw}$). The series current can then be defined in terms of the circuit voltages and tank impedance, such that

$$\bar{I} = \frac{1}{Z_T e^{j\theta_Z}} \left(V_A e^{j\theta_A} + V_B e^{j\theta_B} + V_C e^{j\theta_C} \right) \tag{13}$$

and the power delivery for a given voltage source k is expressed as

$$\begin{aligned} P_k &= \frac{1}{2} Re \left\{ \bar{V}_k \bar{I}^* \right\} \\ &= \frac{1}{2} Re \left\{ V_k e^{j\theta_k} \frac{\left(V_A e^{-j\theta_A} + V_B e^{-j\theta_B} + V_C e^{-j\theta_C} \right)}{\left(Z e^{-j\theta_Z} \right)} \right\}. \end{aligned} \tag{14}$$

For a single block, this power transfer equation requires seven parameters: the switching frequency, and the magnitude and phase for the three voltage sources. This list can be reduced by choosing to define one phase as the reference, eliminating it as an unknown. Additionally, having implemented phase-shift modulation for the buffer and cycloconverter, in combination with their measurable terminal voltages, results in known voltage magnitudes for V_B and V_C. This leaves the switching frequency $f_{\rm sw}$, phases θ_B, and θ_C, and the effective driving voltage of the full-bridge V_A. The single-phase power flow requirements for the converter, given in (1)–(3), provide two independent constraints, and the remaining two are imposed by selecting an appropriate value for the switching frequency $f_{\rm sw}$ and full-bridge pulse-width δ_A (for control of V_A). To solve for θ_B and θ_C, one can take advantage of the inherently constrained domain of the phase variables to perform a direct search. Implementing an iterative solver is also effective, but often complicated by the existence of multiple solutions.

With a solution method in place for finding the unknown phase angles, it is repeated for additional combinations of the free variables $f_{\rm sw}$ and δ_A. This can also be accomplished by creating a map of the solutions, or an optimization algorithm can be implemented to converge toward a desirable result, such as minimizing loss. This process is again repeated for changing operating conditions, expanding the required solution space across power level $P_{\rm avg}$, input voltage $V_{\rm PV}$, and line voltage $V_{\rm line}$.

TABLE II
PROTOTYPE CONVERTER TARGET REQUIREMENTS

Parameter	Value	
Input Voltage	25–40	V_{DC}
Output Voltage	240 ± 10%	V_{AC}
Input Power	0–200	W
Line Frequency	50–60	Hz

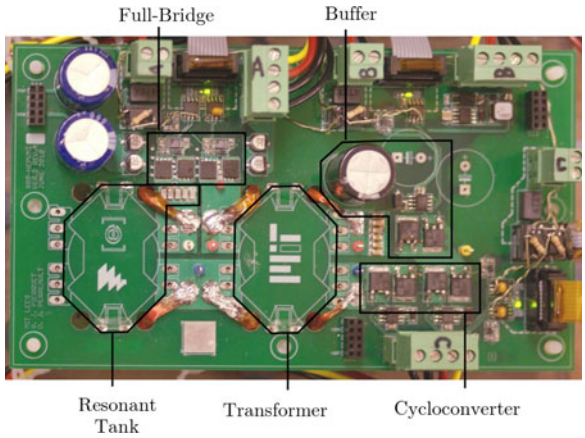

Fig. 14. Annotated photograph of the proof-of-concept implementation for the series buffer-block topology. The transformer and resonant inductors are located on the bottom side of the board. Outer dimensions: 18 × 11 cm.

IV. HARDWARE IMPLEMENTATION

To illustrate the performance and functionality of the series-connected buffer topology, as described in this paper, a prototype platform has been designed for interfacing a 72-cell photovoltaic module, to a single-phase 240-V mains. The operating requirements for the converter are outlined in Table II, and an annotated photograph of the converter can be seen in Fig. 14. The converter's primary power-stage topology follows directly the circuit shown in Fig. 3, with the components listed in Table III. Additional support circuitry, such as the required gate drive, isolation, and control hardware can be found in [25].

The resonant inductor value and transformer turns ratio were selected such as to meet the highest power transfer requirement at the lowest input voltage, while also providing enough inductive energy for ZVS transitions at light loads. The resonant inductance of the circuit includes both the discrete inductor and the leakage inductance of the transformer, totaling 6.73 μH. The resonant capacitance was selected such that its reactance was half of the inductor at the minimum operating frequency range of 100 kHz. This results in a value of 0.6 μF, and places the resonant frequency at 79 kHz.

TABLE III
OPERATING RANGE AND COMPONENT LISTING FOR PROOF-OF-CONCEPT CONVERTER IMPLEMENTATION

Parameter	Value	
Switching Frequency	100–500	kHz
Buffer Voltage	170	V_{DC}
Buffer Capacitance	141	μF
Resonant Inductor	6.44[1]	μH
Resonant Capacitance	0.60[2]	μF
Transformer	1:5[3]	
Full-bridge MOSFETs[4]	60	V
	8.0	mΩ
Cycloconverter and	650	V
Buffer-block MOSFETs[5]	299	mΩ

The resonant component values are listed as the values measured in-circuit.

[1] Resonant Inductor — 9 turns, 325 strand 38AWG litz; RM14-3F3 core, 3.8mm center-post gap.

[2] Resonant Capacitors — 6 Murata 0.1 μF 50V C0G, part number GCM31C5C1H104JA16L.

[3] Transformer — Primary: 5 turns, 300 strand 40AWG litz; Secondary: 25 turns, 100 strand 40AWG litz; RM14-3F3 core, ungapped.
Leakage Inductance (Primary): 0.288 μH, Magnetizing Inductance (Primary): 154.5 μH, Parallel Capacitance (Secondary): 23.9 pF.

[4] NXP part number: PSMN8R5-60YS.

[5] STMicroelectronics part number: STD16N65M5.

A. Experimental Operation

The operation and performance of the converter is measured in two different configurations. First, the converter is operated in dc–dc mode, stepped over a set of discrete operating points approximating an ac output. Second, the converter is operated in stand-alone dc–ac mode. In both configurations the converter is fed with constant-voltage at its input, and pre-populated lookup tables are used by the converter for the hardware control parameters.

The oscilloscope waveform captures in Fig. 15 are used to illustrate the switching-level operation of the converter at three points in the line cycle, with an output power of 100 W, an input voltage of 32 V, and a buffer voltage of 170 V. Starting at the zero crossing of the line, a line phase of 0° (0 V), Fig. 15(a) shows the buffer-block absorbing power, with its switching waveform nearly in-phase with the negative portion of the resonant current. The second capture occurs at a line phase of 30° (170 V), where the buffer block and cycloconverter are each absorbing 50 W from the source, with voltage waveforms switching complimentary to each other. At a line phase of 90° (340 V), shown in Fig. 15(c), the buffer and source are each providing 100 W to the cycloconverter, which is providing 200 W out.

In the dc–dc operation, the converter's efficiency over a line cycle was measured for five average-power levels, at an input voltage of 32 V. These results, shown in Fig. 16, demonstrate efficiencies above 91% for all conditions, with peaks above 98%. These are power stage efficiencies, and the inclusion of the gate drive and auxiliary power accounts for an additional loss of 1–1.8%. This was also performed at two additional input voltages [25], resulting in an approximate CEC efficiency [24] of 95.5%.

The converter was also operated in the full dc–ac mode, into a 60 Hz 240 V_{ac} line simulator, with an input voltage and power of 32 V and 100 W. This matches the operating conditions of the static waveform captures in Fig. 15, and one dataset in Fig. 16. The simplistic control implementation relied solely on

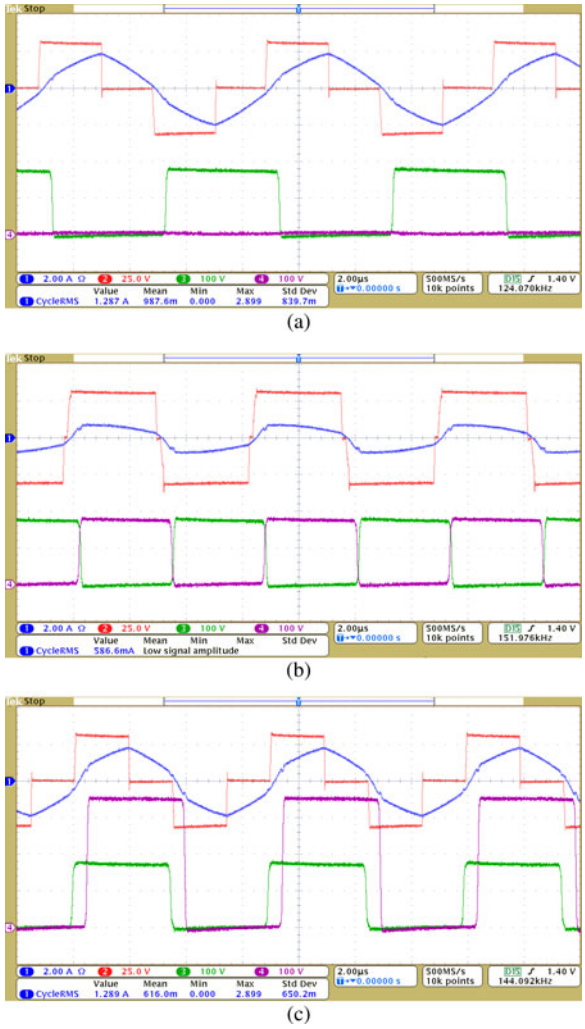

Fig. 15. Converter operation with 32 V input, 100 W average power, at three points in the line cycle: (a) 0°, 0 V; (b) 30°, 170 V; (c) 90°, 340 V. Waveform channel number and color key; (1) blue: current, (2) red: full-bridge, (3) green: buffer-block, and (4) purple: cycloconverter. Channels 1 and 2 are referenced to the top marker, while channels 3 and 4 are referenced to the bottom marker.

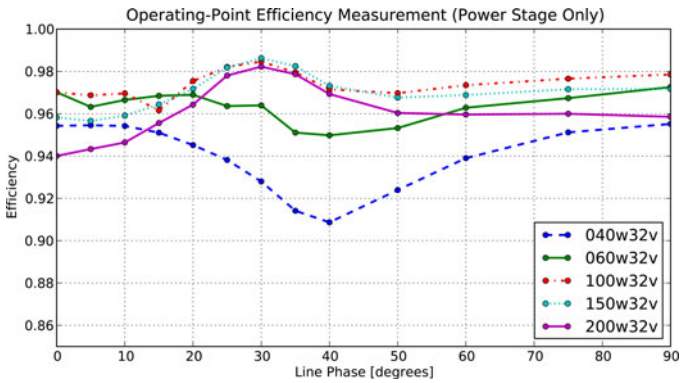

Fig. 16. Experimentally obtained power-stage conversion efficiencies for the prototype converter, at an input voltage of 32 V, over one-quarter of a line cycle.

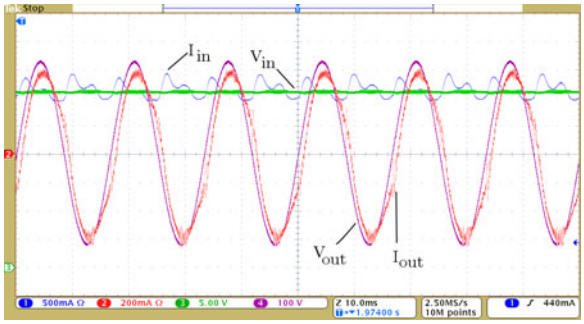

Fig. 17. Experimentally obtained dc input and (unfiltered) ac output waveforms, at an input voltage of 32 V. Waveform channel number and color key; (1) blue: input current, (2) red: output current, (3) green: input voltage, (4) purple: output voltage. Channels 2 and 4 are referenced to the center marker, while channels 1 and 3 are referenced to the bottom maker.

a control parameter lookup-table, indexed by its output voltage measurement.

This dc–ac operation results in a 95.3% efficiency, including all gate and auxiliary power. The voltage and current waveform measurements for the dc input and ac output of the converter are shown in Fig. 17. The ideal waveforms would have a constant input voltage and input current with a sinusoidal output current in-phase with the output voltage; however, the measured results deviate slightly from this. The largest contributor to the discrepancy comes from the uncompensated delay associated with voltage measurement, and more significantly, the time duration required to update the converter operating parameters; a total delay of 1 ms. This update latency primarily manifests itself as an unintended phase-shift in the output current relative to the line voltage (reactive power transfer), ultimately reflecting back as input-power ripple (seen as current ripple). This unintended operation also illustrates the well-behaved nature of the cycloconverter near the line zero crossings, where the opposing half-bridge circuits can be operated synchronously to prevent short-circuit conditions when the voltage polarity may be uncertain [9].

The residual current ripple drawn by the converter, intentional or not, must be suppressed to maintain a fixed point on the PV module I–V curve. This can be achieved with a relatively small additional capacitance at the input, stabilizing the voltage for MPPT. It is expected that effective compensation of the control loop delay will reduce, if not negate, the input ripple and this extra energy storage.

V. Conclusion

The converter design and implementation presented in this paper has demonstrated a new topology with an energy-storage buffer in the series-connected path with the line interface. It has an increased complexity relative to traditional designs, but allows control over the energy storage voltage and ripple, permitting the use of electrolytic or film capacitors. It also maintains the capability of reactive power transfer and high efficiency, as demonstrated.

The presented bench prototype provides verification of the functionality and performance of the design process. While not the primary focus, the standalone dc–ac test demonstrated 95.3% efficiency under representative operating conditions (100 W, 32 V input, 240 V output), all inclusive. Further improvements on these successful results are expected with optimized magnetics and online tuning of control parameters.

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