A DMOS integrated 320mW capacitive 12V to 70V DC/DC-converter for LIDAR applications

Tom Van Breussegem, Mike Wens, Jean-Michel Redouté, Eldert Geukens, David Geys and Michiel Steyaert
MICAS-ESAT Kasteelpark Arenberg 10 3000 Leuven Belgium, tvanbreu@esat.kuleuven.be

I. ABSTRACT

A 320mW integrated switched capacitor DC-DC converter is realized in a 0.35μm DMOS high voltage technology. This 10 stage converter generates 70V from a 12V voltage supply, at a maximum efficiency of 85.5% per stage. An on-chip control system varies the clock frequency from 0 to 35.4MHz in order to regulate the output voltage at varying loads and supply voltages. Each of the stages uses an integrated capacitor of 74pF. The total area of the chip is 6mm^2.

II. INTRODUCTION

Integrated DC/DC-converters have grown in importance due to the increased need for multiple on-chip voltages. In high voltage applications however, DC/DC-converters are still implemented with bulky discrete components, especially in the automotive industry [1] [2]. The cost of a DC/DC-converter is heavily determined by its components and its assembly cost. These factors clearly suggest the need for integrated high voltage DC/DC-converters. Integrated converters do not need bulky and expensive external passives: additionally since there are no external components, the assembly time and effort is reduced significantly. Besides those advantages, full integration makes it possible to reduce the overall system size since the DC/DC-converter will be integrated on one compact die, hereby making the use of these converters even more attractive.

The proposed converter is an integrated capacitive step-up converter. It is used to step up a 12V supply voltage to 70V in a Light Detecting and Ranging (LIDAR) system and to supply 320mW to this application. This LIDAR can measure distances by means of emitting a laser pulse. It is used in automotive industry to measure distances from one car to an other. A simple system diagram is shown in Fig. 1.

This LIDAR needs a 70v DC supply which is not present in the 12V environment, making a DC/DC-converter indispensable. The LIDAR generates a 50ns pulse and discharges in a 18nF capacitor hereby triggering the laser diode. During the pulse, 11A is flowing through the laser diode. In the off-cycle the capacitor is charged again by the DC-DC converter. This cycle will repeat itself after 150μs. When the transistor-switch is opened, current will continue to flow due to the parasitic inductance. Therefore a diode is added across the current limiting resistor. A 100nF capacitor is used to absorp this kickback current and this capacitor maintains an almost constant load current seen by the DC/DC-converter.

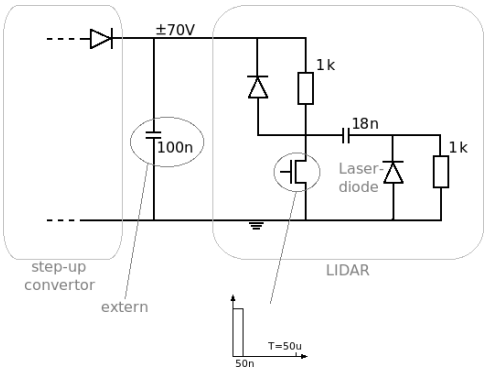

Fig. 1. The LIDAR-system

III. THE CHARGE PUMP

In integrated DC/DC-converter design the die area, which is related to the cost, is of great importance. Thus the key question is how to realize an integrated DC/DC using the smallest die area possible or to optimize the use of a given die area in terms of voltage conversion and wanted output power. Therefore, an area driven optimization was performed by the authors and recently published [3]. It is proven in this publication that a Dickson type implementation is superior to a cascaded voltage doubler implementation. Therefore it is investigated whether the Dickson topology can indeed meet the specs imposed by the LIDAR application.

This converter (shown in Fig. 2) is a two-phase converter. Charge transfer is established by toggling the capacitors in consecutive stages between ground and the input voltage supply. During the first phase, the bottom plates of the even numbered capacitors are charged to 12V, while the bottom plates of the odd capacitors are discharged to ground level. Thus in this phase charge is transferred from the even numbered to the odd numbered capacitors through the forward biased diodes. During the second phase, the bottom plates of the odd numbered capacitors are charged to 12V, while the bottom plates of the even numbered capacitors are discharged to ground level. In the second phase, charge is transferred from the odd numbered to the even numbered capacitors.

During both phases, charge is transferred from the input towards the output of the DC/DC-converter. Therefore in unloaded conditions the voltage over every stage's capacitor will increase with 12V, so that in steady state, the N-th stage output voltage is N+1 times the input voltage. Under loaded conditions the output voltage will be slightly lower because of the charge transfer towards the load [4]. However, the

operation principle remains identical.

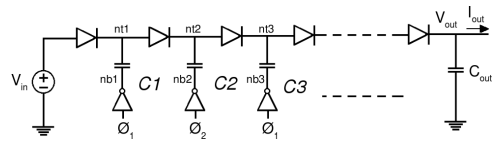

Fig. 2. Dickson topology

The output voltage of a Dickson chargepump is determined to be [5]:

$$V_{out} = V_{in} + \frac{N}{1+\alpha_{st}}(V_{in} - \frac{I_{out}}{fC}) \tag{1}$$

In which α_{st} is the percentage stray capacitance of the capacitors. The stray capacitance is mainly parasitic capacitance between the capacitor's plates and the die substrate (shown in Fig. 3 a)). By means of (1) the total capacitance that is necessary to generate an output voltage V_{out} and an output current I_{out} while switching at frequency f is determined. This yields:

$$C_{tot} = NC = \frac{I_{out}}{f}\frac{N^2}{NV_{in} + (V_{in} - V_{out})(1+\alpha_{st})} \tag{2}$$

The losses in a Dickson type converter are heavily determined by charging and discharging the stray capacitances of the capacitors and the parasitic capacitances in the drivers. The power loss is given by:

$$P_{loss} = f\left(C_{par,cap} + C_{par,drivers}\right)V_{in}^2 \tag{3}$$

$$P_{loss} = P_{loss,cap} + P_{loss,drivers} \tag{4}$$

$$P_{loss} = f\left(C_{tot}\alpha_{st} + C_{par,drivers}\right)V_{in}^2 \tag{5}$$

Equation (1) proves that for the same load, there is a trade-off between frequency and total capacitance. If less capacitance is available, the frequency needs to be higher. However based on (3) it can be seen there is no impact on $P_{loss,cap}$ since the change in frequency and in total capacitance, cancel each other out. But since the drivers have to be sized up in order to support the higher switching frequency, the power loss due to the parasitic capacitances of the clock inverters ($P_{loss,drivers}$) increases.

The main advantage of a Dickson-type charge pump topology (Fig. 3 a)), is that the bottom stray capacitances of the capacitors are not charged through the diode chain of the converter. These capacitances are charged directly by the input voltage source through the switch drivers. Therefore the bottom stray capacitances do not influence the required capacitance. The stray capacitance reduces the system efficiency only by increasing the switching losses in the driver chain. The top stray however will be charged and discharged through the diode chain and will influence the required C_{tot}. In most integrated capacitor types the top stray capacitance is much smaller than the bottom stray capacitance.

The capacitors are realized using finger-capacitors. Four metal layers are used. In total ten stages are implemented

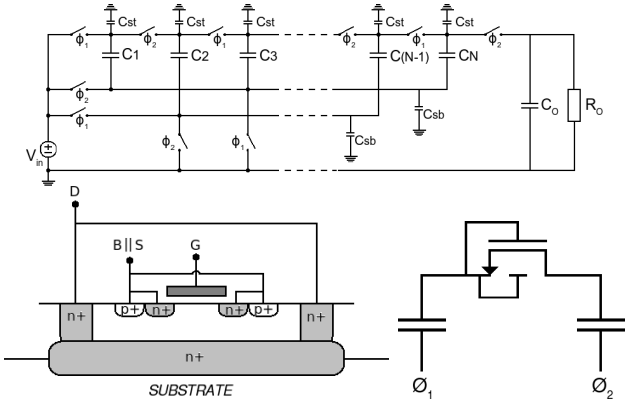

Fig. 3. a) A non-ideal N-stage Dickson converter b) Schematic view on a vertical NDMOS-transistor c) Inverted diode-configuration of the vertical NDMOS-transistor

each with a capacitor of 74pF with an area of 0.287mm^2 each. The diodes are implemented as vertical N-type DMOS devices(Fig. 3 b)). This device cannot be used in the obvious MOS-diode configuration since the gate source voltage will swing up to 12V which is higher than the maximum voltage rating of the devices (3.6V). Therefore the gate and source terminal are connected as shown in Fig. 3 c). The current flows through the diode between the P-type bulk and the N-type drain. Since there is only a small voltage drop in forward bias, this configuration proves to be a good solution.

IV. The control Loop

This charge pump is used under closed-loop regulation to ensure a constant output voltage independent of load variations. Therefore, the frequency of this converter is dynamically controlled by a control loop. The output voltage is measured using a resistor voltage divider and an error-amplifier (realized by means of a symmetrical OTA). This error-amplifier controls the VCO's frequency by comparing the sensed output voltage with the reference voltage.

The VCO is a current starved voltage controlled oscillator [6]. This topology is chosen for its large tuning range. In front of the VCO, an extra AB-gain-stage is added to realize more gain. Figure 4 illustrates the circuit of the implemented VCO.

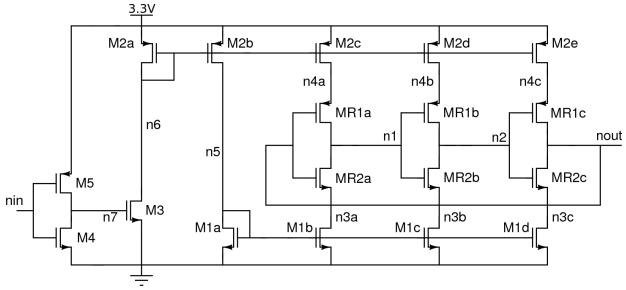

Fig. 4. Current starved VCO

V. Implementation of the switch drivers

In this high voltage charge pump, the implementation of the switch drivers is not trivial due to extra voltage constraints

on the devices. In most capacitive converters ([7] [8] [9]), the switch drivers are implemented as a simple inverter chain in the technology's native devices, which support the nominal voltage over all terminals. In this high voltage SC-SMPS, the DMOS-devices are used for implementing the switch drivers. These devices only support a 3.6V gate source voltage and need to be driven by the low voltage control circuit. The P-DMOS need a gate swing between 12V and 8.7V and the N-DMOS a gate swing between 0 and 3.3V. The N-DMOS devices can thus been driven directly by the control circuitry and the P-DMOS devices will be driven by a level shifter [10]. A latch based level shifter was designed to support the 8.7V-12V gate swing (shown in Fig. 5 a)).

The latch based level shifter requires a voltage rail of 8.7V for the upper driver chain and the latch. This voltage rail is generated internally by a linear voltage regulator. The schematic of this regulator is shown in Fig. 5 b). It is implemented by two resistor voltage dividers, a symmetrical OTA and a NDMOS-transistor Mv. The shown inverters between the 8.7V and 12V supply lines represent the driver chains which drive the PDMOS-transistors of the clock inverters. A MOSCAP decoupling capacitor is added between the 8.7V and 12V supply lines. It smoothens the voltage ripple between both lines. Finally a diode stack is placed between the 8.7V and 12V supply lines to compensate the current through the resistor voltage divider which discharges the 8.7V supply line when the drivers do not transfer any charge.

To ensure that upper and lower control signals are in-phase, the upper control signals are generated by means of the bottom control signals. A bottom clock signal is boosted up by means of a small capacitor C (426fF) (shown in Fig. 5 a)). Moving the capacitor up and down will toggle the state of the latch. The latch ensures that the top node of the capacitor is at all times between 8.7V and 12V. A series of power trains amplify these clock signals and drive the clock inverters. The rise and fall time of the inverters from the inverter chain are identical. Because of this the power consumption and the clock skew is minimal [11]. A non-overlapping clocking scheme was foreseen to eliminate the short circuit currents in the charge pumps as well as in the drivers. An overview of the entire converter system is shown in Fig. 5 c).

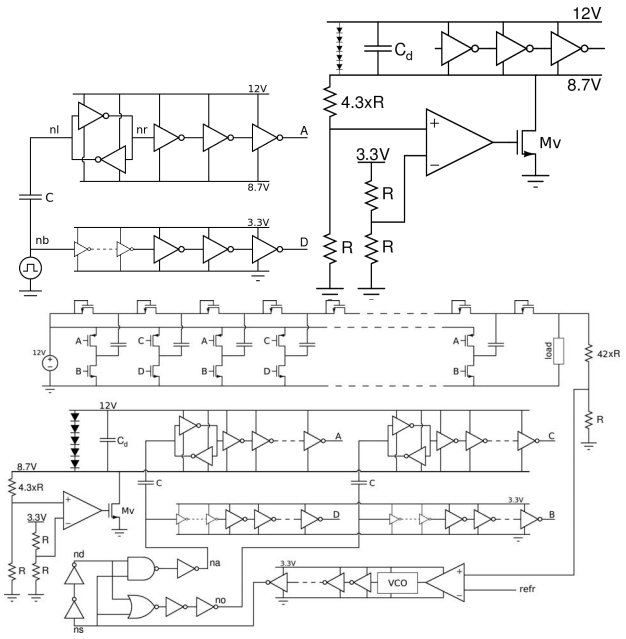

Fig. 5. a) Driver circuit with capacitor and latch b) Linear voltage regulator c)Total System

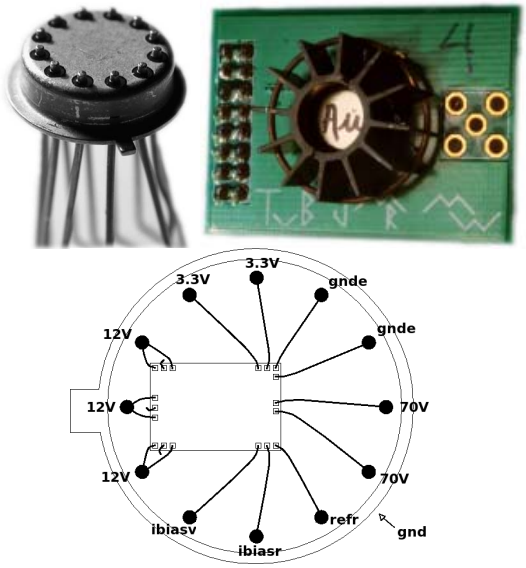

Fig. 6. a)The 12-pin TO-5 package without cover b)The packaged chip with heatsink c)Positioning and bonding of the chip in the package

VI. Packaging

The chip is packaged in a 12 pin Transistor Outline (TO-5) package Fig. 6 a). Due to high power conversion and the efficiency between 10% and 20% under full load about 1800mW must be dissipated internally. This type of package was chosen based on its favorable thermal conduction capability and the possibility to fix a proper heat sink easily. Fig. 6 b) shows the packaged chip with a heatsink Fisher KK510 heatsink(38C/W) mounted on top.

Position of the chip (shown in Fig. 5) c) in the package is crucial since it influences the length of the bondwire at each terminal. Therefore it was positioned as such that bondwire length was smallest for the most crucial terminals. Especially bonding of the ground and 12V power connection was taken special care of. By positioning the chip as shown in Fig. 6 c), the power connections are kept sufficiently short and bondwire inductance is kept minimal, so that the on-chip decoupling capacitance is minimized as well. By using multiple bonding wires the bond wire resistance as well as the bond wire inductance is reduced further.

VII. Measurements

The DC/DC-converter is measured under current-load and biased for an output voltage of 60-70-80V. To the authors knowledge the peak output power of 320mW, outnumbers any

known integrated capacitive converters output power capability. The efficiency is measured over a power range between 20mW to 320mW. For this range a maximum efficiency of 85% per stage is attained. The measured overall efficiency is plotted in Fig. 7. Over the whole output voltage range the overall efficiency remains above 17% for a 50mW to 250mW output power range. The maximum efficiency 21% is attained for a 80V output voltage and a 150mW generated output power. Fig. 8 a) shows the output voltage ripple under maximum load. The maximum ripple is measured to be 750mV which is less than 1.1% of the output voltage. The load regulation was measured for a 50kHz load variation between 35mW and 315mW output power (shown in Fig 8 b)). An output voltage variation of 2.7V at an output voltage of 70V was measured, which is less than 4%. Table I gives a comparison between the designed converter and several converters known in literature. An output power of 320mW is achieved with a voltage conversion ratio of 5.83. The designed converter (Chip micro-photograph shown in Fig 8 c)) proves that a whole new era of integrated converters is possible.

TABLE I

COMPARISON OF THE DESIGNED CONVERTER AND KNOWN CONVERTERS IN LITERATURE

	V_{in} [V]	V_{out} [V]	f [MHz]	P_{out} [mW]	Type
This	12	70	35.4	320	Capacitive
[8]	1.8	8.4	60	1.4	Capacitive
[12]	1.8	7.5	100	2.25	Capacitive
[9]	5	20	10	0.5	Capacitive
[9]	5	50	10	2.5	Capacitive
[13]	5	20	10	4	Capacitive
[7]	3	8.4	100	3.5	Capacitive
[8]	1	7.5	75	1.1	Capacitive
[14]	1.8	6.0	60	3.6	Inductive
[15]	1.8	3.3	100	150	Inductive

Table II gives a comparison between the efficiency of the designed converter and several multistage capacitive converters known in literature. In [8] [9] [13] the efficiency was not published so only [12] and [7] can be compared with the proposed converter. From Table II it is clear that this integrated converter is not only superior in output power but also in its efficiency per stage.

TABLE II

COMPARISON OF THE EFFICIENCY OF KNOWN CAPACITIVE HIGH VOLTAGE CONVERTERS IN LITERATURE

	$stages$	$efficiency_{overall}(\%)$	$efficiency_{perstage}(\%)$
This	10	21	85.5
[12]	3	55	82
[7]	4	39.5	79.3

VIII. CONCLUSION

A 10 stage integrated capacitive DC/DC-converter converts 12V to 70V at a maximum efficiency of 85.5% per stage and an overall efficiency of 21%. The control system keeps the output voltage constant at varying loads and supply voltages. The system has been designed in 0.35μm high voltage technology. A maximum output power of 320mW is achieved.

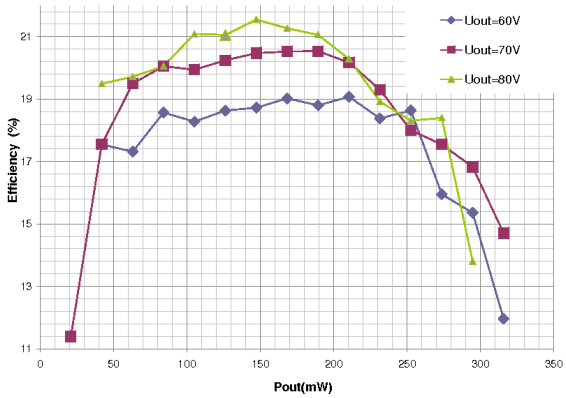

Fig. 7. Efficiency plot over the measured output power range

Fig. 8. a) Detail of the measured Ripple b) Output voltage variation during a load regulation measurement c) Chip

The maximum switching frequency is 35.4MHz. The chip measures 2mm x 3mm.

IX. ACKNOWLEDGMENT

The authors thank the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT-Vlaanderen) and ON Semiconductor for providing the technology.

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