A Design Methodology for Matching Improvement in Bandgap References

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Abstract

Errors caused by tolerance variations and mismatches among components severely degrade the performance of integrated circuits. These random effects in process parameters significantly impact manufacture costs by decreasing yield and so by including extra-circuits for adjustment. In this paper we propose a design methodology based on the Pelgrom's MOS transistor-mismatching model devices. Our main objective is to calculate the size of each component considering their relation between area and mismatching. Therefore, in order to validate our proposal methodology, we used as a design target a bandgap reference circuit fabricated in 0.35µm CMOS technology. Its temperature coefficient attains an average value of 40ppm/ºC and an average output voltage of 1,20714V. It also includes a straightforward 4-bits trim circuit to achieve more process independence variation. As a result of our methodology, the considerable area of 400x350µm² was occupied due to our matching design requirements.

1. Introduction

Usefulness and performance in integrated circuits design relies on good device matching. The accurate characterization of mismatch parameters and their inclusion as part of simulator model libraries are extremely important to ensure circuit yield during the design phase [1,2]. Transistor mismatch model is one of the main parameters determining the accuracy–speed–power tradeoff in analog circuit design [3]. Either for digital CMOS, it is considered to be one of the barriers to the device continuous downscaling dimensions [4]. Mismatch modeling is therefore of crucial importance in order to be able to characterize a technology. To keep a link between model and technology parameters, the model has to be physically/measured based [5,6]. Particularly in analog MOS integrated circuits, the design depends heavily upon matching accuracy [7].

Commonly the key elements are bipolar and/or MOS transistors, but in some applications matching accuracy of resistors and/or capacitors are also critical. Notwithstanding handling statistical design aspects is not often a standardized step in the design flow [8-9]. For that reason, in this work we focused our design in order to afford the maximum matching among circuit components. For this, we contribute to improve the theory developed in [5] and link that as a design variable to reach the best size of each circuit component. Therefore, in order to validate our theory we use as a design target a bandgap reference circuit, which is a renowned architecture characterized by its well-defined accuracy requirement. Implemented in AMS0.35µm CMOS technology, the circuit also includes a straightforward 4-bits trim to achieve more process independence variation. Hence, the development of the design methodology is described in section 2. The design of a Bandgap Reference is demonstrated in section 3. Section 4 describes the inclusion of Extra-Circuits like trim circuit. In section 5 some simulations and measurement results are analyzed. Finally, in section 6 we have the conclusion.

2. Design Towards Matching

Mismatch modeling include two terms [5]: 1) a distance dependent term (global mismatch) and 2) a size dependent term (local mismatch). The distance dependent term can be compensated through layout techniques (such as common centroids and dummy structures). However, only the size dependent term is discussed in this work and it will be include as a design step of a Bandgap Reference circuit. Concerns like finding the optimum area allocated for minimum mismatching [10], accurate modeling [5] and the magnitude of each error among components [1], were considered to obtain the resistor and transistor sizes.

Thus, for resistor size calculation the following criteria were considered:

2.1 Resistors

The following Pelgrom model [5] that describes the standard deviation between two rectangular devices depending on the area is characterized by

$$\sigma_R = \sigma\left(\frac{\Delta R}{R}\right) = \frac{K_R}{\sqrt{W \cdot L}} \quad (1)$$

supposing $\sigma_R \leq 0.1\%$ as a start point [1] and K_R=11% for polysilicon in the AMS 0.35µm CMOS technology. Consequently, the value of W.L is 12100 µm^2. Since is required R=5KΩ then the resistor made by polysilicon (50Ω/□) occupies the area of W=1000µm and L=10µm.

Furthermore, for MOS Transistor size calculation the following criteria were considered

2.2 MOS Transistors

Threshold voltage V_T and current factor β (β=C_{OX}.µ.W/L) variotions are the dominant sources of mismatch among MOS transistors [5]. Their random differences have a normal distribution and their standard deviation depends on the device area W.L and device spacing distance. For our purpose, only area effects are considered. The standard deviation of V_T and β differences are defined respectively as

$$\sigma(\Delta V_T) = \frac{A_{V_T}}{\sqrt{W \cdot L}} \quad (2)$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{W \cdot L}} \quad (3)$$

where A_{VT} and A_β are constants technology-dependent. Considering the standard deviation of the drain-source current model valid in all regions of operations [7], the following expression is easily obtained as,

$$\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \left(\frac{\Delta\beta}{\beta}\right) + \frac{gm}{I_{DS}} \cdot (\Delta V_T) \quad (4)$$

Thus combining (2) and (3) in (4), it seems to be coherent to assume that the following expression must represent the standard deviation of the mismatched drain-source current in term of dimensions (W & L), technology parameters (A_β & A_{VT}) and bias (gm/I_{DS}).

$$\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \left(\frac{A_\beta}{\sqrt{W \cdot L}}\right) + \frac{gm}{I_{DS}} \cdot \left(\frac{A_{V_T}}{\sqrt{W \cdot L}}\right) \quad (5)$$

Concerning the transistor biased point we may considered at weak inversion $gm/I_{DS}=1/(n.U_T)$. Given n the slope factor parameter and U_T the thermal voltage (26mV at 300K). However in strong inversion then $gm/I_{DS}=2/(V_{GS}-V_T)$.

3. Bandgap Reference Design

The Bandgap Reference Circuit is the most stable and popular reference voltage generator. It is a circuit required in many analog and mixed-signal circuits, such as ADC, DAC, DRAM and flash memories, and so forth. It is commonly designed to be insensitive to temperature, supply voltage and process variations. Much work has been done to improve performance concerning temperature and supply voltage variations [11-15]. However, the development of high-performance CMOS bandgap reference has been hindered by several limiting factors attributable to process variations [1,9]. Even though the stress in their design is mostly on temperature compensation, process variations have the biggest impact on the absolute value of the reference voltage, and postprocessing trim techniques are used for their compensation.

In our case for clarity and convenience the analysis is performed within the context of the bandgap's basic building block. The schematic is shown in figure 1,

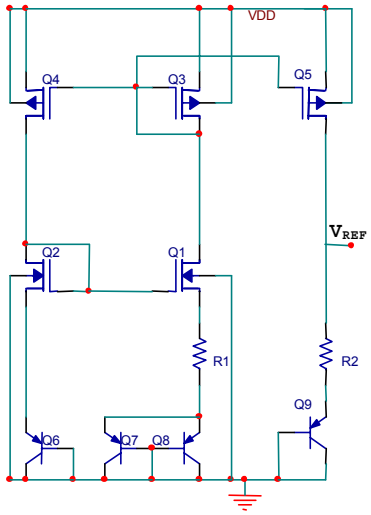

Figure 1. Architecture of the CMOS Bandgap Reference.

The proportional to absolute temperature current (I_{PTAT}) is produced by differences between the emitter-base voltage in the transistors Q_6 and the pair Q_7/Q_8 over R_1. However, considering the current mirror formed by Q_3/Q_5 the output voltage may be written as

$$\begin{aligned} V_{REF} &= R_2 \cdot I_{PTAT_5} + V_{EB9} \\ &= R_2\left[\frac{(W/L)_5 \cdot k}{(W/L)_3 q \cdot R_1} \cdot \ln(N)\right] \cdot T + V_{EB9} \end{aligned} \quad (6)$$

assuming R_1=R_2 over all the temperature range, V_{EB09}=$-1.826mV$, N=2 and doing the derivative as a function of temperature then

$$\frac{\partial V_{REF}}{\partial T} = 0 = R_2\left[\frac{(W/L)_5 \cdot k}{(W/L)_3 q \cdot R_1} \cdot \ln(N)\right] + \frac{\partial V_{EB09}}{\partial T}$$
$$\Rightarrow K_{REF} = \frac{(W/L)_5}{(W/L)_3} = \frac{-\frac{\partial V_{EB09}}{\partial T}}{\frac{k}{q}\ln(N) V/^{o}C} \cong 30 \quad (7)$$

in this case, K_{REF} is the number of transistors is parallel with Q_5 to produce the stable reference voltage (V_{REF}).

Therefore, using the formula obtained in section 2.2 and considering our transistors biased in strong inversion then $gm/I_{DS}=2/(V_{GS}-V_T)$. Thus, the following mismatch model equation may be written as

$$\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \left(\frac{A_\beta}{\sqrt{W \cdot L}}\right) + \frac{2}{(V_{GS} - V_T)} \cdot \left(\frac{A_{V_T}}{\sqrt{W \cdot L}}\right) \quad (8)$$

hence the following formula may infer about the calculus of each transistor dimension

$$\sqrt{W \cdot L} = \frac{2 \cdot A_{VT} + A_\beta (V_{GS} - V_T)}{\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) \cdot (V_{GS} - V_T)} = \frac{K_{MOS}}{\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right) \cdot (V_{GS} - V_T)} \quad (9)$$

where $2 \cdot A_{VT} + A_\beta (V_{GS} - V_T) = K_{MOS}$ is a constant value dependent on technology and the bias point. In our case K_{PMOS}= $3.15\%.\mu m.V$ and K_{NMOS}=$2.84\%.\mu m.V$. Thus, drawing squared transistors and desiring an average value for the mismatched drain-source current less than 0.1% [1], then the dimensions of each N_{MOS} and P_{MOS} transistor is respectively:

$$W_{NMOS} = L_{NMOS} \cong \frac{2.84\%.\mu m.V}{0.1\% \cdot 0.368V} = 77.2\mu m \quad (10)$$

$$W_{PMOS} = L_{PMOS} \cong \frac{3.15\%.\mu m.V}{0.1\% \cdot 0.460V} = 68.5\mu m \quad (11)$$

By this manner the transistors were built with sizes of W_{NMOS}=L_{NMOS}=80µm and W_{PMOS}=L_{PMOS}=70µm. Table I summarizes the final dimensions of each component.

TABLE I. FINAL COMPONENTS DIMENSIONS

Component	Value
Q1, Q2	*W=80µm, L=80µm*
Q3, Q4	*W=70µm, L=70µm*
Q6…Q9	*32.6µm² (Vertical BJT)*
Q5, Q10…Q35	*W=20µm, L=20µm*
Q36	*W=10µm, L=20µm*
Q37	*W=5µm, L=20µm*
Q38	*W=1µm, L=80µm*
Q39, Q40	*W=10µm, L=1µm*
R1	*W=10µm, L=1000µm-5KΩ*
R2	*W=10µm, L=1000µm-5KΩ*

4. Extra-circuits

4.1 Trim circuit

Trim regulation is a well known strategy to set the temperature coefficient to a desired value [16,17]. In our case, is made by adjusting the K_{REF} factor. Since transistors and resistors were calculated to reach our matching expectations at 0.1%, there are some others sources of errors like: V_{BE} spread, Early voltage due to bipolar transistors, package shift, and packages stress [1]. For convenience these errors will not be analyzed here but will be taken into account by increasing the entire value of the variability of V_{REF} i.e., the target value will be ΔV_{REF}=0.5%. We also assume that the bandgap reference in the worst case may expect an initial value of ΔV_{REF}=5%. Based on [16] the design of the trim range is defined by the fundamental accuracy desired and by the expected initial value of an untrimmed reference. In other words, the numbers of trim bits is determined by the least significant bit (LSB) and by the value of the full-scale range trim expected. Thus, the following rule must be respected

$$\#Bits \geq \frac{\ln\left(\frac{V_{FS}}{V_{LSB}} + 1\right)}{\ln(2)} \quad (12)$$

where V_{FS} is the full-scale voltage and V_{LSB} is the LSB voltage. Since ideally V_{REF}=1.2V then

$$V_{FS} = 5\% \cdot 1.2 = 60mV \quad (13)$$

$$V_{LSB} = 0.5\% \cdot 1.2 = 6mV \quad (14)$$

Accordingly formula (12) #Bits=3.4594, in a such wise the trim circuit is made by 4 bits. This feature was implemented through 4 MOS transistors with the terminals of gate (G) and source (S) connected in parallel to Q_5 and their drain (D) terminal connected to four additional Pads. Assuming a binarily weighted algorithm, their sizes were in steps by $2W_5$, W_5, $W_5/2$ and $W_5/4$. These transistors are Q_{33}, Q_{34}, Q_{35}, Q_{36}, Q_{37}. Consequently, the current through R2 can be adjusted in up to 16 levels, proportionally to the current that flows through R1 by connecting or not these 4 Pads to the V_{REF} node.

4.2 Start-up circuit

To prevent this circuit from stabilizing at an inadequate bias point, our strategy was the imclusion of an auxiliary circuit. It will supply the gate terminals of Q3 and Q4 transistors, forcing them to enter in conduction. The start-up circuit is designed in order to operate only at the starting moment, being deactivated when entering in normal operation. This circuit is formed by the transistors

Q38, Q39 and Q40. Q38 works like an active load for Q40. Q39 supplies the polarization for the gate of transistors Q3/Q4 during the startup process. The Bandgap reference including a start-up circuit is depicted in the figure 2,

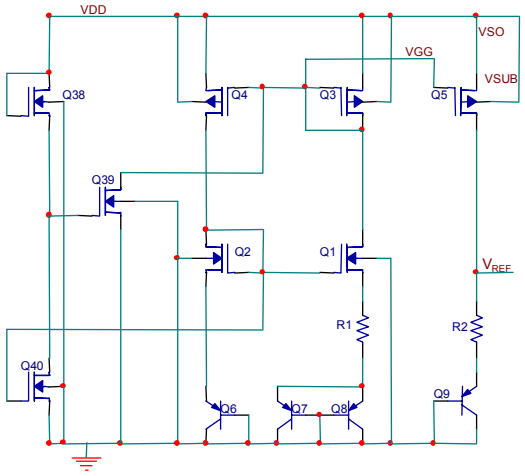

Figure 2. Schematic with start-up circuit

Additionally all the parallel transistors with Q_5 and the trim circuit are shown in the figure 3,

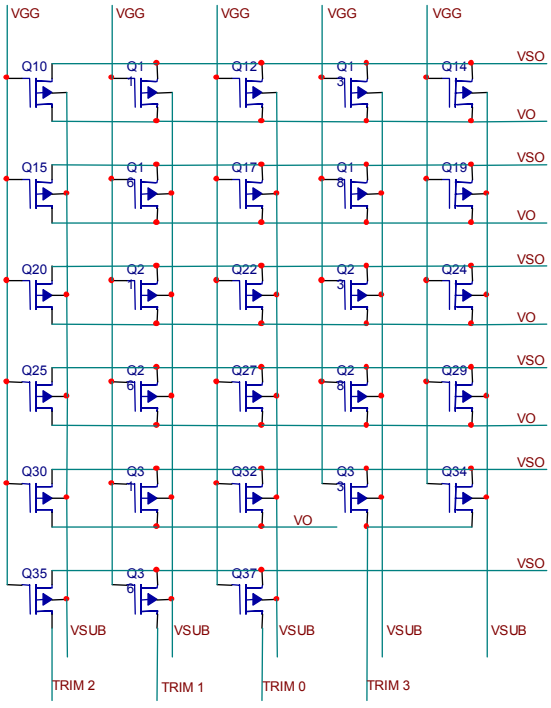

Figure 3. Transistors in parallel with Q_5 and the Trim circuit.

5. Simulations and Measurement Results

We fabricated a test chip with analog circuits and test vehicles in AMS0.35µm CMOS technology. The chip is composed by analog blocks such as: OTAs, Comparators, Gm-C Filters, TAT and T-Shape Transistors and a Bandgap Reference. Figure 4 shows the chip micrograph. All modules fitted to 4.55 mm^2 of total area. However, the Bandgap Reference Circuit fits an area of 350x400µm ($0.14mm^2$).

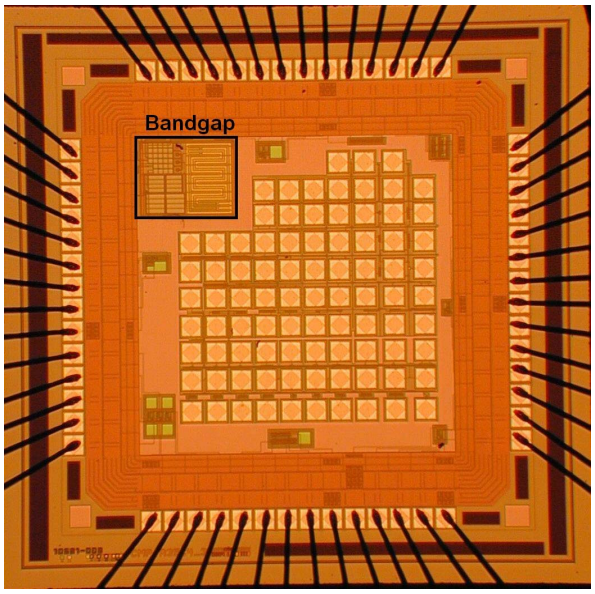

Figure 4. Analog test chip micrograph.

5.1 Temperature Variation

The curves in figure 5 present the simulated output voltage V_{REF} as a function of the temperature for all values of the trim circuit. We are able to adjust our stable voltage reference in 16 discrete levels.

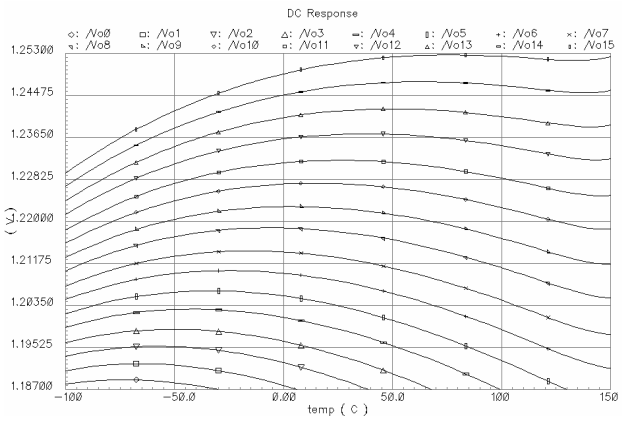

Figure 5. all possible combinations of the trim circuit

Figure 6 shows the variation of the zero-drift point of each of the 16 bandgap curves (Fig. 5). The circuit works in a wide range of temperatures from -75ºC to 75ºC. For instance, we are able to set up an application specific bandgap circuit according their working temperature.

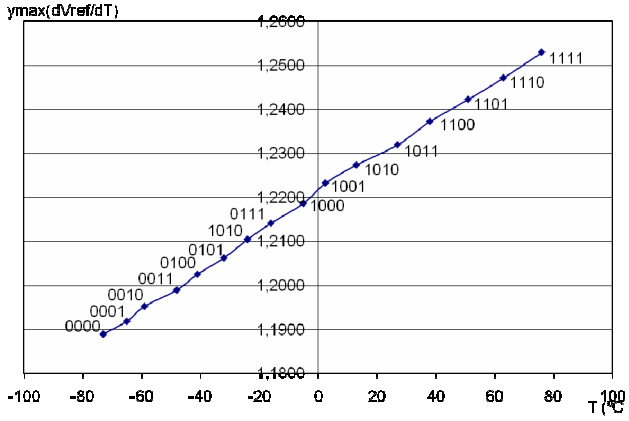

Figure 6. V_{REF}/trim range versus Temperature

Finally, in order to ensure the values found by our design methodology in figure 7 is shown the Monte Carlo analyses. We have used Monte Carlo Resistor and MOS/Bipolar Transistor models. This simulation was done only for one trim configuration (trim=1001), because the value of its zero-drift point is basically at room temperature.

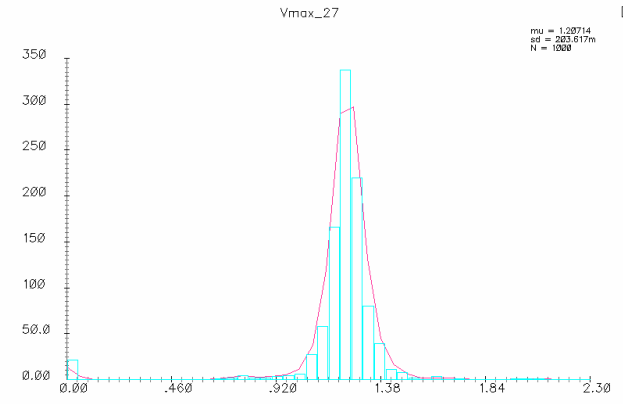

Figure 7. Monte Carlo Histogram analysis

In order to resume the estimated, simulated, and measured values we put together our results in the next tables II and III:

TABLE II. SUMMARY OF MEASURED AND SIMULATED RESULTS

	Simulated	Measured
V_{REF} (T=27ºC) trim=0000	1.1890V	1.1732V
TC (trim=0000)	40ppm/ºC	47ppm/ºC
Supply Dependence	1%/ºC	1%/ºC
I_{DD} (T=27ºC@V_{DD}=3.3V)	350µA	420µA
Start-up time	2us	6.35us

TABLE III. SUMMARY OF ESTIMATED, SIMULATED AND MEASURED RESULTS FOR STATISTICAL REQUIREMENTS

	Estimated	Simulated	Measured
MonteCarlo mean	1,22300V	1,20714V	-
MonteCarlo σ	60mV (5%)	203,617mV (17%)	-
V_{FS}	60mV	64mV	61mV
V_{LSB}	6mV	3,5mV	4,3mV

6. Conclusion

A new methodology concerning the mismatching among components was analyzed. It was developed an analytical expression based on the Pelgrom MOS transistor-mismatching model and inserted as a design variable in the design of a Bandgap Reference. The circuit was implemented in AMS 0.35µm CMOS technology. To strengthen the maximum matching among their components it also includes a trim circuit. The final circuit has the large area of 350x400µm (0.14mm^2) due to our matching requirements. Observing the results, the values concerning mismatch modeling, Monte Carlo analysis and measured results are a little bit disjointed. This might be happened due to some weak point in our mismatch-model. On account of our large circuit area, some characteristics like distance consideration could be the reason of this difference. However, the statistical model (Monte Carlo model) provided by the foundry (AMS) could be also a weak point considered. Therefore, the trim circuit matches with all our expectations.

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7. References

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