A 1-V 140-μW 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS

Libin Yao, *Student Member, IEEE*, Michiel S. J. Steyaert, *Fellow, IEEE*, and Willy Sansen, *Fellow, IEEE*

***Abstract*—A single-loop third-order switched-capacitor Σ-Δ modulator in 90-nm standard digital CMOS technology is presented. The design is intended to minimize the power consumption in a low-voltage environment. A load-compensated OTA with rail-to-rail output swing and gain enhancement is chosen in this design, which provides higher power efficiency than the two-stage OTA. To lower the power consumption further, class-AB operation is also adapted in the OTA design. Due to the relatively low threshold voltage of the advanced technology, no clock bootstrapping circuits are needed to drive the switches and the power consumption of the digital circuits is reduced. All the capacitors are implemented using multilayer metal-wall structure, which can provide high-density capacitance. The modulator achieves 88-dB dynamic range in 20-kHz signal bandwidth with an oversampling ratio of 100. The power consumption is 140 μW under 1-V supply voltage and the chip core size is 0.18 mm^2.**

***Index Terms*—Analog–digital conversion, Sigma-Delta modulation, switched-capacitor circuits, low voltage, low power, operational amplifiers.**

I. Introduction

In RECENT years, portable electronics, such as personal wireless communication devices, digital cameras, personal audio devices, etc., find booming markets. Powered by batteries, their supply voltage is often limited, and the battery lifetime is of great importance for these devices. All these factors address the requirements of low-voltage low-power system building blocks. At the same time, mainly driven by digital circuits, the feature size of transistors is continuously being scaled down. The working voltage is decreased as a consequence of the size shrinking to avoid transistors breaking down, forcing the design to work at lower supply voltage. These factors make low-voltage low-power circuits a hot topic recently. However, the decreased supply voltage restricts the signal swing in circuits and brings some difficulties for analog designs [1]. In low-voltage environments, the transistor characteristics degrade and some circuit techniques can no longer be used, rendering the low-voltage design different from the traditional circuit design technique.

As an important building block, analog-to-digital converters (ADCs) are widely used in various systems. The movement of digital circuits into ultra-deep-submicron technology presents strong demands to low-voltage low-power ADCs. Among different ADC topologies, Σ-Δ ADCs efficiently trade speed for accuracy, providing an effective way to implement high-resolution ADCs without stringent matching requirements or calibration in low-voltage environment. By means of oversampling and noise shaping, the Σ-Δ ADC transfers most of the signal processing tasks to the digital domain where the power consumption can be drastically reduced by the technology scaling down and supply voltage decreasing. Meanwhile, the use of an intrinsically linear single-bit quantizer exempts the stringent matching requirement, which is power-hungry. For high-resolution ADCs, the Σ-Δ ADC is more power-effective and robust compared to other architectures.

While moving into ultra-deep-submicron CMOS technologies, for low-voltage low-power designs, certain advantages can be gained. On the other hand, some disadvantages are also foreseen. Limited by the transistor breakdown voltage, the rated supply voltage is low in ultra-deep-submicron CMOS technologies. As a result, the threshold voltage of the transistor is also low, which is advantageous to implement low-voltage applications. No specially designed low-voltage circuits are needed, which simplifies the circuits and lowers the power consumption. Many low-power low-voltage Σ-Δ ADCs reported to date are implemented in submicron CMOS technologies [2], [3]. The common point of these works is that they work on a reduced supply voltage that is lower than their rated supply voltage. To sufficiently drive the switches, clock bootstrapped driving circuits are employed. In this case, some internal node voltages might be higher than the supply voltage. Damaging the transistor or having a reliability problem are potential risks. Low-V_T technologies can also be used. However, this needs extra processing steps and is expensive. Some works [4] were implemented with the switched-opamp technique [5], which solves the driving problem of the sampling switches in the succeeding stage, but the first sampling switch still cannot be driven sufficiently. With ultra-deep-submicron technologies, the threshold voltage is reduced as the supply voltage is decreased. This makes the driving of the switches possible without bootstrapping circuits. Hence, ultra-deep-submicron technologies help to reduce the power consumption further in a low-voltage environment. For the digital part of the converter, the shorter the transistor length, the less power that is consumed. That is the driving force of the technology scaling down. Generally speaking, in terms of low-power low-voltage, it is advantageous indeed to move into ultra-deep-submicron technologies.

It is meaningful to explore the possibilities of implementing high-performance Σ-Δ modulators in a standard digital process in ultra-deep-submicron technologies. Presented in this paper is a single-loop third-order switched-capacitor (SC) Σ-Δ modulator implemented in a standard digital 90-nm CMOS

Manuscript received March 10, 2004; revised June 16, 2004.

The authors are with the Katholieke Universiteit Leuven, Department of Elektrotechniek, ESAT-MICAS, B-3001 Leuven-Heverlee, Belgium (e-mail: Libin.Yao@esat.kuleuven.ac.be).

Digital Object Identifier 10.1109/JSSC.2004.835825

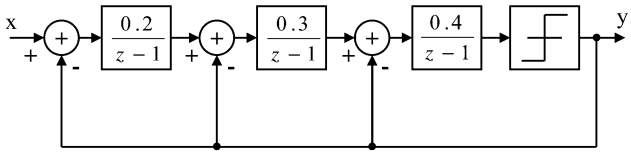

Fig. 1. Single-loop third-order topology.

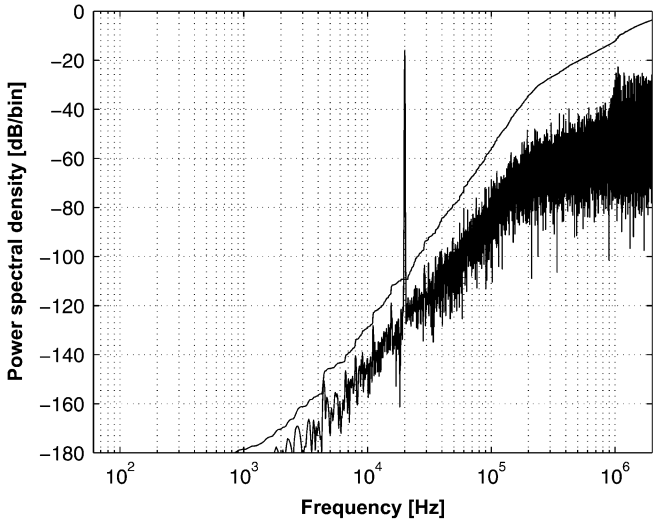

Fig. 2. Output spectrum of the proposed topology with a 20-kHz input signal.

technology. The modulator achieves 88-dB dynamic range in 20-kHz signal bandwidth, while consuming 140 μW under 1-V supply voltage.

II. Low-Voltage Low-Power Design Considerations

A. Modulator Topology Selection

Single-loop topology is preferable for low-voltage low-power designs since it is less sensitive to circuit nonidealities, e.g., OTA dc gain and switch on-resistance. The Σ-Δ ADC is known for its high tolerance for circuit nonidealities compared to other ADC architectures. However, in a low-voltage environment and ultra-deep-submicron technologies, circuit nonidealities become more severe and their impact on the ADC performance should be reconsidered. A third-order single-loop topology was chosen in this design, shown in Fig. 1. The loop coefficients are set to [0.2 0.3 0.4]. Fig. 2 shows a behavioral simulation result of the modulator. The behavioral simulation was done by setting all of the OTA gains to 40 dB and the oversampling ratio to 100. Compared to loop coefficients in [6], the modulator with these coefficients has the same noise-shaping ability but higher overload level, which is good for expanding the dynamic range in low-voltage environments. More importantly, this topology is quite tolerant to the inaccurate coefficients caused by capacitance mismatches. Fig. 3 shows the output swing of each integrator of the modulator normalized to the reference voltage while feeding a -3-dB input signal. The output swings reach 80% of the reference voltage, which means the reference voltage should be almost the same as the output swing of the integrator. If distortion performance is taken into consideration, then the reference voltage should be even smaller. Fig. 4 shows the obtained SNR versus the OTA gains in the proposed

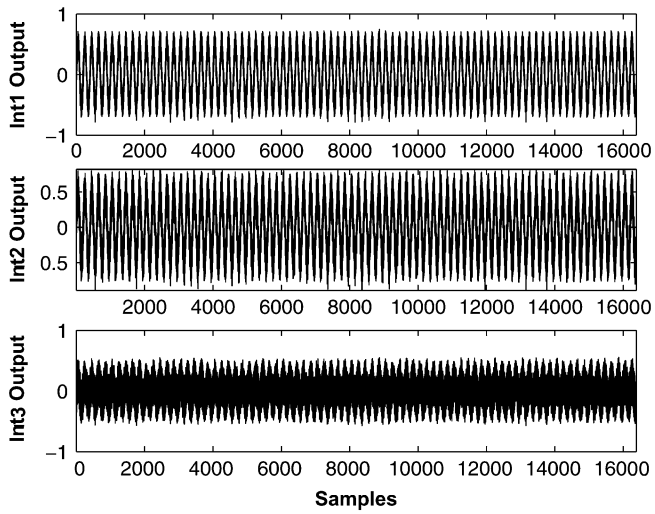

Fig. 3. Normalized output of each integrators of the proposed topology.

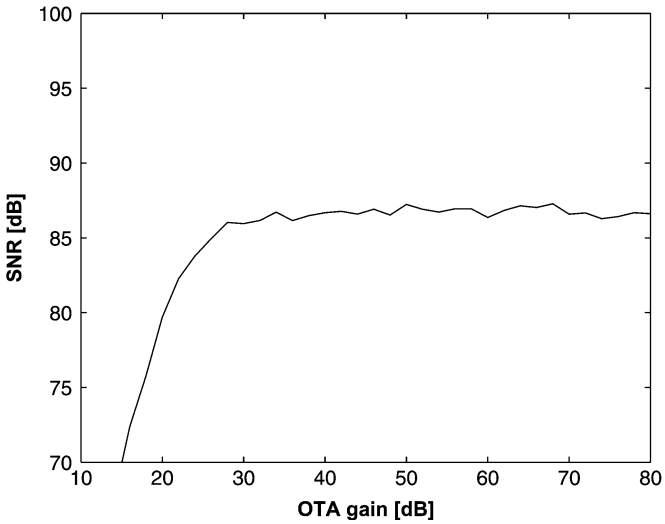

Fig. 4. SNR versus OTA dc gain of the third-order single-loop Σ-Δ modulator.

topology. The minimum gain requirement for OTAs is 30 dB to ensure 85-dB SNR of the modulator. This gain requirement is drawn only from the noise shaping consideration. However, taking the distortion into consideration, the higher the OTA gain, the better the distortion performance that can be achieved.

B. OTA Topology Selection

The OTA composes the main building block of the Σ-Δ modulator. It determines the main power consumption of the modulator. The requirements for the OTA are mainly output swing, dc gain, and gain bandwidth (GBW). The output swing is of great importance in low-voltage designs, as mentioned before. It determines the reference voltage, hence the sampling capacitance and finally the power consumption. For a kT/C noise-dominated modulator, the dynamic range can be written as

$$\mathrm{DR} = \frac{P_{\mathrm{in}_{\max}}}{P_{kT/c}} = \frac{V_{\mathrm{in}_{\max}}^2 \cdot \mathrm{OSR} \cdot C_s}{2kT} \tag{1}$$

where $V_{\mathrm{in}_{\max}}$ is the maximum input amplitude of the modulator and C_S is the sampling capacitance of the first integrator. The

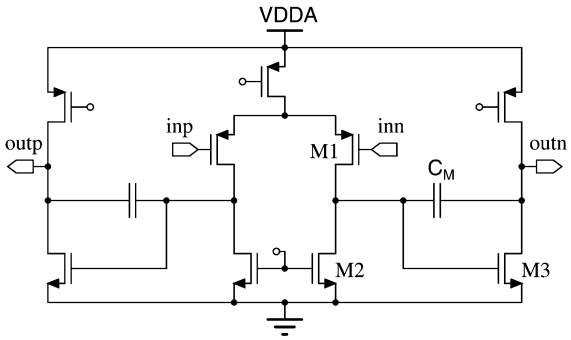

Fig. 5. Miller compensated two-stage OTA.

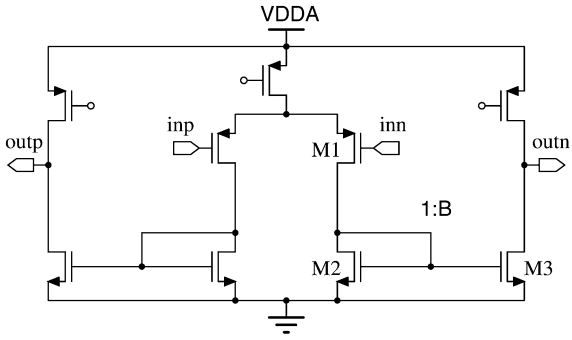

Fig. 6. Current mirror OTA.

maximum input amplitude of the modulator is defined by the output swing of the OTA, as can be seen in Fig. 3. For certain dynamic range, an increase in the output swing can result in a large reduction of sampling capacitance and hence power consumption. The importance of the output swing can be clearly seen here in (1). An OTA topology that can provide the rail-to-rail output swing is absolutely required in low-voltage low-power designs.

In ultra-deep-submicron technology, the intrinsic voltage gain of the transistor is low due to the lower output impedance. The low-voltage environment and output swing constraint prohibit the usage of the cascoding transistors to increase the voltage gain. The natural solution is two-stage or multistage topologies. However, the two-stage OTA is not load compensated. Extra compensation capacitance is needed to ensure the closed-loop stability. For a given GBW and load capacitance C_L, the current drawn by a fully differential class-A Miller OTA, shown in Fig. 5, can be calculated.

$$\frac{g_{m1}}{C_M} = \mathrm{GBW} \cdot 2\pi \tag{2}$$

where C_M is the Miller compensation capacitance. Combining this with the MOSFET equation

$$g_{m1} = \frac{2I_{D1}}{V_{GS1} - V_T} \tag{3}$$

gives

$$I_{D1} = \mathrm{GBW} \cdot \pi \cdot (V_{GS1} - V_T) \cdot C_M. \tag{4}$$

The nondominant pole, which is created by the load capacitance, should be placed beyond the three times of the GBW. This criteria

$$\frac{g_{m3}}{C_M + C_L} = 3 \cdot \mathrm{GBW} \cdot 2\pi \tag{5}$$

gives

$$I_{D3} = \mathrm{GBW} \cdot \pi \cdot (V_{GS3} - V_T) \cdot (3C_M + 3C_L). \tag{6}$$

Assuming all transistors have the same overdrive voltage, the total current of the Miller OTA is then

$$I_{\mathrm{Miller}} = \mathrm{GBW} \cdot \pi \cdot (V_{GS} - V_T) \cdot (8C_M + 6C_L). \tag{7}$$

Similarly, for the same GBW and load capacitance C_L, the current drawn by fully differential class-A single-stage OTAs is calculated as follows. The current drawn by the the single-stage telescopic cascode OTA is

$$I_{tc} = \mathrm{GBW} \cdot \pi \cdot (V_{GS} - V_T) \cdot (2C_L). \tag{8}$$

For the folded cascode OTA, there are two current branches and normally the current of both current branches are the same. The current drawn by the single-stage folded cascode OTA is

$$I_{fc} = \mathrm{GBW} \cdot \pi \cdot (V_{GS} - V_T) \cdot (4C_L). \tag{9}$$

The current drawn by a current mirror OTA with a current ratio of $1:B$, shown in Fig. 6, can be calculated as follows. For the given GBW and C_L, we have

$$\frac{g_{m1} \cdot B}{C_L} = \mathrm{GBW} \cdot 2\pi \tag{10}$$

then

$$I_{D1} = \mathrm{GBW} \cdot \pi \cdot (V_{GS1} - V_T) \cdot \frac{C_L}{B}. \tag{11}$$

And for the current mirror OTA, we have

$$I_{D3} = B \cdot I_{D1}. \tag{12}$$

Then the total current of the current mirror OTA is

$$I_{\mathrm{cm}} = \mathrm{GBW} \cdot \pi \cdot (V_{GS} - V_T) \cdot \left(2C_L + \frac{2C_L}{B}\right). \tag{13}$$

It is clearly seen that for the same condition, the single-stage OTA is more power efficient than the two-stage OTA, since no power is wasted in driving the compensation capacitance in the single-stage OTA.

According to the above discussion, the single-stage OTA is preferred in terms of power-efficiency. In the low-voltage environment, the rail-to-rail output swing for the OTA is highly preferred. The only single-stage topology that can provide rail-to-rail output swing is the current mirror OTA. However, the voltage gain of the current mirror OTA is only in the order of $g_m \cdot r_o$, which is normally around 20–40 dB in ultra-deep-submicron technologies. According to behavioral simulations, the requirement of the OTA dc gain is above 40 dB. To ensure enough gain, a gain enhancement technique is used, which can enhance the gain for 10–20 dB without extra

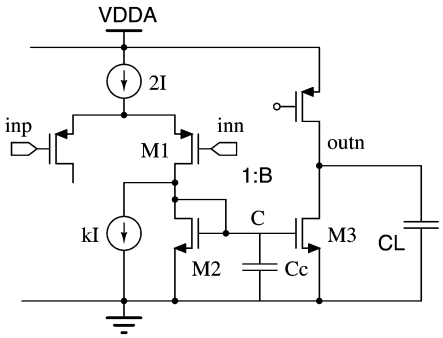

Fig. 7. Current mirror OTA with gain enhancement.

power consumption [7], shown in Fig. 7. The gain of the current mirror OTA can be expressed as

$$A_0 = g_{m1} \cdot B \cdot r_{o3} = \frac{2 \cdot I_{D1}}{(V_{GS1} - V_T)} \frac{B}{\lambda_3 \cdot I_{D3}} \tag{14}$$

where λ is the channel length modulation coefficient and B is the current ratio of the current mirror.

$$I_{D3} = BI_{D1}. \tag{15}$$

Then the gain of the current mirror OTA can be written as

$$A_0 = \frac{2}{(V_{GS1} - V_T)\lambda_3}. \tag{16}$$

When we shunt a portion of currents from the current mirror, for example, $k \cdot I$, shown in Fig. 7, the current mirrored to transistor M3 is reduced to

$$I_{D3} = B(1-k)I_{D1}. \tag{17}$$

Note that the k factor is between 0 and 1. Then, finally, the gain of the OTA is given by

$$A_{en} = \frac{1}{1-k} \frac{2}{(V_{GS1} - V_T)\lambda_3} = \frac{A_0}{1-k}. \tag{18}$$

Equation (18) clearly shows the gain enhancement. It is seen that the gain has been boosted $1/(1-k)$ times. If the k factor is set to near one, then the gain can be enhanced largely.

This technique actually increases the impedance of the internal node C. As a result, the nondominant pole frequency, which is created in this node, is decreased. Doing this may cause degradation of the phase margin of the OTA and cause a stability problem. A closer look reveals relations between the k factor and related parameters.

Suppose the parasitic capacitance of node C is C_C, which is mainly composed of C_{GS2} and C_{GS3}, the gate-source capacitance of transistor M2 and M3. The nondominant pole in node C can be given by

$$P_{nd} = \frac{g_{m2}}{2\pi \cdot C_C} = \frac{2 \cdot (1-k) I_1}{2\pi \cdot C_C (V_{GS2} - V_T)} \tag{19}$$

while the GBW of the OTA can be written as

$$\text{GBW} = \frac{B \cdot g_{m1}}{2\pi \cdot C_L} = \frac{2 \cdot B \cdot I_1}{2\pi \cdot C_L (V_{GS1} - V_T)}. \tag{20}$$

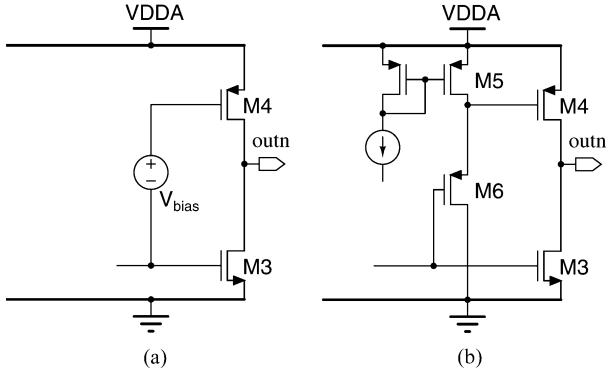

Fig. 8. Class-AB operation of the output stage. (a) Class-AB biasing of the output PMOS transistor. (b) Implementation of the class-AB biasing.

To maintain a reasonably safe phase margin, the nondominant pole has to be placed more than three times of the GBW [8]:

$$\text{GBW} = 3 \cdot P_{nd}. \tag{21}$$

Suppose the overdrive voltages of the transistors are the same, and then the following criteria can be obtained:

$$k \leq 1 - 3B\frac{C_C}{C_L}. \tag{22}$$

Equation (22) shows the maximum gain enhancement that can be achieved. The smaller the C_C/C_L ratio, the more gain enhancement can be achieved. If the OTA drives a large capacitance load, then higher gain can be reached.

The class-AB output stage is considered to be more power efficient than the class-A output stage in SC circuits [9]. Higher slew rate can be obtained from the class-AB output stage with less power consumption. To save power, a class-AB output stage should be adopted in this low-voltage low-power design. Shown in Fig. 8(a), the class-AB operation is made by driving the PMOS transistor M4 by a floating voltage source V_{bias}. This is a very crude class-AB output scheme. The class-AB characteristics are not so good. But here in SC circuits, high slew rate is more important than good class-AB output characteristics. As long as the output settles to the required final value, the settling procedure is not important. This class-AB stage increases the current sourcing ability of the output stage. As a result, the slew rate of the OTA is increased. The floating voltage source V_{bias} is implemented by a level-shifter, shown in Fig. 8(b). The transistors M5 and M6 are identical and have the same drain current. As a result, their gate-source voltages are also identical. By properly biasing M5, a certain V_{bias} can be obtained.

Common-mode feedback is essential to fully differential circuits. A switched-capacitor common-mode feedback (CMFB) is the best solution in terms of power consumption.

C. Transistor Biasing

The biasing of a transistor determines the most important specifications of the transistor. Generally speaking, the transistor reaches the maximum g_m/I_D ratio and low saturation voltage when it operates in the weak inversion region, hence

the maximum power efficiency is achieved. However, the frequency response is degraded and the silicon area occupied is larger when in the weak inversion region. A compromise is made here between speed and power consumption. The specifications of the whole modulator should be taken into consideration in making tradeoffs among speed, power, and area. In this design, the main transistors in the OTAs are biased in the moderate inversion region, e.g., $V_{GS} - V_T \approx 0.1$ V.

D. Scaling of Integrators

One of the most interesting property of Σ-Δ modulators is the noise suppression inside the loop. Utilizing this feature can result in a large amount of power saving. For a single-loop Σ-Δ modulator, the noise suppression in node k can be calculated by [10]

$$F_{\mathrm{sup},k} = \frac{\mathrm{OSR}^{2k+1}}{\pi^{2k}}(2k+1)\prod_{i=0}^{k} a_i^2 \tag{23}$$

where F is the noise suppression factor, OSR is the oversampling ratio, and a_i denotes the loop coefficient of the ith stage. For the proposed topology, the noise suppression of the first, second, and third stage is 41, 63, and 86 dB, respectively. This allows the sampling capacitances of these stages to be scaled down proportionally to corresponding ratios. The only restriction is from the matching requirements. Reducing the sampling capacitance results in a reduction of the load capacitance of the OTA and hence reduces the power consumption.

III. Building Block Circuits

A. Low-Voltage Low-Power OTAS

Depicted in Fig. 9, the OTA used in this design is the current mirror OTA with gain enhancement. This OTA features rail-to-rail output swing and class-AB operation. And most importantly, it is a single-stage structure, which reduces the power consumption effectively.

As mentioned in Section II-B, the k factor determines the gain reached and the phase margin. In this design, the k factor was set to 0.8 and the current mirror ratio was 10. These ratios can be realized by sizing the relevant transistors. Matching issues should be taken into consideration here. Two identical transistors, M5 and M6, function as a voltage level-shifter. The shifted signal drives transistor M4, providing extra current to the load when large signal presents. The biasing voltage Bp defines the class-AB operating point of the output stage. The switched-capacitor CMFB circuit is presented in Fig. 10. The precharged capacitor C_b senses the output common-mode voltage and shift the voltage to proper level in node CMFB. Capacitor C_a periodically recharges the sensing capacitor to provide a constant voltage in the sensing capacitor. The main feature of this CMFB circuit is that it is very power efficient. To ensure that the speed of the common-mode loop is faster than the differential loop in the OTA, the transconductance of transistor M4c should be higher than that of transistor M1 in Fig. 9.

The simulated frequency response of the proposed OTA with a 6-pF load is depicted in Fig. 11. The gain reaches 50 dB and the

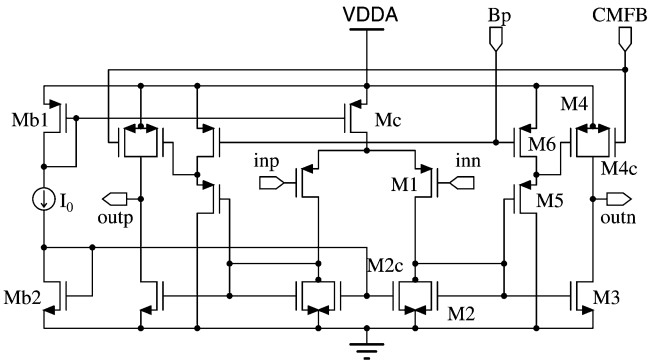

Fig. 9. Schematic of the gain enhanced current mirror OTA.

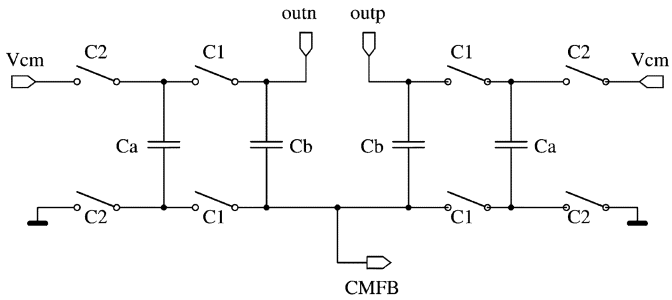

Fig. 10. Schematic of the switched-capacitor CMFB circuit.

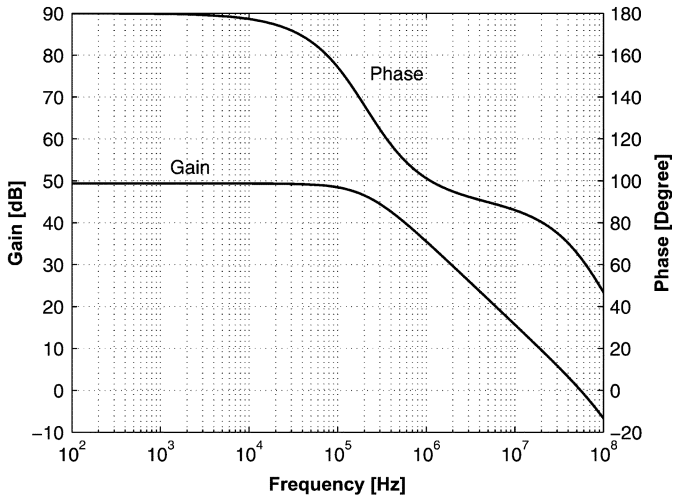

Fig. 11. Simulated OTA frequency response.

GBW is 57 MHz while the phase margin is kept at 57 degrees, with a power consumption of only 80 μW.

B. One-Bit Quantizer Circuits

The one-bit quantizer is realized with a dynamic comparator and an SR latch, shown in Fig. 12 [11]. While clock C1 is low, nodes P and Q are precharged to Vdd. While clock C1 goes high, the precharged parasitic capacitances of nodes P and Q are discharged by transistors M1a and M1b, respectively. The discharge rate of each branch depends on the input voltage. When the voltage of node P or Q drops to the threshold voltage of the latch formed by two cross-coupled inverters, the regeneration process starts. Finally, the voltage of nodes P and Q reaches the rail voltage according to the decision made. The result is

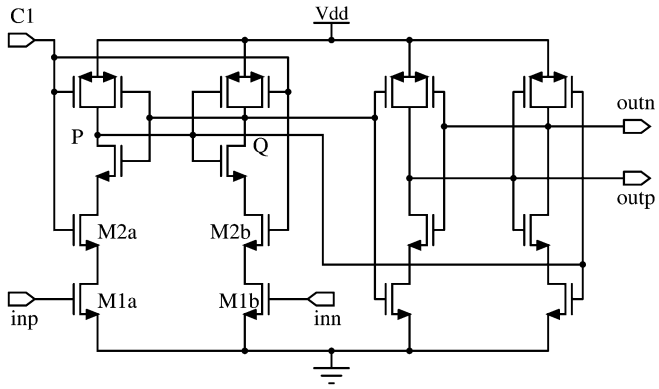

Fig. 12. Schematic of the comparator and latch.

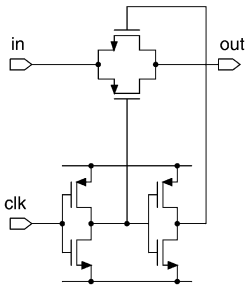

Fig. 13. Switch implementation and the local driver.

then latched by the SR latch following. The whole comparator is a pure dynamic circuit, which is very power efficient. For a single-bit Σ-Δ modulator, the requirement for the quantizer is quite relaxed as nonidealities in this stage can be largely suppressed (see Section II-D). The offset voltage is mainly defined by matching of the input transistors.

C. Switch Driving Circuits

All switches are implemented with transmission gates. As the circuit is working on its rated supply voltage, there is no need to use any clock bootstrapping circuit to boost the driving voltage. Simple inverters are employed to drive switching transistors, shown in Fig. 13. The maximum driving voltage is the supply voltage. So no node inside the whole circuits is exposed to a voltage higher than Vdd or lower than Vss, which is essential for high-reliability operation of the circuit.

D. Other Circuits

The on-chip clock generator is shown in Fig. 14 [6]. The external clock input signal is buffered and then two nonoverlapping clock signals are generated. To avoid the signal dependent charge injection, two delayed clocks, i.e., C1d and C2d, are also generated [12].

IV. Implementation

The ultimate goal of this design is to reduce the power consumption as much as possible. To lower the power consumption, the main consideration is to lower the power consumption in the first integrator. Since in Σ-Δ modulators, the first integrator dominates the overall performance of the modulator and most of the power is consumed here. As mentioned in Section II-D, the

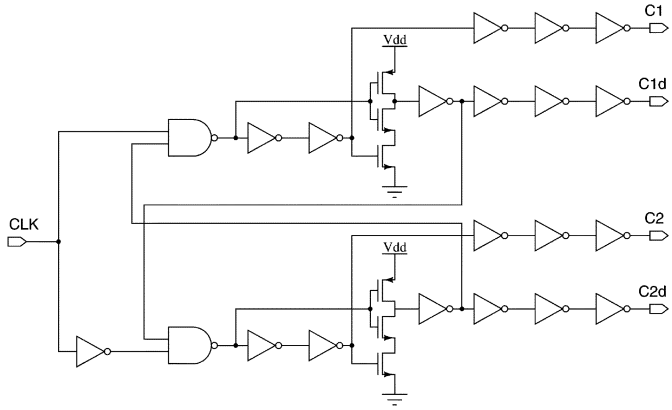

Fig. 14. Schematic of the clock generator.

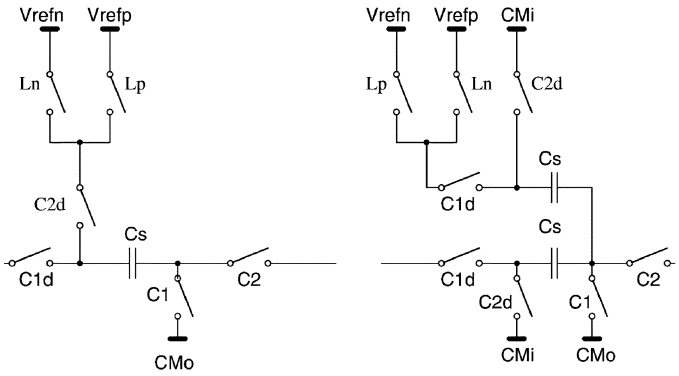

Fig. 15. Different feedback configurations.

second and third integrators can be scaled down to reduce the power consumption. The thermal noise level of the modulator determines the value of the first sampling capacitor, hence the power consumption of the first integrator. The value of the first sampling capacitor is 6 pF, which is sufficient to provide 95-dB peak SNR with 0.6-V reference level. Considering the matching property of the capacitors, both the second and third sampling capacitors are set to 0.4 pF.

Another practical low-power consideration is the feedback scheme of the integrator. Fig. 15 shows two different feedback schemes. The left one directly connects the feedback signal to one terminal of the sampling capacitor during clock period C2, i.e., the integration phase of the integrator. The right one uses two sampling capacitors to sample the input signal and feedback signal, respectively, and then sums these two signals during the integration phase of the integrator. Both of these two schemes have the same function, while the right scheme uses more capacitors and switches. On the left circuit, the sampling capacitor is discharged to either Vrefp or Vrefn during the integration phase, and during the sampling phase the sampling capacitor is charged to the input voltage. During the charge and discharge cycle, the voltage change on the sampling capacitor is from either Vrefp or Vrefn to Vin, which is quite large. Most importantly, the charge current is provided by the preceding OTA. This large signal charge requires a high slew rate of the OTA and consumes power. On the right circuit, the large charge current is provided by the reference voltage. The OTA only charges the sampling capacitor from 0 to the input voltage, which is smaller.

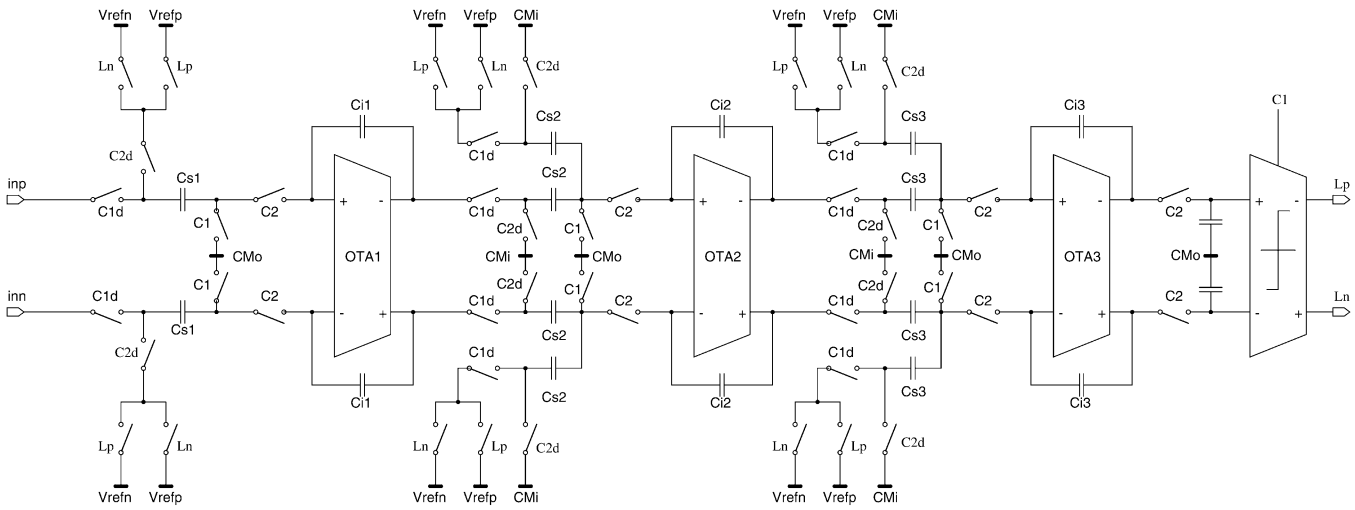

Fig. 16. Schematic of the proposed third-order Σ-Δ modulator.

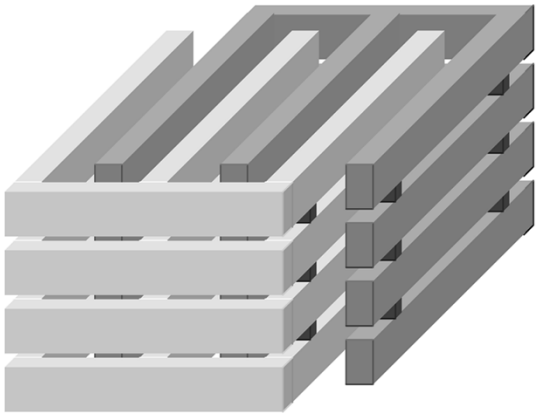

Fig. 17. Proposed metal-wall capacitor structure.

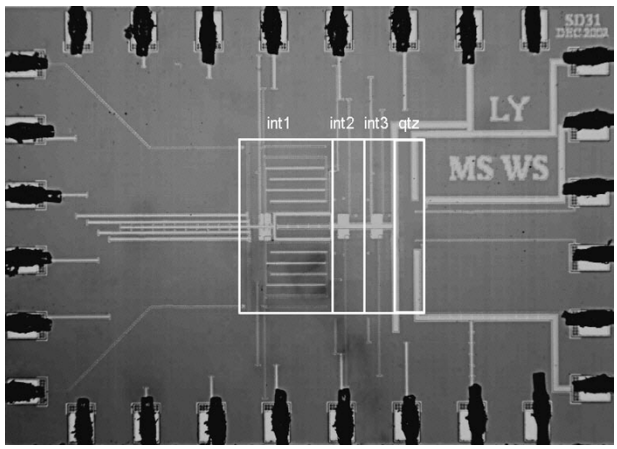

Fig. 18. Chip micrograph.

So the right circuit relaxes the requirement for the preceding OTA and consumes less power.

The common-mode input and output voltages are chosen differently in a low-voltage environment. For signal swing consideration, the output common-mode voltage is set to the middle of the supply voltage, i.e., 0.5 V. However, if the input common-mode voltage is set to the middle of the supply voltage, rail-to-rail input capability is required for the OTA, which cannot be offered by the normal differential input stage. If the input common-mode voltage is set near the supply rail, the normal OTA can be used without the rail-to-rail input requirement. In this design, the common-mode input voltage is set to be 0.2 V. The whole circuit is shown in Fig. 16.

As the process technology used is a standard digital technology, no standard metal–insulator–metal (MIM) capacitor is available. All capacitances are implemented by metal wall structure, shown in Fig. 17 [13]. This structure uses the lateral capacitance instead of the vertical capacitance normally used. In ultra-deep-submicron technologies, the lateral spaces between metal lines in the same layer are smaller than the vertical spaces between metal layers, and the lateral spaces are well controlled. Only one metal layer is occupied for connecting, and the remaining layers can be used to build the capacitor, which means the unit capacitance can be large. Calculation shows the unit capacitance is around 1.7 fF/μm^2 in the technology used, which is higher than that of normal MIM capacitors. However, the matching property is worse than that of MIM capacitor. As the loop coefficients are defined by the capacitance ratios, robust loop coefficients are chosen to be more tolerant to the mismatched capacitance. This kind of capacitance is widely used in this design as decoupling capacitors around the chip.

The chip was fabricated in a standard digital 90-nm CMOS technology. The power supply voltage was 1 V and the reference voltage was 0.6 V. The chip core size was 0.42 mm $\times$ 0.42 mm, as illustrated in Fig. 18. The analog part is separated from the digital part by guard rings. To reach the maximum common-mode rejection ratio, all the analog parts are laid out symmetrically. The surroundings of the unit capacitances are identical to ensure good matching.

V. Measurement Results

To shield the chip from the external interferences, the chip is mounted on a thick-film ceramic substrate and then encapsulated in a copper–beryllium box. Separate power supplies for analog and digital parts and the output buffer are used in the

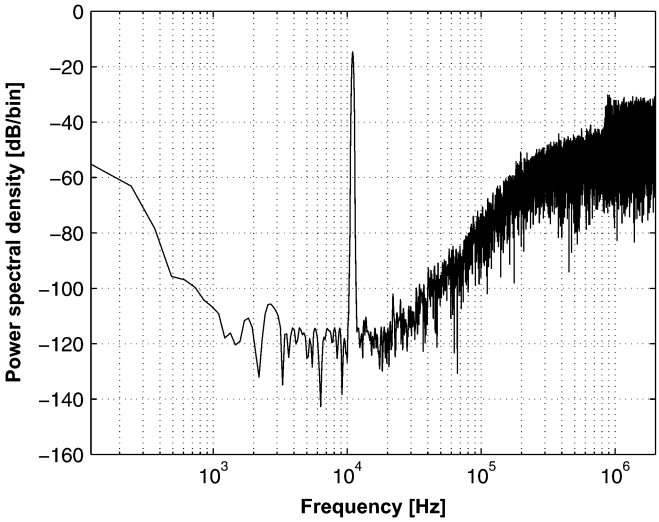

Fig. 19. Measured output spectrum of an 11-kHz sinusoidal input.

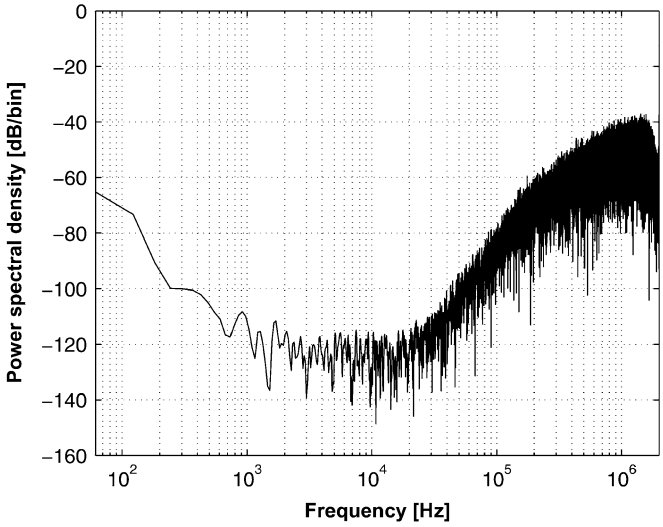

Fig. 20. Measured noise floor of the modulator with inputs short-circuited.

measurement. Local decoupling capacitors are used in power supplies and biasing sources.

Clocked at 4 MHz, the output data of the modulator is captured by a logic analyzer and processed by software. Fig. 19 shows the measured output spectrum of an 11-kHz sinusoid signal. Fig. 20 shows the output spectrum with the inputs short-circuited to ground. Fig. 21 shows the measured SNR and SNDR versus the input signal amplitudes normalized by reference voltage. The peak SNR reaches 85 dB while peak SNDR reaches 81 dB. The dynamic range is 88 dB in a 20-kHz signal bandwidth. The analog core power consumption is 130 μW. The digital power consumption is 10 μW, excluding the power consumption of the output buffer. Table I gives the summary of the performance.

Table II shows the performance comparison of recently published low-voltage low-power Σ-Δ modulators whose supply

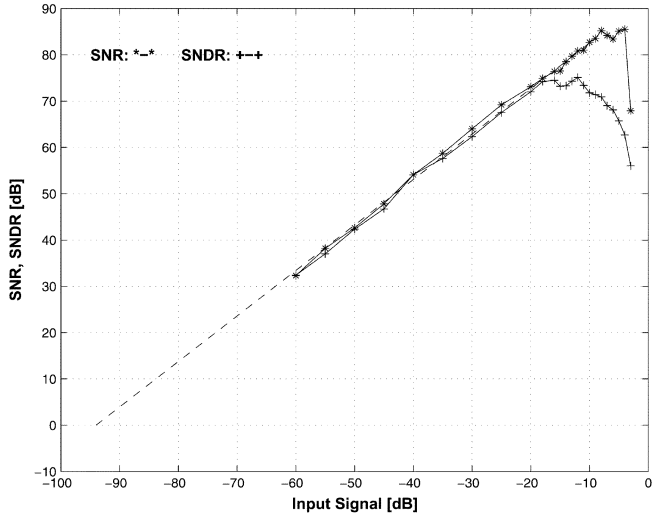

Fig. 21. Measured SNR and SNDR versus input amplitude.

TABLE I
MEASURED PERFORMANCE SUMMARY

Sampling frequency	4	MHz
Signal bandwidth	20	kHz
Over sampling ratio	100	
Supply voltage	1	V
Analog power consumption	130	μW
Digital power consumption	10	μW
Peak SNR	85	dB
Peak SNDR	81	dB
DR	88	dB
Reference voltage	0.6	V
Active die area	0.18	mm^2

voltage is less than 1.5 V. The figure-of-merit (FOM) is defined as [2]

$$\text{FOM} = \frac{4kT \cdot f_B \cdot \text{DR}}{P} \tag{24}$$

where k is Boltzmann's constant; T is the absolute temperature; f_B and P are the signal bandwidth and power consumption of the Σ-Δ ADC, respectively. The FOM is a measure of the power efficiencies of Σ-Δ ADCs, taking signal bandwidth and dynamic range into consideration. However, the supply voltage is not taken into consideration here. To make a fair comparison, all converters should be operating at the same supply voltage. This work achieves the highest FOM among these Σ-Δ ADCs.

There are two reasons for the high power efficiency of this work. One is the specially designed building blocks, especially the OTAs, and the other is the use of the advanced 90-nm technology. Following the low-voltage and low-power design strategies described in Section III, the power consumption of the whole converter has been effectively decreased. For digital parts, the smaller transistor feature size helps to decrease the power consumption. Clocked at 4 MHz, the total digital part of this modulator consumes only 10 μW.

TABLE II
PERFORMANCE COMPARISON

Names and year	Supply Voltage [V]	DR [dB]	Signal Bandwidth [kHz]	Power [μW]	FOM
Keskin,2002 [14]	1.0	80	20	5600	5.9e-6
Sauerbrey,2002 [15]	0.7	75	8	80	52e-6
Dessouky,2001 [3]	1.0	88	25	950	275e-6
Peluso,1998 [4]	0.9	77	16	40	330e-6
This work	1.0	88	20	140	1493e-6

VI. CONCLUSION

A low-voltage low-power switched-capacitor Σ-Δ modulator has been presented. By proper topology selection, the modulator enables the usage of single-stage OTAs with rail-to-rail output swing in ultra-deep-submicron CMOS technology. A gain enhancement technique has been adopted in the OTA to satisfy the distortion requirements of the modulator. A metal-wall structure has been employed to implement the capacitance in this standard digital technology. This capacitance has good matching properties and higher unity capacitance, which helps to reduce chip area. Special measures were taken in the circuit design to reduce power consumption. The design has been verified by measurements. The results have proven the possibility of implementing high-performance Σ-Δ ADCs in ultra-deep-submicron standard digital CMOS technologies. Compared to other CMOS technologies, ultra-deep-submicron CMOS technologies (e.g., 90-nm technology) have advantages in the implementation of low-power low-voltage Σ-Δ modulators.

ACKNOWLEDGMENT

The authors would like to thank D. Draxelmayr and Infineon Technologies for technical support and processing of the circuit.

REFERENCES

[1] W. Sansen, M. Steyaert, V. Peluso, and E. Peeters, "Toward sub-IV analog integrated circuits in submicron standard CMOS technologies," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1998, pp. 186–187.
[2] S. Rabii and B. A. Wooley, "A 1.8-V digital-audio Sigma-Delta modulator in 0.8-μ CMOS," *IEEE J. Solid-State Circuits*, vol. 32, pp. 783–796, June 1997.
[3] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Delta\Sigma$ modulator with 88-dB dynamic range using local switch-bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, pp. 349–355, Mar. 2001.
[4] V. Peluso, P. Vancorenland, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 900-mV low-power A/D converter with 77-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1887–1897, Dec. 1998.
[5] M. Steyaert and J. Crols, "Switched-opamp: An approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, pp. 936–942, Aug. 1994.
[6] A. Marques, V. Peluso, M. Steyaert, and W. Sansen, "Optimal parameters for Delta-Sigma modulator topologies," *IEEE Trans. Circuits Syst.*, vol. 45, pp. 1232–1241, Sept. 1998.
[7] L. Yao, M. Steyaert, and W. Sansen, "A 0.8-V, 8-μW CMOS OTA with 50-dB gain and 1.2-MHz GBW in 18-pF load," in *Proc. Eur. Solid-State Circuits Conf.*, Sept. 2003, pp. 297–300.
[8] K. R. Laker and W. M. Sansen, *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, 1994.
[9] F. Wang and R. Harjani, "Power analysis and optimal design of opamps for oversampled converters," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 359–369, Apr. 1999.
[10] S. Norsworthy, R. Schreier, and G. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE Press, 1996.
[11] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 166–172, Mar. 1995.
[12] D. Haigh and B. Singh, "A switching scheme for switched capacitor filters which reduces the effects of parasitic capacitances associated with switch control terminals," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 1983, pp. 586–589.
[13] R. Aparicio and A. Hajimiri, "Capacity limits and matching properties of integrated capacitors," *IEEE J. Solid-State Circuits*, vol. 37, pp. 384–393, Mar. 2002.
[14] M. Keskin, U. Moon, and G. C. Temes, "A 1-V 10-MHz clock-rate 13-bit CMOS $\Delta\Sigma$ modulator using unity-gain-reset opamps," *IEEE J. Solid-State Circuits*, vol. 38, pp. 817–824, July 2002.
[15] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, "A 0.7-V MOSFET-only switched-opamp $\Delta\Sigma$ modulator in standard digital CMOS technology," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1662–1669, Dec. 2002.

Libin Yao (S'01) received the B.Sc. degree from the University of Electronic Science and Technology of China in 1989 and the M.Eng. degree from the Nanjing University of Science and Technology in 2000. He is currently working toward the Ph.D. degree at the Katholieke Universiteit Leuven, Belgium.

From 1989 to 2000, he was a Researcher with the Kunming Institute of Physics, China. Since 2000, he has been a Research Assistant in the ESAT-MICAS Laboratory, Katholieke Universiteit Leuven. His research interest is mainly in the area of high-performance analog-to-digital converters in deep-submicron CMOS technologies.

Michiel S. J. Steyaert (S'85–A'89–SM'92–F'04) was born in Aalst, Belgium, in 1959. He received the Masters degree in electrical-mechanical engineering and the Ph.D. degree in electronics from the Katholieke Universiteit Leuven (K.U.Leuven), Heverlee, Belgium, in 1983 and 1987, respectively.

From 1983 to 1986, he obtained an IWNOL fellowship (Belgian National Fundation for Industrial Research) which allowed him to work as a Research Assistant at the Laboratory ESAT at K.U. Leuven. In 1987, he was responsible for several industrial projects in the field of analog micropower circuits at the Laboratory ESAT as an IWONL Project Researcher. In 1988, he was a Visiting Assistant Professor at the University of California at Los Angeles. In 1989, he was appointed by the National Fund of Scientific Research (Belgium) as Research Associate, in 1992 as a Senior Research Associate and in 1996 as a Research Director at the Laboratory ESAT, K.U.Leuven. Between 1989 and 1996, he was also a part-time Associate Professor. He is now a Full Professor at the K.U.Leuven. His current research interests are in high-performance and high-frequency analog integrated circuits for telecommunication systems and analog signal processing.

Prof. Steyaert received the 1990 and 2001 European Solid-State Circuits Conference Best Paper Award. He received the 1991 and the 2000 NFWO Alcatel-Bell-Telephone award for innovative work in integrated circuits for telecommunications. Prof.Steyaert received the 1995 and 1997 IEEE-ISSCC Evening Session Award, the 1999 IEEE Circuit and Systems Society Guillemin-Cauer Award and is currently an IEEE-Fellow.

Willy Sansen (S'66–M'72–SM'86–F'95) has received the M.Sc. degree in electrical engineering from the Katholieke Universiteit Leuven in 1967 and the Ph.D. degree in electronics from the University of California at Berkeley in 1972.

In 1972, he was appointed by the National Fund of Scientific Research (Belgium) at the ESAT Laboratory of the K.U.Leuven, where he has been a Full Professor since 1980. During 1984–1990, he was the head of the Electrical Engineering Department. Since 1984, he has headed the ESAT-MICAS Laboratory on analog design, which counts about 60 members and which is mainly active in research projects with industry. He is a member of several boards of directors. In 1978, he was a Visiting Professor at Stanford University, in 1981 at the EPFL Lausanne, in 1985 at the University of Pennsylvania, Philadelphia, in 1994 at the T.H. Ulm, and in 2004 at Infineon, Villach. He has been involved in design automation and in numerous analog integrated circuit designs for telecommunications, consumer electronics, medical applications and sensors. He has been supervisor of over 50 Ph.D. theses in these fields. He has authored and coauthored 12 books and more than 550 papers in international journals and conference proceedings.

Prof. Sansen is a member of several editorial and program committees of journals and conferences. He is cofounder and organizer of the workshops on Advances in Analog Circuit Design in Europe. He is a member of the executive and program committees of the IEEE ISSCC conference, and was program chair of the ISSCC 2002 conference.