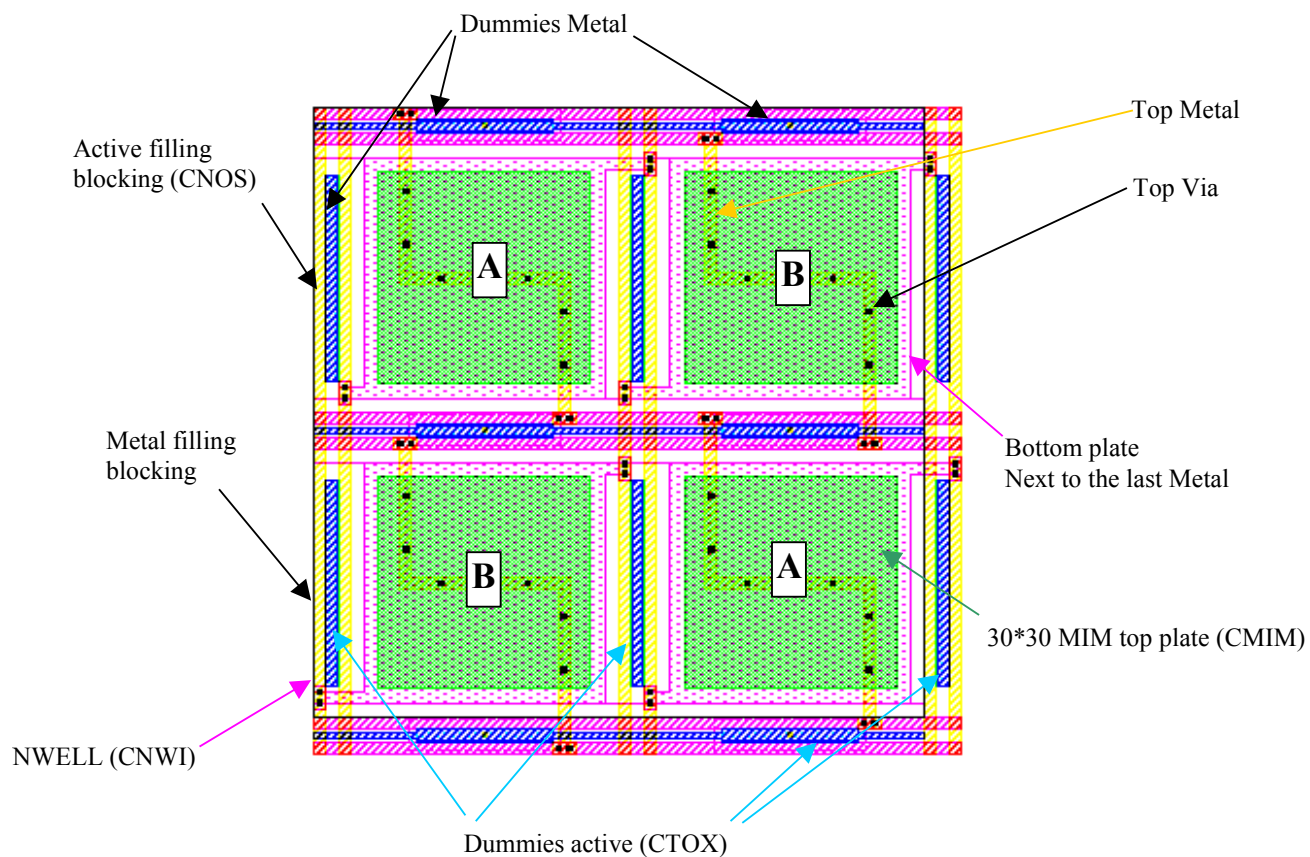


0.18 $\mu$ m process: MIM capacitance =  $(1 \pm 0.15) \text{ fF}/(\mu\text{m})^2$

### 7.3: MIM capacitor mismatch:

The layout of matched pair of MIM capacitor should be done with specific care.

The following layout example has been used for the mismatch characterization:



Maximum allowed MIM metal area is 150\*150 $\mu\text{m}$ . However in order to obtain a better control of the bottom plate to substrate parasitic capacitance, it is recommended to not drawn MIM area greater than 30\*30  $\mu\text{m}$ . In this sample, automatic metal and active filling is blocked. However, it is mandatory to drawn dummies active and dummies metal manually around each elementary capacitor. In this case, the dummies are totally controlled and symmetrical around each side of capacitor.

The active and metal filling blocking should be use only **and only** over the matched capacitor pair.

Parasitic to substrate capacitor could be reduced also by adding NWELL under the capacitor (floating or biasing to VDD).

The layout is available under request to the Technology Development Department.

#### MIM capacitor mismatch model:

$$\text{Sigma } (\Delta C) / C = A(C) / [\text{Sqrt (Top plate Area)}]$$

$$A(C) \text{ \%. um: } 1.6 \text{ (+/- 3sigma : 4.8)}$$

MIM-cap-mismatch = 1.6% /  $\sqrt{(W*L)}$  for 1sigma distribution or 4.8% /  $\sqrt{(W*L)}$  for 3sigma