ABSTRACT

In the past 20 years, analog CMOS circuits have evolved from low-speed, low-complexity, small-signal, high-voltage topologies to high-speed, high-complexity, low-voltage "mixed-signal" systems containing a great deal of digital circuitry. While device scaling has enhanced the raw speed of transistors, unwanted interaction between different sections of integrated circuits as well as non idealities in the layout increasingly limit both speed and precision of such system. Today's analog circuit design is very heavily influenced by layout.

We study principles of layout, emphasizing effects that manifest themselves when analog and digital circuits coexist on a chip. For the sake of brevity, we use the term analog to mean both "analog" and "mixed-signal". Beginning with an introduction, we study a number of topics related to the layout of analog circuits, including matching of transistors, causes of mismatch, design rules. Next, we deal with fingers and multipliers, common centroid layout, use of dummies and guard rings.

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CHAPTER 1: INTRODUCTION

1.1 Schematic & Layout

Schematic is a "Circuit Diagram" or a drawing of how it will work. It doesn't necessarily tell everything about physical implementation of the circuit, but schematic is easier to read and understand, comparing to layout.

Layout (circuit board layout) is a geometrical model of the circuit. It's usually intended for fabrication. Different layouts can be made for one and the same schematic, if needed.

1.2 Analog Vs Digital Layout

In **Digital Layout**, the W/L ratios used are the minimum feature size. This is done to minimize the area and maximize the packing density. When the area is minimized, the delay also gets minimized. Digital design is easier because we can use cell-based methodology to do a layout, wherein you already have predefined layouts of cells and use them to create larger blocks. This saves time and money. Transistor acts as switch.

Analog layout on the other hand is tougher as more importance is given to transistor details. This is done to achieve matching and the required currents and voltages. Analog design is based mostly on the drain currents and bias voltages. So, layout has to be done carefully to achieve these voltages and currents else the design will fail when manufactured. Transistor acts as amplifiers, resistors or others.

The design flow of analog integrated circuits is shown in Fig 1.1.

Fig 1.2 shows the Schematic of basic Current Mirror and Differential Pair done using Cadence® EDA tool. This circuit block finds its application in a 2 stage Opamp. The values of W & L of transistors are:

Current mirror: PM0: W=36.09µ, L=2.6µ

PM1: W=36.09µ, L=2.6µ

Differential Pair: NM0: W=24.375µ, L=2.6µ

NM1: W=24.375µ, L=2.6µ

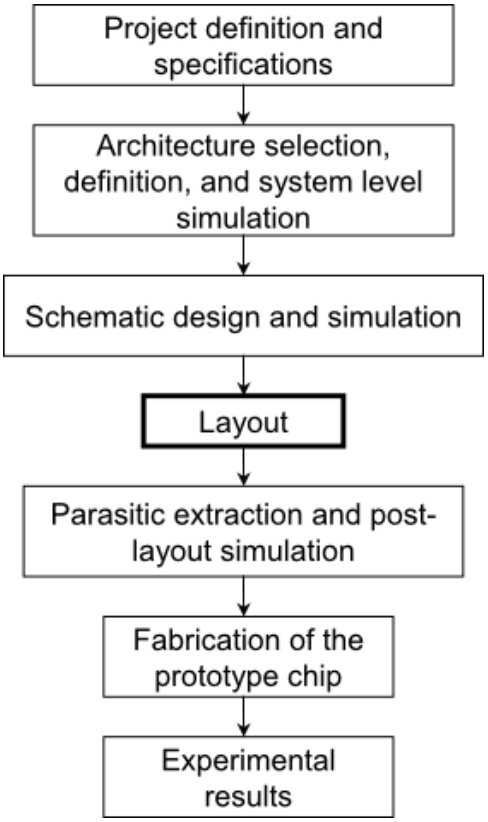


Fig 1.1: Design flow of analog integrated circuits

Fig 1.3 shows the Floor planning of basic Current Mirror and Differential Pair.

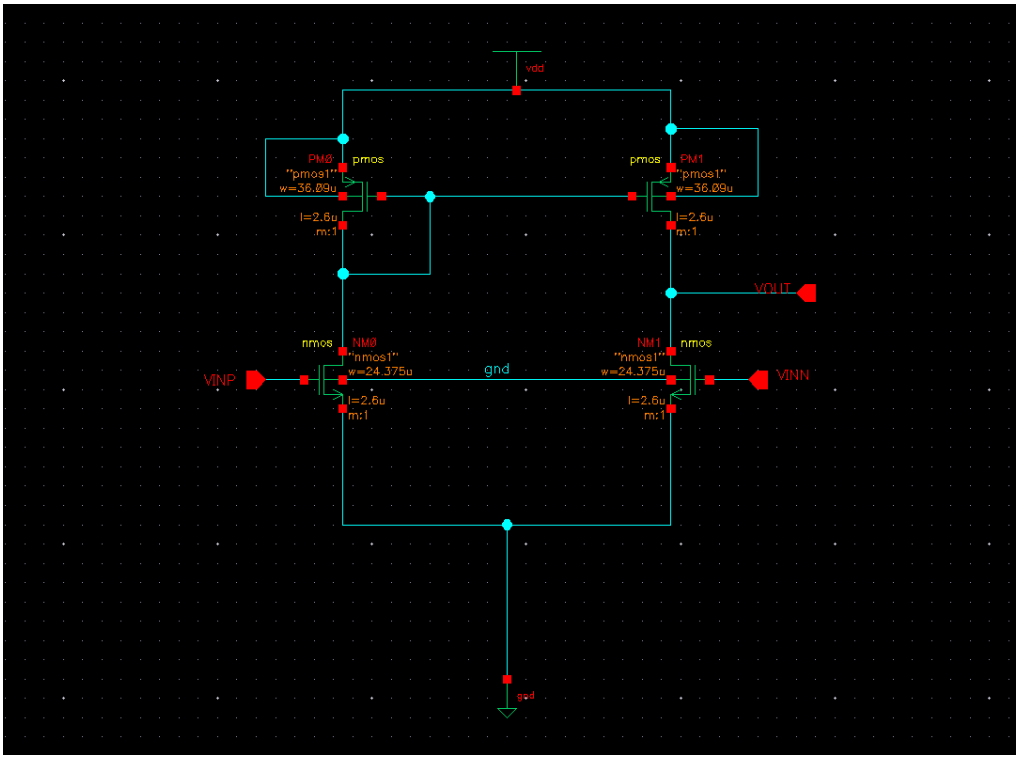


Fig 1.2: Schematic of basic Current Mirror and Differential Pair

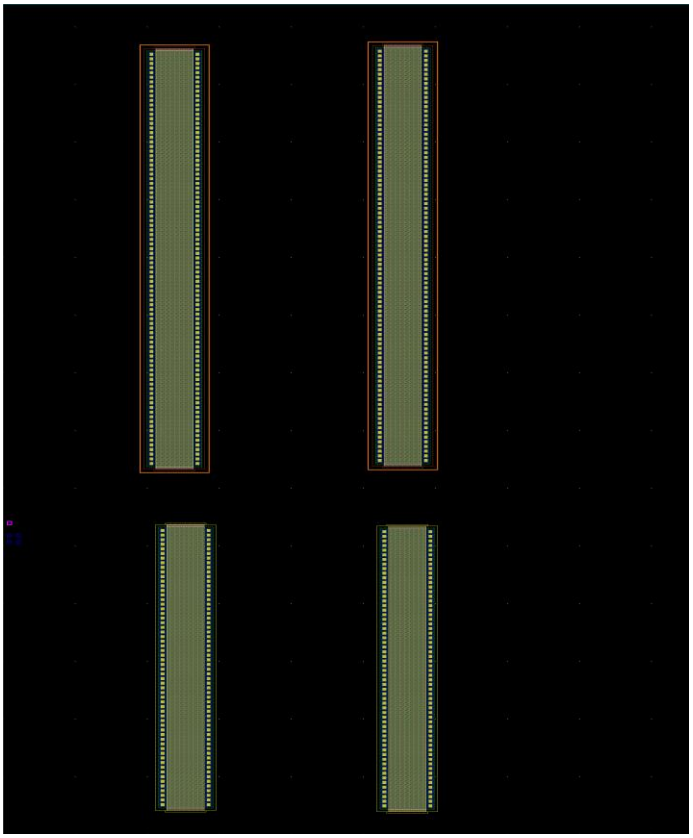


Fig 1.3: Floor planning of basic Current Mirror and Differential Pair

1.3 Basics of Fabrication

Modern CMOS technologies involve more than 200 processing steps; we can view the sequence as a combination of the following operations:

1) Wafer processing to produce the proper type of substrate.
2) Photo Lithography to precisely define each region.
3) Oxidation, Deposition and Ion implantation to add materials to the wafer.
4) Etching to remove materials from the wafer.

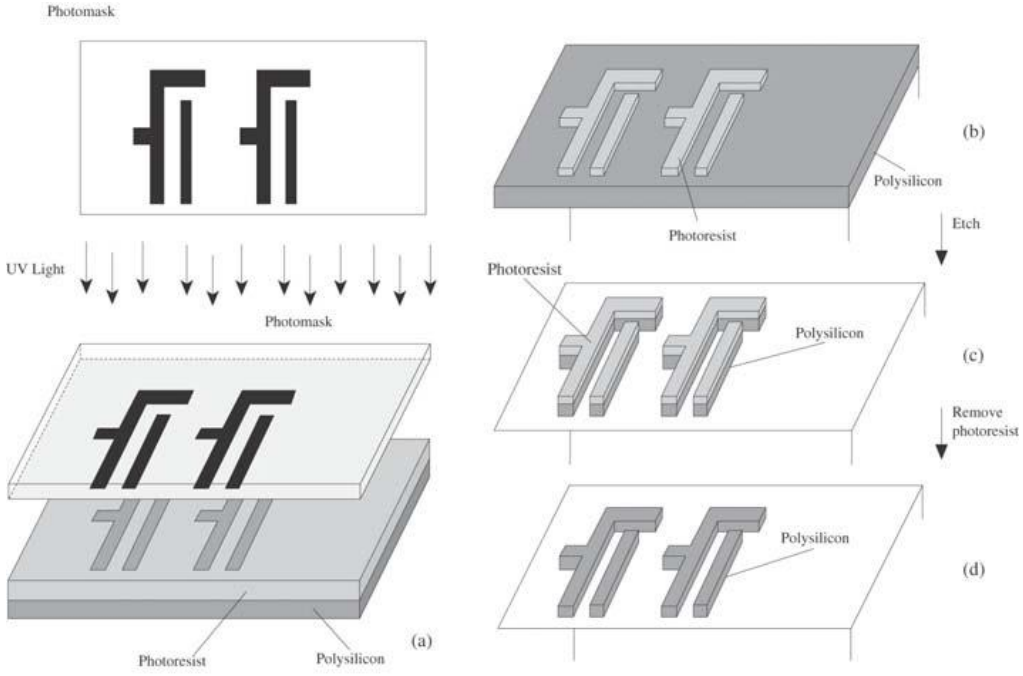


Fig 1.4: Photo mask and Photo lithography

Photo lithography is the first step in transferring the circuit layout information to the wafer.

The layout consists of polygons representing different types of layers. Eg n-well, S/D regions, polysilicon, contacts etc.
For fabrication purposes, we decompose the layout into these layers.

To understand how a layer is transferred from the layout to the wafer, let us consider the poly pattern as shown in Fig 1.4. This pattern is written to a transparent glass mask by a precisely controlled electron beam. The layer is covered by a thin layer of photresist, a material whose etching properties change upon exposure to light. Subsequently, the mask is placed on top of the wafer and the pattern is projected onto the layer by UV light. The photoresist hardens in the regions exposed the light and remains soft under the opaque pattern. The layer is then placed in an etchant that dissolves the soft photresist area, thereby exposing the polysilicon surface.

CHAPTER 2:
Matching of devices

Why special attention to matching?

A large variety of analog circuits rely on matching of transistors. Circuits like differential pair rely on gate to source voltage matching while current mirrors rely on current matching.

Most integrated resistors and capacitors have a tolerance of about 20% to 30%. All of the devices in an integrated circuit occupy the same piece of silicon, so they all experience similar manufacturing conditions. If one component's value increases by 10%, then all similar components experience similar increases. The ratio of two similar components on the same IC can be controlled to a tolerance of 0.1% by proper matching of the components.

2.1 Measuring Mismatch

The mismatch between any two devices is expressed as a deviation of the measured device ratio from the intended device ratio.

Suppose a designer lays out a pair of matched 10kΩ resistors. After fabrication, these resistors are found to equal 12.47kΩ and 12.34kΩ. The ratio between these resistors equals 1.0105 or approximately 1% more than the intended ratio of 1.0000. This pair of resistors therefore exhibits a mismatch of approximately 1%.

2.2 Causes of Mismatch

Mismatch in integrated circuits are generally of two types:

Random mismatches due to microscopic fluctuations in dimensions, doping, oxide thickness and other parameters that influence component values.

Systematic mismatches which are caused by:

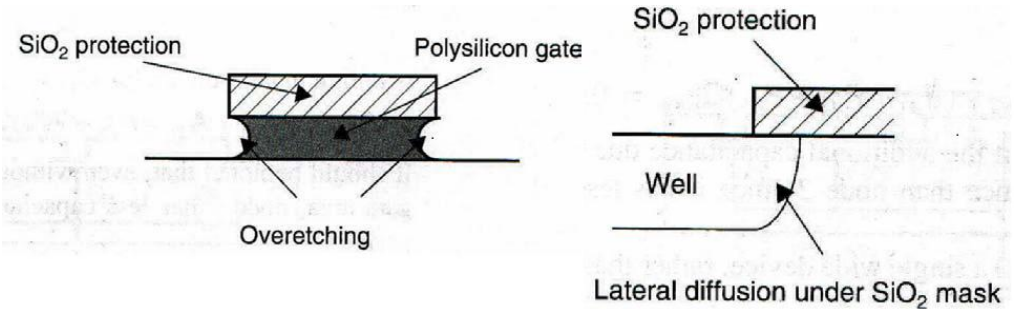
Process biases

Stress gradients and Package shifts.

2.2.1 Process Bias

The dimensions of geometries fabricated in silicon never exactly match those in the layout database because the geometries shrink or expand during photolithography, etching, diffusion and implantation.

The difference between the drawn width of geometry and its actual measured width constitutes the term process bias.



(a) (b)

Fig 2.1 (a) Overetching (b)Lateral diffusion during S/D region mplantation.

2.2.2 Stress Gradients and Package Shifts

Silicon is piezoresistive i.e. it exhibits changes in resistivity under stress. Variations in stress across the die will produce corresponding variations in matching.

Metal cans have been used to package semiconductors from the earliest days of the industry. Although they are expensive, they can provide a reliable low-stress means of packaging.

Plastic packages are much more widely used now.

Measurement of electrical parameters before and after packaging will reveal differences called *package shifts* proportional to the level of residual stress.

Careful layout can usually reduce the sensitivity of a circuit to mechanical stress, which can in turn reduce the magnitude of package shifts.

Gradients

Isobaric Contour Plot

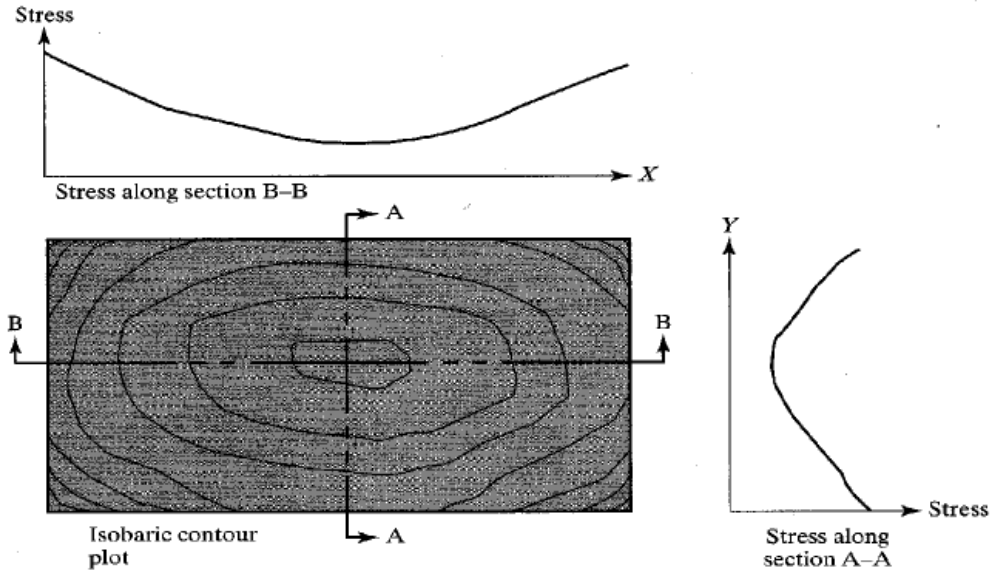


Fig 2.2: Isobaric contour plot of the stress distribution across the surface of a typical plastic packaged silicon die, together with two graphs showing the stress along the section lines A-A and B-B

Fig 2.2 graphically illustrates the stress distribution across a typical integrated circuit. The drawing at the lower left is called isobaric contour plot. The curved lines (called isobars) indicate the stress levels at various points on the die surface. The stress intensity rises from a broad minimum in the middle of the die to maxima at the four corners. The graph above the contour plot shows the stress intensity along a line bisecting the die

horizontally, while the graph at the right shows the stress intensity along a line bisecting the die vertically.

The rate of change of stress intensity is called the stress gradient. This gradient is usually smallest in the middle of the die and slowly increases as one moves out toward the edges.
The stress gradient is usually much greater at the extreme corners of the die than at any other point (Fig 2.3)

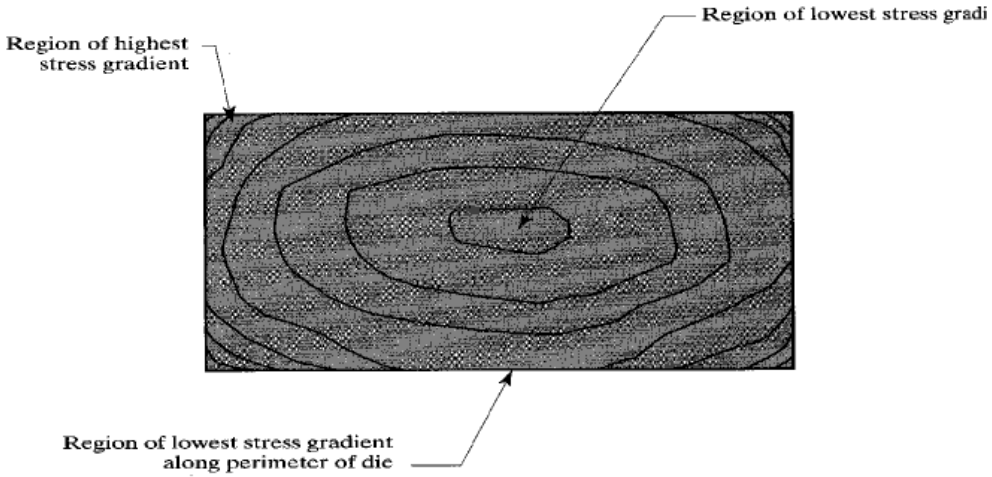


Fig 2.3: Isobaric contour plot showing regions of highest and lowest stress gradient.

Many of the systematic inaccuracies can be avoided through good layout style.

CHAPTER 3:

Design rules

Layout rules or design rules are a set of rules that guarantee successful fabrication of integrated circuits despite various tolerances in each step of the processing.

Most design rules can be categorized under one of four groups described below.

Minimum width

Fig 3.1: Excessive width variation in a narrow poly line.

The widths (and lengths) of the geometries defined on a mask must exceed a minimum value imposed by both lithography and processing capabilities of the technology. For example, if a polysilicon rectangle is too narrow, then, owing to fabrication tolerances, it may simply break or suffer from a large local resistance.

Minimum spacing

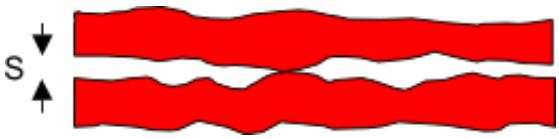


Fig 3.2: Short between two excessively close poly lines.

The geometries built must be separated by a minimum spacing. As an example, if 2 polysilicon lines are placed too close, they may be shorted.

Minimum enclosure

The n-well or the p+ implant must surround the transistor with sufficient margin to make sure that the device is contained within. Below is an example of enclosure rule for poly and metal surrounding a contact. To ensure that the contact remains inside the poly and metal1, both geometries must enclose the contact with enough margin.

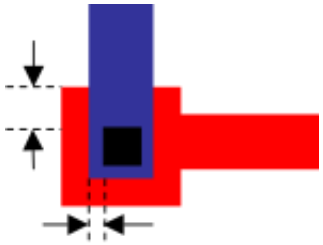


Fig 3.3: Enclosure rule for poly and metal surrounding a contact.

Minimum Extension

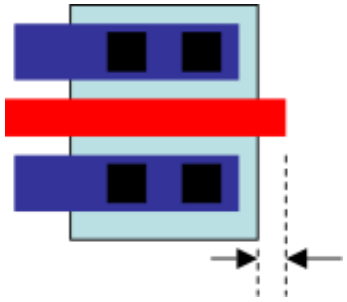


Fig 3.4: Extension of poly beyond the gate area.

Some geometries must extend beyond the edge of others by a minimum value. As an example, the poly gate must have a minimum extension beyond the well to ensure that the transistor functions properly at the edge of well.

CHAPTER 4:

Analog Layout Techniques

4.1 Fingers and Multipliers

FINGERS: It will give you a unique cell with the complete transistor with all the fingers (folds).

Useful when you want a cell as compact as possible.

Results into MOSFET sharing drain or source.

MULTIPLIERS: It will give you as much transistors as the multiplicity indicates (unit width multiplied by the multiplier).

Useful when you want to split the transistor to make some interdigitation matching technique.

Commonly used in current mirrors when making multiple bias currents.

Results individual MOSFET having their own separated source and drain.

To recap, this is exactly the same and the better one depends on what is your need with the transistor.

Example of Fingers:

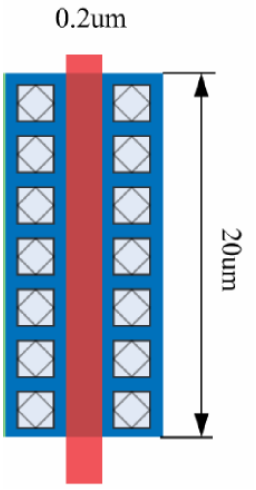


Fig 4.1: The basic transistor layout with channel length (L) of 0.2um and a channel width (W) of 20um.

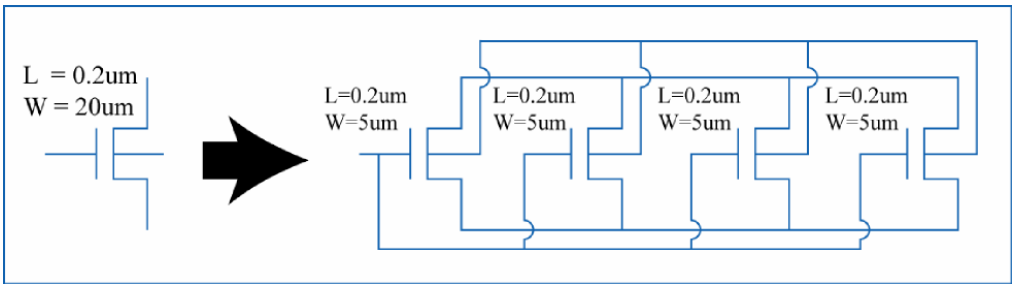


Fig 4.2: Transistor with W=20um and L=0.2um is similar to having 4 transistors connected in parallel, each with a W=5um and L=0.2um.

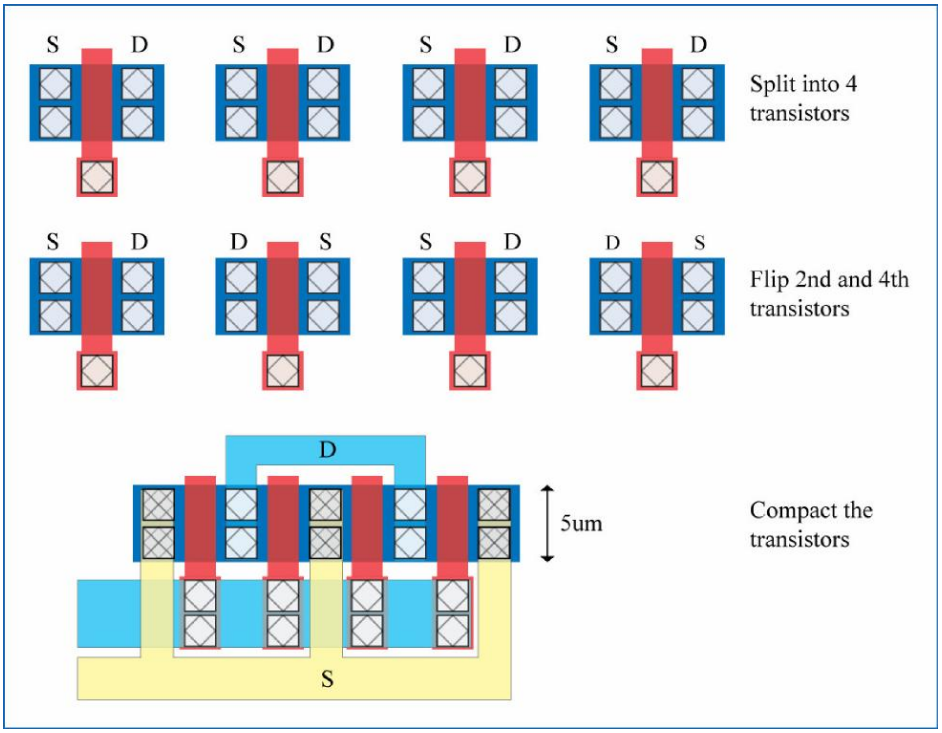


Fig 4.3: layout of the transistor with 4 fingers.

4.2 Common Centroids

Matched devices should reside as close to one another as possible to minimize the difference in stresses between them. Assume that the

stress gradient is approximately constant in the region between the matched devices. The stress difference between two matched devices is proportional to the product of the stress gradient and the separation between them. For the purposes of this calculation, the location of each device is computed by averaging the contribution of each portion of the device to the whole. The

resulting location is called the ***centroid*** of the device. The centroid of a rectangular device lies in its exact center. The centroids of other geometries can often be located by applying the ***principle of centroidal symmetry,*** which states that the centroid of a geometry must lie on any axis of symmetry of that geometry. Fig 4.4 shows how this principle can determine the centroid of a rectangle.

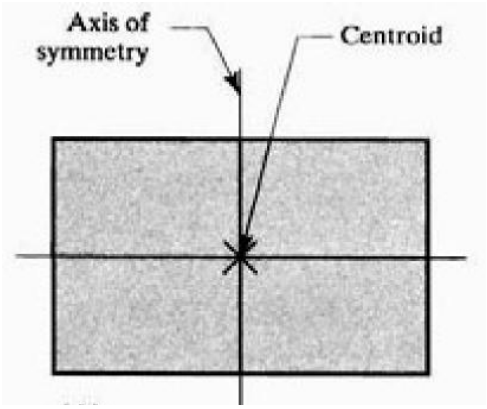


Fig 4.4: Locating centroid of a rectangle

The effects of stress can be quantified in terms of piezoresistivity,
centroid locations, and stress gradients. The magnitude of the stress-induced mismatch δ_s between two devices equals

$$\delta_s=\pi_c d_c \nabla S_c \qquad \text{----- [4.1]}$$

Where π_c is the piezoresistivity along the line connecting the centroids of the two matched devices, ∇S_c is the stress gradient along this same line, and d_c equals the distance between the centroids. This formula reveals several ways to minimize stress sensitivity. First, the designer can reduce the piezoresistivity, by orienting the resistors in the direction of minimum piezoresistivity. Second, the designer can reduce the magnitude of the stress gradient, by proper location of the devices and by selecting low-stress packaging materials. Third, the designer can reduce the separation between the centroids of the device, d_c. So we will now focus on reducing the separation of the centroids.

4.3 Common Centroid Layout

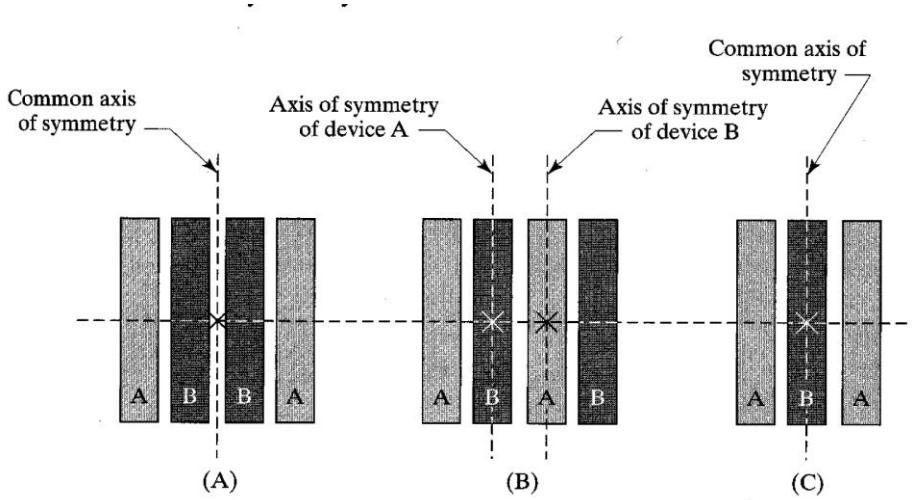


Fig 4.5: Examples of one dimensional common centroid arrays

Suppose that a matched device is divided into sections. If these sections are all identical, and if they are arranged to form a symmetric pattern, then the centroid of the device will lie at the intersection of the axes of symmetry passing through the array. It is actually possible to arrange two arrayed devices so that they share common axes of symmetry. If this can be achieved, then the principle of centroidal symmetry ensures that the centroids of the two devices coincide. Fig 4.5 shows an example of such a common-centroid layout. The two devices are marked A and B, their axes of symmetry are shown as dotted lines, and their centroids are denoted by an "X" where the two axes of symmetry intersect.

Equation [4.1] predicts that the stress-induced mismatch of a common-centroid layout equals zero because the separation between the centroids equals zero. This does not actually occur, because the stress gradient never remains precisely constant. Despite this limitation, common-centroid layout is still the single most powerful technique available for minimizing stress-induced mismatches.

Fig (4.5) shows three examples of common-centroid layouts produced by

arraying segments of matched devices along one dimension. These types of layouts are usually called **interdigitated** arrays because the sections of one device interpenetrate the sections of the other like the intermeshed fingers of two hands.

Fig (4.5) (A) shows an interdigitated array consisting of two devices, each composed of two segments. If the devices are denoted by the letters A and B, then the arrangement of the segments follows the interdigitation pattern (or weave) ABBA. This pattern has an axis of symmetry that divides it into two mirror-image halves (AB and BA).

Arrays that use the interdigitation pattern ABBA require dummies because the segments of one device occupy both ends of the array.

The pattern ABAB Fig (4.5) (B) does not completely align the centroids of the two devices. It is moderately matched.

Common-centroid layouts can also consist of devices of different sizes. Fig (4.5) (C) shows an example that implements a 2:1 ratio using the pattern ABA.

The best interdigitation patterns obey all four rules of common-centroid layout listed in Table.

The ***rule* of *coincidence*** states that the centroids of the matched devices should coincide at least approximately. Patterns that do not achieve coincidence exhibit larger stress sensitivities than those that do.

The ***rule* of *symmetry*** states that the array should be symmetric around both axes. A one dimensional array should derive one of its axes of symmetry from its interdigitation pattern. For example, an array using the pattern ABBA will have an axis of symmetry dividing it into two mirror-image halves (AB and BA). A one-dimensional array must rely on the symmetries of the individual segments to produce its second axis of symmetry.

1. ***Coincidence:*** The centroids of the matched devices should coincide at least approximately. Ideally, the centroids should exactly coincide.
2. ***Symmetry:*** The array should be symmetric around both the X- and Y-axes. Ideally, this symmetry should arise from the placement of segments in the array and not from the symmetry of the individual segments.
3. ***Dispersion:*** The array should exhibit the highest possible degree of dispersion; in other words, the segments of each device should be distributed throughout the array as uniformly as possible.
4. ***Compactness:*** The array should be as compact as possible. Ideally, it should be nearly square.

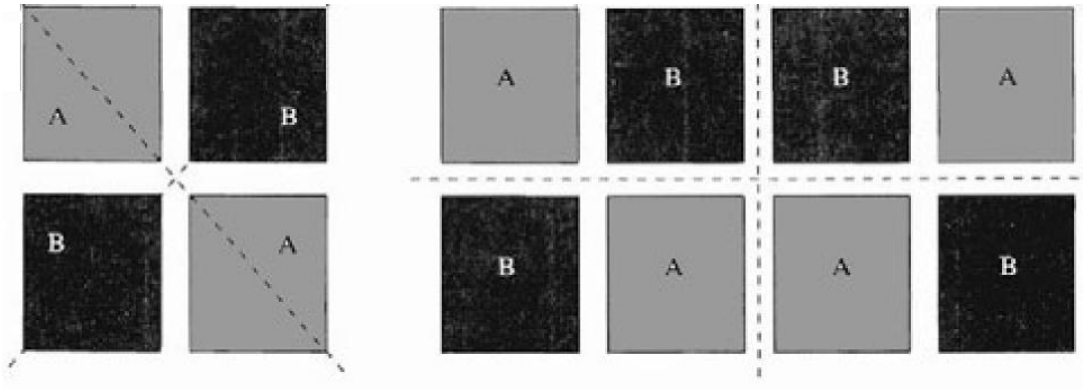
Table 4. 1: The 4 rules of common-centroid layout.

The ***rule of dispersion*** states that the segments of each device should be distributed throughout the array as uniformly as possible. The degree of dispersion is often evident to the eye. Dispersion helps reduce the sensitivity of a common-centroid array to higher-order gradients (nonlinearities).

The ***rule of compactness*** states that the array should be as compact as possible. Ideally, it should be square, but in practice it can have an aspect ratio of 2:1 or even 3:1 without introducing any significant vulnerability. If the aspect ratio of the array exceeds 2:1, then consider breaking the array into a larger or smaller number of segments.

All of the common-centroid layouts discussed so far array the devices in only one dimension. Such a ***one-dimensional array*** derives one of its axes of symmetry from its interdigitation pattern and one of its axes of symmetry from the symmetry of its segments. The segments can also be arranged to form a ***two-dimensional array*** deriving both of its axes of symmetry from its interdigitation pattern. This type of arrangement generally provides better cancellation of gradients than one-dimensional arrays, primarily because of the superior compactness and dispersion possible within a two-dimensional array.
Fig (4.6) (a) shows two matched devices, each composed of two segments arranged in an array of two rows and two columns. This arrangement is often called a ***cross-coupled pair.***

If the matched devices are large enough to segment into more than two pieces, then the cross-coupled pair can be further subdivided as shown in Fig (4.6) (b). This array exhibits more dispersion than a cross-coupled pair and is therefore less susceptible to higher-order gradients. This two-dimensional interdigitation pattern, or ***tiling,*** can be indefinitely extended in both dimensions.



(a) (b)

Fig 4.6: Examples of two dimensional common centroid arrays

The rules for creating one-dimensional arrays also apply to two-dimensional arrays. The sections should be arranged so that the array has two or more axes of symmetry intersecting at the point where the centroids of the matched devices coincide.

Example: For process variation in local area, we can assume that the gradient of the variation is described as:

$$y = mx + b \quad \text{---------- [4.2]}$$

Assume component A, which is composed of units A1 and A2, should be twice the size of component B.

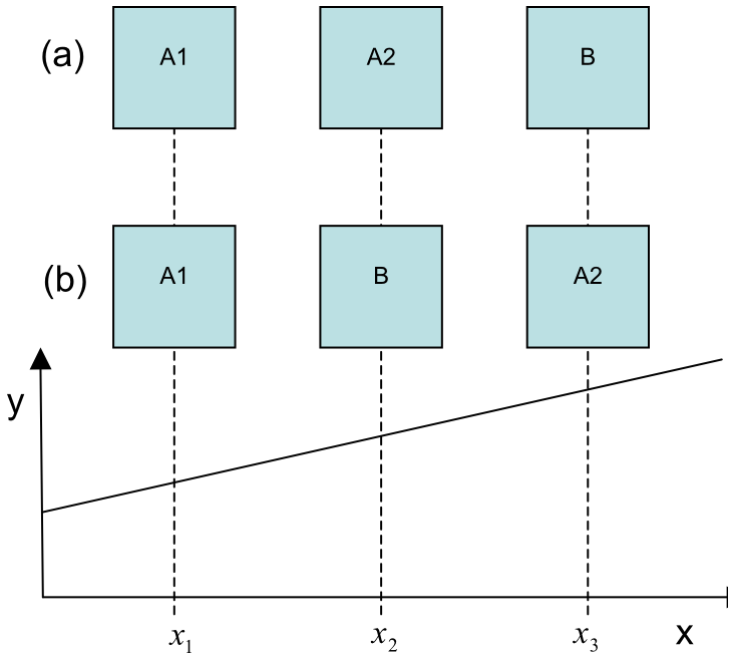


Fig 4.7: Process variation of $y = mx + b$

For a layout of (a) we have :

$$A1 = mx_1 + b$$
$$A2 = mx_2 + b$$
$$B = mx_3 + b$$
$$\frac{A1 + A2}{B} = \frac{m(x_1 + x_2) + 2b}{mx_3 + b} \neq 2 \qquad \text{---------- [4.3]}$$

For a layout like (b) we have :

$$A1 = mx_1 + b$$
$$A2 = mx_3 + b$$
$$B = mx_2 + b$$
$$\frac{A1 + A2}{B} = \frac{m(x_1 + x_3) + 2b}{mx_2 + b} = 2 \qquad \text{---------- [4.4]}$$

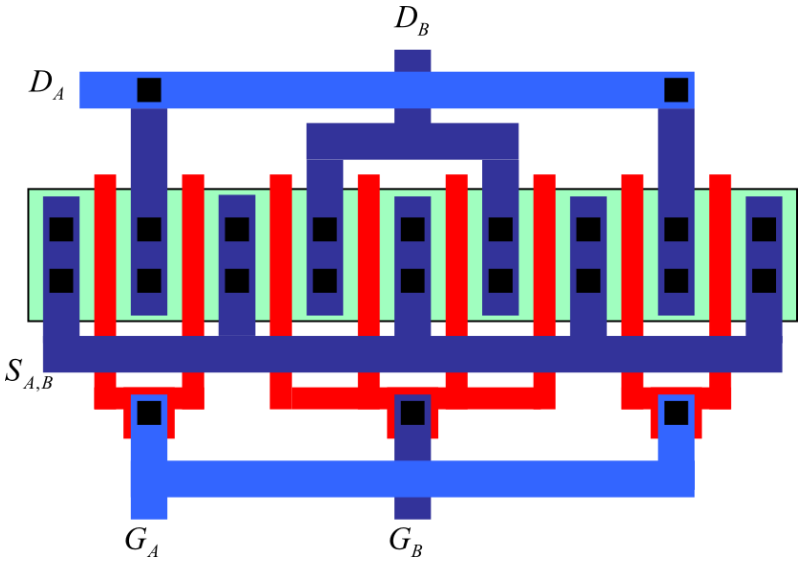


Fig 4.8: Common Centroid layout of above Fig 4.7

4.4 Use of Dummies

Fig 4.9 shows an improved version of the layout above. Two dummy transistors are added to the left and right sides. On the layout above, transistor A sees different ambient environment to the left and to the right. Dummy transistors improve the matching between transistor A and B by providing similar environment to the circuit that is on the boundary of a layout.

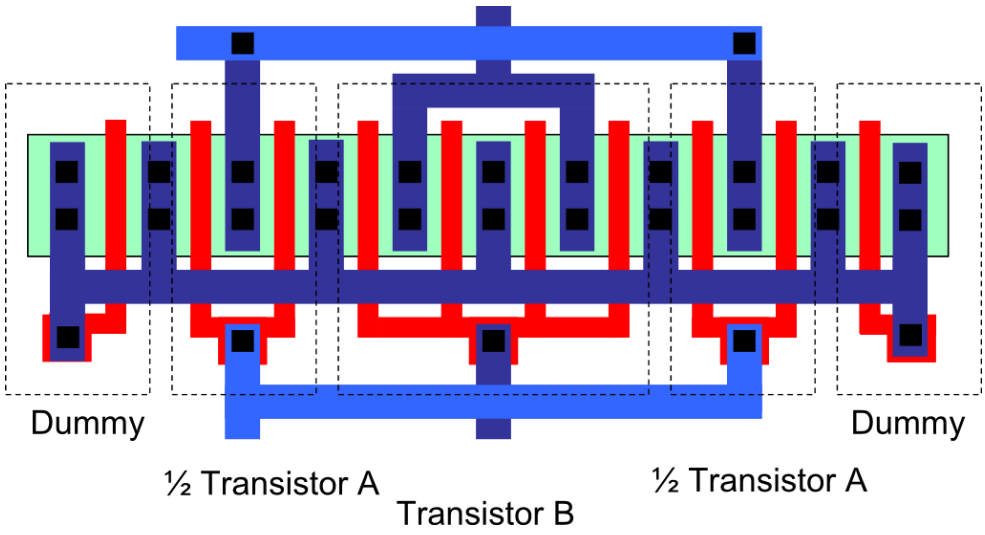


Fig 4.9: Using dummy transistors.

4.5 Use of Guard Rings

Analog design performances are sensitive to electrical disturbance. Disturbance in the substrate should be minimized as much as possible.

Two common types of substrate disturbance are

• Disturbance from minority carrier

• Substrate coupling noise

Disturbance from minority carrier

Minority carriers are injected into the substrate from the source diffusions and the drain diffusions when

• The source potential or the drain potential of NMOS is below the substrate potential

• The source potential or the drain potential of PMOS is above the N-well potential

The drifting of the minority carriers in the substrate and the N-well create a potential difference that can affect the performance of the circuit, or trigger a latch-up.

Substrate coupling noise

Consider the cross section of a transistor as shown in Fig 4.10.

P-diff in p-substrate is known as p-tap, while n-diff in N-well is known as n-tap.

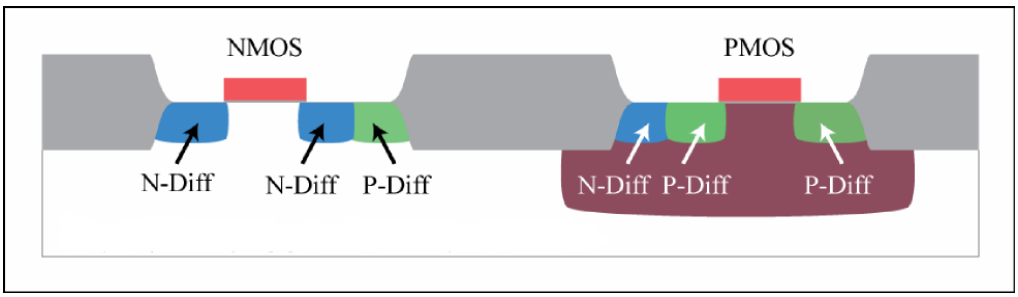


Fig 4.10: Cross section of a transistor.

Connections from the metal routings to the substrate and the Nwells are made through the p-tap and the n-tap. This is necessary to ensure the wells are properly tied down and the transistors are isolated. The p-substrate should be biased to the lowest voltage potential while the N-well should be biased to the highest voltage potential. In this way, all the P-N junctions are reverse biased and hence the transistors are electrically isolated from one another as shown in the diagram below.

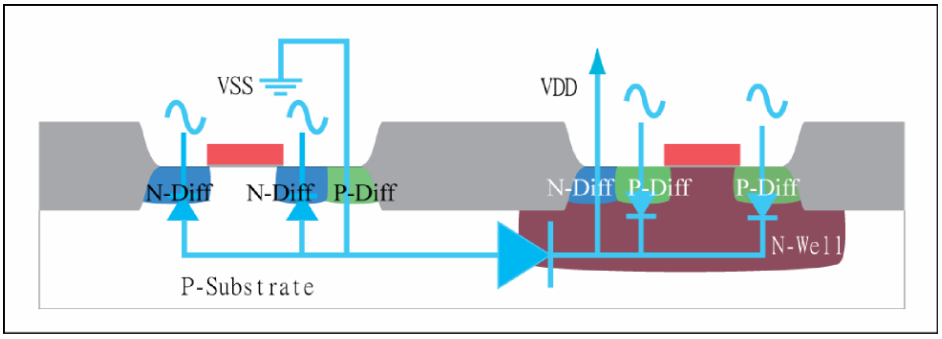


Fig 4.11: Cross section of transistor

A reverse biased diode has the electrical properties of a capacitor. Circuit signals can be coupled through the substrate as illustrated in the diagram below.

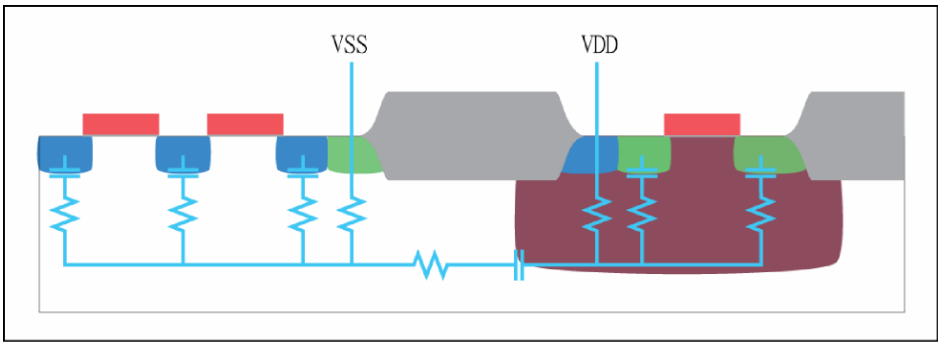


Fig 4.12: Effect of substrate coupling noise.

To reduce disturbances from **minority carrier**, you may use **guard ring** in the following configuration around noisy transistors.

• Surround NMOS in the p-substrate with N-well guard ring. Tie the N-well guard ring to VDD. The N-diffusions from the NMOS could inject stray electrons into the substrate. These stray electrons could be collected efficiently by the N-well guard ring that is biased to VDD to attract the electrons.

• Surround the PMOS in the N-well with P-diffusion guard ring. Tie the P-diffusion guard ring to ground. P-diffusions from the PMOS inject stray holes into the N-well. These stray holes could be collected efficiently by the P-diffusion guard ring that is biased to ground to attract the holes.

For the guard rings to be effective, the resistance in the path from the straying minority carrier to the guard ring and then to the voltage source must be kept as low as possible. Hence, the minority carrier noise guard rings are *made wider* so as to decrease it resistance. The guard rings are also placed around the critical transistors to minimize stray electrons and stray holes from affecting the critical transistors.

To reduce **substrate coupling noise**, you may use **guard ring** in the following configuration around critical transistors.

• Surround NMOS in the p-substrate with p-tap guard ring that is connected to ground.
• Surround PMOS in the N-well with n-tap guard ring that is connected to VDD.

The following layouts show both PMOS and NMOS surrounded with double guard rings.

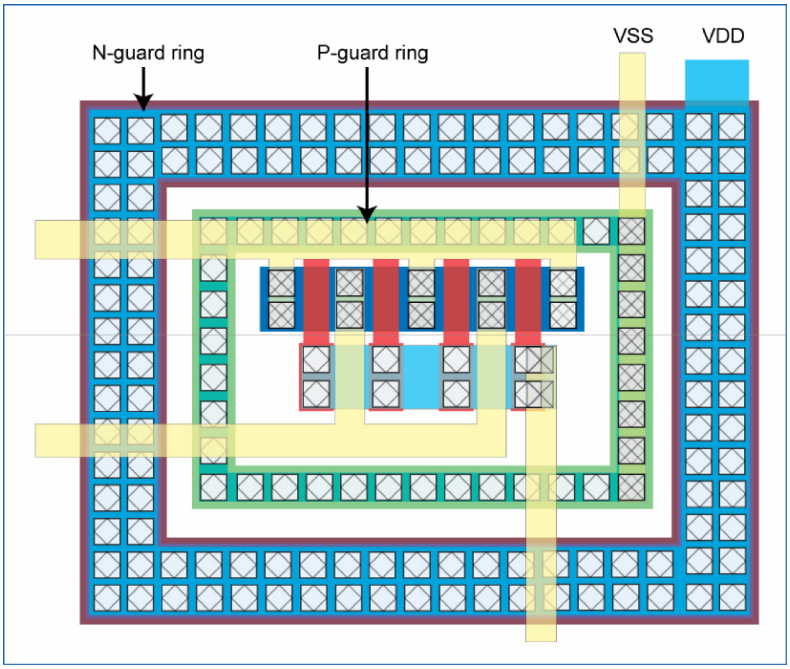


Fig 4.13: NMOS surrounded by double guard ring.

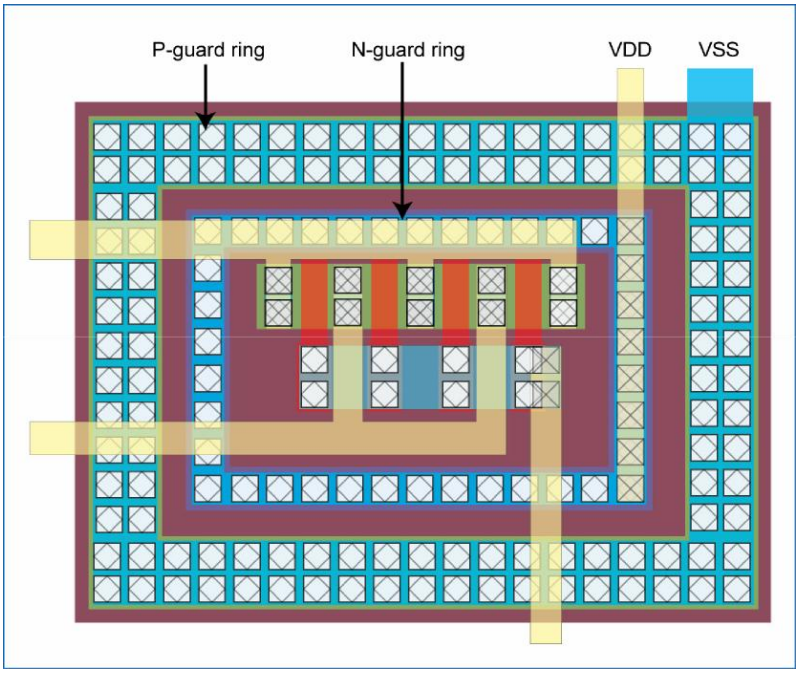


Fig 4.14: PMOS surrounded by double guard ring.

Example: Fig shows Layout of basic current mirror and differential pair. The layout uses above mentioned concepts of Analog Layout Techniques. By using these analog layout techniques the process variations can be minimized, the performance can be increased.

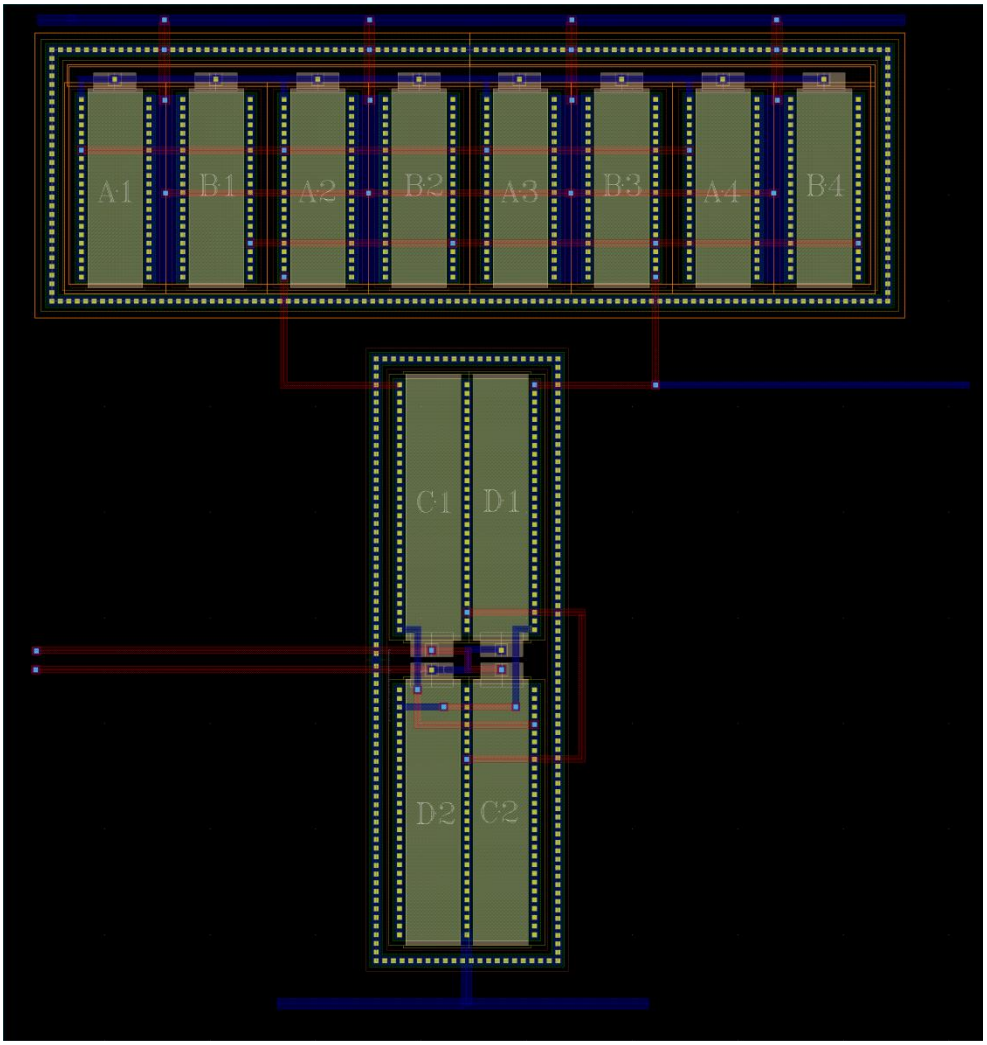


Fig 4.15: Layout of basic current mirror and differential pair.

CONCLUSION

In doing layouts for digital circuits, the speed and the area are the two most important issues. In contrast, in doing layout for analog circuits, everything should be considered simultaneously. In addition to the speed and the area, other equally critical considerations should be taken into account.

Every analog circuit has some matching required, so we use common centroid, dummy devices for designing the layout. To reduce disturbances from minority carrier and to reduce substrate coupling noise, we use guard ring. Without proper layout, the mismatches and the coupled noise would be quite large and would significantly degrade the performance device.

BIBLIOGRAPHY

- http://www.rficdesign.com/vlsi/analog-layout
- www.edaboard.com
- Razavi, Behzad. Design of Analog CMOS Integrated Circuits. Tata McGraw-Hill, 2002.
- Hastings, Alan. The Art of Analog Layout. New Jersey: Prentice Hall, 2001.
- Lee Eng Han. CMOS Transistor Layout Kung Fu, 2005
- CMOS Circuit Design, Layout and Simulation. R. J. Baker. Wiley IEEE Press