CPIC

CAVE CREEK PLUG IN CARD (REV 1.2)

REVISION HISTORY:

REV0.5	INITIAL CUSTOMER RELEASE
REV0.6	CHANGES BASED ON TESTING OF REV A BUILD 1
REV1.0	CHANGES BASED ON TESTING OF REV A BUILD 2 (POWER SEQUENCE DIAGRAM & 4 BOM STUFFING DEFAULTS FOR R261, R122, R149, R150)
REV1.1	UPDATED CAVE CREEK SYMBOL, ADDED VSS CONNECTIONS ON SYMBOL SECTION 12
REV1.2	UPDATE CPIC VCC1P0_PWR SUPPLY TO SUPPORT GREATER THAN 10A CAVE CREEK B0 ICC CURRENTS

Prepared For:
Intel Corporation
5000 W. Chandler Blvd
Chandler, AZ 85226
www.intel.com

Prepared By:
ADI Engineering, Inc.
1758 Worth Park
Charlottesville, VA 22911
www.adiengineering.com

TITLE	CPIC	
SIZE B	DWG NO 453503	REV 1.2
DATE 2-22-2012_11:11	SHEET 1 of 34	

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked reserved or undefined. Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

This document contains information on products in the design phase of development.

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See http://www.intel.com/products/processor_number for details.

Code Names are for use by Intel to identify products, platforms, programs, services, etc. (products) in development by Intel that have not been made commercially available to the public, i.e., announced, launched or shipped. They are never to be used as commercial names for products or intended to function as trademarks.

Intel, Intel logo, and Xeon are trademarks of Intel Corporation in the U.S. and other countries.

*Other names and brands may be claimed as the property of others.

DISCLAIMER

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE: CPIC		
SIZE: B	DWG NO: 453503	REV: 1.1
DATE: 2-22-2012_11:11	SHEET 2 of 34	

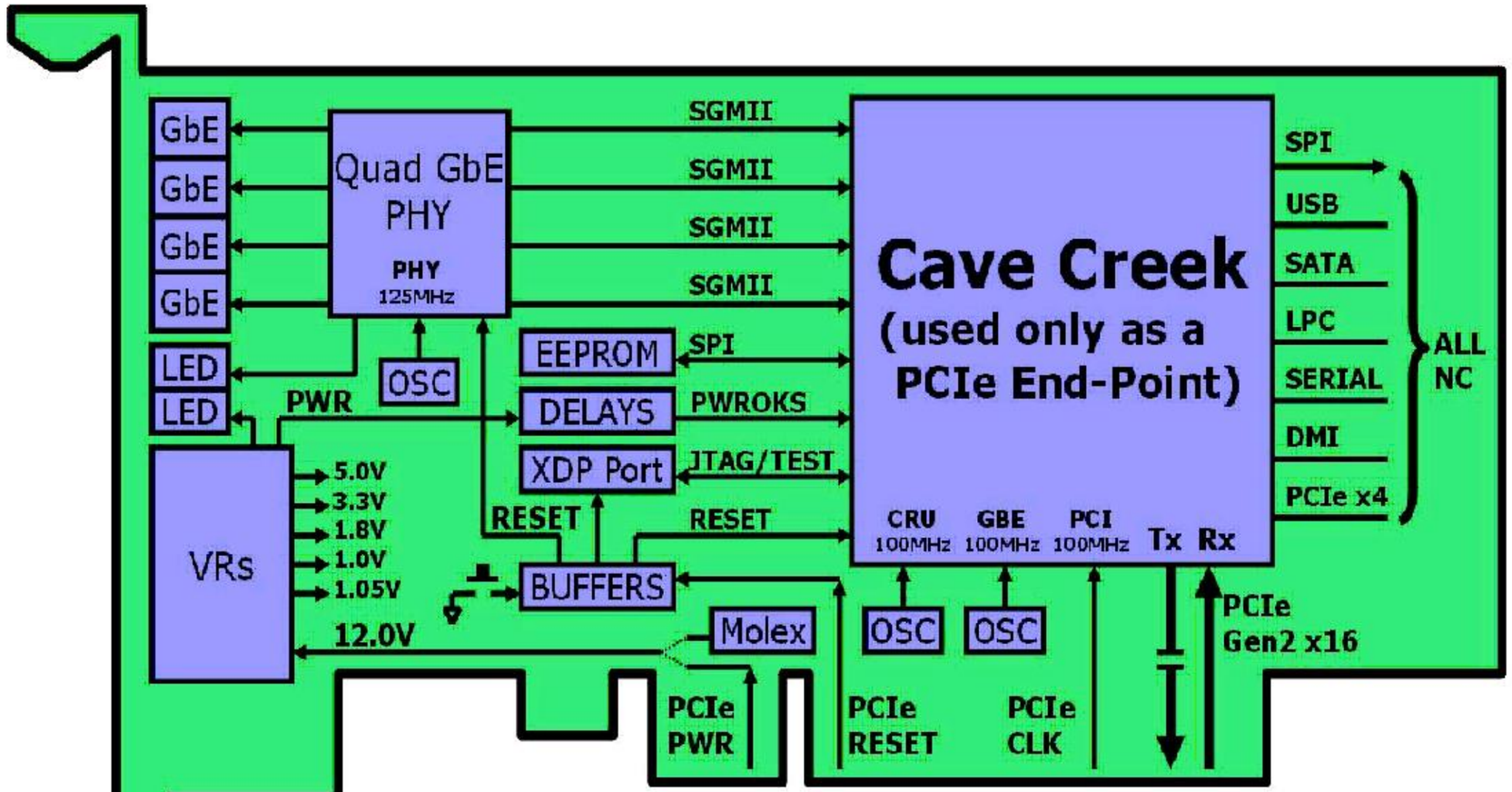
TABLE OF CONTENTS

INTEL CONFIDENTIAL

Prepared For:
Intel Corporation
5000 W. Chandler Blvd
Chandler, AZ 85226
www.intel.com

Prepared By:
ADI Engineering, Inc.
1758 Worth Park
Charlottesville, VA 22911
www.adiengineering.com

TITLE	CPIC	
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 3 of 34	



CPIC Design Requirements:

- Form Factor: shall comply with standard Height/ Half Length per PCI-Express* Gen II specification
- Backplane: shall operate in x16 slot standard mechanical environment and (x1, x4, x8) slot with adapter
- Front Panel: shall provide four 10/100/1000 Ethernet RJ-45 connectors utilizing all Cave Creek 1GbE ports
- Memory: shall support a EEPROM for storing configuration information for all four Ethernet MACs.
- Validation: shall support an XDP port for debug and test, including headers for supplies and key signals.
- Voltage: shall operate using 12V and 3V as defined by the PCI-express Generation II Base Specification.
- Power: shall have a maximum thermal budget of 15W @ 55ºC

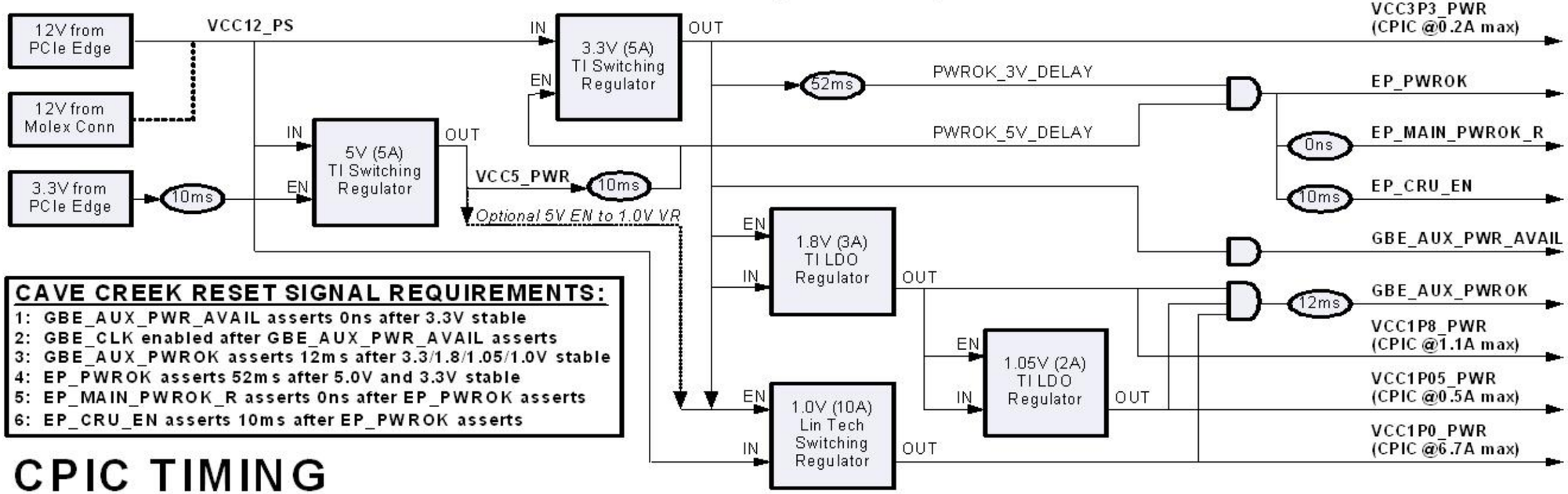
CPIC BLOCK DIAGRAM & REQUIREMENTS (3/17/10)

CPIC BLOCK DIAGRAM

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 4 of 34	

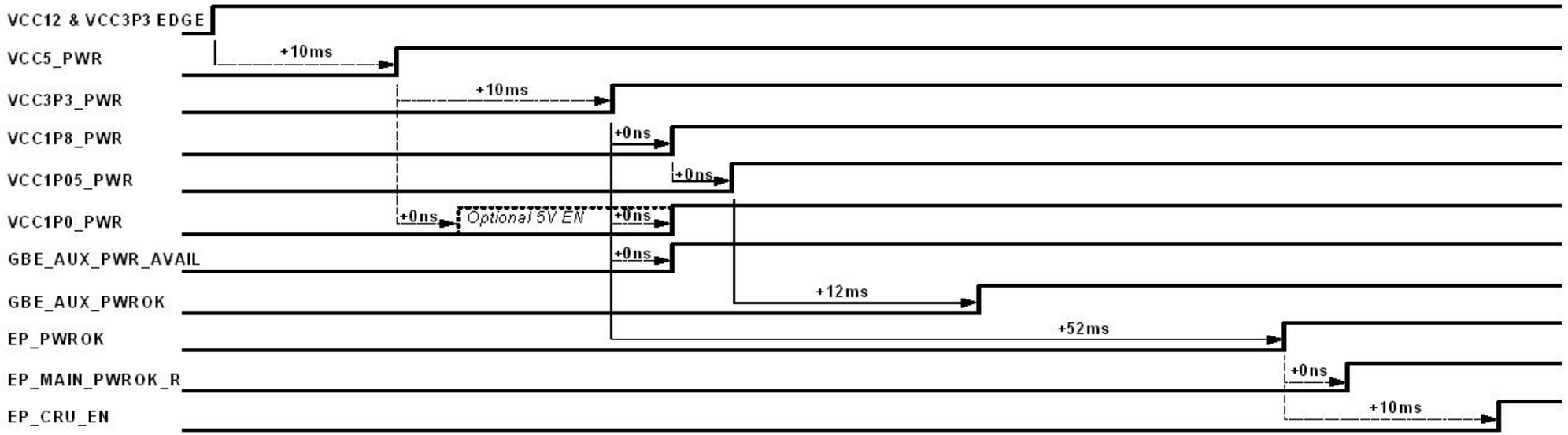
CPIC POWER-ON SEQUENCE (1/5/11)



CAVE CREEK RESET SIGNAL REQUIREMENTS:

1: GBE_AUX_PWR_AVAIL asserts 0ns after 3.3V stable
2: GBE_CLK enabled after GBE_AUX_PWR_AVAIL asserts
3: GBE_AUX_PWROK asserts 12ms after 3.3/1.8/1.05/1.0V stable
4: EP_PWROK asserts 52ms after 5.0V and 3.3V stable
5: EP_MAIN_PWROK_R asserts 0ns after EP_PWROK asserts
6: EP_CRU_EN asserts 10ms after EP_PWROK asserts

CPIC TIMING



CPIC POWER-ON SEQUENCE

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 5 of 34	

CLOCKS & PCIE X16 INTERFACE

BLANK

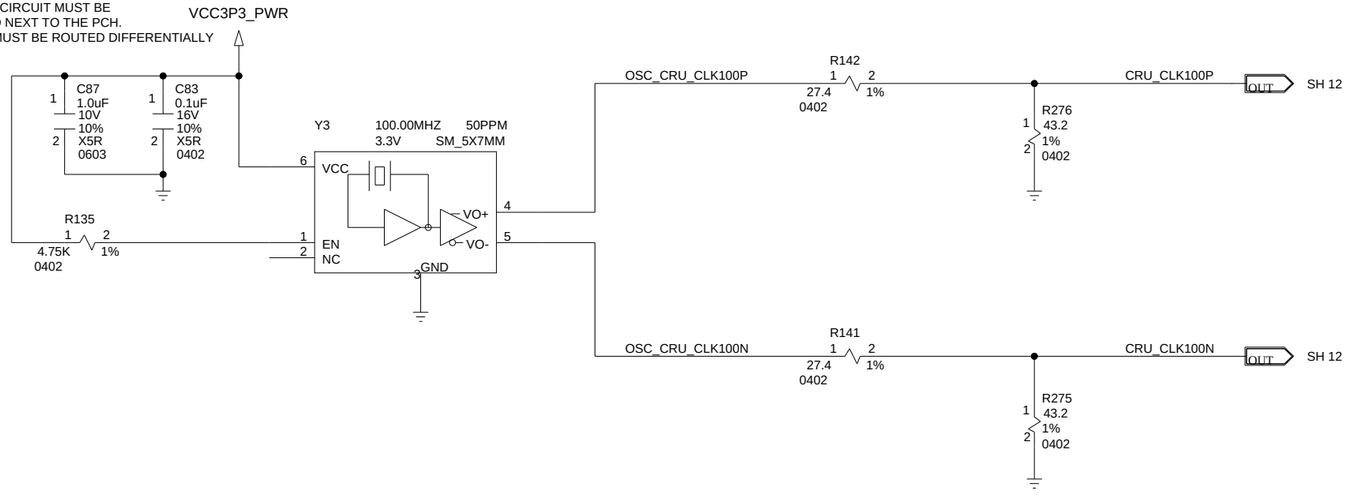
INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 6 of 34	

CRU CLOCK CIRCUIT (50PPM OSC.)

CAD NOTE:
* THIS OSC CIRCUIT MUST BE PLACED NEXT TO THE PCH.
* CLOCKS MUST BE ROUTED DIFFERENTIALLY



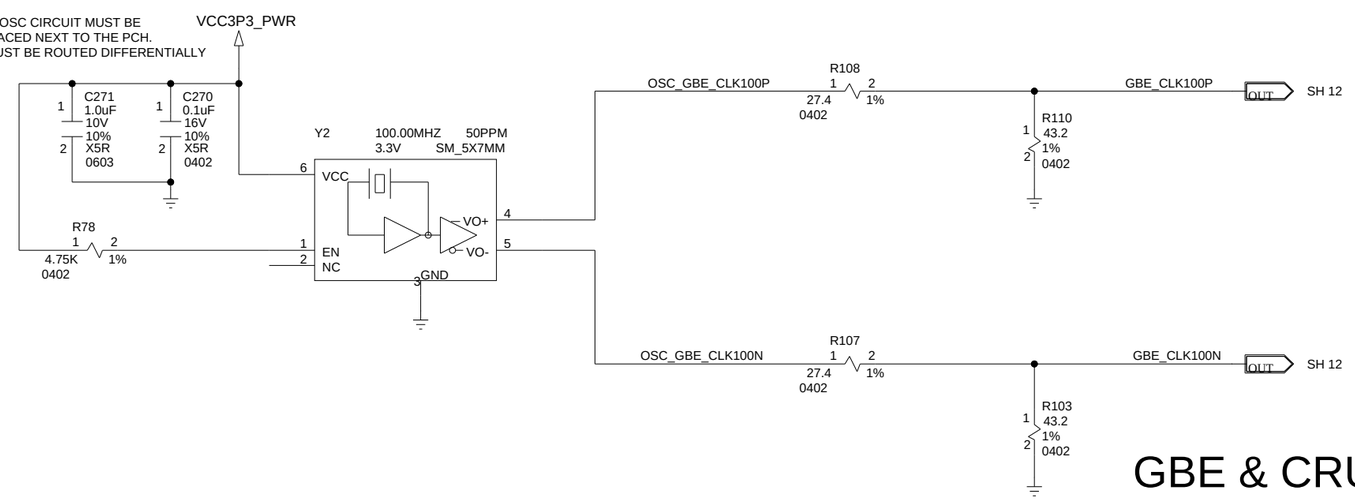
DIFFERENTIAL OUTPUT TERMINATION TABLE

DIF Z0 (OHM)	RS(OHM)	RP(OHM)
85 OHMS *	27	43.2
100 OHMS	33	50

* = DEFAULT

GBE CLOCK CIRCUIT (50PPM OSC.)

CAD NOTE:
* THIS OSC CIRCUIT MUST BE PLACED NEXT TO THE PCH.
* CLOCKS MUST BE ROUTED DIFFERENTIALLY



DIFFERENTIAL OUTPUT TERMINATION TABLE

DIF Z0 (OHM)	RS(OHM)	RP(OHM)
85 OHMS *	27	43.2
100 OHMS	33	50

* = DEFAULT

GBE & CRU CLOCKS

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE			
CPIC			
SIZE: B	DWG NO: 453503		REV: 1.2
DATE: 2-22-2012_11:11	SHEET 7 of 34		

+12V SPARE INPUT USING MOLEX

SU3

2D SERIAL NUMBER LABEL
0.375 X 0.375

C7 22uF 16V 20% X5R 1206

C6 0.1uF 25V 10% X7R 0603

FERRIT BEAD INSTALLATION TABLE

* = DEFAULT

+12V SOURCE	FB1	FB2
FROM PCI EDGE *	DEPOPULATE	INSTALL
FROM MOLEX HDR	INSTALL	DEPOPULATE

VCC12_PS

DNI FB1 BEAD 4.0A 100 OHM 0805

FB2 BEAD 4.0A 100 OHM 0805

J1 4X1 HDD PWR RT ANG TH-0.2

VCC5_SPARE

J3 SINGLE PIN HEADER TH-VERTICAL

J25 SINGLE PIN HEADER TH-VERTICAL

VCC3P3_SPARE OUT SH 21

J26 PCI EXPRESS X16 EDGE FINGERS

A2 12V1 A3 12V2 B1 12V3 B2 12V4 B3 12V5

A9 3.3V1 A10 3.3V2 B8 3.3V3

B10 3.3VAUX

GND1 A4 GND2 A12 GND3 A15 GND4 A18 GND5 A20 GND6 A23 GND7 A24 GND8 A27 GND9 A28 GND10 A31 GND11 A34 GND12 A37 GND13 A38 GND14 A41 GND15 A42 GND16 A45 GND17 A46 GND18 A49 GND19 A51 GND20 A54 GND21 A55 GND22 A58 GND23 A59 GND24 A62 GND25 A63 GND26 A66 GND27 A67 GND28 A70 GND29 A71 GND30 A74 GND31 A75 GND32 A78 GND33 A79 GND34 A82 GND35 B4 GND36 B7 GND37 B13 GND38 B16 GND39 B18 GND40 B21 GND41 B22 GND42 B25 GND43 B26 GND44 B29 GND45 B32 GND46 B35 GND47 B36 GND48 B39 GND49 B40 GND50 B43 GND51 B44 GND52 B47 GND53 B49 GND54 B52 GND55 B53 GND56 B56 GND57 B57 GND58 B60 GND59 B61 GND60 B64 GND61 B65 GND62 B68 GND63 B69 GND64 B72 GND65 B73 GND66 B76 GND67 B77 GND68 B80

PCI EXPRESS X16 EDGE FINGERS

J26 RSVD1 A19, RSVD2 A32, RSVD3 A33, RSVD4 A50 — PCI EXPRESS X16 EDGE FINGERS

J26 RSVD5 B12, RSVD6 B30, RSVD7 B82 — PCI EXPRESS X16 EDGE FINGERS

INSTALL J15 JUMPER
AS THE CPIC DEFAULT

INSTALL GBE_SMB JUMPERS
AS THE CPIC DEFAULT

PCIE_TX_DP_P[0:15] IN SH 9

PCIE_TX_DP_N[0:15] IN SH 9

PCH_RX_DP_P[0:15] OUT SH 11

PCH_RX_DP_N[0:15] OUT SH 11

J26 PCI EXPRESS X16 EDGE FINGERS

RX15P A80, RX15N A81, RX14P A76, RX14N A77, RX13P A72, RX13N A73, RX12P A68, RX12N A69, RX11P A64, RX11N A65, RX10P A60, RX10N A61, RX9P A56, RX9N A57, RX8P A52, RX8N A53, RX7P A47, RX7N A48, RX6P A43, RX6N A44, RX5P A39, RX5N A40, RX4P A35, RX4N A36, RX3P A29, RX3N A30, RX2P A25, RX2N A26, RX1P A21, RX1N A22, RX0P A16, RX0N A17

TX15P B78, TX15N B79, TX14P B74, TX14N B75, TX13P B70, TX13N B71, TX12P B66, TX12N B67, TX11P B62, TX11N B63, TX10P B58, TX10N B59, TX9P B54, TX9N B55, TX8P B50, TX8N B51, TX7P B45, TX7N B46, TX6P B41, TX6N B42, TX5P B37, TX5N B38, TX4P B33, TX4N B34, TX3P B27, TX3N B28, TX2P B23, TX2N B24, TX1P B19, TX1N B20, TX0P B14, TX0N B15

JTAG_TMS A8, JTAG_TDO A7, JTAG_TDI A6, JTAG_TCK A5, JTAG_TRST# B9

PRSNT2_4# B81, PRSNT2_3# B48, PRSNT2_2# B31, PRSNT2_1# B17, PRSNT1# A1

REFCLK+ A13, REFCLK- A14

PERST# A11

SMCLK B5

SMDAT B6

WAKE# B11

PCIE_PRESENT_N

PCIE_EP_CLK100P OUT SH 11

PCIE_EP_CLK100N OUT SH 11

PCIE_RESET_N OUT SH 24

PCIE_SMCLK

PCIE_SMDAT

NOTE:
WAKE_N NOT USED.
WOL NOT SUPPORTED.

J22, J19, J17, J15 — 2X1 VERTICAL TH-0.1

J16, J18, J20, J12 — 2X1 VERTICAL TH-0.1

ID_SMBCLK

ID_SMBDAT

GBE_SMBCLK OUT SH 12,19

GBE_SMBDAT BI SH 12,19

VCC3P3_PWR

PLACE RES ON TOP SIDE

C315 0.1uF 25V 10% X7R 0603

R153 4.75K 1% 0603

R154 4.75K 1% 0603

U22 AT24HC02BN SOIC8

VCC, A0, A1, A2, SDA, SCL, WP, GND

MODULE_A0

MODULE_A1

MODULE_A2

DNI R134 1.00K 1% 0603

DNI R132 1.00K 1% 0603

DNI R127 1.00K 1% 0603

R133 10.0K 1% 0603

R131 10.0K 1% 0603

R126 10.0K 1% 0603

CPIC MODULE ID EEPROM
SMBUS ADDRESS = 0XA0

J24 3X1 VERTICAL TH-0.1

MODULE ID PGM HEADER

J23 2X1 VERTICAL TH-0.1

MODULE_WP

R138 10.0K 1% 0603

OPEN: WRITE ENABLE
(DEFAULT)

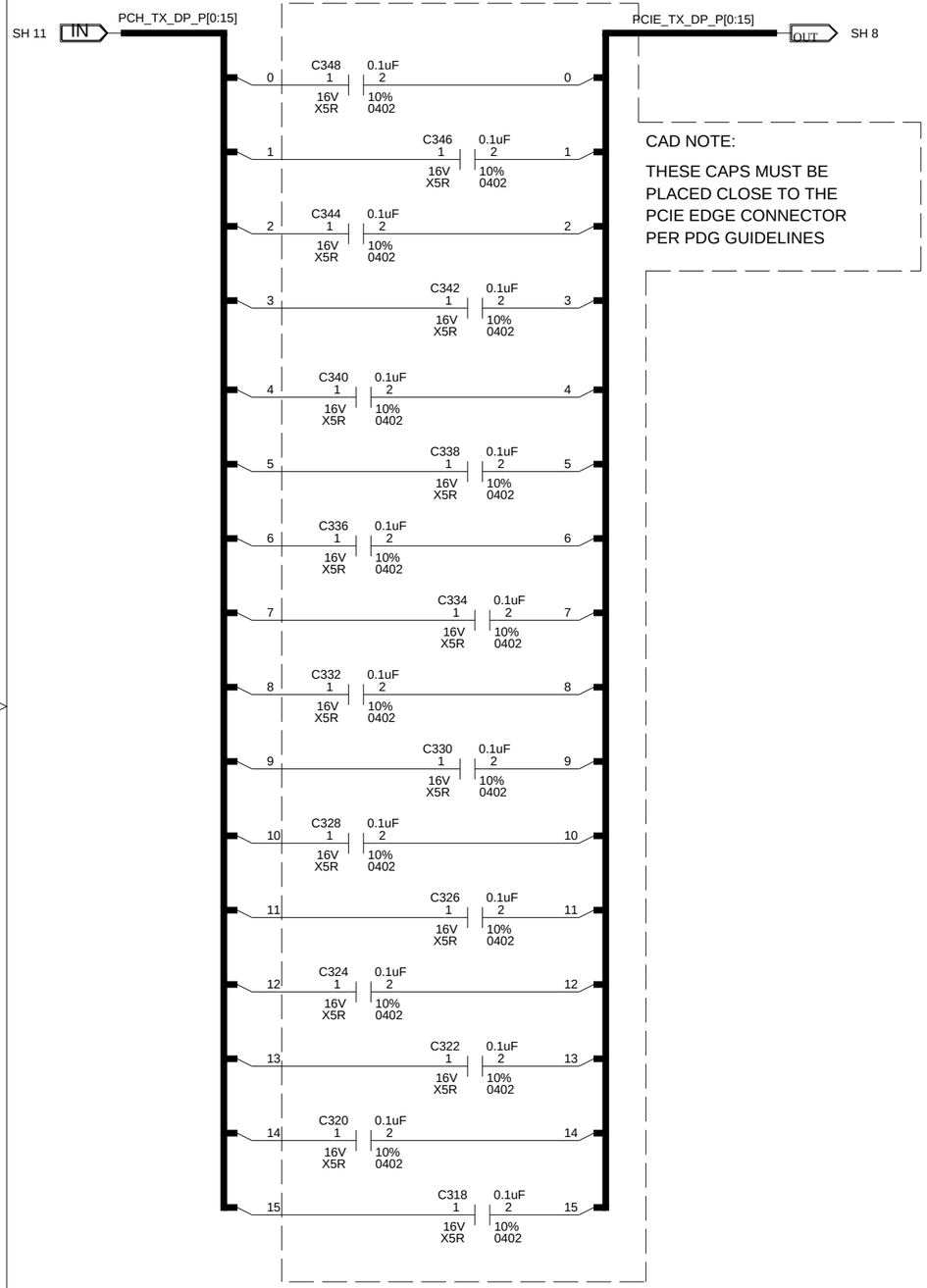
PCIE GEN2
EDGE X16

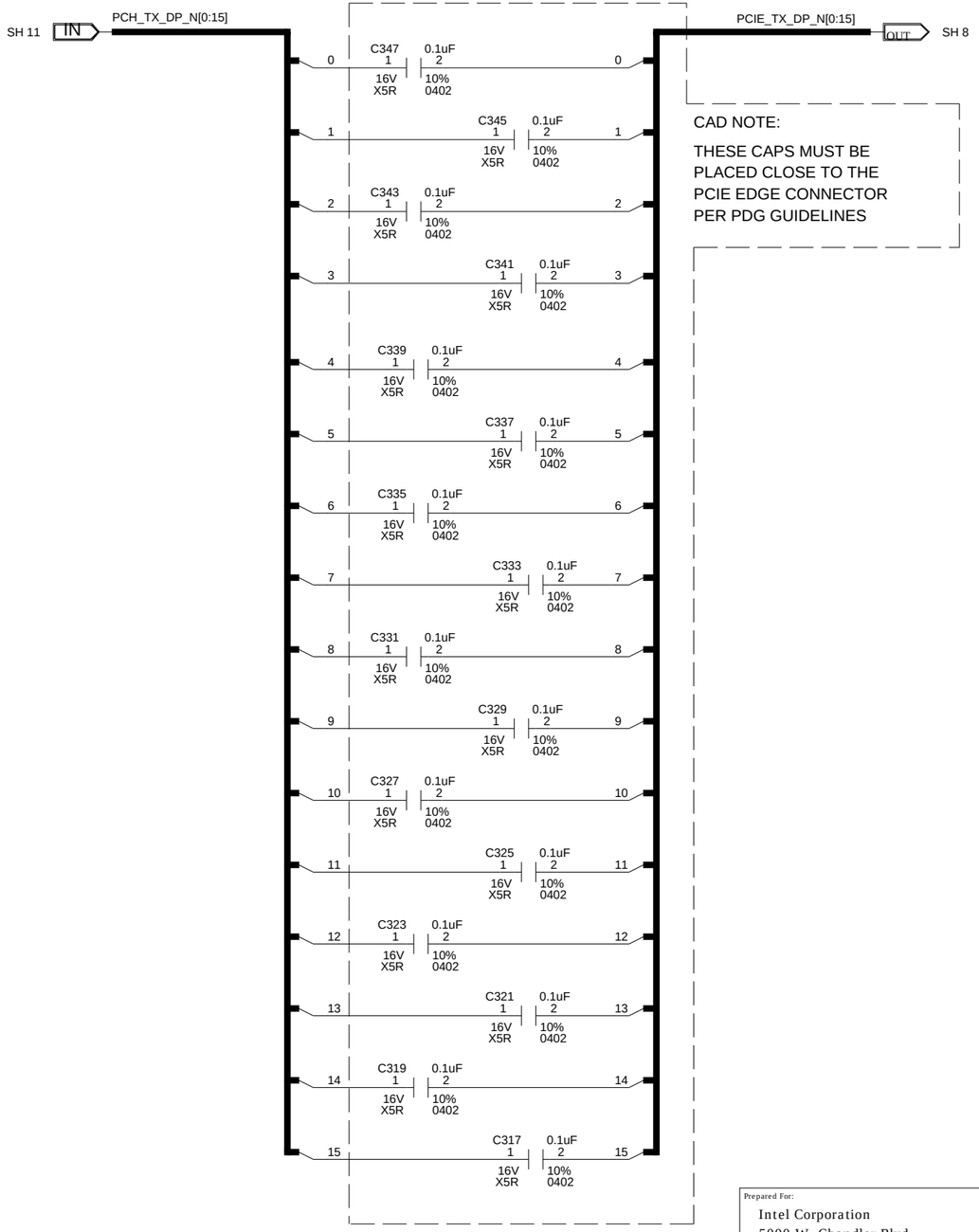
PCIE GEN2 EDGE X16

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE: CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 8 of 34	





PCIE X16 TX AC CAPS

INTEL CONFIDENTIAL

Prepared For: Intel Corporation, 5000 W. Chandler Blvd, Chandler, AZ 85226, www.intel.com	Prepared By: ADI Engineering, Inc., 1758 Worth Park, Charlottesville, VA 22911, www.adiengineering.com
TITLE: CPIC	
SIZE: B	DWG NO: 453503 — REV: 1.2
DATE: 2-22-2012_11:11	SHEET 9 of 34

PCH

BLANK

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE: CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 10 of 34	

NOTE: SOME P/N PAIRS SWAPPED HERE FOR EASE OF LAYOUT

SH 8 IN PCH_RX_DP_P[0:15]

0	PCH_RX_DP_P0	
1	PCH_RX_DP_P1	
2	PCH_RX_DP_P2	
3	PCH_RX_DP_P3	
4	PCH_RX_DP_P4	
5	PCH_RX_DP_P5	
6	PCH_RX_DP_P6	
7	PCH_RX_DP_P7	
8	PCH_RX_DP_P8	
9	PCH_RX_DP_P9	
10	PCH_RX_DP_P10	
11	PCH_RX_DP_P11	
12	PCH_RX_DP_P12	
13	PCH_RX_DP_P13	
14	PCH_RX_DP_P14	
15	PCH_RX_DP_P15	

SH 8 IN PCH_RX_DP_N[0:15]

0	PCH_RX_DP_N0	
1	PCH_RX_DP_N1	
2	PCH_RX_DP_N2	
3	PCH_RX_DP_N3	
4	PCH_RX_DP_N4	
5	PCH_RX_DP_N5	
6	PCH_RX_DP_N6	
7	PCH_RX_DP_N7	
8	PCH_RX_DP_N8	
9	PCH_RX_DP_N9	
10	PCH_RX_DP_N10	
11	PCH_RX_DP_N11	
12	PCH_RX_DP_N12	
13	PCH_RX_DP_N13	
14	PCH_RX_DP_N14	
15	PCH_RX_DP_N15	

VCC1P8_PWR

R257 1 10.5K 1% 2 0402

CAD NOTE:

* PLACE THIS RESISTOR NEAR PCH

U21

PCH_RX_DP_N0	N56	PCIE_EP_RXP0	
PCH_RX_DP_N1	L53	PCIE_EP_RXP1	
PCH_RX_DP_N2	G56	PCIE_EP_RXP2	
PCH_RX_DP_N3	D51	PCIE_EP_RXP3	
PCH_RX_DP_N4	C46	PCIE_EP_RXP4	
PCH_RX_DP_N5	D45	PCIE_EP_RXP5	
PCH_RX_DP_N6	B43	PCIE_EP_RXP6	
PCH_RX_DP_N7	B41	PCIE_EP_RXP7	
PCH_RX_DP_N8	E39	PCIE_EP_RXP8	
PCH_RX_DP_N9	E37	PCIE_EP_RXP9	
PCH_RX_DP_N10	C36	PCIE_EP_RXP10	
PCH_RX_DP_N11	D35	PCIE_EP_RXP11	
PCH_RX_DP_N12	B33	PCIE_EP_RXP12	
PCH_RX_DP_P13	B31	PCIE_EP_RXP13	
PCH_RX_DP_N14	C29	PCIE_EP_RXP14	
PCH_RX_DP_N15	B27	PCIE_EP_RXP15	
PCH_RX_DP_P0	N54	PCIE_EP_RXN0	
PCH_RX_DP_P1	M55	PCIE_EP_RXN1	
PCH_RX_DP_P2	G54	PCIE_EP_RXN2	
PCH_RX_DP_P3	B51	PCIE_EP_RXN3	
PCH_RX_DP_P4	B47	PCIE_EP_RXN4	
PCH_RX_DP_P5	B45	PCIE_EP_RXN5	
PCH_RX_DP_P6	D43	PCIE_EP_RXN6	
PCH_RX_DP_P7	C42	PCIE_EP_RXN7	
PCH_RX_DP_P8	E41	PCIE_EP_RXN8	
PCH_RX_DP_P9	C39	PCIE_EP_RXN9	
PCH_RX_DP_P10	B37	PCIE_EP_RXN10	
PCH_RX_DP_P11	B35	PCIE_EP_RXN11	
PCH_RX_DP_P12	D33	PCIE_EP_RXN12	
PCH_RX_DP_N13	E31	PCIE_EP_RXN13	
PCH_RX_DP_P14	E29	PCIE_EP_RXN14	
PCH_RX_DP_P15	E27	PCIE_EP_RXN15	
SH 8 IN PCIE_EP_CLK100P	R41	PCIE_EP_CLK100P	
SH 8 IN PCIE_EP_CLK100N	U43	PCIE_EP_CLK100N	
PCIE_EP_ICOMPI	U38	PCIE_EP_ICOMPI	
		PCIE_EP_TXP0	R50 PCH_TX_DP_N0
		PCIE_EP_TXP1	M46 PCH_TX_DP_N1
		PCIE_EP_TXP2	M48 PCH_TX_DP_N2
		PCIE_EP_TXP3	K49 PCH_TX_DP_N3
		PCIE_EP_TXP4	H48 PCH_TX_DP_N4
		PCIE_EP_TXP5	H46 PCH_TX_DP_P5
		PCIE_EP_TXP6	J43 PCH_TX_DP_P6
		PCIE_EP_TXP7	H41 PCH_TX_DP_P7
		PCIE_EP_TXP8	M38 PCH_TX_DP_P8
		PCIE_EP_TXP9	J38 PCH_TX_DP_N9
		PCIE_EP_TXP10	J36 PCH_TX_DP_N10
		PCIE_EP_TXP11	P36 PCH_TX_DP_N11
		PCIE_EP_TXP12	J33 PCH_TX_DP_P12
		PCIE_EP_TXP13	R33 PCH_TX_DP_N13
		PCIE_EP_TXP14	J31 PCH_TX_DP_N14
		PCIE_EP_TXP15	P31 PCH_TX_DP_N15
		PCIE_EP_TXN0	R49 PCH_TX_DP_P0
		PCIE_EP_TXN1	R46 PCH_TX_DP_P1
		PCIE_EP_TXN2	M49 PCH_TX_DP_P2
		PCIE_EP_TXN3	K50 PCH_TX_DP_P3
		PCIE_EP_TXN4	H50 PCH_TX_DP_P4
		PCIE_EP_TXN5	J46 PCH_TX_DP_N5
		PCIE_EP_TXN6	L43 PCH_TX_DP_N6
		PCIE_EP_TXN7	J41 PCH_TX_DP_N7
		PCIE_EP_TXN8	P38 PCH_TX_DP_N8
		PCIE_EP_TXN9	H38 PCH_TX_DP_N9
		PCIE_EP_TXN10	H36 PCH_TX_DP_P10
		PCIE_EP_TXN11	M36 PCH_TX_DP_P11
		PCIE_EP_TXN12	L33 PCH_TX_DP_N12
		PCIE_EP_TXN13	P33 PCH_TX_DP_P13
		PCIE_EP_TXN14	H31 PCH_TX_DP_P14
		PCIE_EP_TXN15	M31 PCH_TX_DP_P15
PCIE_EP_CLK100P		PCIE_EP_CLK100P	M41 RSVD61
PCIE_EP_CLK100N		PCIE_EP_CLK100N	P43 RSVD62
		PCIE_EP_ICOMPI	Y44 PCIE_EP_VREF1P8

1 OF 12

CAVE CREEK
BGA942

RSVD61

RSVD62

PCH_TX_DP_P[0:15] OUT SH 9

PCH_TX_DP_P0	0	
PCH_TX_DP_P1	1	
PCH_TX_DP_P2	2	
PCH_TX_DP_P3	3	
PCH_TX_DP_P4	4	
PCH_TX_DP_P5	5	
PCH_TX_DP_P6	6	
PCH_TX_DP_P7	7	
PCH_TX_DP_P8	8	
PCH_TX_DP_P9	9	
PCH_TX_DP_P10	10	
PCH_TX_DP_P11	11	
PCH_TX_DP_P12	12	
PCH_TX_DP_P13	13	
PCH_TX_DP_P14	14	
PCH_TX_DP_P15	15	

PCH_TX_DP_N[0:15] OUT SH 9

PCH_TX_DP_N0	0	
PCH_TX_DP_N1	1	
PCH_TX_DP_N2	2	
PCH_TX_DP_N3	3	
PCH_TX_DP_N4	4	
PCH_TX_DP_N5	5	
PCH_TX_DP_N6	6	
PCH_TX_DP_N7	7	
PCH_TX_DP_N8	8	
PCH_TX_DP_N9	9	
PCH_TX_DP_N10	10	
PCH_TX_DP_N11	11	
PCH_TX_DP_N12	12	
PCH_TX_DP_N13	13	
PCH_TX_DP_N14	14	
PCH_TX_DP_N15	15	

DNI R128 1 2 0 JMPR 0603

DNI R121 1 2 0 JMPR 0603

CAD NOTE:

THESE RESISTORS MUST BE ACCESSIBLE FOR PROBING.

VCC1P8_PWR

PCIE_EP_VREF1P8

R258 1 2 0 JMPR 0603

C81 1 2 1.0uF 6.3V 20% X5R 0402

C80 1 2 22UF 6.3V 20% X5R 0805

CAD NOTE:

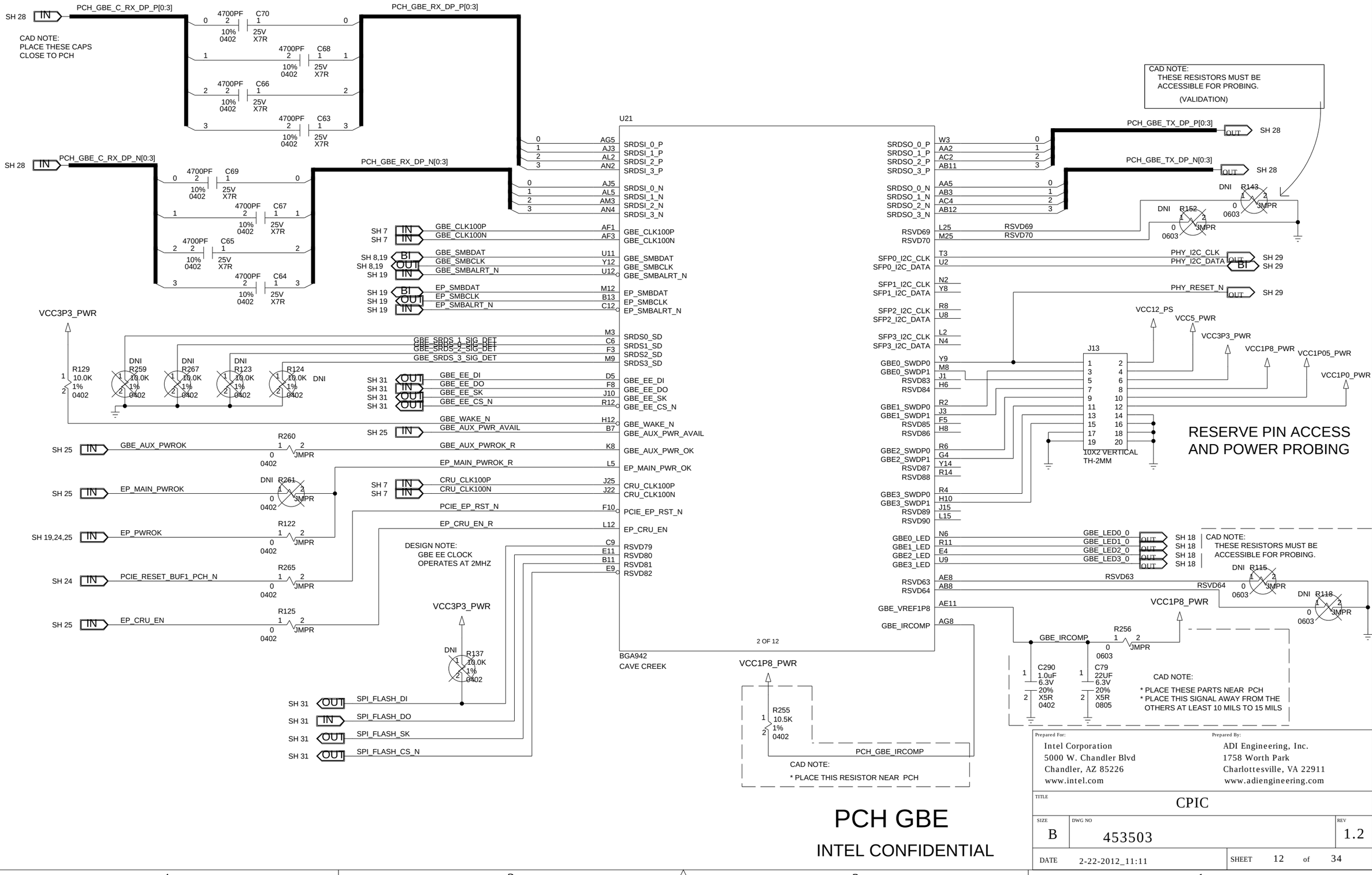
* PLACE THESE PARTS NEAR PCH
* PLACE THIS SIGNAL AWAY FROM THE OTHERS AT LEAST 10 MILS TO 15 MILS

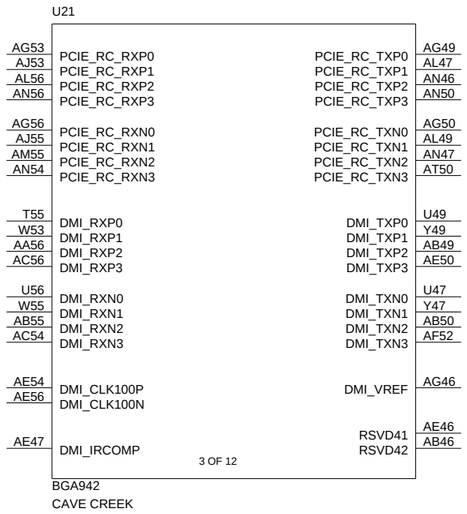
PCH PCIE

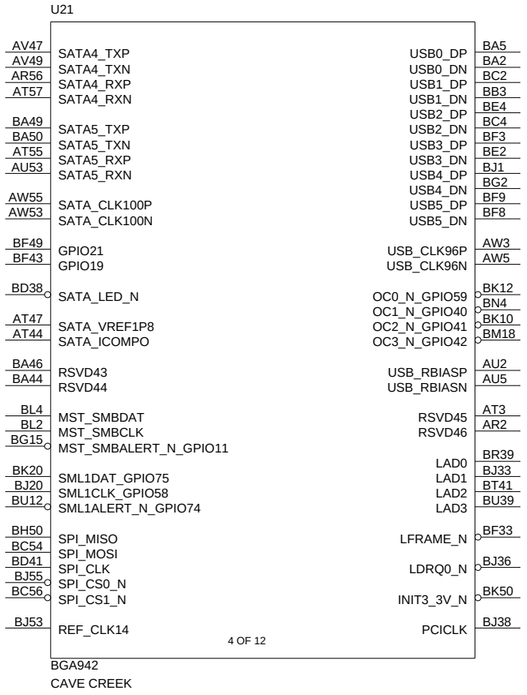
INTEL CONFIDENTIAL

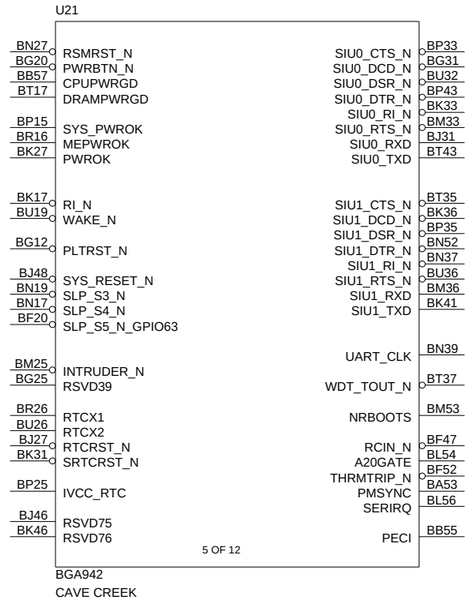
Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

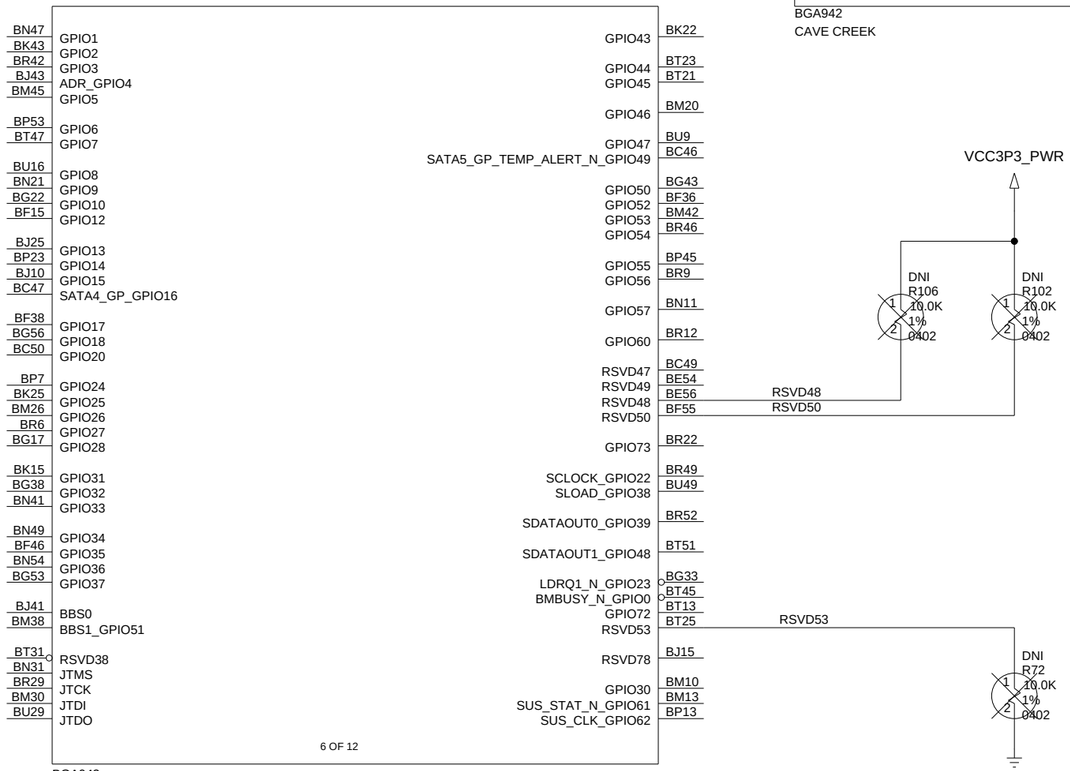
TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 11 of 34	


PCH_GBE_C_RX_DP_P[0:3]
PCH_GBE_RX_DP_P[0:3]
CAD NOTE:
PLACE THESE CAPS
CLOSE TO PCH
4700PF C70
4700PF C68
4700PF C66
4700PF C63
10% 0402 25V X7R
PCH_GBE_C_RX_DP_N[0:3]
PCH_GBE_RX_DP_N[0:3]
4700PF C69
4700PF C67
4700PF C65
4700PF C64
U21
SRDSI_0_P
SRDSI_1_P
SRDSI_2_P
SRDSI_3_P
SRDSI_0_N
SRDSI_1_N
SRDSI_2_N
SRDSI_3_N
GBE_CLK100P
GBE_CLK100N
GBE_SMBDAT
GBE_SMBCLK
GBE_SMBALRT_N
EP_SMBDAT
EP_SMBCLK
EP_SMBALRT_N
GBE_SRDS_1_SIG_DET
GBE_SRDS_2_SIG_DET
GBE_SRDS_3_SIG_DET
SRDS0_SD
SRDS1_SD
SRDS2_SD
SRDS3_SD
GBE_EE_DI
GBE_EE_DO
GBE_EE_SK
GBE_EE_CS_N
GBE_WAKE_N
GBE_AUX_PWR_AVAIL
GBE_AUX_PWROK_R
EP_MAIN_PWROK_R
CRU_CLK100P
CRU_CLK100N
PCIE_EP_RST_N
EP_CRU_EN_R
RSVD79
RSVD80
RSVD81
RSVD82
DESIGN NOTE:
GBE EE CLOCK
OPERATES AT 2MHZ
VCC3P3_PWR
R129 10.0K 1% 0402
DNI R259 10.0K 1% 0402
DNI R267 10.0K 1% 0402
DNI R123 10.0K 1% 0402
DNI R124 10.0K 1% 0402
R260 0 JMPR 0402
DNI R261 0 JMPR 0402
R122 0 JMPR 0402
R265 0 JMPR 0402
R125 0 JMPR 0402
DNI R137 10.0K 1% 0402
GBE_AUX_PWROK
EP_MAIN_PWROK
EP_PWROK
PCIE_RESET_BUF1_PCH_N
EP_CRU_EN
SPI_FLASH_DI
SPI_FLASH_DO
SPI_FLASH_SK
SPI_FLASH_CS_N
BGA942
CAVE CREEK
2 OF 12
VCC1P8_PWR
R255 10.5K 1% 0402
PCH_GBE_IRCOMP
CAD NOTE:
* PLACE THIS RESISTOR NEAR PCH
CAD NOTE:
THESE RESISTORS MUST BE
ACCESSIBLE FOR PROBING.
(VALIDATION)
PCH_GBE_TX_DP_P[0:3]
PCH_GBE_TX_DP_N[0:3]
DNI R143 0 JMPR 0603
DNI R152 0 JMPR 0603
PHY_I2C_CLK
PHY_I2C_DATA
PHY_RESET_N
VCC12_PS
VCC5_PWR
VCC3P3_PWR
VCC1P8_PWR
VCC1P05_PWR
VCC1P0_PWR
J13
10X2 VERTICAL TH-2MM
RESERVE PIN ACCESS AND POWER PROBING
GBE_LED0_0
GBE_LED1_0
GBE_LED2_0
GBE_LED3_0
DNI R115 0 JMPR 0603
DNI R118 0 JMPR 0603
R256 0 JMPR 0603
C290 1.0uF 6.3V 20% X5R 0402
C79 22UF 6.3V 20% X5R 0805
CAD NOTE:
* PLACE THESE PARTS NEAR PCH
* PLACE THIS SIGNAL AWAY FROM THE OTHERS AT LEAST 10 MILS TO 15 MILS
Prepared For:
Intel Corporation
5000 W. Chandler Blvd
Chandler, AZ 85226
www.intel.com
Prepared By:
ADI Engineering, Inc.
1758 Worth Park
Charlottesville, VA 22911
www.adiengineering.com
TITLE
CPIC
SIZE B
DWG NO 453503
REV 1.2
DATE 2-22-2012_11:11
SHEET 12 of 34
PCH GBE
INTEL CONFIDENTIAL









PCH UNUSED SIGNALS

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com
TITLE: CPIC	
SIZE: B	DWG NO: 453503
REV: 1.2	
DATE: 2-22-2012_11:11	SHEET 13 of 34

CAD NOTE:
THESE RESISTORS MUST
BE PLACED CLOSE TO PCH.

SH 19 OUT XDP1_RSVD10 — R117 1 2 22.6 1% 0402 — EP_RSVD10
SH 19 OUT XDP1_RSVD11 — R147 1 2 22.6 1% 0402 — EP_RSVD11
SH 19 OUT XDP1_RSVD12 — R116 1 2 22.6 1% 0402 — EP_RSVD12
SH 19 OUT XDP1_RSVD13 — R148 1 2 22.6 1% 0402 — EP_RSVD13
SH 19 OUT XDP1_RSVD14 — R139 1 2 22.6 1% 0402 — EP_RSVD14
SH 19 OUT XDP1_RSVD15 — R140 1 2 22.6 1% 0402 — EP_RSVD15
SH 19 OUT XDP1_RSVD16 — R130 1 2 22.6 1% 0402 — EP_RSVD16
SH 19 OUT XDP1_RSVD17 — R274 1 2 22.6 1% 0402 — EP_RSVD17
SH 19 OUT XDP1_RSVD18 — R281 1 2 22.6 1% 0402 — EP_RSVD18

U21

E2	RSVD0	
B5	RSVD1	
B2	RSVD2	
F1	RSVD3	
D1	RSVD4	
B15	RSVD5	
C4	RSVD6	
H17	RSVD7	
A6	RSVD8	
F18	RSVD9	
M17	RSVD10	
B17	RSVD11	
P17	RSVD12	
C16	RSVD13	
J20	RSVD14	
M20	RSVD15	
F13	RSVD16	
H22	RSVD17	
F22	RSVD18	
BP1	RSVD65	
BM1	RSVD66	
BP3	RSVD67	
BN2	RSVD68	
P25	RSVD71	
L27	RSVD72	
BT33	RSVD77	
M15	EP_JTDO	
Y15	EP_JTDI	
J17	EP_JTMS	
A12	EP_JTCK	
D13	EP_JTRST_N	

RSVD71 — C316 100pF 50V 5% NPO 0402
RSVD72 — R262 1.00K 1% 0402

F23	RSVD19	
R20	RSVD20	
B21	RSVD21	
D15	RSVD22	
D23	RSVD23	
L20	RSVD24	
B23	RSVD25	
E17	RSVD26	
A22	RSVD27	
C19	RSVD28	
B25	RSVD29	
F20	RSVD30	
D25	RSVD31	
H27	RSVD32	
M22	RSVD33	
E21	RSVD34	
H25	RSVD35	
D55	RSVD51	
C54	RSVD52	
D53	TS0_IREF_N	
E56	RSVD54	
D57	RSVD55	
BU6	RSVD56	
BT5	RSVD57	
BH9	TS1_IREF_N	
BU4	RSVD59	
BP5	RSVD60	
BM5	RSVD73	
BH8	RSVD74	
R15	RSVD36	
U15	RSVD37	

7 OF 12

BGA942
CAVE CREEK

TS0_IREF_N — R136 8.06K 1% 0402
TS1_IREF_N — R254 8.06K 1% 0402

CAD NOTE:
THESE RESISTORS MUST
BE PLACED CLOSE TO PCH.

EP_RSVD19 — R144 1 2 22.6 1% 0402 — XDP1_RSVD19 OUT SH 19
EP_RSVD20 — R268 1 2 22.6 1% 0402 — XDP1_RSVD20 OUT SH 19
EP_RSVD21 — R146 1 2 22.6 1% 0402 — XDP1_RSVD21 OUT SH 19
EP_RSVD22 — R279 1 2 22.6 1% 0402 — XDP1_RSVD22 OUT SH 19
EP_RSVD23 — R283 1 2 22.6 1% 0402 — XDP1_RSVD23 OUT SH 19
EP_RSVD24 — R270 1 2 22.6 1% 0402 — XDP1_RSVD24 OUT SH 19
EP_RSVD25 — R145 1 2 22.6 1% 0402 — XDP1_RSVD25 OUT SH 19
EP_RSVD26 — R280 1 2 22.6 1% 0402 — XDP1_RSVD26 OUT SH 19
EP_RSVD27 — R282 1 2 22.6 1% 0402 — XDP1_RSVD27 OUT SH 19

VCC1P0_PWR
DNI R149 1.00K 1% 0402

PCH_JTAG_EN — OUT SH 19
R150 1.00K 1% 0603

SH 19 OUT PCH_EP_XDP_TDO

VCC1P0_PWR
R114 51 5% 0402
SH 19 IN PCH_EP_XDP_TDI

VCC1P0_PWR
R119 51 5% 0402
SH 19 IN PCH_EP_XDP_TMS

SH 19 IN PCH_EP_XDP_TCK0
R278 51 5% 0402

CAD NOTE:
THE PD/PU RESISTOR MUST
BE PLACED CLOSE TO PCH.

PCH PCIE

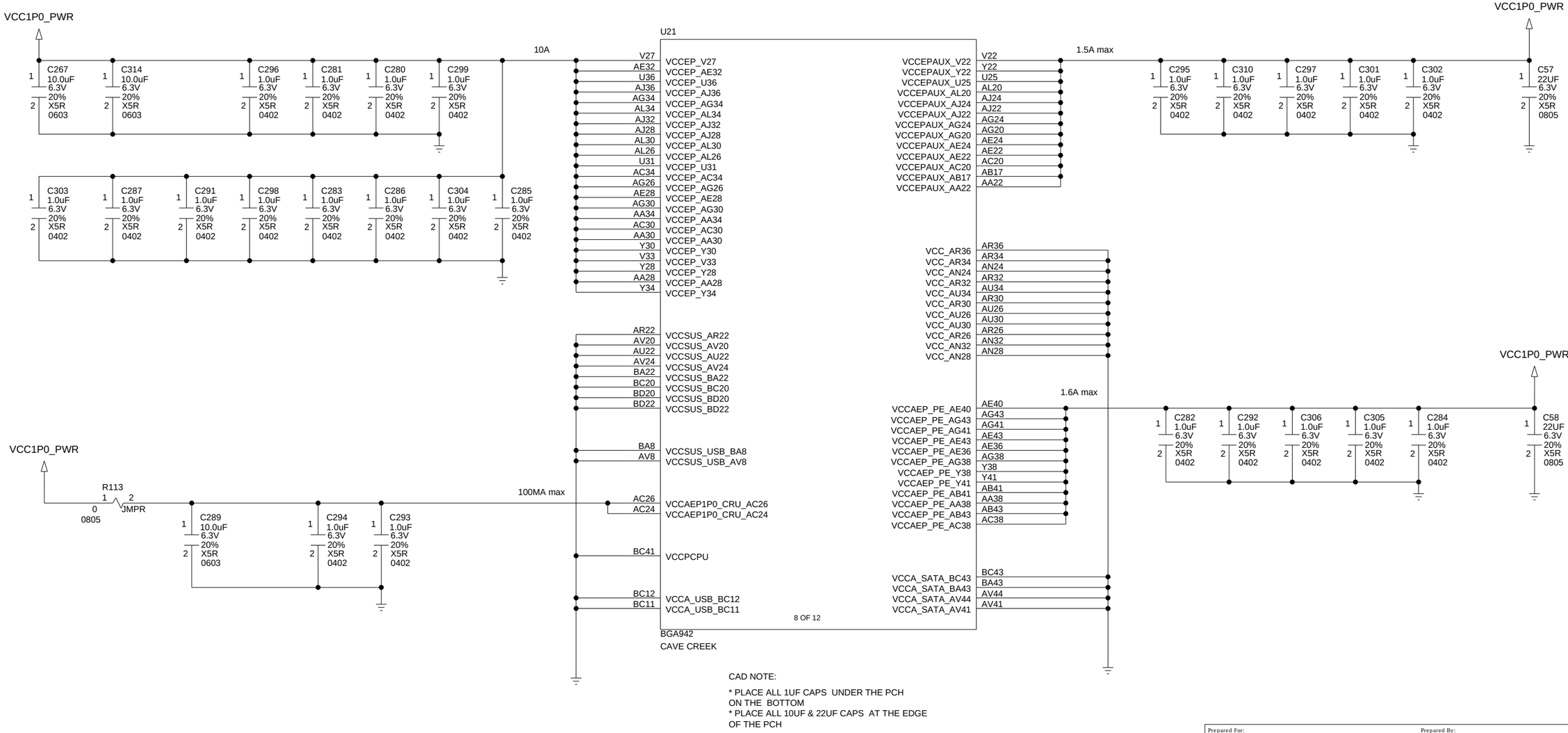
INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE: CPIC

SIZE	DWG NO	REV
B	453503	1.2

DATE 2-22-2012_11:11 — SHEET 14 of 34



CAD NOTE:

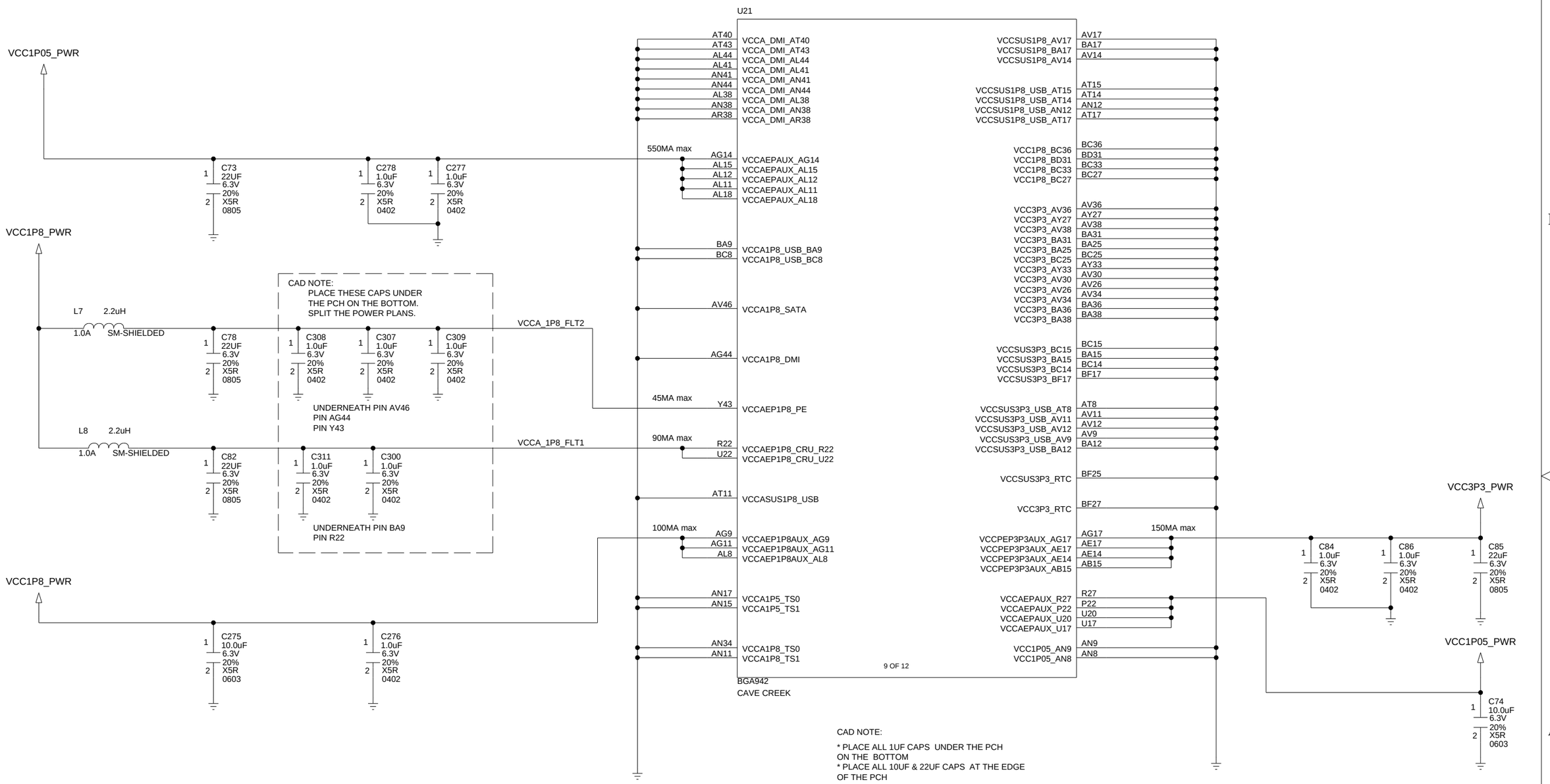
* PLACE ALL 1UF CAPS UNDER THE PCH ON THE BOTTOM
* PLACE ALL 10UF & 22UF CAPS AT THE EDGE OF THE PCH

PCH POWER & FILTERS

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:13	SHEET 15 of 34	

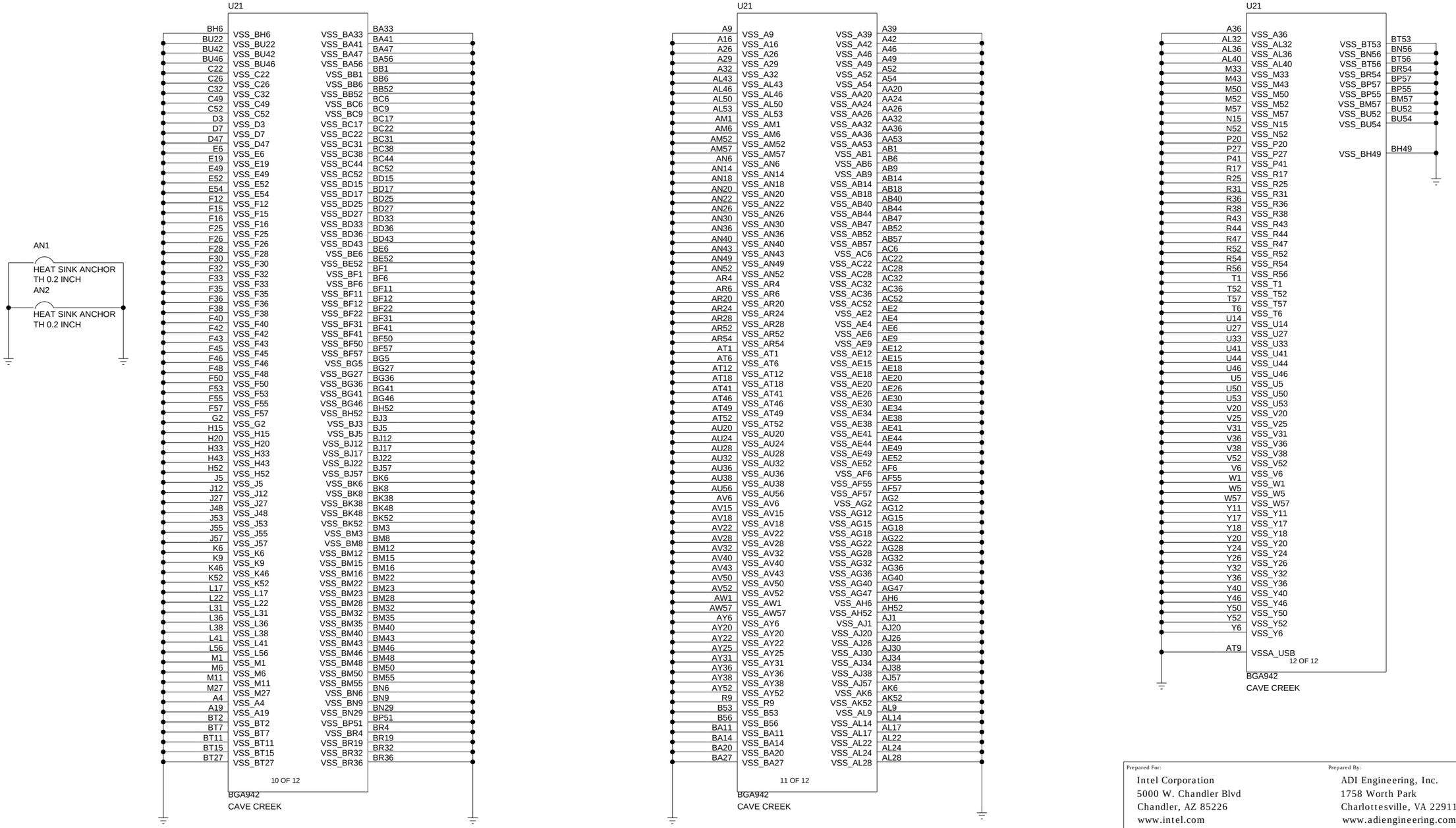


PCH POWER & FILTERS

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE: CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:22	SHEET 16 of 34	



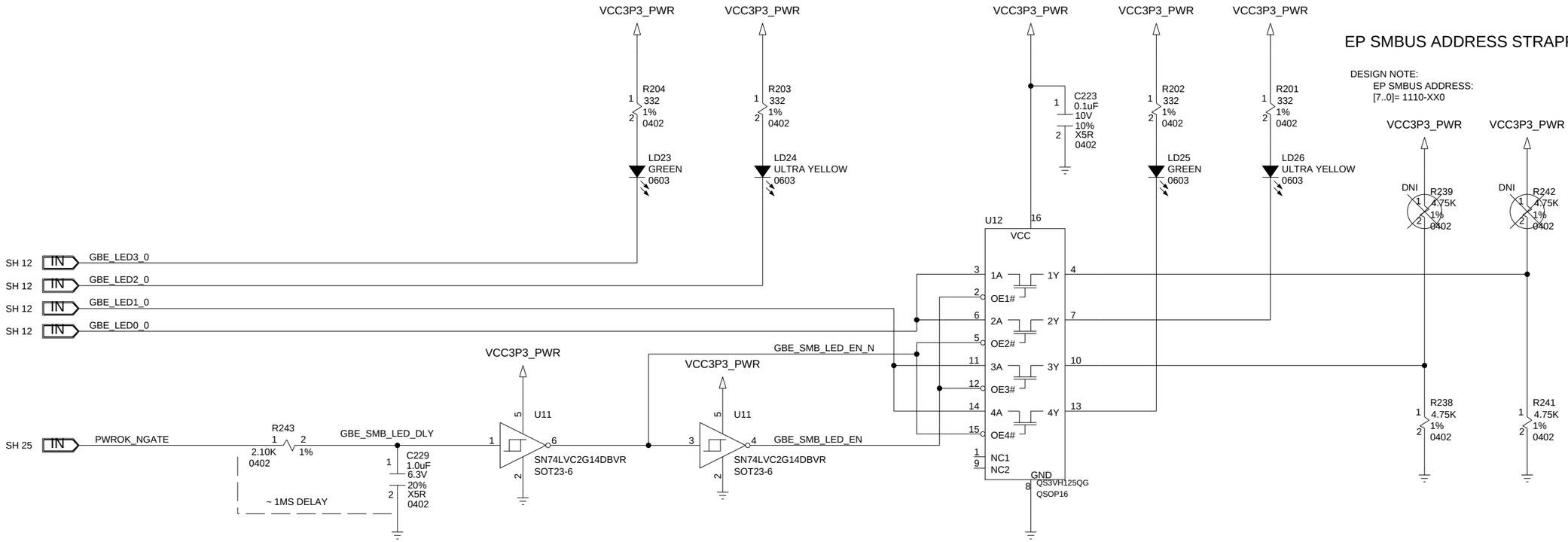
PCH GROUND

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 17 of 34	

GBE POWER LEDS



EP SMBUS ADDRESS STRAPPING

DESIGN NOTE:
EP SMBUS ADDRESS:
[7..0]= 1110-XX0

PCH GBE POWER LEDS

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE: CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 18 of 34	

XDP1 (PCH)

VCC1P05_PWR

R264 1 2 0 JMPR 0603

XDP1_VCC1P05_P43

VCC1P05_PWR

R263 1 2 0 JMPR 0603

XDP1_VCC1P05_P44

J14

30X2 VERTICAL SM-0.5MM

SH 14 IN	XDP1_RSVD10	1 2	XDP1_RSVD18 IN SH 14
SH 14 IN	XDP1_RSVD11	3 4	XDP1_RSVD19 IN SH 14
SH 14 IN	XDP1_RSVD12	5 6	XDP1_RSVD20 IN SH 14
SH 14 IN	XDP1_RSVD13	7 8	XDP1_RSVD21 IN SH 14
SH 14 IN	XDP1_RSVD14	9 10	XDP1_RSVD22 IN SH 14
SH 14 IN	XDP1_RSVD15	11 12	XDP1_RSVD23 IN SH 14
SH 14 IN	XDP1_RSVD16	13 14	XDP1_RSVD24 IN SH 14
SH 14 IN	XDP1_RSVD17	15 16	XDP1_RSVD25 IN SH 14
		17 18	XDP1_RSVD26 IN SH 14
		19 20	XDP1_RSVD27 IN SH 14
		21 22	
		23 24	
		25 26	
		27 28	
		29 30	
		31 32	
		33 34	
		35 36	
		37 38	
		39 40	
		41 42	
		43 44	
		45 46	
		47 48	
		49 50	
		51 52	
		53 54	
		55 56	
		57 58	
		59 60	

SH 12,24,25 IN EP_PWROK

SH 12 BI EP_SMBDAT

SH 12 BI EP_SMBCLK

R272 1 2 0 JMPR 0402

R271 1 2 0 JMPR 0402

XDP1_SMB_DAT

XDP1_SMB_CLK

SH 14 OUT PCH_EP_XDP_TCK0

XDP1_PCIE_RESET_N

XDP1_DBRST_N OUT SH 24

R266 1 2 1.00K 1% 0402

PCIE_RESET_BUF2_XDP_N IN SH 24

PCH_EP_XDP_TDO

PCH_JTAG_EN

PCH_EP_XDP_TDI IN SH 14

PCH_EP_XDP_TMS OUT SH 14

PD_XDP1_PRESENT_N OUT SH 14

R269 1 0 2 JMPR 0402

VCC1P0_PWR

R273 1 51 2 5% 0402

IN SH 14

CAD NOTE:
PLACE THIS PU RESISTOR
CLOSE TO THE XDP CONN.

EP SMBUS

VCC3P3_PWR

R75 1 4.75K 1% 2 0402

R79 1 4.75K 1% 2 0402

R104 1 4.75K 1% 2 0402

SH 12 BI EP_SMBALRT_N

J9

4X1 VERTICAL TH-0.1

1	
2	
3	
4	

GBE SMBUS

VCC3P3_PWR

R76 1 4.75K 1% 2 0402

R80 1 4.75K 1% 2 0402

R105 1 4.75K 1% 2 0402

SH 12 BI GBE_SMBALRT_N

SH 8,12 IN GBE_SMBCLK

SH 8,12 BI GBE_SMBDAT

J10

4X1 VERTICAL TH-0.1

1	
2	
3	
4	

INTEL CONFIDENTIAL

PCH SMBUS & XDP1

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE: CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 19 of 34	

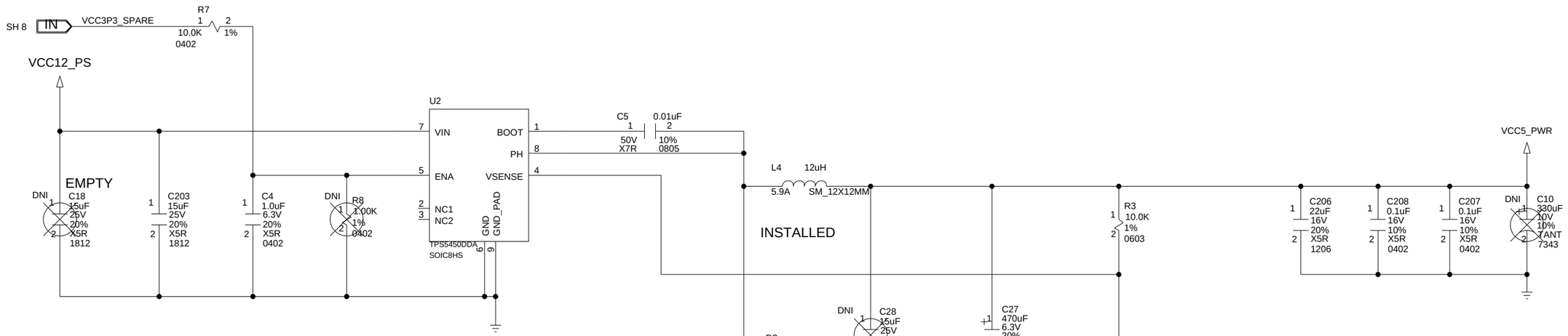
POWER GOOD & SUPPLY

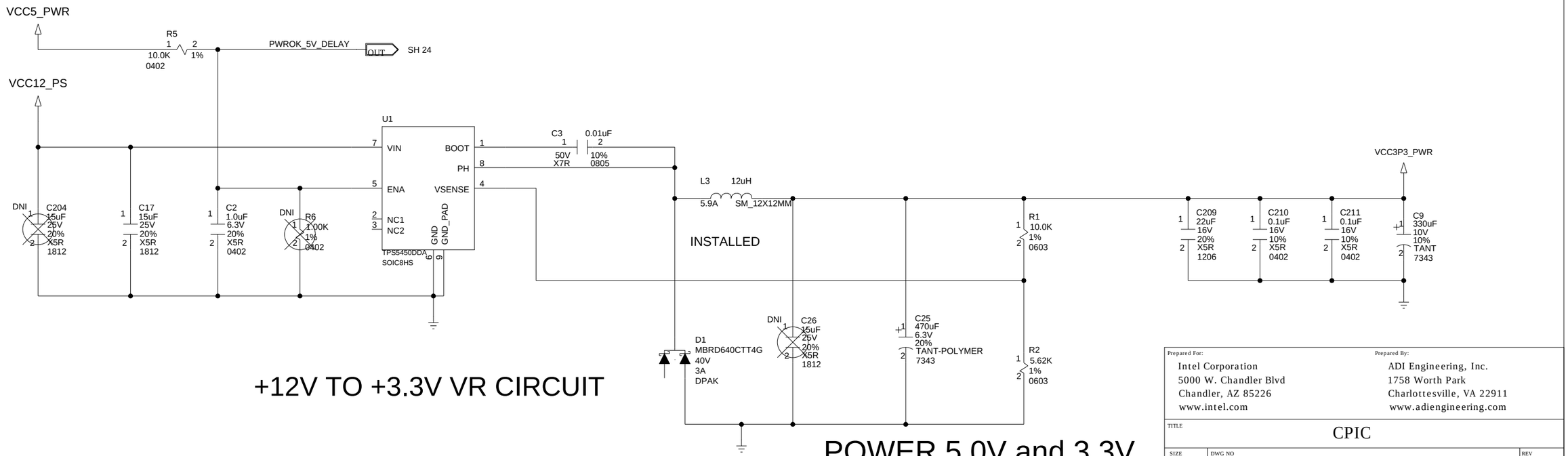
BLANK

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 20 of 34	





POWER 5.0V and 3.3V

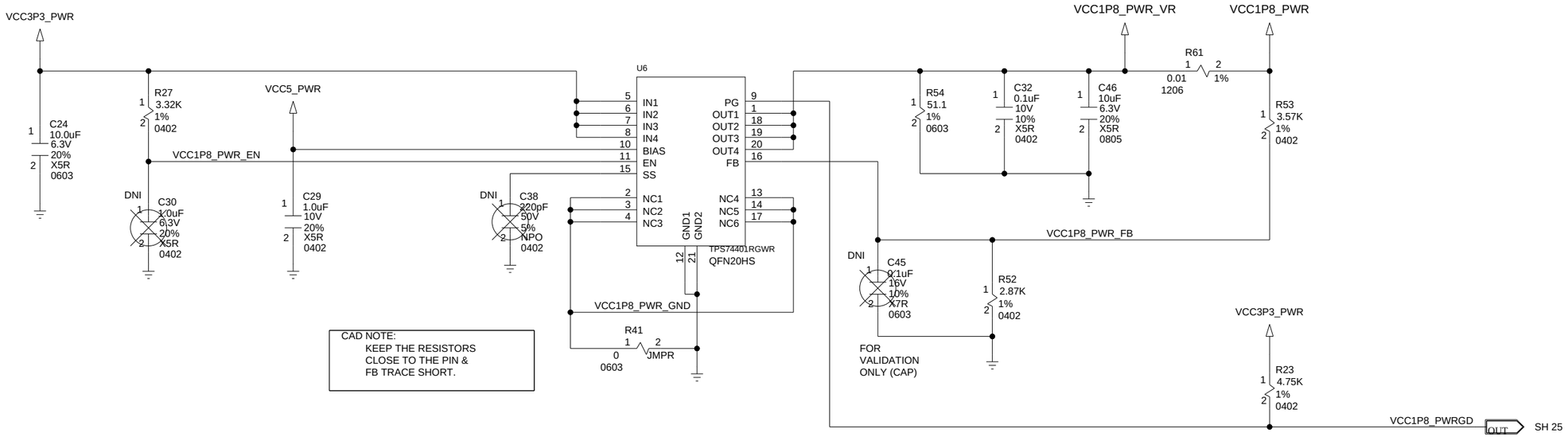
INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 21 of 34	

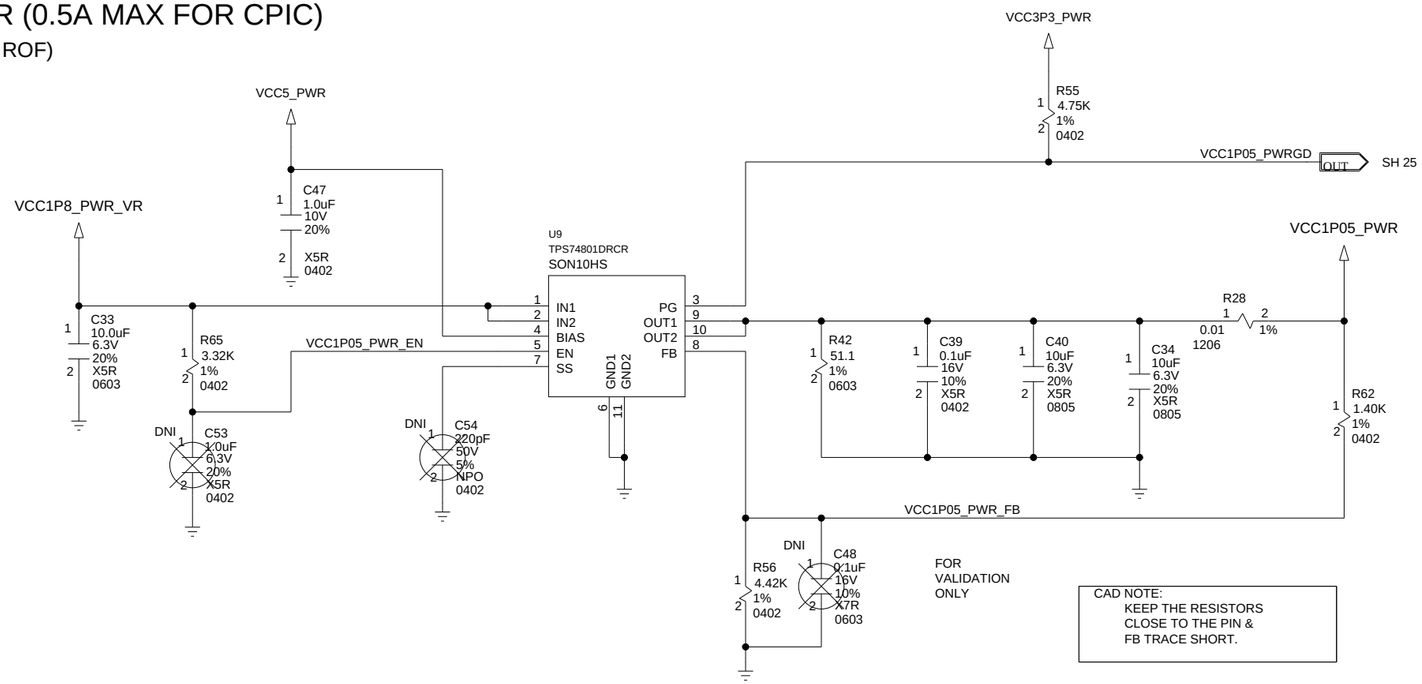
1.8V REGULATOR (1.8A MAX FOR CPIC)

VOUT = 0.8 * (1 + RFB / ROF)



1.05V REGULATOR (0.5A MAX FOR CPIC)

VOUT = 0.8 * (1 + RFB / ROF)



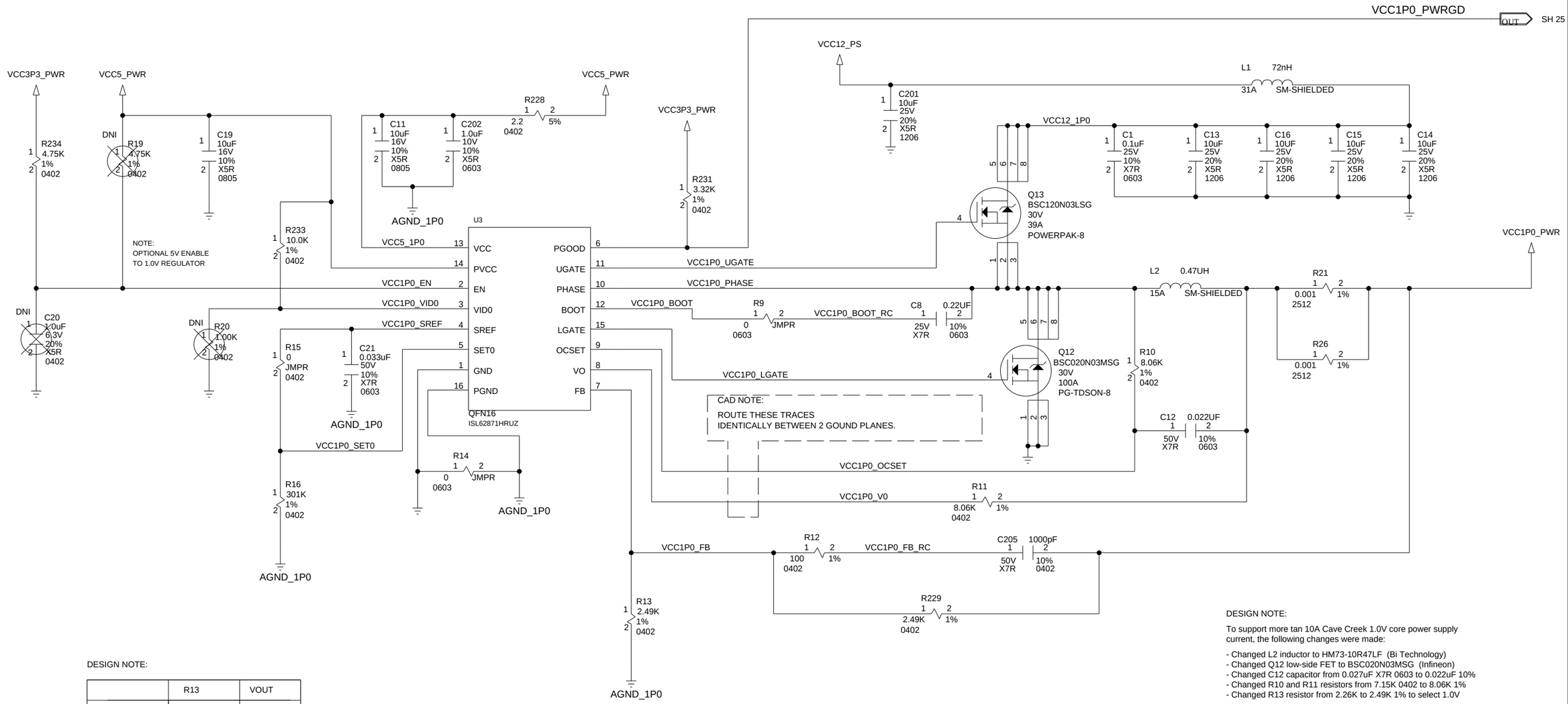
POWER 1.8V and 1.05V

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE			
CPIC			
SIZE	DWG NO		REV
B	453503		1.2
DATE	2-22-2012_11:11	SHEET 22 of 34	

1.0V REGULATOR (13.2A MAX FOR CPIC)



DESIGN NOTE:

To support more tan 10A Cave Creek 1.0V core power supply current, the following changes were made:

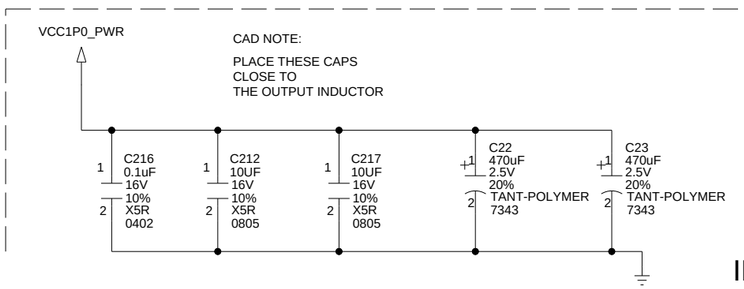
- Changed L2 inductor to HM73-10R47LF (Bi Technology)
- Changed Q12 low-side FET to BSC020N03MSG (Infineon)
- Changed C12 capacitor from 0.027uF X7R 0603 to 0.022uF 10%
- Changed R10 and R11 resistors from 7.15K 0402 to 8.06K 1%
- Changed R13 resistor from 2.26K to 2.49K 1% to select 1.0V

DESIGN NOTE:

	R13	VOUT
CCK	2.49K	1.0V
PET	2.26K	1.05V

DESIGN NOTE:

VID0	VOUT
HI	VOUT = 0.5 (1 + RFS/ROFS)
LOW	VOUT = 0.55 (1 + RFS/ROFS)



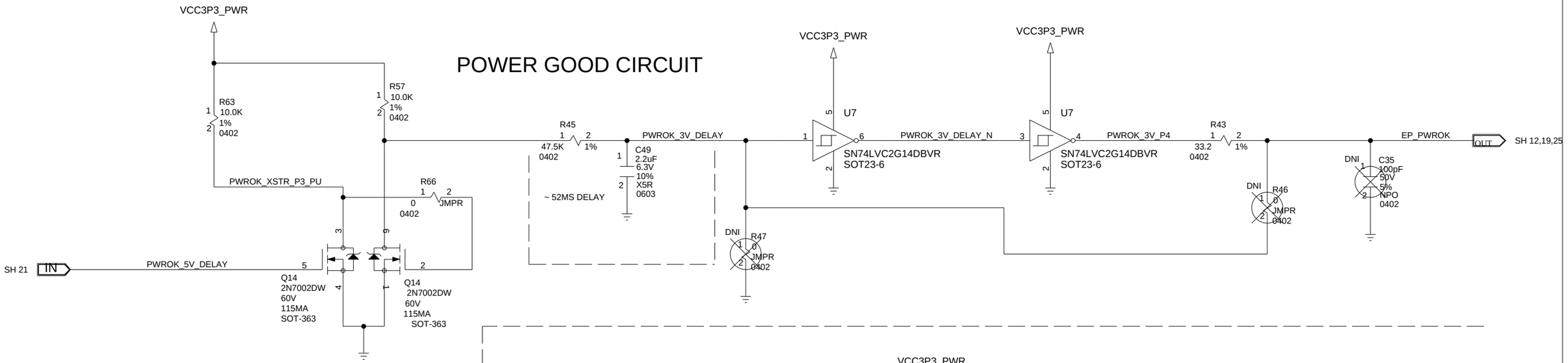
INTEL CONFIDENTIAL

POWER 1.0V REGULATOR

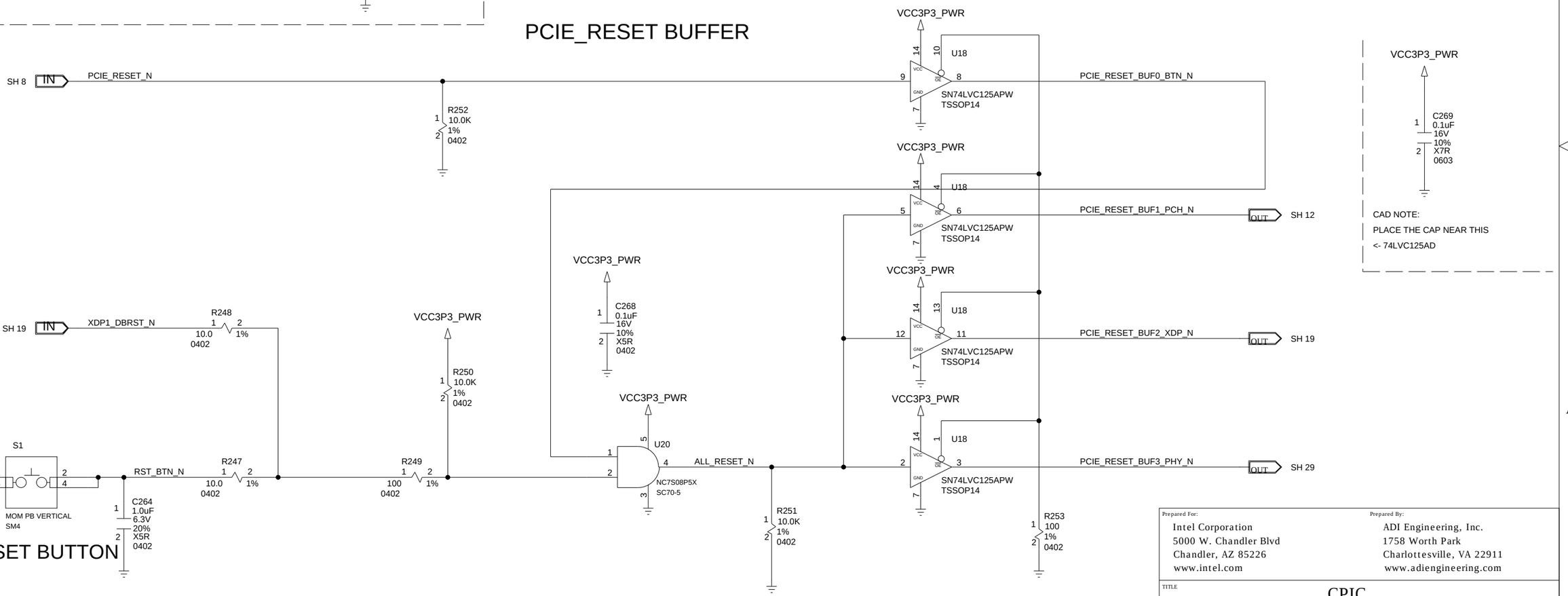
Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:42	SHEET 23 of 34	

POWER GOOD CIRCUIT



PCIE_RESET BUFFER



RESET BUTTON

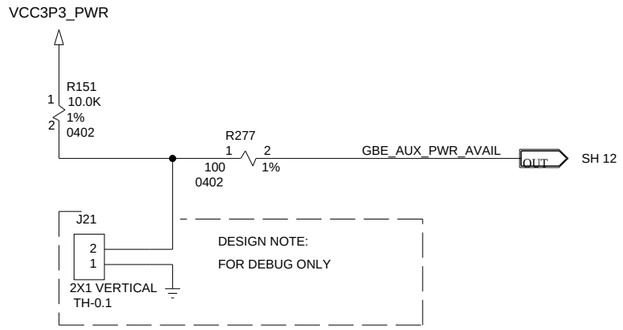
POWER GOOD & RESET BUFF

INTEL CONFIDENTIAL

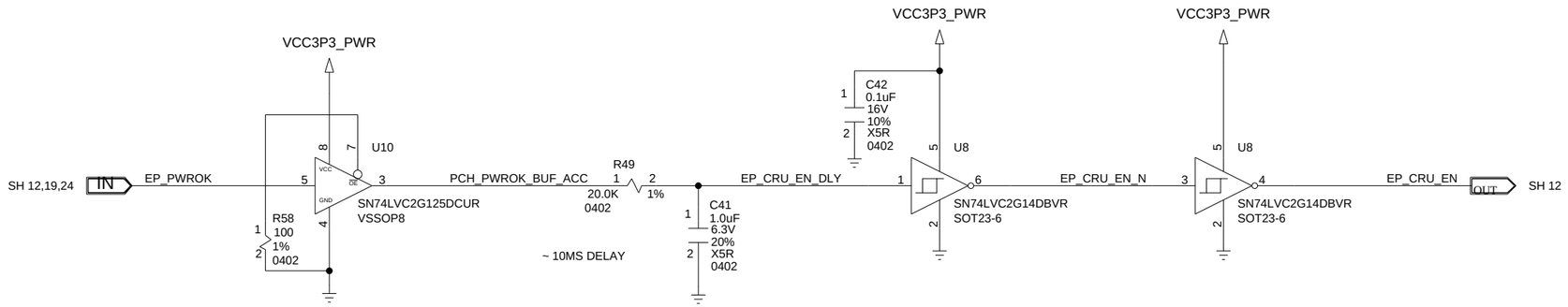
Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 24 of 34	

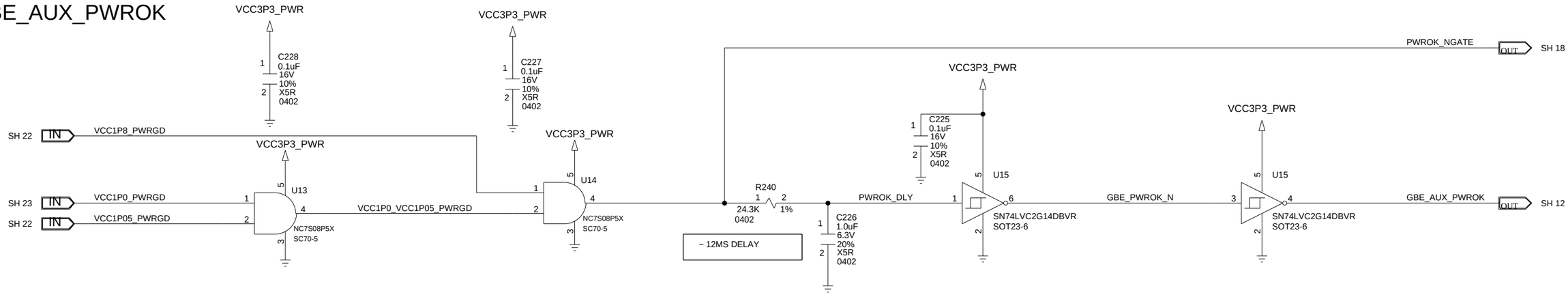
GBE_AUX_PWR_AVAIL



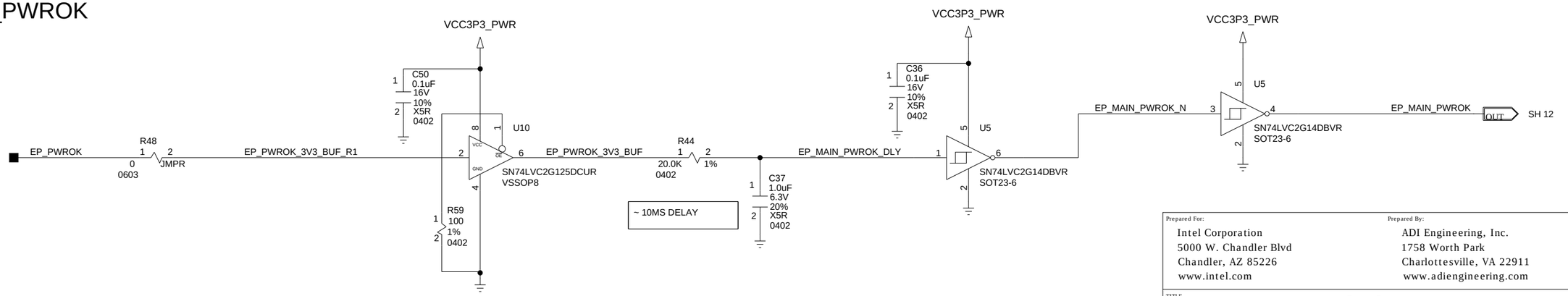
PCH POWER GOOD LOGIC



GBE_AUX_PWROK



EP_MAIN_PWROK



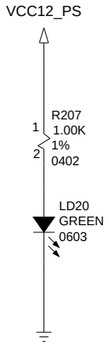
POWER SEQUENCE DELAYS

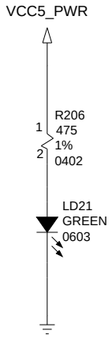
INTEL CONFIDENTIAL

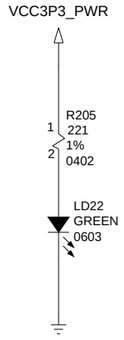
Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 25 of 34	

LEDS AND HEADERS







POWER LEDS

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 26 of 34	

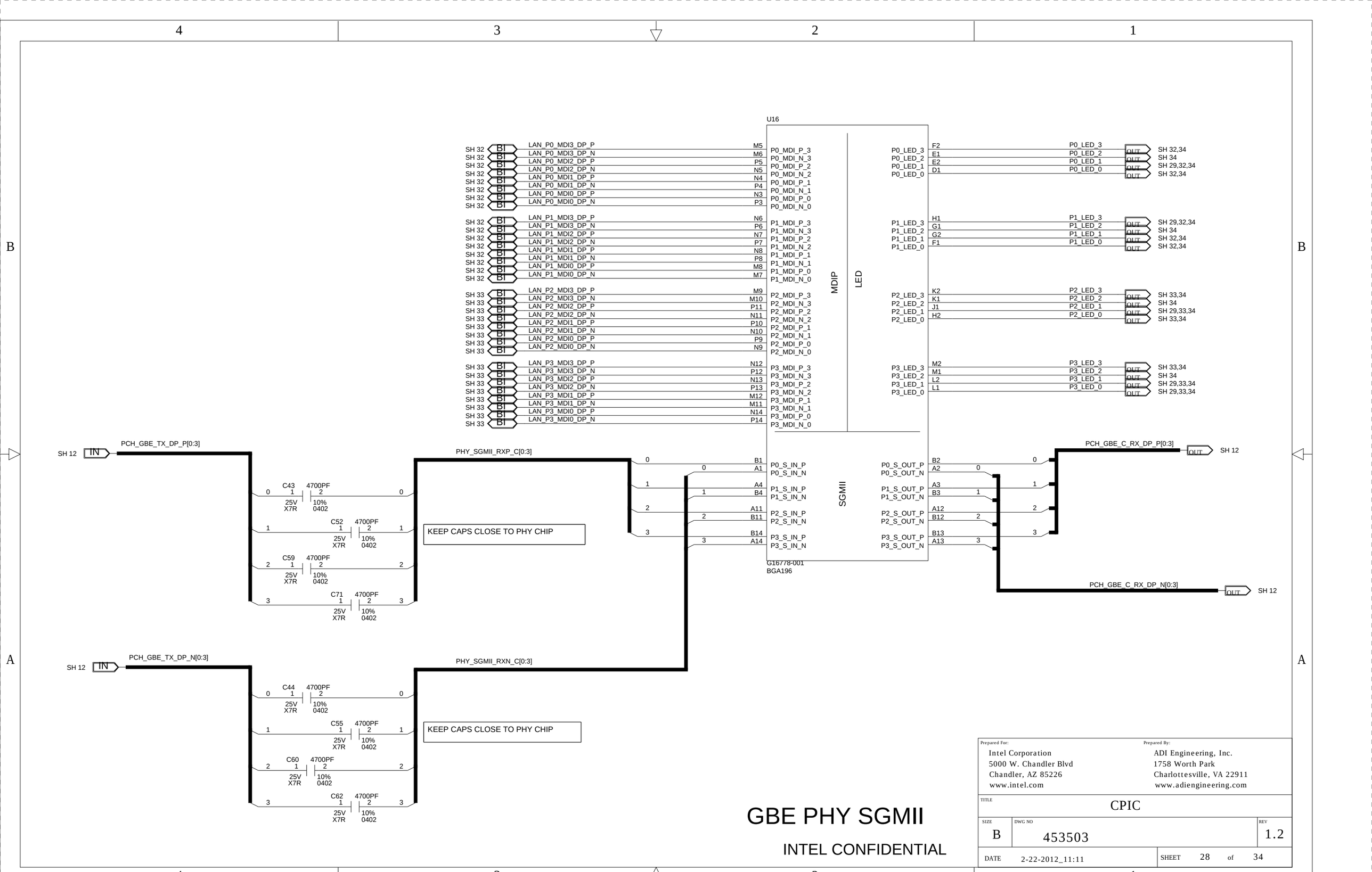
GBE QUAD PHY

BLANK

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 27 of 34	



Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE: CPIC

GBE PHY SGMII

INTEL CONFIDENTIAL

SIZE	DWG NO	REV
B	453503	1.2

DATE 2-22-2012_11:11 SHEET 28 of 34

CLK_SEL[1:0] CONFIG	
00	156.25 REF
01	125MHZ REF
10 (DEFAULT)	25MHZ XTAL
11	25MHZ XTAL

CLK SOURCE CONFIG		
	POP	DE-POP
REF	R77,R92	R83,R85 R74,R91
XTAL	R83,R85 R74,R91	R77, R92

J5	
OFF	NORMAL
ON	RESET

CONFIG[0]	0000	
CONFIG[1]	1111	
CONFIG[2]	1100 1101	POWER ON POWER OFF
CONFIG[3]	0001	PTP DISABLE

PLACE RES ON TOP SIDE

PLACE CLOSE ENOUGH TO USE
0805 RESISTOR NETWORK

PLACE CLOSE TO OSC

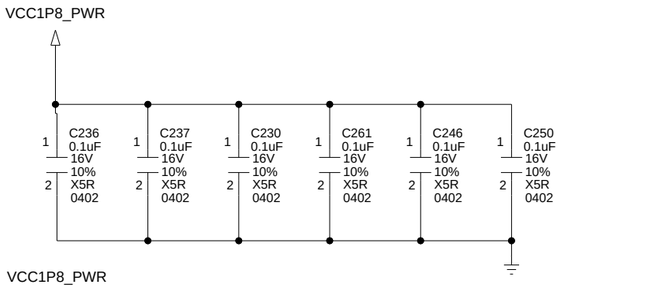
GBE JTAG HEADER

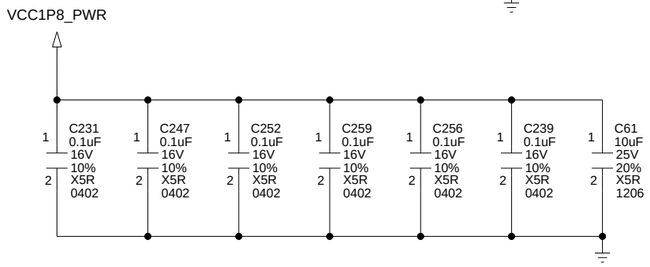
GBE PHY & CLOCK

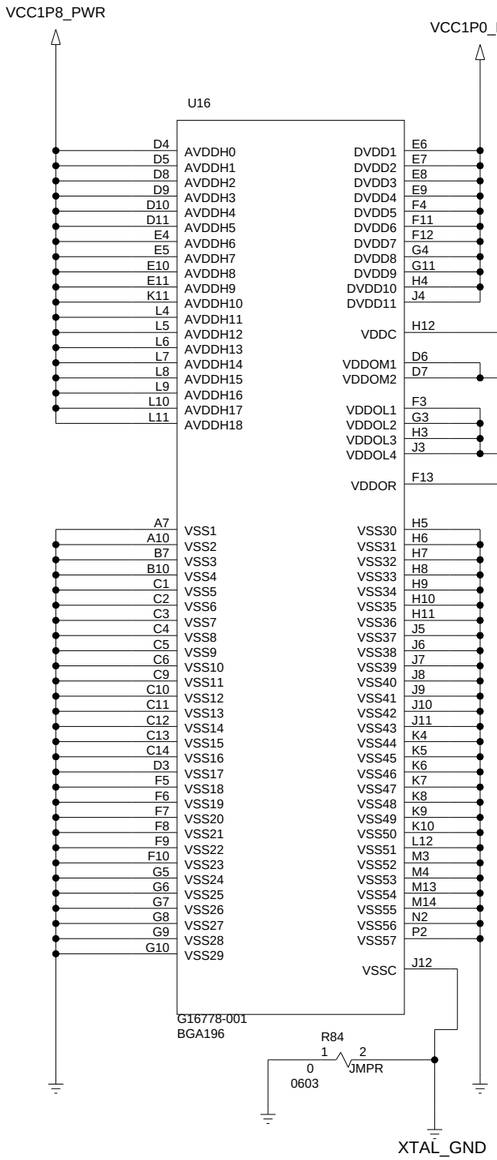
INTEL CONFIDENTIAL

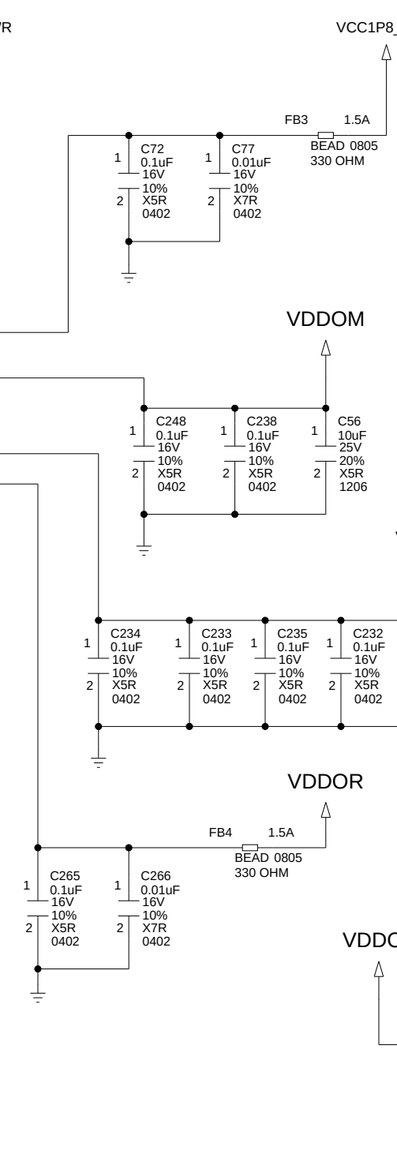
Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

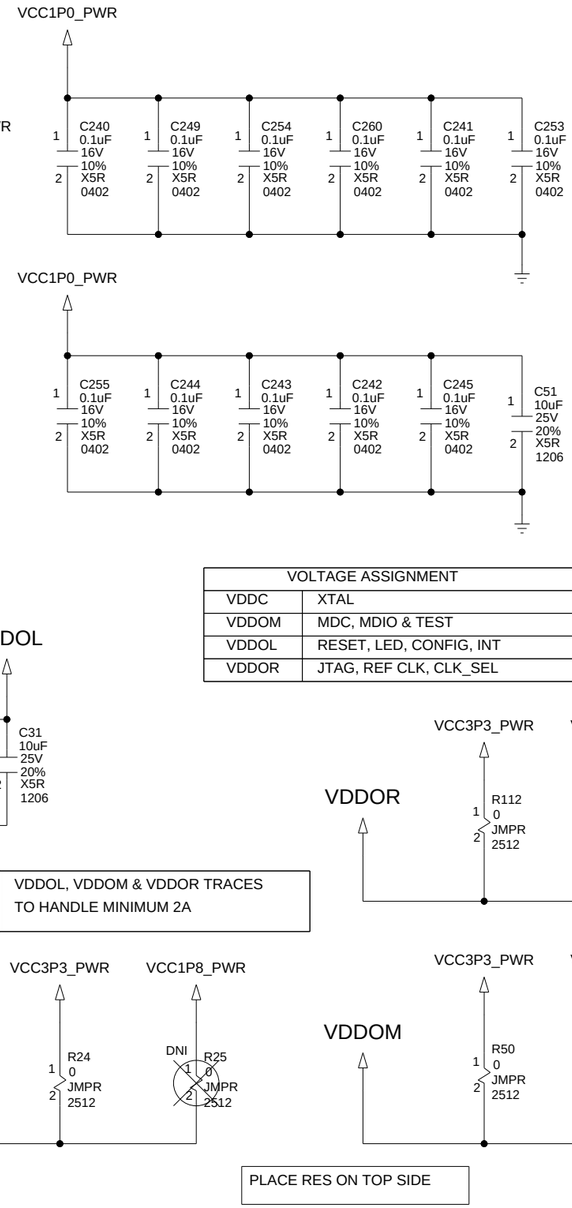
TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET: 29 of 34	











VOLTAGE ASSIGNMENT	
VDDC	XTAL
VDDOM	MDC, MDIO & TEST
VDDOL	RESET, LED, CONFIG, INT
VDDOR	JTAG, REF CLK, CLK_SEL

VDDOL, VDDOM & VDDOR TRACES TO HANDLE MINIMUM 2A

PLACE RES ON TOP SIDE

VDDOM CONFIG			
VOLT	R70	R50	R51
3.3 V	INSTALL	INSTALL	X
1.8 V	X	X	INSTALL

VDDOR CONFIG			
VOLT	R90	R112	R111
3.3 V	INSTALL	INSTALL	X
1.8 V	X	X	INSTALL

VDDOL CONFIG			
VOLT	R35	R24	R25
3.3 V	INSTALL	INSTALL	X
1.8 V	X	X	INSTALL

X = NO INSTALL

GBE PHY PWR/DECOUPLE

INTEL CONFIDENTIAL

Prepared For:
Intel Corporation
5000 W. Chandler Blvd
Chandler, AZ 85226
www.intel.com

Prepared By:
ADI Engineering, Inc.
1758 Worth Park
Charlottesville, VA 22911
www.adiengineering.com

TITLE: CPIC

SIZE: B | DWG NO: 453503 | REV: 1.2

DATE: 2-22-2012_11:11 | SHEET 30 of 34

ON BOARD SPI FLASH

VCC3P3_DEDIPRO

J6
NC 1 2 NC
3 4
5 6
7 8
NC 9 10 NC
5X2 VERTICAL
SM-0.1

SH 12 OUT / BI SPI_FLASH_CS_N / SPI_FLASH_DO
SPI_FLASH_SK / SPI_FLASH_DI OUT / BI SH 12

DEDI PROG HEADER (SPI FLASH)

VCC3P3_PWR

D201 SMA — 30V 1A MBRA130LT3G
C218 0.1uF 25V 10% X7R 0603
VCC3P3_SPI

OCP1 1.5A — SM1206 6V

D202 SMA — 30V 1A MBRA130LT3G
C219 0.1uF 25V 10% X7R 0603

J2
NC 1 2 NC
3 4
5 6
7 8
NC 9 10 NC
5X2 VERTICAL
SM-0.1

SH 12 OUT / BI GBE_EE_CS_N / GBE_EE_DO
GBE_EE_SK / GBE_EE_DI OUT / BI SH 12

DEDI PROG HEADER (SERIAL EEPROM)

VCC3P3_SPI

R246 10.0K 1% 0603
R68 10.0K 1% 0603
R71 10.0K 1% 0603
R244 10.0K 1% 0603

C258 0.1uF 25V 10% X7R 0603

SPI_FLASH_HOLD_N

U17
8 VCC
5 SI/IO0
6 SCK
1 CS#
HOLD#/IO3 7
SO/IO1 2
SPI_FLASH_WP_N 3 WP#/IO2
4 GND
W25Q16BVSSIG
SOIC8

SPI_FLASH_DO

J7
1
2
2X1 VERTICAL
TH-0.1

OPEN: WRITE ENABLE
(DEFAULT)

SU1
SOIC8 SOCKET FOR 208 MIL SPI FLASH
SOIC8SKT

VCC3P3_SPI

R245 10.0K 1% 0603

ON BOARD GBE EEPROM

VCC3P3_SPI

R235 10.0K 1% 0603
R17 10.0K 1% 0603
R22 10.0K 1% 0603
R230 10.0K 1% 0603

C215 0.1uF 25V 10% X7R 0603

GBE_EE_HOLD_N

U4
8 VCC
5 SI
6 SCK
1 CS#
HOLD# 7
SO 2
GBE_EE_WP_N 3 WP#
4 GND
25AA512-I/SM
SOIC8

VCC3P3_SPI

R232 10.0K 1% 0603

GBE_EE_DO

J4
1
2
2X1 VERTICAL
TH-0.1

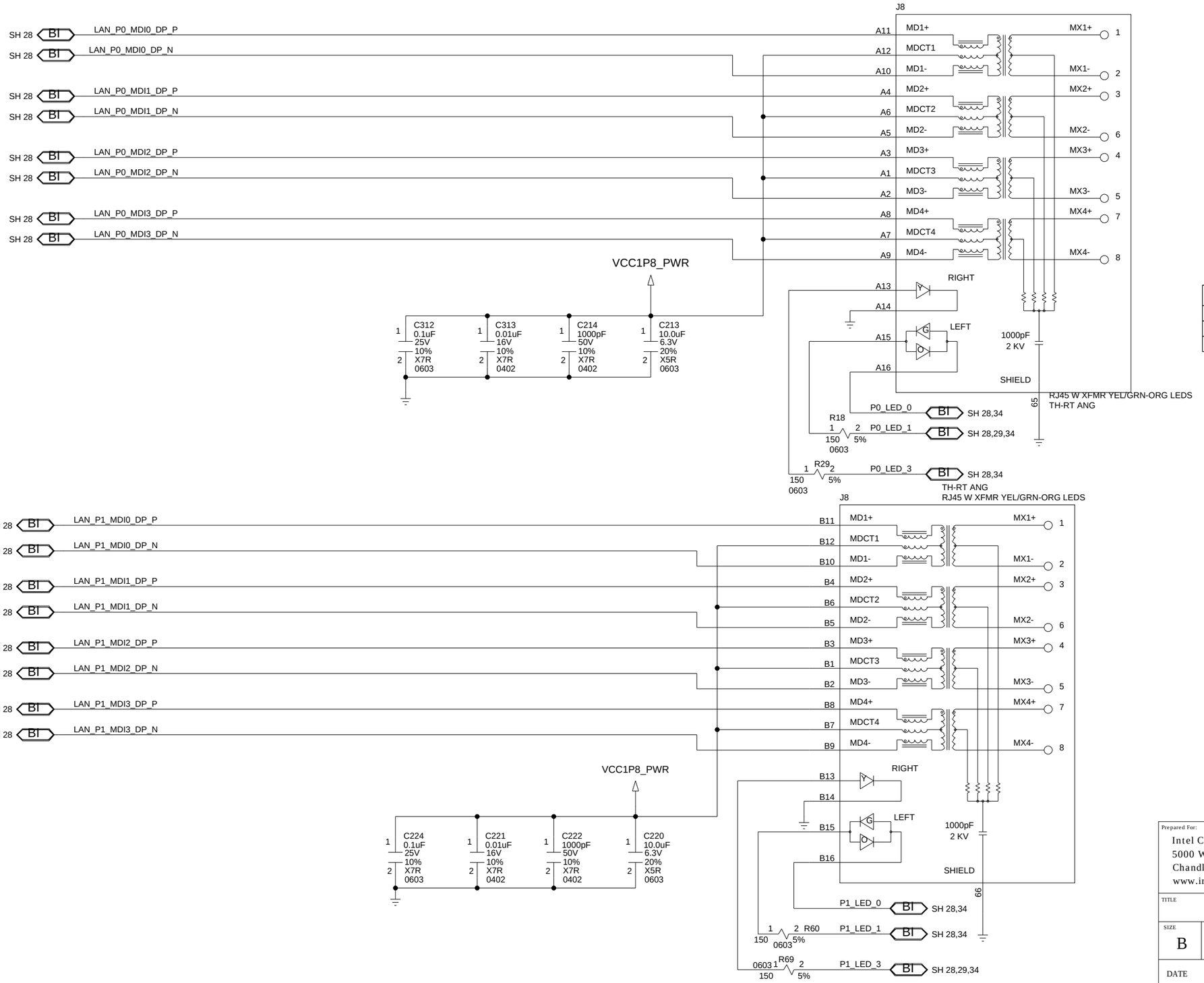
OPEN: WRITE ENABLE
(DEFAULT)

SU2
SOIC8 SOCKET FOR 208 MIL SPI FLASH
SOIC8SKT

GBE EEPROM & SPI FLASH

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 31 of 34	



LED	COLOR	ON	OFF	BLINK
LED_0	GREEN	1000 LINK	10 LINK	N/A
LED_1	ORANGE	100 LINK		N/A
LED_3	YELLOW	LINK	NO LINK	ACTIVITY

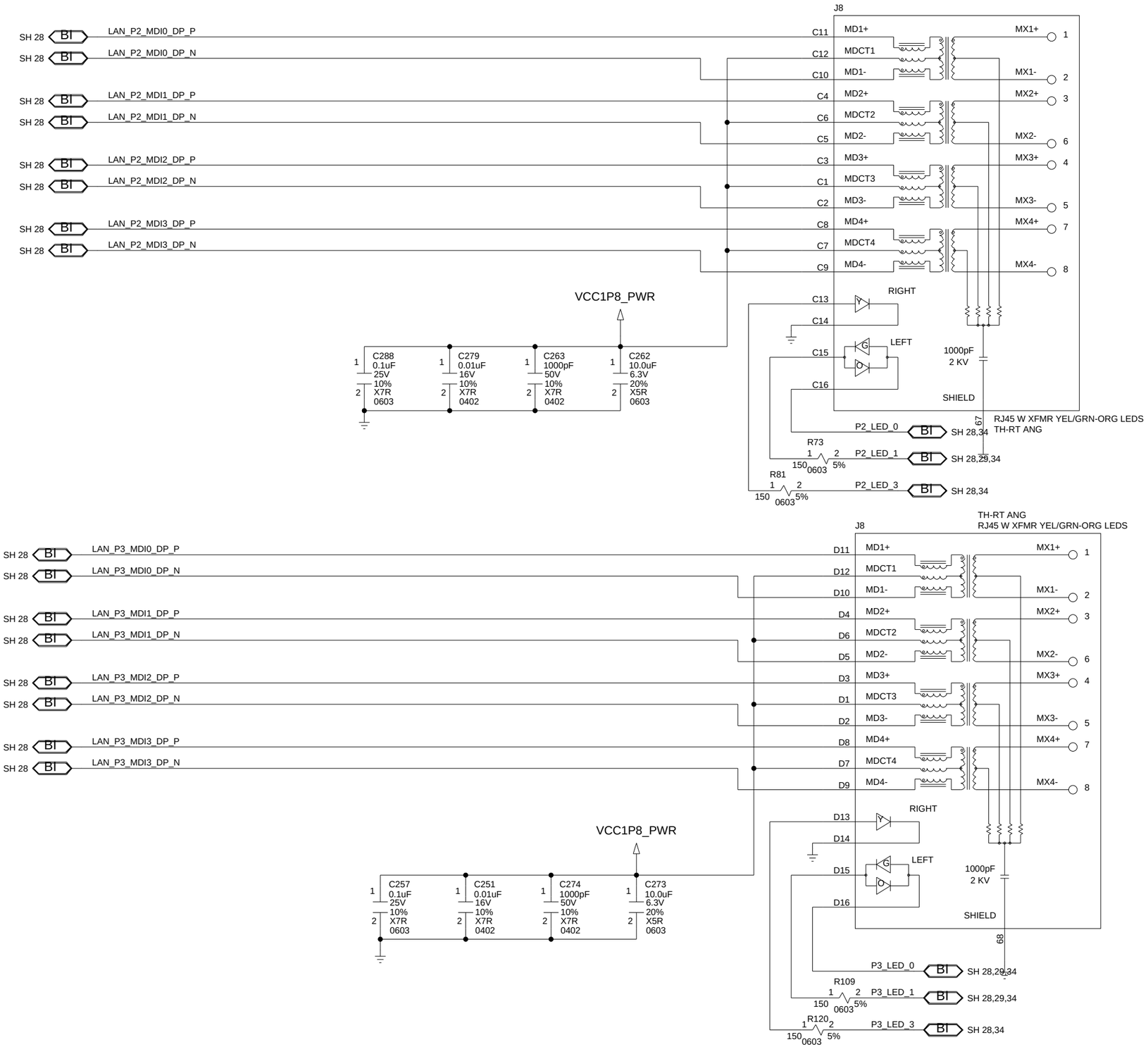
KEEP LED LINES AWAY FROM MDI P/N LINES
TO AVOID SIGNAL CROSSTALK

GBE LAN PORT 0 & 1

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE			
CPIC			
SIZE: B	DWG NO: 453503		REV: 1.2
DATE: 2-22-2012_11:11	SHEET 32 of 34		



KEEP LED LINES AWAY FROM MDI P/N LINES
TO AVOID SIGNAL CROSSTALK

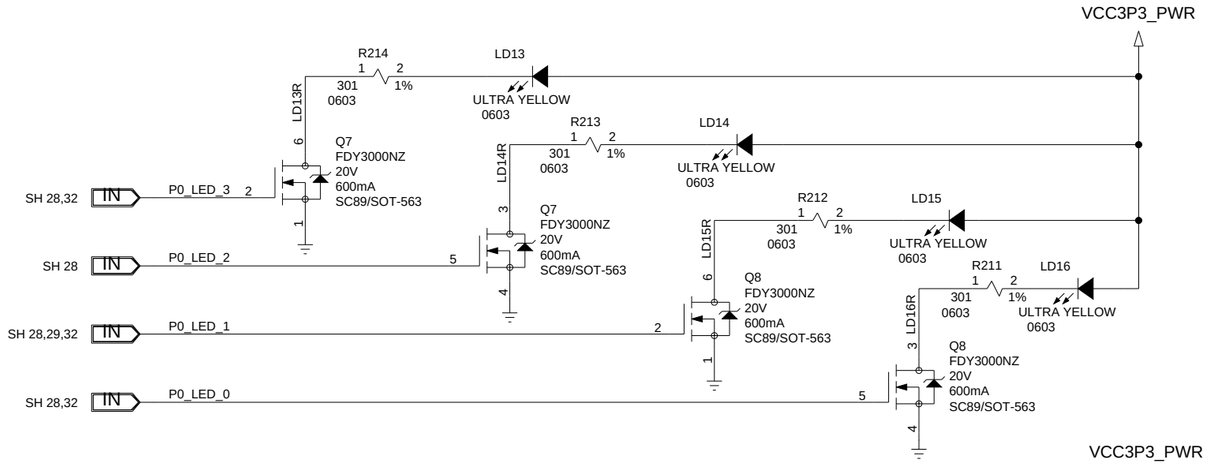
LED	COLOR	ON	OFF	BLINK
LED_0	GREEN	1000 LINK	10 LINK	N/A
LED_1	ORANGE	100 LINK		N/A
LED_3	YELLOW	LINK	NO LINK	ACTIVITY

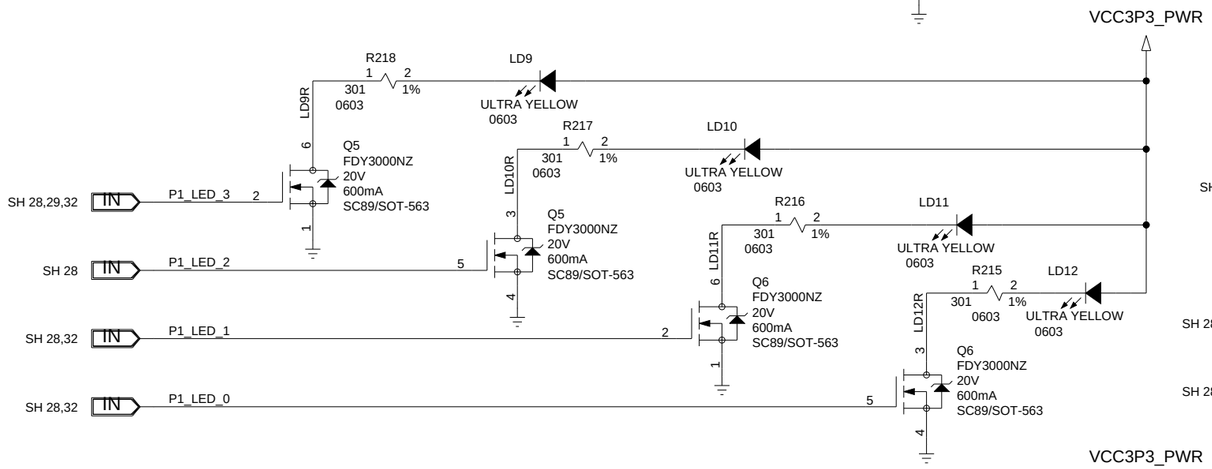
GBE LAN PORT 2 & 3

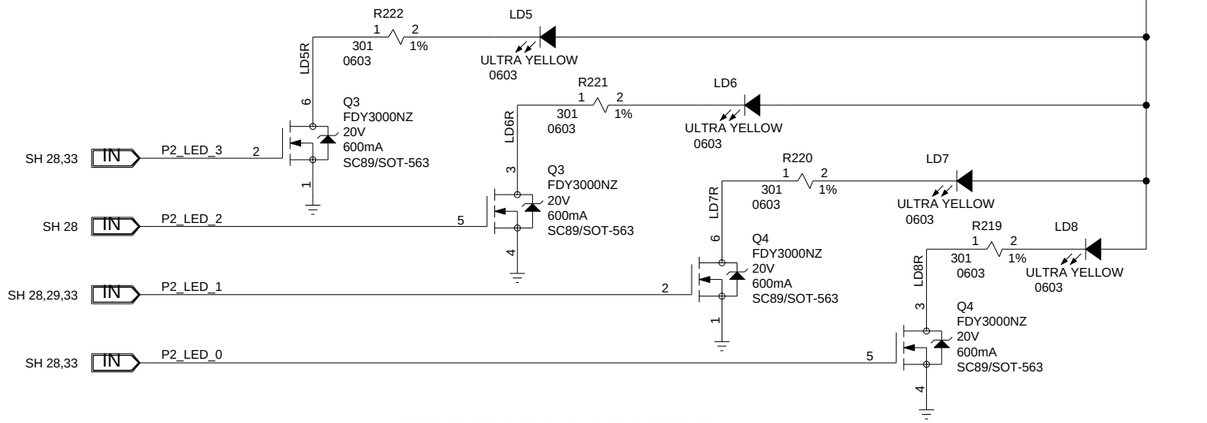
INTEL CONFIDENTIAL

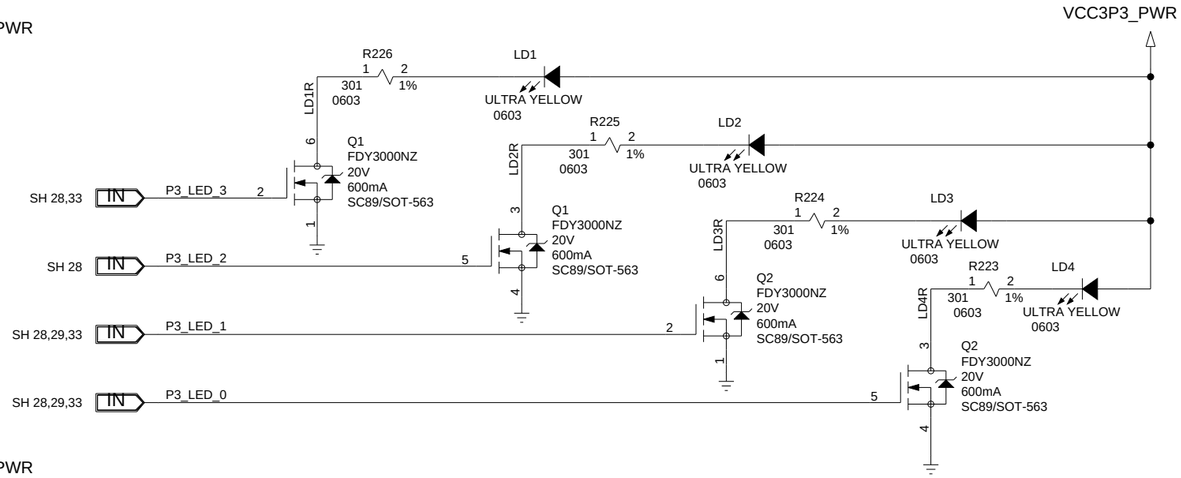
Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE			
CPIC			
SIZE	DWG NO		REV
B	453503		1.2
DATE	2-22-2012_11:11	SHEET 33 of 34	









INDIVIDUAL LAN LEDS

GBE LAN LEDS

INTEL CONFIDENTIAL

Prepared For:	Prepared By:
Intel Corporation 5000 W. Chandler Blvd Chandler, AZ 85226 www.intel.com	ADI Engineering, Inc. 1758 Worth Park Charlottesville, VA 22911 www.adiengineering.com

TITLE		
CPIC		
SIZE: B	DWG NO: 453503	REV: 1.2
DATE: 2-22-2012_11:11	SHEET 34 of 34	