

### 3-9-3. SOURCE BLOCK SECTION

The source block section is composed of the A4 high power amplifier/dc bias and the A5 signal source boards. The A4 board is only installed for the Option 001.

The A5 signal source board generates the AC voltage (5 mVrms to 1 Vrms), and also generates 1.5V/2.0V DC voltages. The A5 signal source consists of three crystal oscillators, the programmed N divider, the quasi-sine wave generator, the attenuator, the D-A Converter, the dc bias voltages (1.5 V/2.0 V), the output amplifier, and the source resistor. (Refer to Figure 3-5.)

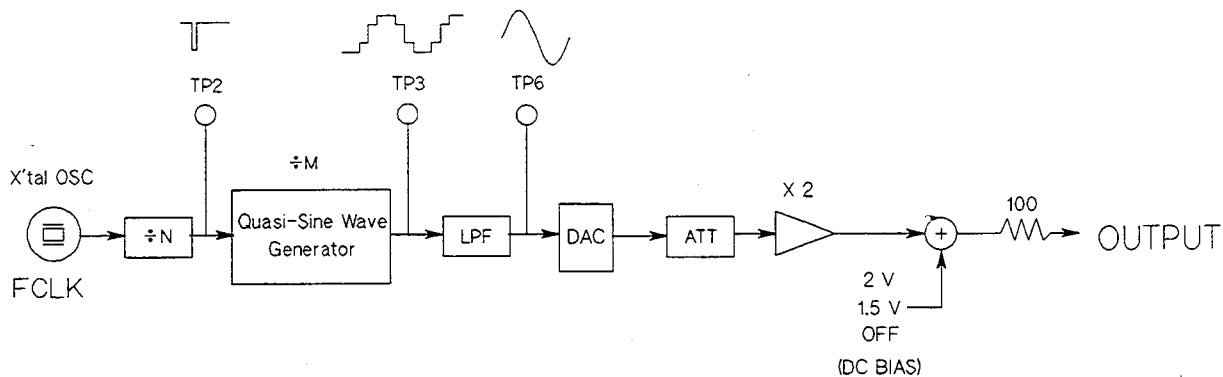


Figure 3-5. Signal Source (A5) Simplified Block Diagram

The crystal oscillators are 19.2 MHz, 16.0 MHz, and 15.36 MHz. One of three crystal oscillators (FCLK) is selected and the output signal is divided by N using the programmed N divider. The divided signal is applied to the quasi-sine wave generator which generates a digital sinewave (staircase waveform). The digital sinewave's frequency is the same as the output test frequency. So the available test frequencies (F) are calculated using the following formula.

$$F = \text{FCLK} / (N \times M)$$

Where,

FCLK: 19.2 MHz, 16.0 MHz, 15.36 MHz

N: 2 to 4095 (integer)

M: 8, 16, 32, 64, 128, 256

The digital sinewave is filtered by the LPF, and the filtered sine wave is input to the D-A converter (DAC) as a voltage reference. So the 4284A covers various test signals with a high resolution by using both the DAC and the attenuator.

The A4 high power amplifier/dc bias board generates the DC output voltage using the DAC, and also amplifies the AC output signal from the A5 board. The A4 high power amplifier/dc bias board consists of the reference voltage, the D-A converter, the attenuator, the power amplifier ( $\times 10$ ), two switching relays. (Refer to Figure 3-6.)

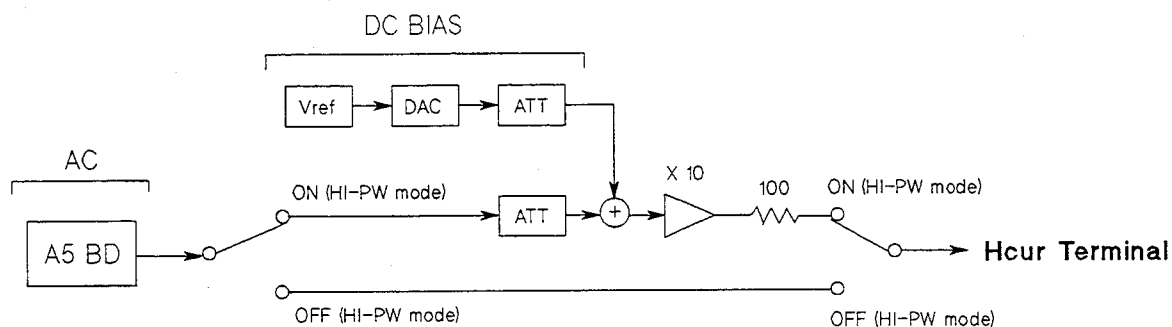


Figure 3-6. High Power Amplifier/DC Bias (A4) Simplified Block Diagrams

The reference voltage ( $V_{ref}$ ) is  $\pm 5$  V whose sign depends on the polarity of the dc bias setting. The  $V_{ref}$  output is applied to the D-A converter (DAC). The output from the DAC is attenuated by the attenuator, and the attenuated dc bias signal is added to the ac signal from the A5 board. The added signal is amplified ( $\times 10$ ), and is output to the Hcur Terminal.

In the case of the 4284A with the Option 001, you can select the high power mode (ON/OFF) which switches two relays.

### 3-9-4. TRANSDUCER BLOCK SECTION

The HP 4284A employs the current-to-voltage converter as an ammeter. See Figure 3-7. The current through the DUT is detected by a current-to-voltage (I-V) converter using a resistor (Range resistor,  $R_r$ ) in the feedback circuit. The I-V converter generates a current flow through the range resistor equal to the current through the DUT. Therefore, the output voltage of the I-V converter is equal to the product of the current through the DUT and the range resistor value. Accordingly, the impedance is calculated using the voltage across the DUT, the output voltage of the I-V converter, and the value of the range resistor. Then the potential at the LOW terminal is approximately zero (the feedback node is at virtual ground), thus, the range resistor value has no effect on the current through the DUT.

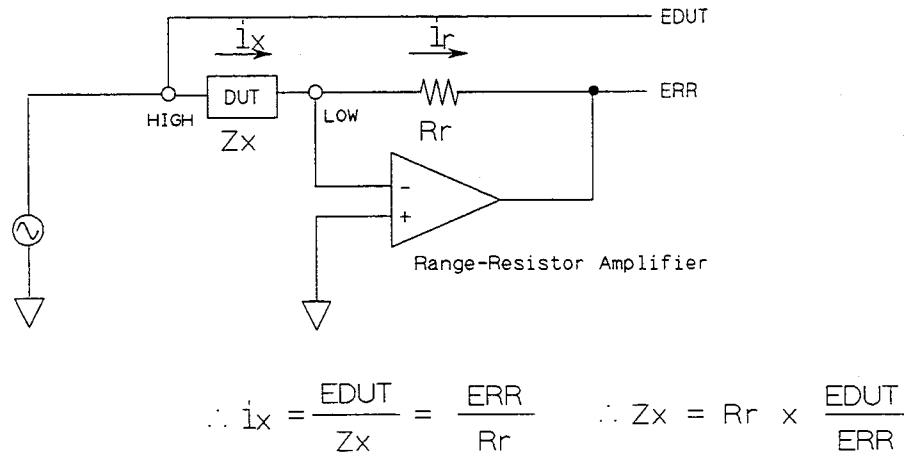


Figure 3-7. I-V Converter

The auto balance bridge circuitry used in the 4284A ensures that the vector voltage across the feedback resistor will be an accurate proportional representation of the current through the device under test. The basic principle of the auto-balance-bridge circuit is explained in terms of the two oscillator model illustrated in Figure 3-8.

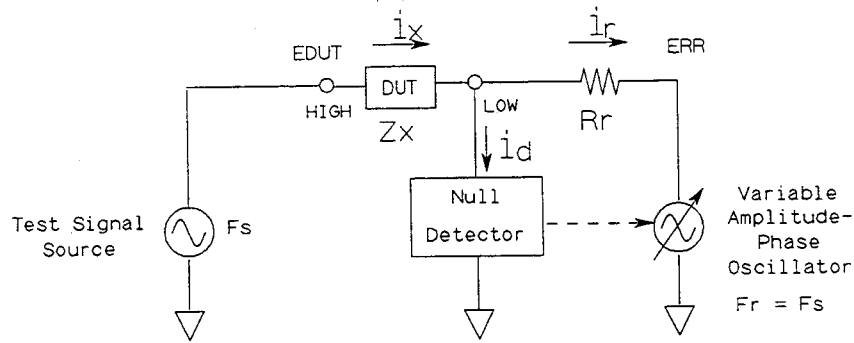


Figure 3-8. Two Oscillators of The Auto Balance Bridge

Currents  $i_x$  and  $i_r$  can be balanced by controlling the output of the variable amplitude phase oscillator as follows. Firstly, the null detector detects the difference ( $i_d$ ) between the current through the DUT ( $i_x$ ) and the current through the range resistor ( $i_r$ ). The unbalance current ( $i_d$ ) which has the information required to balance the bridge, is output to the feedback control circuit for the variable amplitude phase oscillator. After the variable amplitude phase oscillator ( $e_r$ ) is adjusted, the  $i_d$  is equal to zero (0). So finally the  $i_x$  is equal to the  $i_r$ , and the impedance of the DUT is calculated as follows.

$$\therefore i_x = \frac{EDUT}{Z_x} = \frac{ERR}{R_r} \quad \therefore Z_x = R_r \times \frac{EDUT}{ERR}$$

The actual auto balance bridge circuit is composed of the A2 modulator and A3 range resistor boards. The auto balance bridge consists of a null detector, a vector generator, and a feedback resistor (range resistor).

The null detector consists of a current-to-voltage (I-V) converter, a phase detector, and an integrator. An I-V converter is used to detect difference between the device under test and the feedback resistor, and outputs this difference as a proportional error voltage. A phase detector and an integrator convert the error voltage into a dc voltage proportional to the orthogonal vector components.

The vector generator consists of two amplitude modulators, a  $90^\circ$  phase shifter, and a summing amplifier. The reference signal from the test oscillator is amplitude modulated using the null detector's dc error voltage output. When the error voltage from the null detector goes negative, the phase of the output signal from the vector generator shifts  $180^\circ$ . The  $0^\circ$  phase component of the error voltage is fed into the input of the modulator and this  $0^\circ$  phase component modulated output of the modulator is fed directly into the input of the summing amplifier. The  $90^\circ$  phase component modulated output of the modulator is fed into a  $90^\circ$  phase shifter before being fed into the summing amplifier. The output voltage of the summing amplifier is fed back through the range resistor to cancel the error current, thereby keeping the bridge balanced.

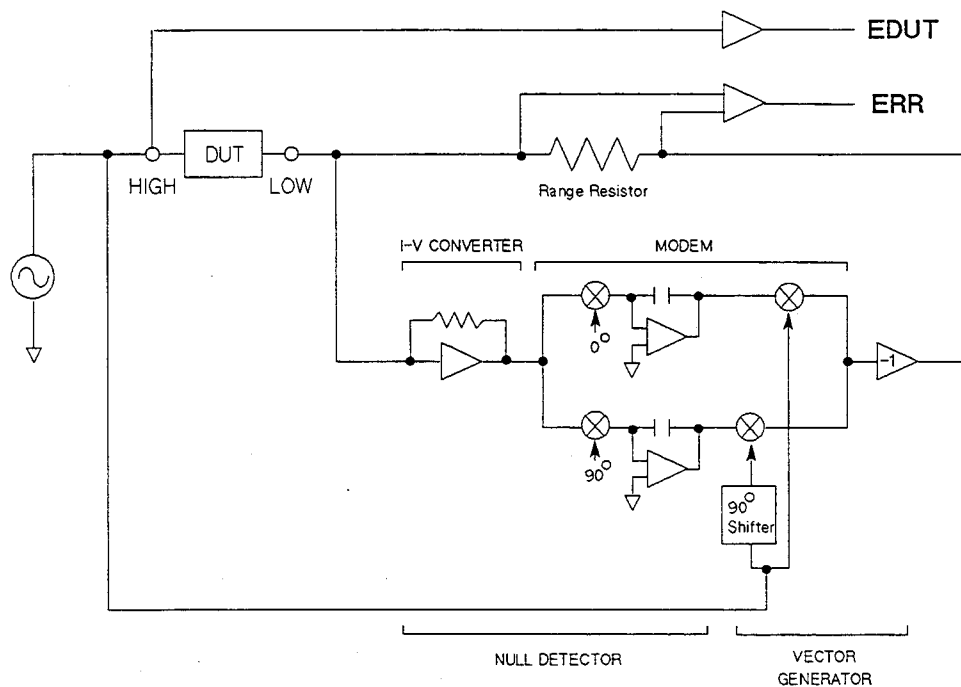


Figure 3-9. Auto Balance Bridge

### 3-9-5. VECTOR RATIO DETECTOR SECTION

The vector ratio detector is the A6 board, and it consists of the phase sensitive detector, the detection phase generator, and the A-D (Analog-to-digital) converter.

The phase sensitive detector detects the ERR voltage and the EDUT voltage using  $0^\circ$  and  $90^\circ$  reference signals from the detection phase generator, and outputs the  $0^\circ$  components of the ERR and EDUT voltages and the  $90^\circ$  components of the ERR and EDUT voltages.

The A-D converter converts each  $0^\circ$  and  $90^\circ$  components to digital signals. After that, each parameter's value is calculated by using these digital values.

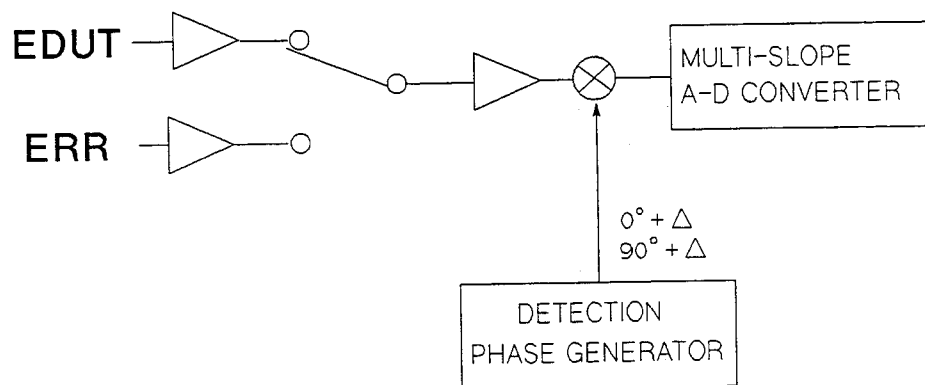


Figure 3-10. Vector Ratio Detector

ANALOG SECTION BLOCK DIAGRAM (STD)

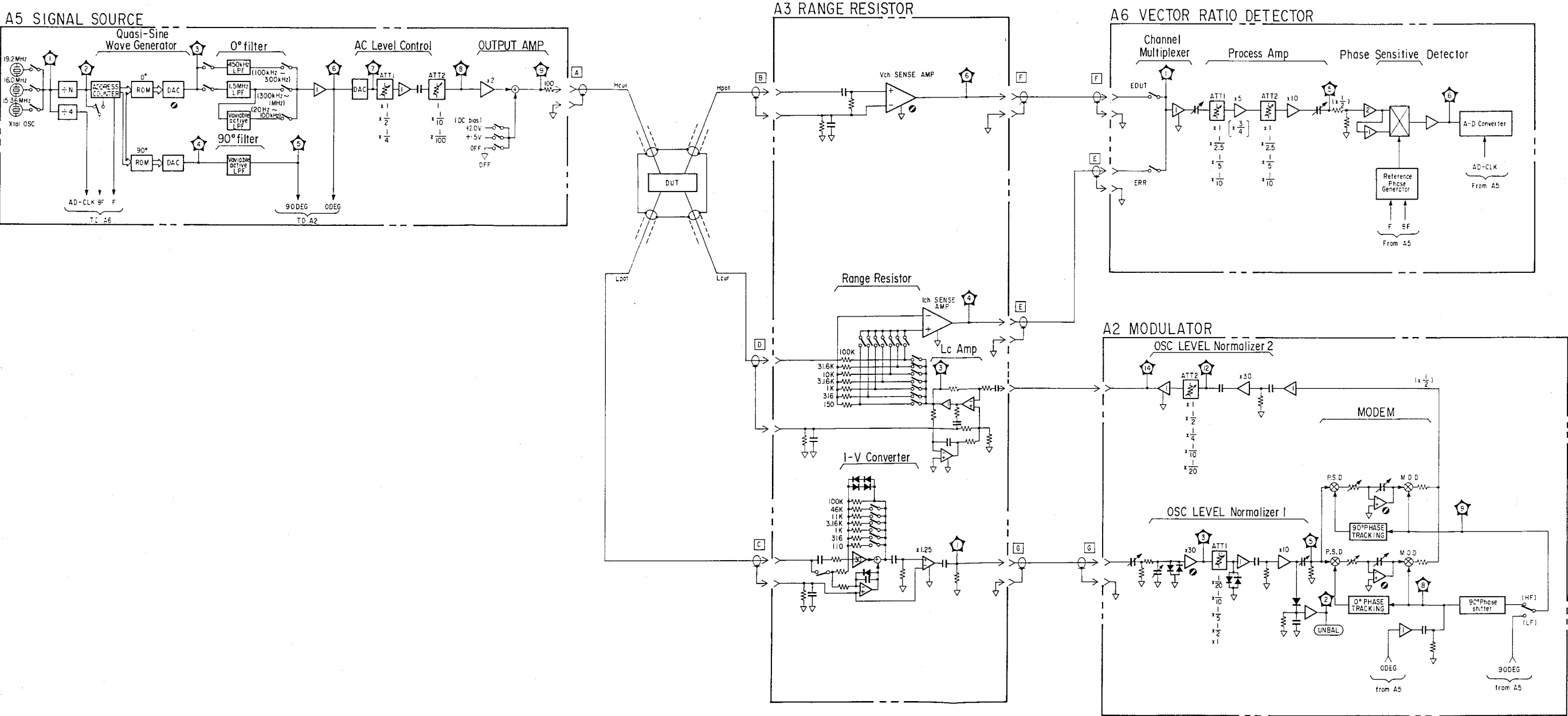


Figure 3-11. Analog Section Block Diagram (Std.)

### ANALOG SECTION BLOCK DIAGRAM (OPT.001)

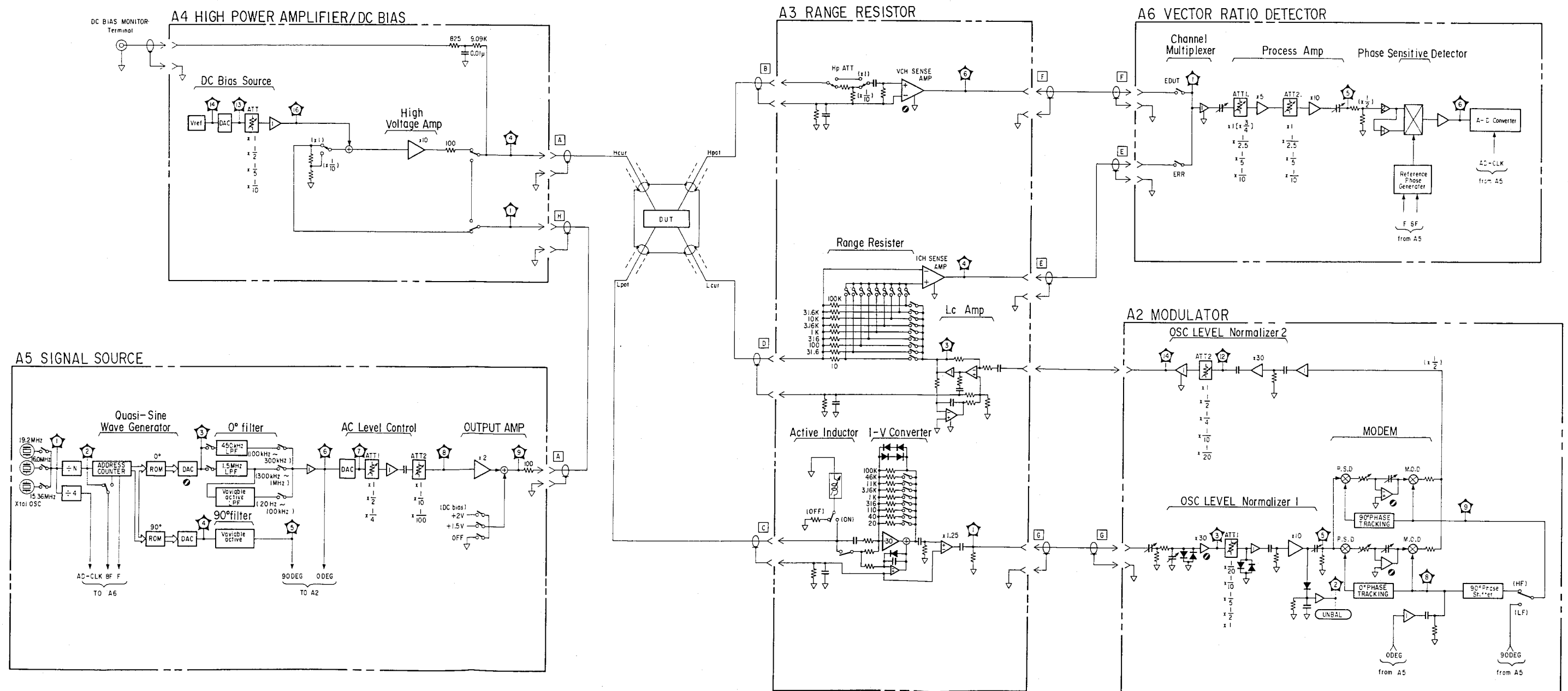


Figure 3-12. Analog Section Block Diagram (Opt.001)