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CMOS-based integrable electronically tunable floating general impedance inverter

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An integrable electronically tunable general impedance inverter (EGII), implemented by a MOS circuit design technique, is described. The driving point impedance of the EGII, that is inversely proportional to a given impedance, can be a positive or a negative value and can be electronically varied. The realization scheme employs proposed voltage-to-current transducers (VCTs) that are designed based on a linearizing technique, as basic circuit building blocks. The applications of the EGII as a gyrator, a general impedance converter and a floating capacitance multiplier are discussed. Experimental and simulation results that demonstrate the characteristics of the EGII are included.

1. Introduction

It is well accepted that general impedance inverters (GIIs) are very useful active circuit elements in the field of network synthesis and design, particularly the GII that can be electronically tuned (Mitra 1970, Moschyz 1974, Pookaiyaudom and Surakampontorn 1980). Two common applications of a GII are a gyrator and a negative impedance converter. In recent years, MOS linear voltage-to-current transducers (VCTs) have become very popular because of their high performance coupled with their broad and wide electronic tunable range. As circuit building blocks VCTs have many advantages over operational amplifiles (op-amps), particularly for a high-frequency application (Khorramabadi and Gray 1984, Torrance *et al.* 1985). For example, they are suitable for the realization of monolithic integrated analogue filters in a frequency range above 1 MHz, because the cut-off frequencies of the VCTs are typically in the range from 50 MHz to several hundred megahertz. On the other hand, the op.-amp. based active filters are no longer practical in the frequency range above 100 kHz.

In the past the circuits proposed for the realization of floating GIIs have been implemented using op.-amps (Norman 1986), or current conveyors (Toumazou *et al.* 1990), or bipolar transistors (Qui 1991). These realizations can be integrated, in principle; however, in practice this is not economical because they require large numbers of active elements. The goal of this paper is to propose a new circuit design technique for the synthesis of an electronically tunable floating general impedance inverter (EGII). We introduce a VCT that is designed based on a linearizing technique, and we then employ the VCT to construct the EGII. The completed EGII circuit requires 28 MOSFETs and one passive element, which is an attractive feature for an LSI implementation.

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2. Circuit descriptions

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. This means that the drain current I_D is characterized by a square-law model as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2, & \text{for } V_{GS} > V_T \\ 0, & \text{for } V_{GS} \leq V_T \end{cases} \tag{1}$$

where $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate–oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and threshold voltages, respectively.

2.1. *Voltage-to-current transducer (VCT)*

Figure 1 shows a single ended output VCT, which is formed by a general MOS source coupled pair circuit. Its DC transfer characteristic can be derived as follows:

$$V_i = V_1 - V_2 = V_{GS1} - V_{GS2} \tag{2}$$

$$i_{OUT} = i_1 - i_2 \tag{3}$$

$$I_B = i_1 + i_2 \tag{4}$$

where V_i is the input voltage, i_{OUT} is the output current and I_B is the bias current. Let us assume that M_1 and M_2 are well matched, the parameters $K_1 = K_2 = K$, and the current mirror formed by M_3 and M_4 has a unity current gain. From (2)–(4), the output current i_{OUT} becomes

$$i_{OUT} = (2I_B K)^{1/2} V_i [1 - (KV_i^2/2I_B)]^{1/2}, \quad \text{for } -(I_B/K)^{1/2} \leq V_i \leq (I_B/K)^{1/2} \tag{5}$$

The transconductance gain G_m of the VCT can be derived by taking the derivative of (5) with respect to V_i, yielding

$$G_m = \mathrm{d}i_{OUT}/\mathrm{d}V_i\Big|_{V_i=0} = (2I_B K)^{1/2} \tag{6}$$

Then

$$i_{OUT} = G_m V_i \qquad = (2I_B K)^{1/2} V_i$$

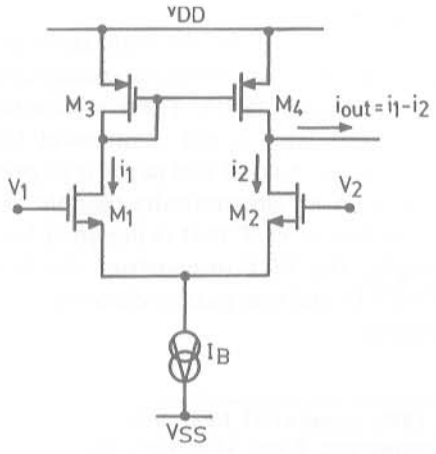

Figure 1. Typical source-coupled pair circuit.

Equation (7) shows that the transconductance gain G_m of the VCT can be varied by the bias current I_B.

2.2. *Electronically tunable general impedance inverter (EGII)*

Figure 2 shows the circuit of the proposed integrable EGII, which is based on the use of the VCT in Fig. 1. The realization scheme can be configured by the circuit diagram of Fig. 3(*a*), and its terminals characteristic can be represented as a floating driving point impedance, as shown in Fig. 3(*b*). The EGII circuit can be divided into two parts. For the first part, MOS transistors M_1–M_8 function as the single-ended output VCT1 that converts a differential input signal voltage $V_{in} = V_A - V_B$ into a signal current i_L to flow into a given or a conversion impedance Z_L. We obtain

$$i_L = G_{m1} V_{in} \tag{8}$$

$$V_L = i_L Z_L = G_{m1} Z_L V_{in} \tag{9}$$

where G_{m1} represents the transconductance gain of the VCT1.

The VCT2 of the second part is formed by M_9–M_{20}. This VCT will convert the voltage V_L into differential signal currents i_{ab}, where for $V_{in} > 0$, the signal currents i_{ab} flow into node A and flow out off node B. If G_{m2} is the transconductance gain of the VCT2, the magnitude of the currents i_{ab} are equal to

$$i_{ab} = G_{m2} V_L \tag{10}$$

By inspecting the polarity of the input voltage and the direction of the small signal currents and from (8) and (9), the driving point impedance of the terminals AB can be given by

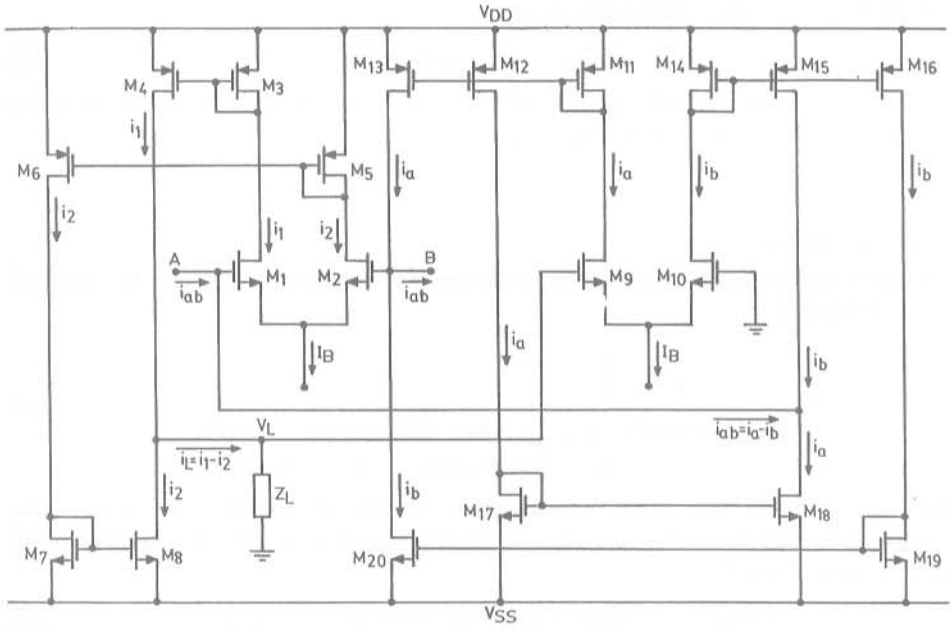

Figure 2. Circuit diagram of CMOS-based EGII.

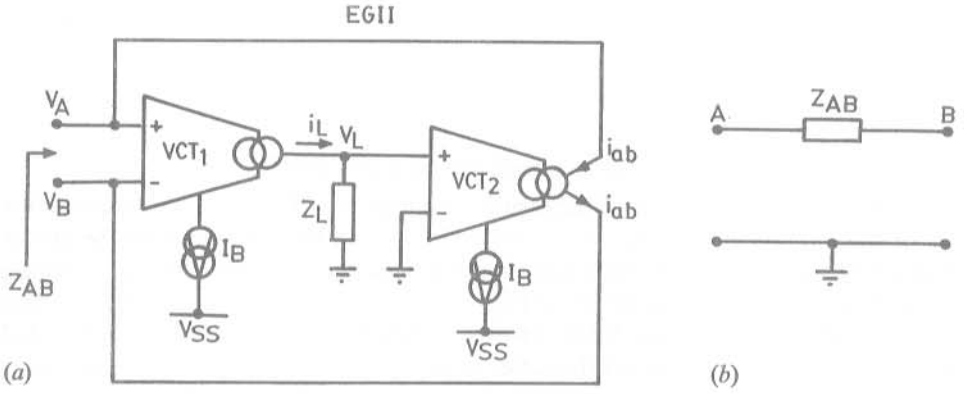

Figure 3. (a) Schematic circuit diagram of the CMOS-based EGII; (b) the floating driving point impedance of CMOS-based EGII.

$$Z_{AB} = V_{in}/i_{ab} = 1/(G_{m1}G_{m2}Z_L) \tag{11}$$

It is clearly seen from (11) that the proposed circuit of Fig. 2 works as a positive impedance inverter. Furthermore, by substitution of (6) into (11) and by making the assumption that transistors M_1, M_2, M_9 and M_{10} are well matched, then we can write

$$Z_{AB} = \{1/(\mu_n C_{ox} W/L)\}(1/I_B Z_L) = 1/(2I_B K Z_L) \tag{12}$$

Now (12) shows that the driving point impedance Z_{AB} can be linearly controlled by the bias current I_B.

On the other hand, if we interchange the drain leads of M_9 and M_{10} with the drain leads of M_{14} and M_{11}, respectively, in this case the EGII will work as a negative floating impedance inverter, where

$$Z_{AB} = -1/(2I_B K Z_L) \tag{13}$$

This means that the EGII has an ability to simulate both positive and negative impedances and can be electronically tuned.

2.3. *Error analysis*

From routine small signal circuit analysis, the impedance Z_{AB} can be approximately expressed as

$$Z_{AB} = \frac{1}{G_{m1}G_{m2}Z_L}\left[\frac{1}{1+\dfrac{(g_{d15}+g_{d18})(g_{d13}+g_{d20})}{G_{m1}G_{m2}(g_{d13}+g_{d15}+g_{d18}+g_{d20})}}\right] \tag{14}$$

where g_{dj} denotes the drain conductance of the device M_i and $G_{m1} = G_{m2} = (2I_B K)^{1/2}$. Therefore, the percentage of the impedance conversion inaccuracy can be approximated by

$$\frac{\delta Z_{AB}}{Z_{AB}} = \frac{(g_{d15}+g_{d18})(g_{d13}+g_{d20})}{2KI_B Z_L(g_{d13}+g_{d15}+g_{d18}+g_{d20})} \times 100\% \tag{15}$$

For example, if $g_{d13} = g_{d15} = g_{d18} = g_{d20} = 1{\cdot}02 \times 10^{-6}\,\mathrm{AV}^{-1}$, $I_B = 100\,\mu A$, $K = \mu_n C_{ox} W/2L = 3{\cdot}378 \times 10^{-4}\,\mathrm{AV}^{-2}$ and $W/L = 200\,\mu\mathrm{m}/10\,\mu\mathrm{m} = 20$, the resulting impedance conversion percentage error, for a conversion impedance $Z_L = R_L = 10\,\mathrm{k}\Omega$, is approximately equal to 0·15%. If a high value of W/L, or I_B or R_L is used, the percentage error can be further reduced.

2.4. *Frequency response*

The high-frequency response of the general impedance inverter can be approximately given by

$$Z_{AB}(s) = \frac{s/C_2 + 1/(C_1 C_2 R_1)}{s^2 + s[(1/C_1 R_1) + (1/C_2 R_2)] + [(2I_B K) R_1 R_2 + 1]/(C_1 C_2 R_1 R_2)} \tag{16}$$

and

$$\left.\begin{aligned} R_1 &= Z_L/[1 + Z_L(g_{d4} + g_{d8})] \\ R_2 &= (g_{d13} + g_{d15} + g_{d18} + g_{d20})/[(g_{d15} + g_{d18})(g_{d13} + g_{d20})] \\ C_1 &= C_{gs9} + (1 + g_{m9}/g_{m11}) C_{gd9} \\ C_2 &= [C_{gs1} + (1 + g_{m1}/g_{m3}) C_{gd1}]//[C_{gs2} + (1 + g_{m2}/g_{m5}) C_{gd2}] \end{aligned}\right\} \tag{17}$$

where g_{mi} denotes the transconductance of the device M_i, C_{gsi} and C_{gdi} represent the gate-to-source and gate-to-drain capacitances, respectively, of the device M_i. The values of g_m, C_{gs} and C_{gd} depend on the thickness of the oxide (t_{ox}) and the lateral diffusion on the drain and source (L_D) of the device. For a typical value of $\gamma = 0{\cdot}5\,\mathrm{V}^{1/2}$, $t_{ox} = 1.0 \times 10^{-7}\,\mathrm{m}$, $L_D = 0{\cdot}3 \times 10^{-6}\,\mathrm{m}$ and $K = \mu_n C_{ox} W/2L = 3{\cdot}378 \times 10^{-4}\,\mathrm{AV}^{-2}$, and if we choose $W/L = 200\,\mu\mathrm{m}/10\,\mu\mathrm{m} = 20$ for all devices and the current $I_B = 10\,\mu\mathrm{A}$, the values of $C_{gd} = 2{\cdot}10 \times 10^{-14}\,\mathrm{F}$, $C_{gs} = 4{\cdot}88 \times 10^{-13}\,\mathrm{F}$, $g_m = 8{\cdot}22 \times 10^{-5}\,\mathrm{AV}^{-1}$ and $g_d = 1{\cdot}02 \times 10^{-7}\,\mathrm{AV}^{-1}$. If the conversion impedance $Z_L = R_L = 10\,\mathrm{k}\Omega$, then from (16) and (17), $R_1 = 10\,\mathrm{k}\Omega$, $R_2 = 9{\cdot}8\,\mathrm{M}\Omega$, $C_1 = 5{\cdot}30 \times 10^{-13}\,\mathrm{F}$, $C_2 = 2{\cdot}65 \times 10^{-13}\,\mathrm{F}$ and the cut-off frequency will be approximately at 35 MHz.

2.5. *Total harmonic distortion (THD)*

The maximum usable input voltage V_{AB} that can be applied across the general impedance inverter of Fig. 2 depends on the value of the bias current I_B and the conversion impedance Z_L. To maintain less than 1% THD and due to the fact that the VCT1 and VCT2 are formed by MOS source coupled pairs, the voltage V_{AB} and V_L should be restricted to the range (Toumazou *et al.* 1990)

$$-0{\cdot}4(I_B/K)^{1/2} \le V_{AB}, \quad V_L \le 0{\cdot}4(I_B/K)^{1/2} \tag{18}$$

If the conversion impedance $Z_L = R_L$, then from (18), it can easily be proved that the maximum usable voltage of V_L and V_{AB} are, respectively, as

$$|V_L|_{max} = (0{\cdot}4/G_{m1} R_L)(I_B/K)^{1/2} = 0{\cdot}4(\sqrt{2} K R_L) \tag{19}$$

$$|V_{AB}|_{max} = 0{\cdot}4(I_B/K)^{1/2} \tag{20}$$

We can see that if $G_{m1} R_L > 1$, the maximum usable voltage is limited by $|V_L|_{max}$ and if $G_{m1} R_L < 1$ then the maximum usable voltage is limited by $|V_{AB}|_{max}$.

These restricted input voltage ranges have been the major limitation for the application of the EGII. However, the large signal handling capability can be improved by either increasing the channel length L or decreasing the channel width W of the transistors M_1, M_2, M_9 and M_{10}.

3. Applications

Some application examples of EGII will be described in this section and their performances will be presented in § 4. The well known useful application of the EGII is a gyrator or a positive impedance inverter that is used for the simulation of an inductor. From Fig. 2, if the conversion impedance Z_L is a capacitive reactance, $Z_L = 1/sC_L$, the driving point impedance Z_{AB} in this case becomes

$$Z_{AB}(s) = s(C_L/2KI_B) = sL_{AB} \tag{21}$$

where the magnitude of the floating simulated inductance is

$$L_{AB} = (C_L/2KI_B) \tag{22}$$

We see that the inductance L_{AB} can be tuned by the bias current I_B. It should be noted that EGII can also be used to simulate a negative inductance, by interchanging the drain leads of M_9 and M_{10} to the drain leads of M_{14} and M_{11}, respectively. However, this property is seldom needed.

If Z_L is a resistance or $Z_L = R_L$, then the EGII will work as an electronically tunable general floating resistance converter. The magnitude of the converted resistance can be written as

$$|R_{AB}| = (1/2KI_BR_L) \tag{23}$$

where both positive and negative resistances can be realized. This property also found useful application for the study of characteristic phenomena in a nonlinear system (Ohnishi and Inaba 1994).

By cascading two EGIIs as shown in Fig. 4, we obtain a floating capacitance multiplier circuit (Moschyz 1974, Khan and Ahmed 1986). The conversion impedance of EGII2 is a capacitive reactance and EGII2 acts as the conversion impedance of the EGII1. Thus, it can easily be shown that the driving point impedance of the ports AB becomes

$$Z_{AB}(s) = \frac{1}{s(I_{B1}/I_{B2})C_L} = \frac{1}{sC_{AB}} \tag{24}$$

and the magnitude of the floating simulated capacitance is

$$C_{AB} = (I_{B1}/I_{B2})C_L \tag{25}$$

It should be noted that in this case the driving point impedance Z_{AB} becomes independent of the parameter $K = \mu_n C_{ox} W/2L$ and the magnitude of the simulated capacitance can be linearly controlled by the ratio of the bias currents I_{B1}/I_{B2}. Again, if we interchange the drain leads of M_9 and M_{10} to the drain leads of M_{14} and M_{11}, respectively, of the EGII1, then a negative floating capacitance multiplier is obtained.

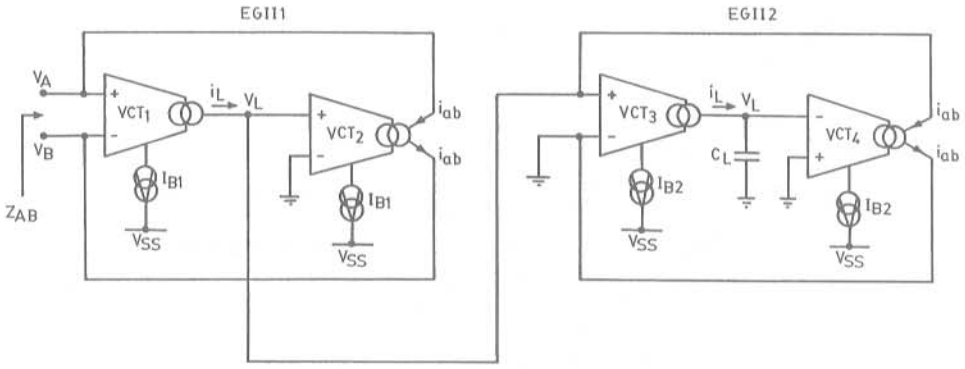

Figure 4. Schematic circuit diagram of the capacitance multiplier.

4. Experimental and simulation results

For experimental purposes, the circuit in Fig. 2 has been constructed on bread-boards. All MOS devices used were in the form of complementary MOS pair (CD 4007). Figure 5 shows the biasing circuit for the current I_B. The properties of the EGII are also demonstrated by using a PSPICE analogue simulation program (Microsim 1980). The CMOS CD4007 transistor parameters were extracted by the method presented by Vladimirescu and Liu (1980), Antognetti and Massobrio (1988), and they can be listed as $K = \mu_n C_{ox} W/2L = 3{\cdot}378 \times 10^{-4}\,\mathrm{AV}^{-2}$, $V_T = 1{\cdot}2\,\mathrm{V}$ and $W/L = 200\,\mu\mathrm{m}/10\,\mu\mathrm{m} = 20$. Figure 6 shows the experimental results and the simulation of floating positive resistances with $V_{DD} = -V_{SS} = 5\,\mathrm{V}$, $Z_L = R_L = 10\,\mathrm{k}\Omega$ and $100\,\mathrm{k}\Omega$, and I_B is varied from $0{\cdot}1\,\mu\mathrm{A}$ to $1000\,\mu\mathrm{A}$. The results show the linear variation of R_{AB} over four decades of the bias current. The DC transfer characteristics of the circuit for $Z_L = R_L = 2\,\mathrm{k}\Omega$ and $I_B = 600\,\mu\mathrm{A}$, $700\,\mu\mathrm{A}$ and $800\,\mu\mathrm{A}$, respectively, are shown in Fig. 7. We can see that the maximum input voltage, for example, for $I_B = 600\,\mu\mathrm{A}$ is approximately equal to $\pm 0{\cdot}4\,\mathrm{V}$, which is close to the predicted value of (19).

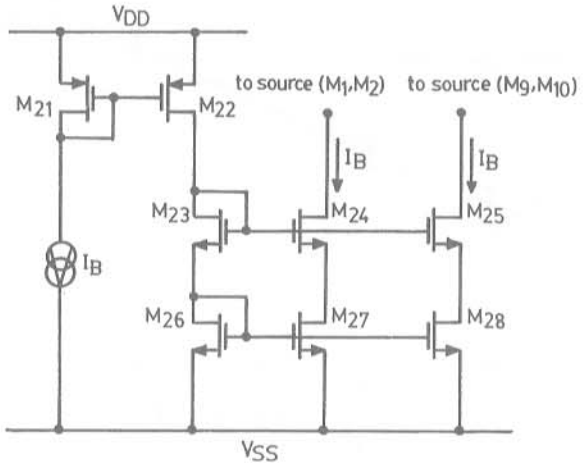

Figure 5. The circuit for the bias currents I_B.

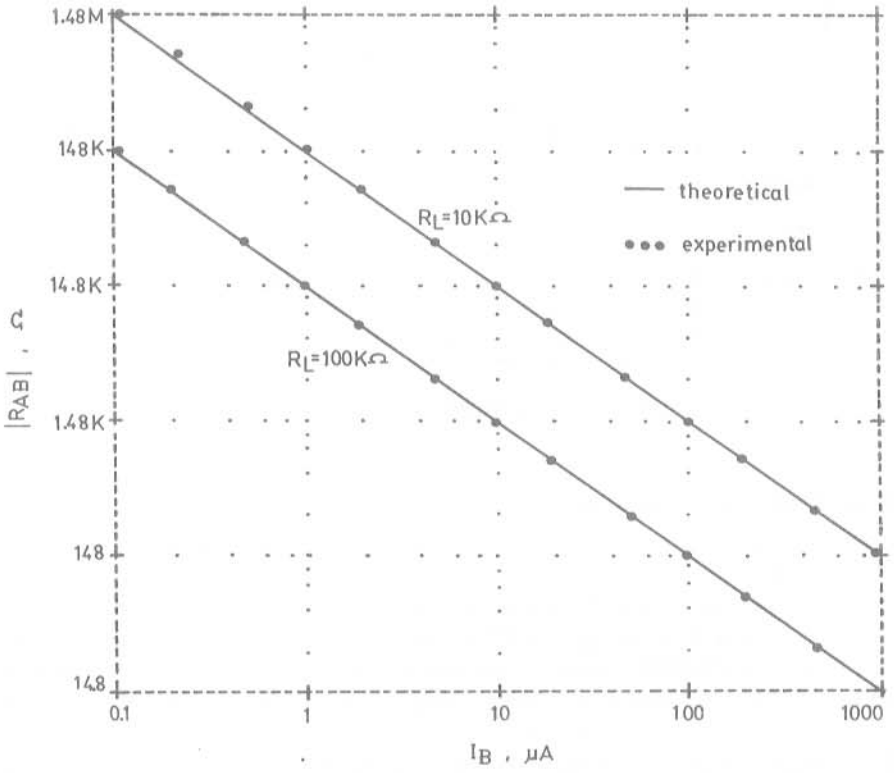

Figure 6. Plots of tunable positive floating resistances R_{AB} versus bias current I_B.

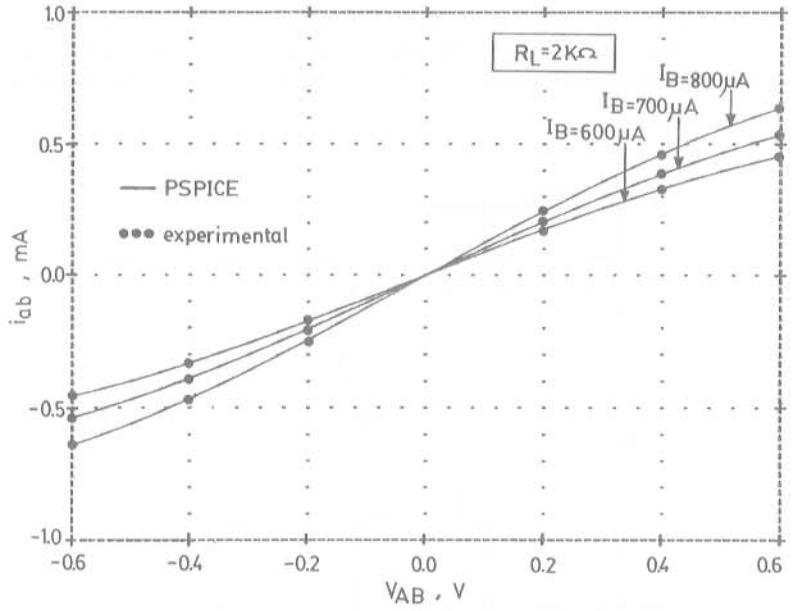

Figure 7. DC transfer characteristics for $I_B = 600\,\mu A$, $700\,\mu A$ and $800\,\mu A$ and for $R_L = 2\,K\Omega$.

Owing to the stray capacitances in the breadboarding circuit, the high-frequency response capability was not measured directly. On the other hand, the high-frequency performance was studied by the use of the PSPICE. The frequency responses for two different values of I_B, i.e. $I_B = 10\,\mu A$, $100\,\mu A$, and three different values of R_L, i.e. $R_L = 30\,k\Omega$, $40\,k\Omega$ and $50\,k\Omega$, are shown in Fig. 8. From (16) if $2I_BKR_1R_2 \gg 1$ the cut-off frequency f_C is determined by $f_C = (2I_BK/C_1C_2)^{1/2}/2\pi\,Hz$, $C_1 = 5{\cdot}30 \times 10^{-13}\,F$, $C_2 = 2{\cdot}65 \times 10^{-13}\,F$ and $K = 3{\cdot}378 \times 10^{-4}\,AV^{-2}$. If the bias current I_B is set to $10\,\mu A$ and $100\,\mu A$, then the cut-off frequencies can be predicted to be $f_C = 35\,MHz$ and $110\,MHz$, respectively.

Next are the simulation results for the case that Z_L is a capacitive reactance, or $Z_L = 1/sC_L$. The magnitude of the floating simulated inductances are shown in Fig. 9, for two different values of C_L, i.e. $C_L = 0{\cdot}001\,\mu F$ and $0{\cdot}01\,\mu F$. The values of the simulated inductances are in close agreement with the predicted values of (22). Figure 10(a) shows the use of the floating simulated inductor to realize an electronically tunable lowpass RL filter. Because the conversion capacitance $C_L = 0{\cdot}001\,\mu F$, $I_B = 100\,\mu A$, then from (22) the value of $L_{AB} = 14{\cdot}8\,mH$. If the output resistor $R_1 = 1\,k\Omega$, $5\,k\Omega$ and $10\,k\Omega$, Fig. 10(b) shows that the cut-off frequencies f_C of the network are at 11 kHz, 54 kHz and 108 kHz, respectively.

The performance of the capacitance multiplier circuit of Fig. 4 is demonstrated through the use of an electronically tunable active high-pass RC filter in Fig. 11(a). The external resistor $R_1 = 1\,k\Omega$ and the conversion capacitance $C_L = 0{\cdot}001\,\mu F$. The bias current ratio I_{B1}/I_{B2} is set to $I_{B1}/I_{B2} = 100\,\mu A/100\,\mu A$, $100\,\mu A/10\,\mu A$ and $100\,\mu A/1\,\mu A$; thus the cut-off frequencies f_C are equal to 159 kHz, 15·9 kHz and 1·59 kHz, respectively. The frequency responses of the high-pas filter are shown in Fig. 11(b).

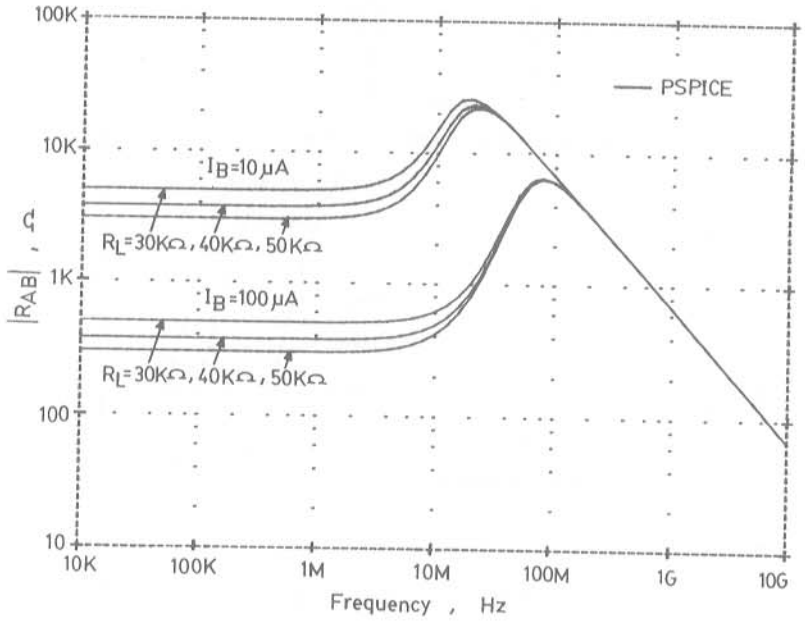

Figure 8. Plots of frequency responses of $|R_{AB}|$.

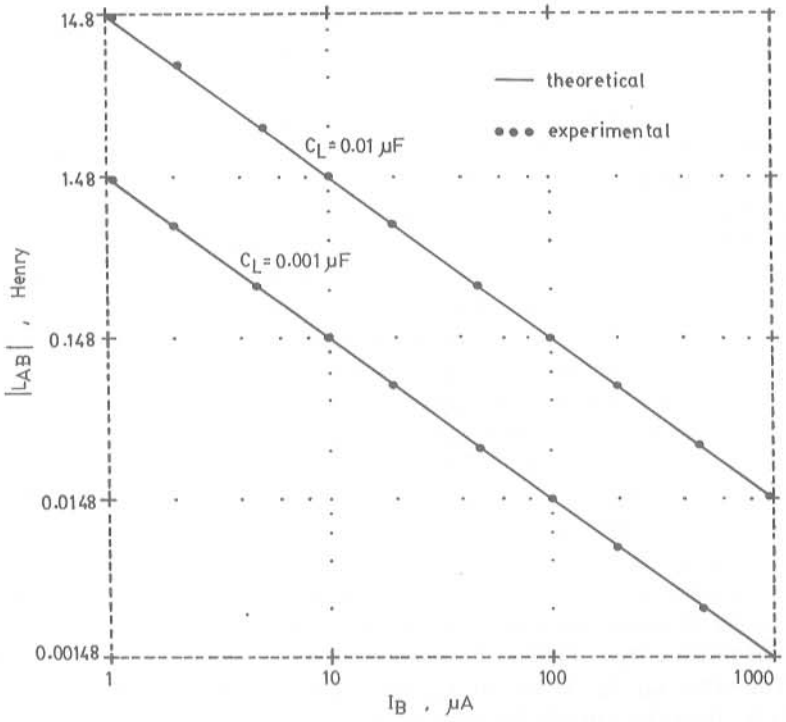

Figure 9. Plots of floating simulated inductances with the bias current I_B.

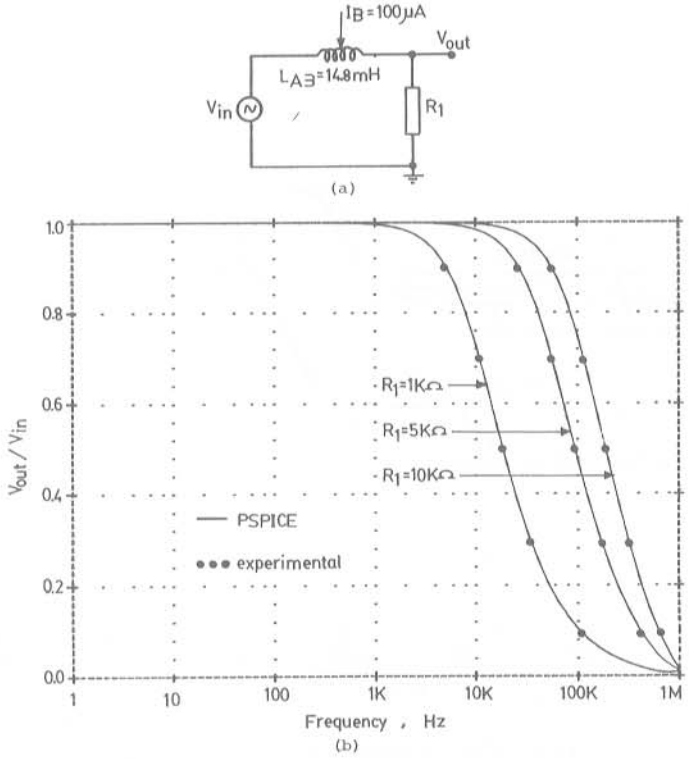

Figure 10. (a) First-order low-pass RL filter; (b) frequency response of the simulated low-pass filter.

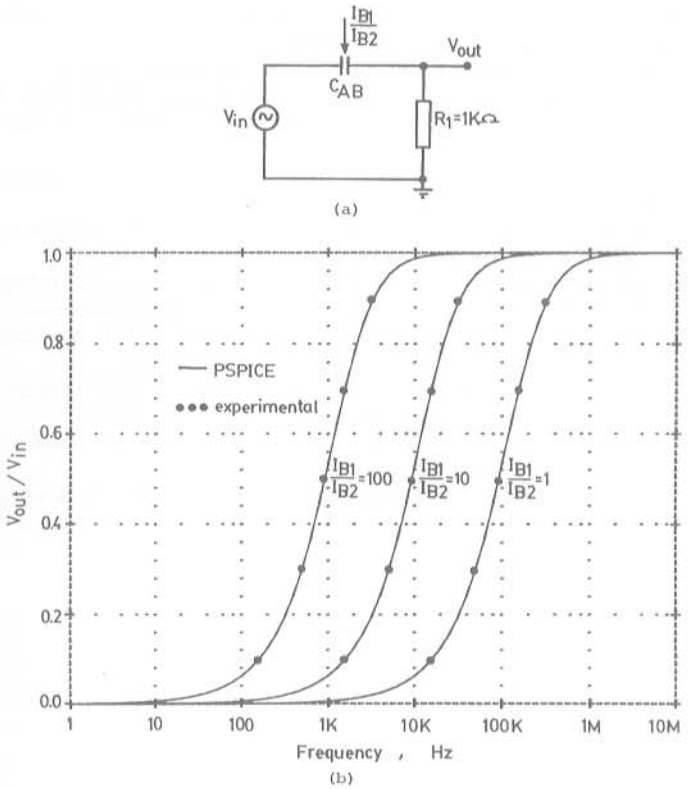

Figure 11. (a) First-order high-pass RC filter; (b) frequency responses of the high-pass filter.

5. Conclusion

An integrable general impedance inverter circuit has been described in this paper. We have termed it the electronically tunable general impedance inverter (EGII), because its terminal impedance is tunable through the external current source I_B. The circuit is composed of one passive component and 28 MOSFETs, which is suitable for fabricating in CMOS LSI implementation. The basic performances of the EGII have been demonstrated through simulation and experimental results. Some applications of the EGII have also been discussed.

Acknowledgments

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