BY JONSENSER ZHAO • PULSE

A new calculation for designing multilayer planar spiral inductors

A NEW, SIMPLE, AND ACCURATE EXPRESSION LETS YOU CALCULATE THE COUPLING FACTOR BETWEEN MULTILAYER PCB INDUCTORS.

Planar spiral inductors are less expensive than either chip or coil inductors for PCB (printed-circuit-board)-based designs. Accuracy in designing a spiral inductor is important because it is difficult to modify the inductor once you have built it on the PCB. Some formulas are available for calculating the spiral inductor for RF-IC applications with inductance of less than 100 nH on a single-layer design. For the application of HPNA (Home Phoneline Networking Alliance) or RF-telecom designs, which need inductances of more than 10 µH, no published paper or report accurately calculates spiral inductors with a large value in multiple layers.

Three options exist for designing large planar spiral inductors on a PCB: Increase the number of turns; increase the inner diameter, D_{IN}; or add layers and increase the coupling between multilayers. The first two options occupy more area on the PCB, so the third option is the best way to accommodate a large inductor when there is limited PCB area.

Multilayer planar spiral inductors offer several advantages over other inductors. They have stable inductance, for example, and, if the PCB has a fixed layout, their inductance tolerance is less than 2%. Further, spiral inductors cost less than chip inductors and require a less complex manufacturing process, making them easier to manufacture with low yield loss.

The traditional formula for calculating inductor size is accurate for single-layer planar spiral inductors, but it does not calculate the inductance for planar spiral inductors built on multilayers and connected with via holes (**Figure 1**).

You can calculate a single-layer inductor's value using **Equation 1**:

$$L=[(\mu_0 N^2 D_{AVG} C_1)/2][\ln(C_2/\rho)+C_3\rho+C_4\rho^2)], \qquad (1)$$

where N is the number of turns; μ_0 is the vacuum permeability, $4\pi\times10^{-7}$; ρ is the fill ratio, $(D_{OUT}-D_{IN})/(D_{OUT}+D_{IN})$; D_{AVG} is the average diameter, $(D_{IN}+D_{OUT})/2$; and $C_1\sim C_2$ are factors
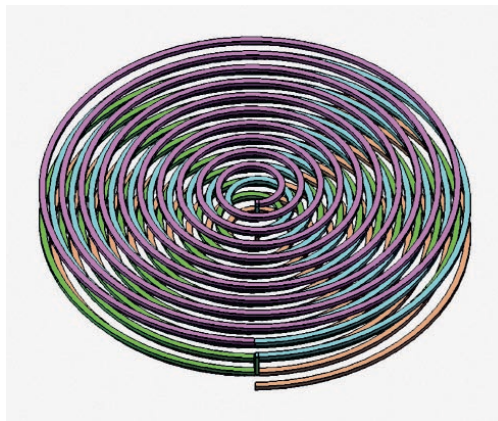

Figure 1 The traditional formula for calculating inductor size is accurate for single-layer planar spiral inductors but does not calculate the inductance of those that employ multiple layers and connect with via holes.

depending on layout (**Table 1**). **Figure 2** defines D_{IN} (inner diameter) and D_{OUT}.

A multilayer inductor creates mutual inductance, however, so 3-D-magnetic-simulation software cannot simulate a multilayer inductor. Even if it could, the process would take a long time, and the results would be inconsistent. Therefore, you must use the following two **equations** for the coupling value, K_C, to obtain the total inductor value with a mutual inductance: $L_{TOTAL}=L_1+L_2\pm2M$, and $M=2\times K_C\times\sqrt{L_1\times L_2}$.

You can obtain another simple and accurate expression for the inductance of a planar spiral by approximating the sides of the spirals using symmetrical current sheets of equivalent current densities (**Reference 1**). Although the accuracy of **Equation 1** decreases as the ratio of space between traces to the trace width increases, it exhibits a maximum error of 8% for a space less than or equal to three times the width. Note that designers typically build practical integrated spiral inductors with space less than or equal to the width because smaller spacing improves the interwinding magnetic coupling and reduces the area the spiral consumes. In PCB design, this practice is not a concern because the intertrace spacing is normally less than the trace width.

Analysis of these **equations** and experimenting with large inductors shows that **Equation 1** is accurate, and the increasing value of the inductor does not affect the accuracy of these **equations**. The result shows an inductance close to the calculated value, with the difference at high frequency due to the actual distribution of parameters throughout the circuit rather than the lumped-parameter analysis of the model (**Figure 3**). Thus, you can use **Equation 1** to calculate a large, single-layer inductor.

Calculations for a multilayer coupled planar spiral inductor are more complex than those for a single-layer spiral inductor.

TABLE 1 LAYOUT-DEPENDENT COEFFICIENTS

Layout	C_1	C_2	C_3	C_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0	0.17
Octagonal	1.07	2.29	0	0.19
Circle	1	2.46	0	0.2

TABLE 2 INDUCTOR TURNS

A	B	C	D
0.184	−0.525	1.038	1.001

The coupling between the inductors on each layer is difficult to simulate because the coupling value depends on the number of turns of the inductor and the distance between the two layers. Experimenting over the range of inductor turns, N, with N equal to a 5- to 20-turns ratio, and the distance between the inductors on the two layers, X, with X equal to a 0.75- to 2-mm distance, yields **Equation 2** to calculate the coupling factor:

$$K_C=[N^2/(AX^3+BX^2+CX+D)\times(1.67N^2-5.84N+65)\times0.64],$$

$$(2)$$

where X is the distance in millimeters between the inductors on the two layers and N is the number of inductor turns that **Figure 2** defines. The inductor turns of both layers must be the same (**Table 2**).

With the coupling factor from **Equation 2** and the single planar-spiral-inductor calculation from **Equation 1**, you can figure the total inductance of a two-layer inductor by using the mutual-inductance formula (**Reference 2**).

On a two-layer coupled inductor, you can calculate the total inductance with the following layout information: 15.75 turns, 0.127-mm (5-mil) width and trace
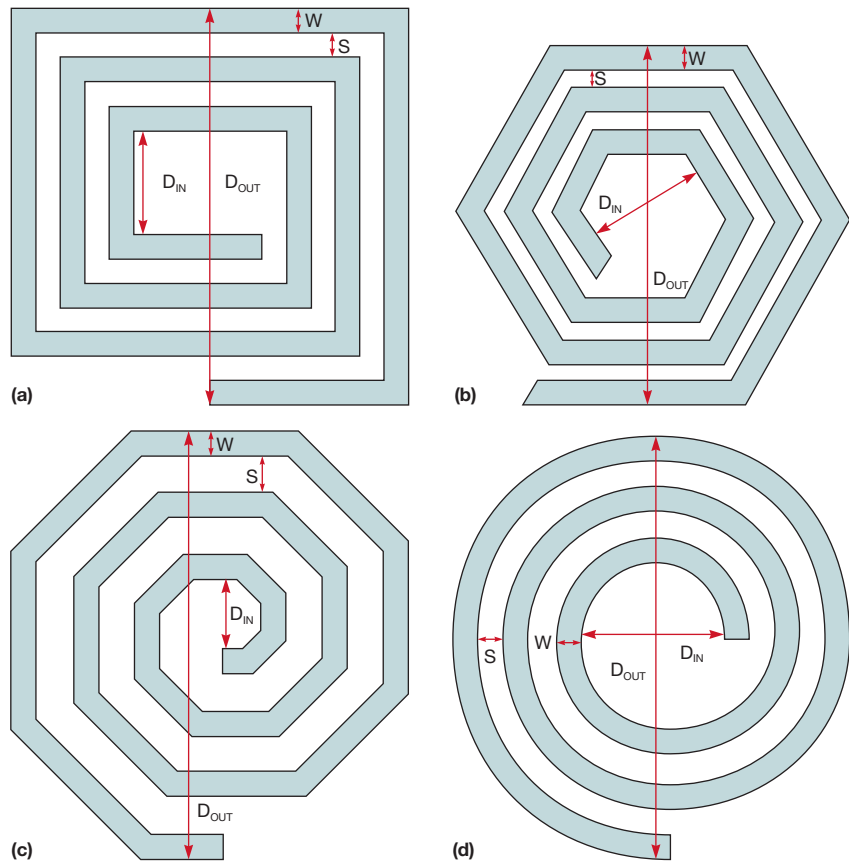

Figure 2 The C_1~C_4 factors depend on layout: square (a), hexagonal (b), octagonal (c), and circle (d).

spacing, 1.0922-mm (43-mil) D_{IN}, and 0.75-mm interlayer distance. First, you must analyze the circular layout to find D_{OUT} and D_{AVG} to obtain the single-layer inductance, L_S, and the coupling factor, K_C: $D_{OUT}=D_{IN}+2\times W+(W+S)\times(2N-1)=8.9972$; $D_{AVG}=(D_{IN}+D_{OUT})/2=5.0927$; $\rho=(D_{IN}+D_{OUT})/(D_{OUT}+D_{IN})=0.7855$; $L_S=[(\mu N^2 D_{AVG}C_1)/2]$

CH1 L_S	10.01 µH/REF 0H	0 52.772 µH

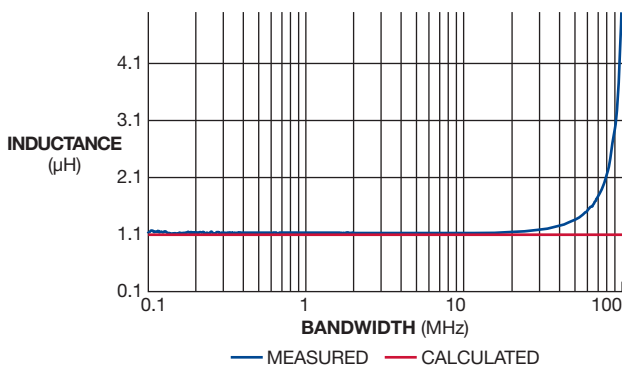| NO.	FREQUENCY	VALUE
0	113.359120598 MHz	52.772 µH
1	100 kHz	1.1618 µH
2	1 MHz	1.1197 µH
3	5 MHz	1.108 µH
4	10 MHz	1.1071 µH
5	15 MHz	1.1137 µH
6	20 MHz	1.1267 µH
7	30 MHz	1.1703 µH

Figure 3 An analysis of the equations shows an inductance close to the calculated value.
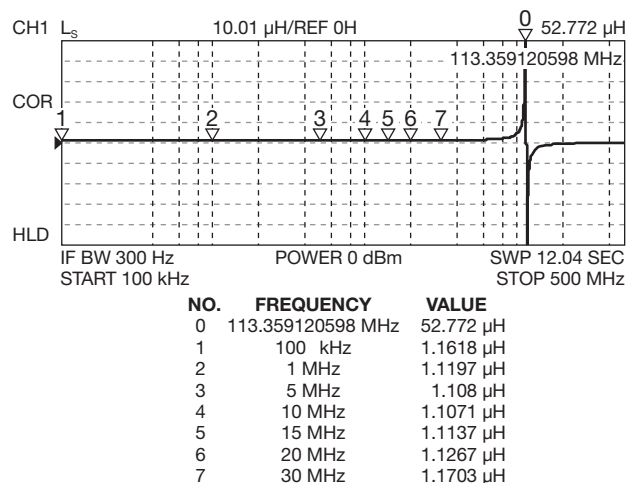
Figure 4 The measured inductor's frequency response is close to the theoretical calculation to a frequency as high as 100 MHz.

TABLE 3 FOUR-LAYER-STACK STRUCTURE			
Layer 1	Spiral inductor	1 mil	0.025 mm
Layer 2	Substrate	34 mils	0.85 mm
	Spiral inductor	1 mil	0.025 mm
Layer 3	Substrate	34 mils	0.85 mm
	Spiral inductor	1 mil	0.025 mm
Layer 4	Substrate	34 mils	0.85 mm
	Spiral inductor	1 mil	0.025 mm

NO.	FREQUENCY	VALUE
0	113.359120598 MHz	921.51 m
1	100 kHz	1.1373 m
2	1 MHz	10.032 m
3	5 MHz	31.196 m
4	10 MHz	45.67 m
5	15 MHz	55.195 m
6	20 MHz	61.729 m
7	30 MHz	71.491 m

Figure 5 The self-resonant frequency is better than that of a chip inductor with the same value.

$(\ln(C_2/\rho)+C_3\rho+C_4\rho^2)]=10^{-6}H=1\ \mu H$; $K_C=0.64$. Per the mutual-inductance connection **equations**, the total inductance is $L_1+L_2+2\times K_C\times=\sqrt{L_1\times L_2}=3.28\ \mu H$.

In a design with more than two layers, there are more coupling factors between any two layers. You can use the same method to obtain each coupling factor and then use the total inductance per the mutual-inductance connection formulas. You can also calculate a four-layer spiral inductor with 15.75 turns, a 5-mil-wide trace, a 5-mil trace spacing, and a 43-mil circular inner diameter. **Table 3** shows the stack structure of the PCB. You must first calculate the single-layer inductance, L_S, which is 1 μH. It has six coupling factors: K_{C12}, K_{C13}, K_{C14}, K_{C23}, K_{C24}, and K_{C34}. $K_{C12}=K_{C23}=K_{C34}=0.618$, $K_{C13}=K_{C24}=0.459$, and $K_{C14}=0.294$. So the total inductance is: $L_1+L_2+L_3+L_4+(2\times K_{C12}+2\times K_{C13}+2\times K_{C14}+2\times K_{C23}+2\times K_{C24}+2\times K_{C34})\times L_1=10.132\ \mu H$. The four-layer inductor has a 10.1-μH inductance.
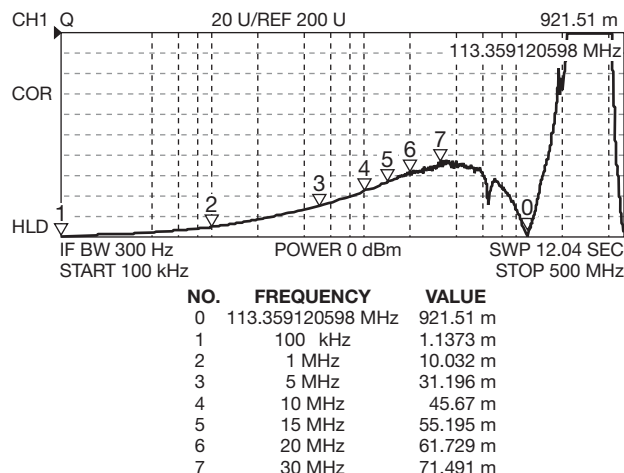
Several samples with different sizes and structures verify the new calculation and measure and compare samples. To perform the verification, you must first increase the size of the single-layer planar inductor and then increase the number of turns from four or five to 15. You must also increase the track width from 4 to 200 microns and increase D_{IN} from 100 to 2400 microns. The inductance calculated using **Equation 1** is 1.1 μH. **Figure 4** shows the measured inductor frequency
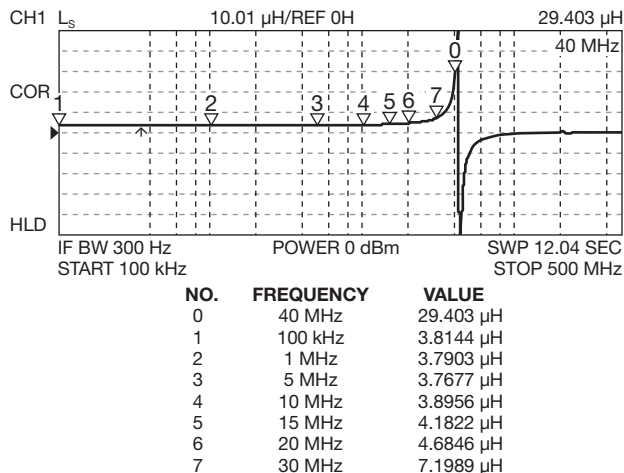
NO.	FREQUENCY	VALUE
0	40 MHz	29.403 µH
1	100 kHz	3.8144 µH
2	1 MHz	3.7903 µH
3	5 MHz	3.7677 µH
4	10 MHz	3.8956 µH
5	15 MHz	4.1822 µH
6	20 MHz	4.6846 µH
7	30 MHz	7.1989 µH

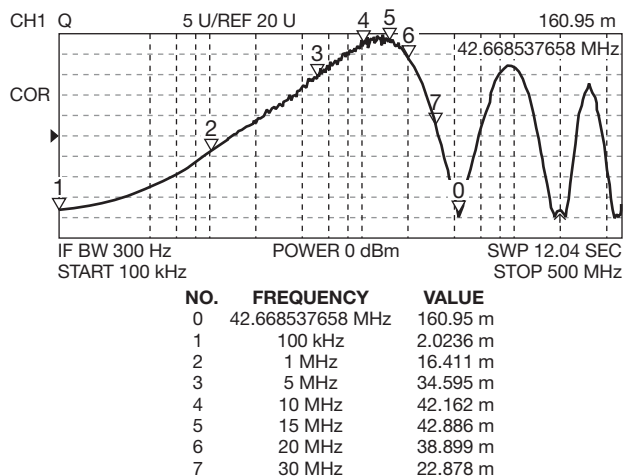Figure 6 The frequency response for the spiral inductor is better than that of a chip inductor with the same value.

NO.	FREQUENCY	VALUE
0	42.668537658 MHz	160.95 m
1	100 kHz	2.0236 m
2	1 MHz	16.411 m
3	5 MHz	34.595 m
4	10 MHz	42.162 m
5	15 MHz	42.886 m
6	20 MHz	38.899 m
7	30 MHz	22.878 m

Figure 7 Two-layer planar spiral inductors have better Q and self-resonant frequency than does a chip inductor.
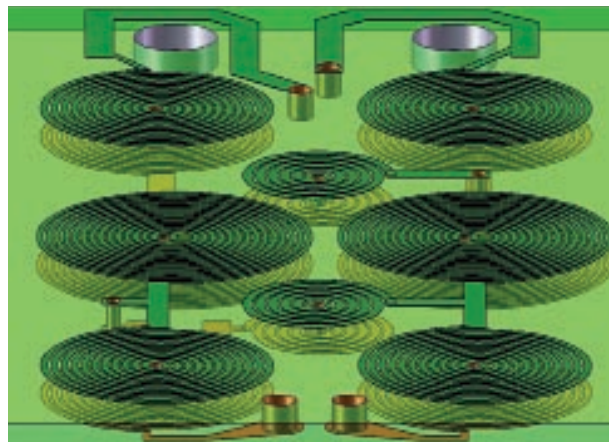

Figure 8 You can build a fifth-order, lowpass filter with a two-layer, coupled spiral inductor.

Figure 9 The performance of the filter matches the simulation result.

response, which is close to the theoretical calculation to a frequency as high as 100 MHz. The Q value and self-reso-nant frequency in **figures 4** and **5** are better than that of the same-value chip inductor. Normally, the chip inductor's Q value is only 15 to 20.

To verify the coupling factor, you build two equally sized, 1.1-µH planar spiral inductors on a two-layer PCB substrate with a thickness of 0.8 mm. The calculated inductor value us-ing **Equation 2** is 3.8 µH. **Figures 6** and **7** show the frequency response. The two-layer planar spiral inductor's Q and self-res-onant frequency are better than that of a chip inductor with the same value.

Figure 8 shows a fifth-order lowpass filter with two-layer coupled planar spiral inductors using the new calculation for the design of this filter. The performance of the filter match-es the simulation result and works for HPNA and other tele-communication applications (**Figure 9**). The simplicity and robustness of these calculations simplify circuit design and optimization applications, which you can incorporate into the computer-circuit model for spiral inductors.**EDN**

REFERENCES

[1] Rosa, Edward B, "Calculation of the self-inductances of single-layer coils," *Bulletin of the Bureau of Standards*, Vol-ume 2, No. 2, 1906, pg 161, http://bit.ly/9YpeeX.
[2] Nilsson, James W, and Susan A Riedel, *Electric Circuits*, Seventh Edition, Prentice Hall, May 17, 2004, ISBN 0131465929.

AUTHOR'S BIOGRAPHY

Jonsenser Zhao is a senior design engineer at the network division of Pulse's Chinese development center, where he is responsible for transformer, fil-ter, and splitter design. Zhao has a bachelor's degree in electronics from the Air Force Missile College (Shaanxi, China). His interests include developing designs for telecommunications applications.