A Silicon-Embedded Transformer for High-Efficiency, High-Isolation, and Low-Frequency On-Chip Power Transfer

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***Abstract*— In this brief, a backside silicon-embedded transformer (BSET) with an improved isolation structure is proposed and demonstrated. The interleaved transformer coils are embedded inside a silicon substrate from the backside and connected to the front-side through vias. The isolation between the coils is achieved by the oxide layer between the Cu coil and the Si substrate, as well as the BCB (BenzoCycloButene) layer covering the backside of the transformer. The 2-mm^2 BSET fabricated shows a best reported monolithic transformer efficiency of over 80% at a low frequency of 20 MHz. A 380 V isolation capability is achieved and shows the potential for various applications, such as USB (Universal Serial Bus) isolation. Only three masks are required for the fabrication. This technology is very suitable for on-chip isolated power transfer applications.**

***Index Terms*— Isolation technology, on-chip transformers, power transfer, through silicon via.**

I. Introduction

RECENTLY, there has been an increasing interest in miniaturization and monolithic integration of transformers for compact isolated low-level power transfer. Among the currently reported monolithic power transformers, coreless transformers [1]–[3] are relatively simple to fabricate and are free of the frequency and current limitations imposed by the magnetic core material, and therefore have already been applied in commercial products [4]. However, the low coil inductance to resistance ratio (L/R) of conventional coreless transformers requires a high operating frequency over 100 MHz to achieve a transformer efficiency of over 70% [1], [3]. Such a high frequency will cause significant power switching and rectifying losses and result in a poor overall efficiency (e.g., 33% [1]) in the isolated power transfer system. A common way to increase the coil L/R ratio of a monolithic power transformer is to apply magnetic core materials for inductance enhancement. The operating frequency of the transformer can then be reduced to around 20 MHz [5], [6]. However, the introduction of magnetic material not only causes core loss and saturation but also increases both the design and fabrication complexity. The reported efficiency is still below 80% [5]. Moreover, most of the reported monolithic power transformers have not considered the isolation capability [3], [5], [6].

Previously, a backside silicon-embedded transformer (BSET) has been proposed and demonstrated to increase the coil L/R ratio of a monolithic power transformer by increasing the metal thickness for resistance reduction [7]. By embedding the interleaved primary and secondary coils inside the silicon substrate from the backside, 100-μm metal thickness was achieved without increasing the chip profile. The front-side chip area overhead is also minimal as the transformer can be built underneath the front-side circuit. However, the reported isolation capability is only 20 V due to the poor isolation design, which is hardly useful in real applications. Moreover, the transformer efficiency is lower than expected (73%) and the operating frequency is still relatively high (50 MHz) due to the nonoptimized design and the electroplated Cu resistivity of 3.9 $\mu\Omega$·cm. Therefore, in this brief, an interleaved BSET with an improved isolation structure, a better design, and an optimized Cu resistivity will be proposed and demonstrated for high efficiency, high-isolation, and low-frequency on-chip power transfer applications.

II. Transformer Design and Fabrication

A. Transformer Design

Fig. 1 shows the schematic 3-D view and cross-sectional view of the proposed interleaved BSET. The interleaved coils were embedded inside the silicon substrate from the backside and connected to the front-side through vias. The three breakdown paths between the two coils are marked as A, B, and C in Fig. 1(b). Path A corresponds to the air breakdown between the exposed pads. The related breakdown voltage (BV) can be increased by increasing the separation between pads. The BV of Path B is determined by the insulation oxide layer

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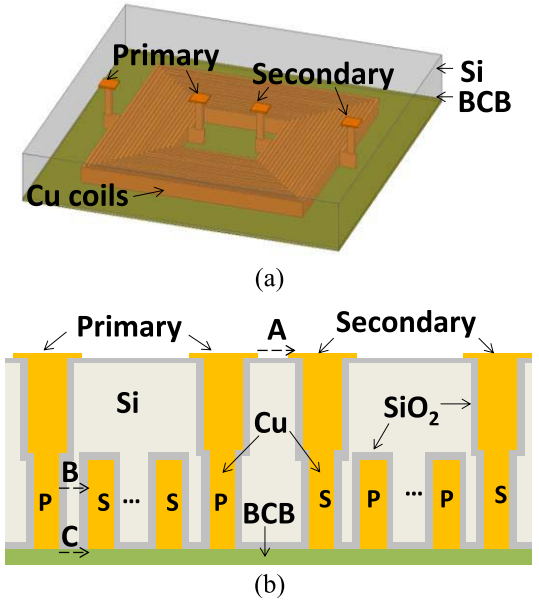

Fig. 1. Schematic (a) 3-D view and (b) cross-sectional view of the proposed interleaved BSET.

between the Cu and Si substrate. It can be increased using thicker and higher quality oxide. Path C corresponds to the air breakdown between adjacent Cu tracks. It is the cause for the poor isolation capability of the previously reported BSET [7]. Since the separation between adjacent Cu tracks cannot be increased much, to achieve a high BV, an isolation BCB layer is applied in this brief to increase the breakdown strength of Path C. For the sake of comparison with prior art, the BSET was designed to have an area of 2 mm^2. The Cu track width, spacing, and thickness are 15, 10, and 100 μm, respectively. A rectangular coil shape and a large coil number of turns of 9:9 are used to increase the inductance density.

B. Transformer Fabrication

The fabrication of the transformer is based on a previously reported backside silicon-embedded inductor technology [8], which is very similar to a through-silicon-via technology. The 300-μm-thick silicon wafer used has a typical CMOS substrate resistivity of 15 Ω·cm. A thermal oxide (1 μm) instead of LPCVD oxide was used as the isolation layer between the Cu and the Si substrate. For post-CMOS integration, PECVD TEOS (TetraEthylOrthoSilicate) oxide can be used to replace the thermal oxide, and whether the TiW layer is sufficient for blocking Cu diffusion also needs to be examined [9]. To protect the thermal oxide from damage, wet etching instead of polishing was used to remove the over-plated Cu and the TiW layer at the backside of the wafer. Finally, a BCB (CYCLOTENE, Dow Chemical) layer was spin coated at the backside of the wafer and cured as the isolation layer for breakdown Path C. The major fabrication steps of the transformer are shown in Fig. 2.

Fig. 3 shows the bottom view of the BSET after backside over-plated Cu wet etching and the cross-sectional view obtained from a test structure for easy cross sectioning of vias. It can be seen that the overetch during the backside over-plated Cu wet etching is not significant, but it still causes some

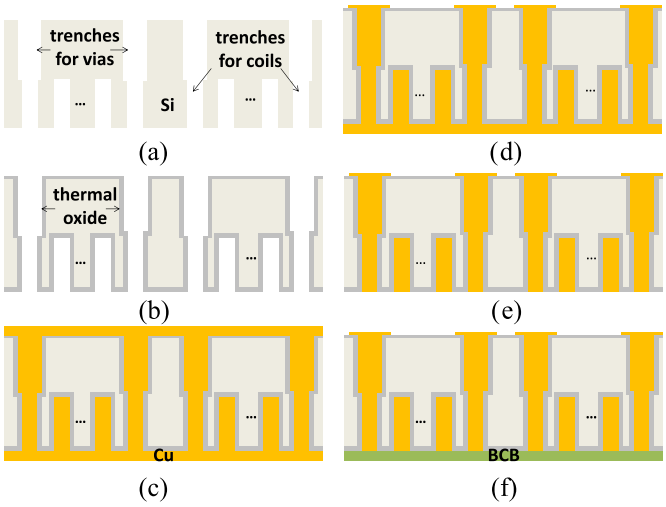

Fig. 2. Schematic of the major BSET fabrication steps: (a) trench formation, (b) thermal oxidation, (c) trench filling, (d) pad formation, (e) backside metal removal, (f) BCB layer formation.

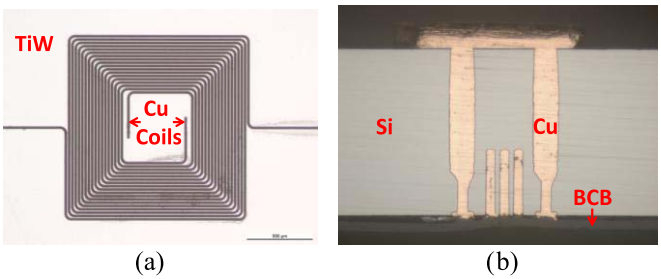

Fig. 3. Microscope images of (a) bottom view of the BSET after backside over-plated Cu wet etching and (b) cross-sectional view of embedded Cu vias and traces as well as BCB layer obtained from a test structure.

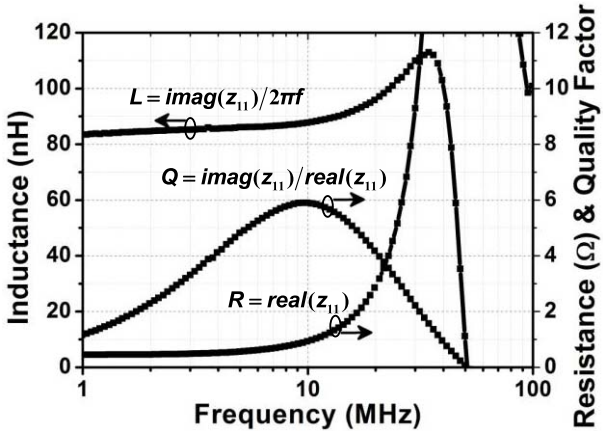

Fig. 4. Measured open-circuit coil inductance, resistance, and quality factor of the BSET.

surface ruggedness. It can also be seen that the BCB layer peels off at some regions. This may be caused by the dicing and polishing for cross section preparation, but still indicates an imperfect BCB coating.

III. Experimental Results

The dc resistances (R_{dc}) of the BSET coils were measured to be 0.445 and 0.446 Ω using the four-point probe method. The corresponding electroplated copper resistivity is 1.9 $\mu\Omega$·cm. The ac performance of the BSET was then

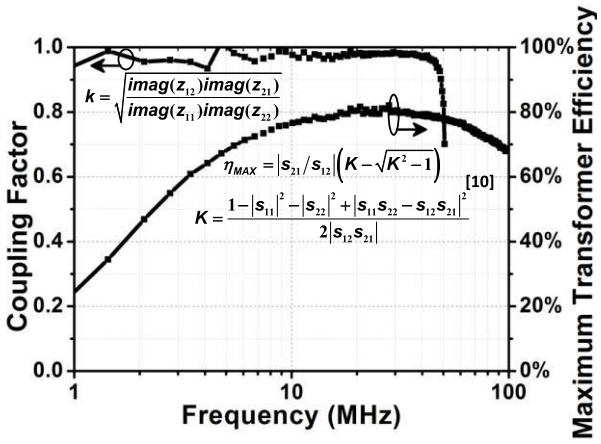

Fig. 5. Measured coupling factor and maximum efficiency of the BSET.

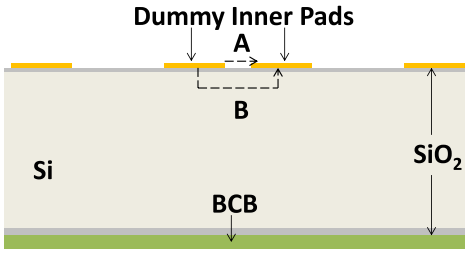

Fig. 6. Illustration of the test structure for BV characterization.

TABLE I
COMPARISON OF MONOLITHIC POWER TRANSFORMERS

	Chen 2008 [1, 2]	Meyer 2010 [3]	Wu 2011 [7]	Wang 2012 [5]	Xing 2013 [6]	This Work
Magnetic Core	No	No	No	Yes	Yes	No
No. of Masks	5	4	3	7	5	3
Area (mm^2)	2	2.3	2	3	5	2
Inductance (nH)	16	46	36	210	35	88
Resistance (Ω)	1.6	2	0.44	1.0	N/A	0.45
Coupling	N/A	0.63	0.95	0.97	0.9	0.98
Efficiency	>70%	78%	73%	75%	N/A	80%
Frequency (MHz)	170	125	50	20	20	20
Isolation (V)	5000	N/A	20	N/A	N/A	380

characterized using an R&S ZVB8 vector network analyzer. Fig. 4 shows the measured open-circuit coil inductance (L), resistance (R), and quality factor (Q). A peak Q of 5.9 is achieved at 10 MHz with an L of 88 nH and an R of 0.94 Ω. The self-resonant frequency is 51 MHz. Fig. 5 shows the measured coupling factor (k) and the maximum transformer efficiency (η_{MAX}), where η_{MAX} is extracted from the measured two-port S-parameters [10]. It can be seen that a good coupling factor of 0.98 and an η_{MAX} of over 80% are achieved at 20–30 MHz. It is worth to note that if a high-resistivity substrate is used, the η_{MAX} can be further improved with a higher Q [11]. Finally, the isolation capability of the BSET was measured using a Tektronix 370A curve tracer. The BV between inner dummy pads (Fig. 6) was first measured to be 880 V, representing the BVs of Path A and Path B. The BV of the BSET was then measured, and hard breakdown was observed when the voltage between the coils approached 380 V. Since the BVs of Path A and Path B are no less than 880 V, this breakdown should be caused by Path C. Considering the reported BCB breakdown strength of 320 V/μm [12], this low BV is potentially due to the imperfect BCB coating on the rugged device backside surface. Nonetheless, this BV is still a big improvement from the previously reported value of 20 V [7], and shows the potential for the structure to be useful for quite a few applications (e.g., USB isolation). Table I compares the performance of the BSET with the prior arts. It can be seen that the best efficiency is achieved at the lowest frequency with a minimal device area, a minimal number of masks, and a reasonably high isolation capability.

IV. CONCLUSION

A BSET with an improved isolation structure was proposed and experimentally demonstrated. The 2-mm^2 BSET achieves a best reported monolithic transformer efficiency of over 80% at a relatively low frequency of 20 MHz and an isolation capability of 380 V with a minimal number of masks of three. This transformer shows great potential for on-chip isolated power transfer applications.

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