Novel High Step-Up DC–DC Converter With Coupled-Inductor and Switched-Capacitor Techniques for a Sustainable Energy System

Yi-Ping Hsieh, Jiann-Fuh Chen, *Member, IEEE*, Tsorng-Juu (Peter) Liang, *Member, IEEE*, and Lung-Sheng Yang

***Abstract*—In this paper, a novel high step-up dc–dc converter is proposed for a sustainable energy system. The proposed converter uses coupled-inductor and switched-capacitor techniques. The capacitors are charged in parallel and discharged in series by the coupled inductor to achieve high step-up voltage gain with an appropriate duty ratio. Besides, the voltage stress on the main switch is reduced with a passive clamp circuit; low on-state resistance $R_{ds(on)}$ of the main switch can be adopted to reduce the conduction loss. In addition, the reverse-recovery problem of the diode is alleviated by a coupled inductor. Thus, the efficiency can be further improved. The operating principle and steady-state analyses of voltage gain are discussed in detail. Finally, a prototype circuit with 24-V input voltage, 400-V output voltage, and 200-W output power is implemented in the laboratory to verify the performance of the proposed converter.**

***Index Terms*—Coupled inductor, high step-up voltage gain, sustainable energy system, switched capacitor.**

I. Introduction

HIGH step-up dc–dc converters are now widely used in many applications. For example, in photovoltaic arraysin a sustainable energy system which are the source with low voltage, the dc–dc converter needs to boost low voltage to high voltage to generate ac utility voltage [1]–[3]. Thus, the high step-up dc–dc converter needs high voltage gain, high efficiency, and small volume [4]–[6]. Theoretically, a conventional boost converter can be adopted to provide high step-up voltage gain with an extremely high duty ratio. In practice, the step-up voltage gain is limited by the effects of power switch, rectifier diode, and equivalent series resistance (ESR) of inductor and capacitor. Also, the extremely high duty-ratio operation may result in serious reverse-recovery problem, low efficiency, and the electromagnetic interference (EMI) problem [7]–[9]. Some converters such as flyback, forward, push-pull, half-bridge, and full-bridge can adjust the turns ratio of a transformer to achieve high step-up voltage gain. However, the main switch of these converters will suffer high voltage spike and high power dissipation caused by the leakage inductor of the transformer [10]. To improve these drawbacks, a nondissipative snubber circuit and an active-clamp circuit are used. However, the cost will be increased due to the extra power switch and high-side driver [11].

Many topologies have been proposed to improve conversion efficiency and achieve high step-up voltage gain [12]–[33]. High step-up gain can be achieved by a switched capacitor or voltage-lift technique [12]–[18]. However, the main switch suffers a high transient current, and the conduction loss is increased. The converterswith the coupled-inductor technique can achieve high step-up gain by adjusting the turns ratio [19], [20]. However, the leakage inductor issue that relates to the voltage spike on the main switch and the conversion efficiency is important. For this reason, the converters using a coupled inductor with an active clamp circuit have been proposed [21], [22]. Also, an integrated boost-flyback converter is presented. The secondary side of the coupled inductor is used as a flyback type to achieve high step-up gain [23], [24]. The energy of a leakage inductor is recycled into the output during the switch-off period. Thus, the voltage spike of the main switch is limited. Additionally, the voltage stress of the main switch can be adjusted through the turns ratio of the coupled inductor. To achieve large high step-up gain, the converter used the secondary side of the coupled inductor used as a flyback and a forward type has been proposed [25]–[27]. Also, many converters using the coupled-inductor technique are proposed to achieve high step-up gain. Several converters that combine the output-voltage stacking to increase voltage gain are proposed [28]–[30]. The boost-sepic converter with the coupled-inductor and output stacking techniques has been proposed [31]. The high step-up boost converters that use multiple coupled inductor of output stacking are proposed [32], [33]. The converters with the coupled-inductor technique increase the voltage gain by adding the number of turns ratio and extra winding stages.

To achieve high voltage gain and high efficiency, this paper proposes a novel high step-up voltage gain converter. The proposed converter uses the coupled-inductor and switched-capacitor techniques to achieve high step-up voltage gain. The coupled inductor is operated as the flyback and forward converters. Thus, the capacitors can charge in parallel and discharge in

Manuscript received October 13, 2010; revised April 12, 2011; accepted June 19, 2011. Date of current version December 6, 2011. This work made use of Shared Facilities supported by the National Science Council, Taiwan, under Award Numbers 99-3113-P-006-004, 100-3113-E-006-004, 100-3113-E-006-013-CC2, and by the Bureau of Energy, Ministry of Economic Affairs, under 100-00204-2. Recommended for publication by Associate Editor R. Zhang.

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Digital Object Identifier 10.1109/TPEL.2011.2160876

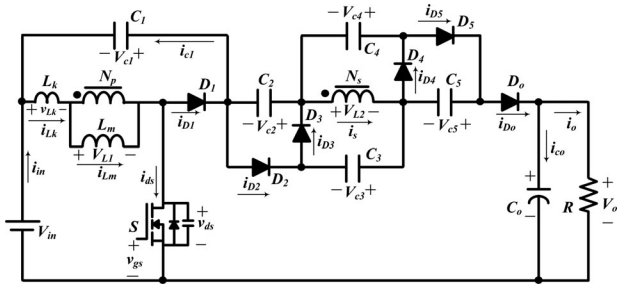

Fig. 1. Circuit configuration of the proposed converter.

series by the secondary side of the coupled inductor. Besides, the secondary-side leakage inductor of the coupled inductor can alleviate the reverse-recovery problem of diodes, and the loss can be reduced. However, the leakage inductor of the coupled inductor may cause high power loss and high voltage spike. Thus, a passive clamping circuit is needed to recycle the energy of the leakage inductor and to clamp the voltage level of the main switch.

II. Operating Principle of the Proposed Converter

Fig. 1 shows the circuit topology of the proposed converter, which is composed of a boost converter with the coupled inductor and switched capacitors. The equivalent circuit model of the coupled inductor includes the magnetizing inductor L_m, leakage inductor L_k, and an ideal transformer. This converter consists of one power switch, six diodes, and six capacitors. The leakage-inductor energy of the coupled inductor is recycled to capacitor C_1, and thus, the voltage across the switch S can be clamped. Also, the voltages across capacitors C_2, C_3, C_4, and C_5 can be adjusted by the turns ratio of the coupled inductor. For this reasons, the voltage level of the switch is reduced significantly and low conducting resistance $R_{\mathrm{ds(on)}}$ of the switch can be used. Thus, the efficiency of the proposed converter can be increased and high step-up voltage gain can be achieved.

To simplify the circuit analysis, the following conditions are assumed.

1) Capacitors C_1–C_5 and C_o are large enough. Thus, V_{c1}–V_{c4} and V_o are considered as constant in one switching period.
2) The power devices are ideal, but the parasitic capacitor of the power switch is considered.
3) The coupling coefficient of the coupled inductor k is equal to $L_m/(L_m+L_k)$ and the turns ratio of the coupled inductor n is equal to N_s/N_p.

The proposed converter operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is analyzed as follows.

A. CCM Operation

Based on the aforementioned assumptions, there are five operating modes discussed in one switching period under CCM operation. Fig. 2 illustrates the typical waveforms and Fig. 3 shows the topological stages of the proposed converter. The operating modes are described as follows.

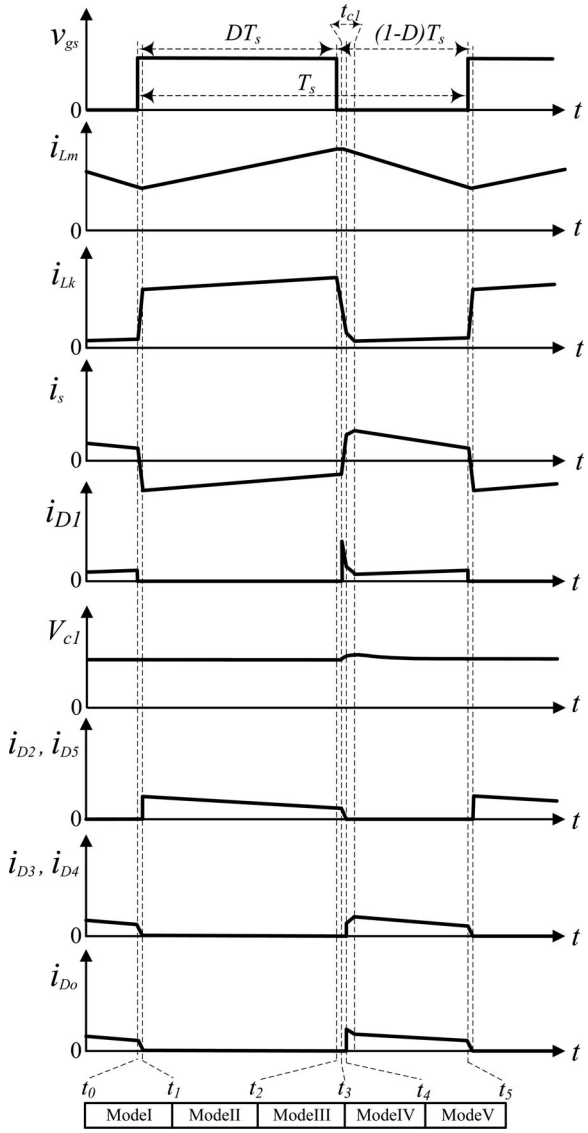

Fig. 2. Some typical waveforms of the proposed converter at CCM operation.

1) *Mode I [t_0, t_1]:* During this time interval, S is turned ON to initiate this mode. Diodes D_1, D_2, and D_5 are reverse biased, and D_3, D_4 and D_o are forward biased. The current-flow path is shown in Fig. 3(a). The primary current of i_{Lk} increases linearly. The magnetizing inductor L_m begins to store the energy from dc source V_{in}. Due to leakage inductor L_k, the secondary-side current i_s decreases linearly. Secondary-side voltages V_{L2}, V_{c2}, and V_{c5} are connected in series to charge the high-voltage output capacitor C_o and to provide the energy to load R. Also, the leakage-inductor energy is recycled to capacitors C_3 and C_4. Because of the leakage inductor of the coupled inductor, the reverse-recovery problem of the diode is alleviated. When current i_s becomes zero, the energy of dc source V_{in} is transferred to capacitors C_2 and C_5 via the coupled inductor. Until the current i_{Do} is equal to zero at $t = t_1$, this operating mode is ended.

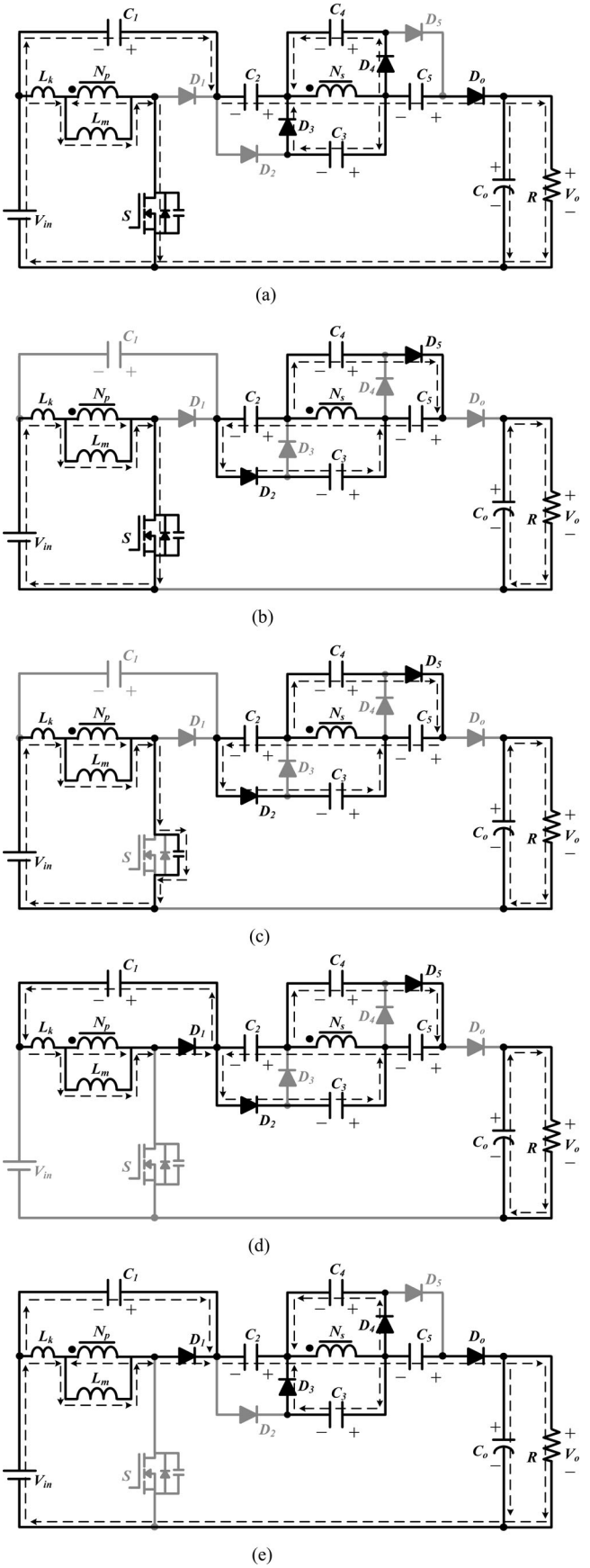

Fig. 3. Current-flow path of operating modes during one switching period at CCM operation. (a) Modes I. (b) Modes II. (c) Mode III. (d) Mode IV. (e) Mode V.

2) *Mode II [t_1, t_2]:* During this time interval, S remains ON. Diodes D_1, D_3, D_4, and D_o are reverse biased, and D_2 and D_5 are forward biased. The current-flow path is shown in Fig. 3(b). The magnetizing inductor L_m stores the energy from dc source $V_{\rm in}$. A part of the energy of dc source $V_{\rm in}$ is transferred to capacitors C_2 and C_5 via the coupled inductor. Also, the energies of C_3 and C_4 are transferred to capacitors C_2 and C_5 together. Meanwhile, voltages V_{c2} and V_{c5} are approximately equal to $nV_{\rm in}+V_{c3}$. The output capacitor C_o provides its energy to load R. This operating mode is ended when switch S is turned OFF at $t = t_2$.
3) *Mode III [t_2, t_3]:* During this time interval, S is turned OFF to initiate this mode. Diodes D_1, D_3, D_4, and D_o are reverse biased, and D_2 and D_5 are forward biased. The current-flow path is shown in Fig. 3(c). The energies of leakage inductor L_k and magnetizing inductor L_m are released to the parasitic capacitor $C_{\rm ds}$ of switch S. Capacitors C_2 and C_5 are charged from dc source $V_{\rm in}$. Output capacitor C_o provides its energy to load R. When the capacitor voltage V_{c1} is equal to $V_{\rm in}+V_{ds}$ at $t = t_3$, diode D_1 is conducted and this operating mode is ended.
4) *Mode IV [t_3, t_4]:* During this time interval, S remains OFF. Diodes D_1, D_2, and D_5 are forward biased, and D_3, D_4, and D_o are reverse biased. The current-flow path is shown in Fig. 3(d). The energies of leakage inductor L_k and magnetizing inductor L_m are released to capacitor C_1. Thus, the voltage across the switch is clamped at $V_{\rm in}+V_{c1}$. The magnetizing energy of L_m starts to transfer energy to capacitors C_3 and C_4. The current $i_{\rm Lk}$ decreases quickly. The secondary-side voltage of the coupled inductor V_{L2} continues to charge capacitors C_2 and C_5 in parallel until the secondary-side current i_s equals zero. Thus, diodes D_2 and D_5 are cut off at $t = t_4$. This operating mode is ended.
5) *Mode V [t_4, t_5]:* During this time interval, S remains OFF. Diodes D_1, D_3, D_4, and D_o are forward biased, and D_2 and D_5 are reverse biased. The current-flow path is shown in Fig. 3(e). The energies of leakage inductor L_k and magnetizing inductor L_m are released to capacitor C_1. Thus, the voltage across the switch is clamped at $V_{\rm in}+V_{c1}$. A part of the magnetizing-inductor energy is released to capacitors C_3 and C_4 in parallel. Simultaneously, secondary side voltage V_{L2} is connected with V_{c2} and V_{c5} in series and the energy of dc sources $V_{\rm in}$, L_m, C_2, and C_5 is released to output capacitor C_o and load R. When primary-side current $i_{\rm Lk}$ is equal to current $i_{\rm Do}$, capacitor C_1 starts to discharge. This mode is ended at $t = t_5$ when S is turned ON at the beginning of the next switching period.

B. DCM Operation

To simplify the analysis of DCM operation, the leakage inductor L_k of the coupled inductor is neglected. Fig. 4 shows typical waveforms of the proposed converter operated in DCM. There are three modes in DCM operation and Fig. 5 shows the operating stages of each mode. The operating modes are described as follows.

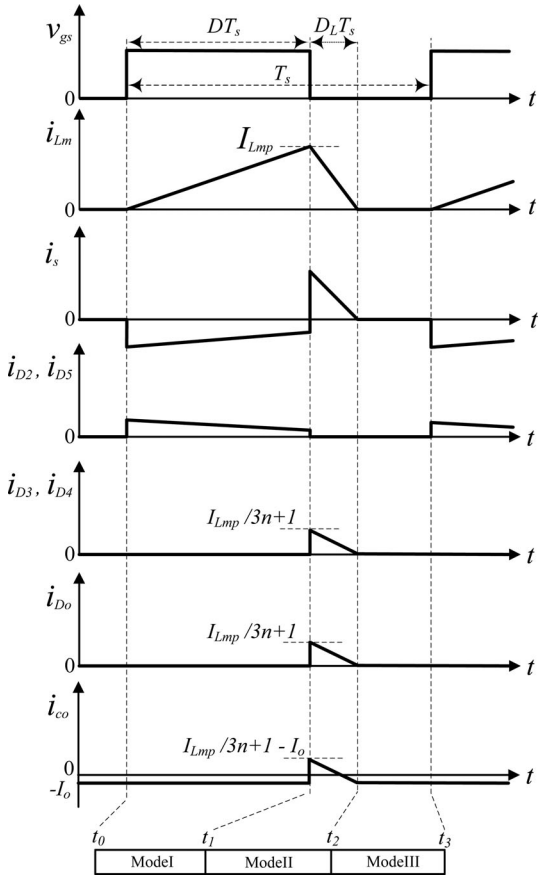

Fig. 4. Some typical waveforms of the proposed converter at DCM operation.

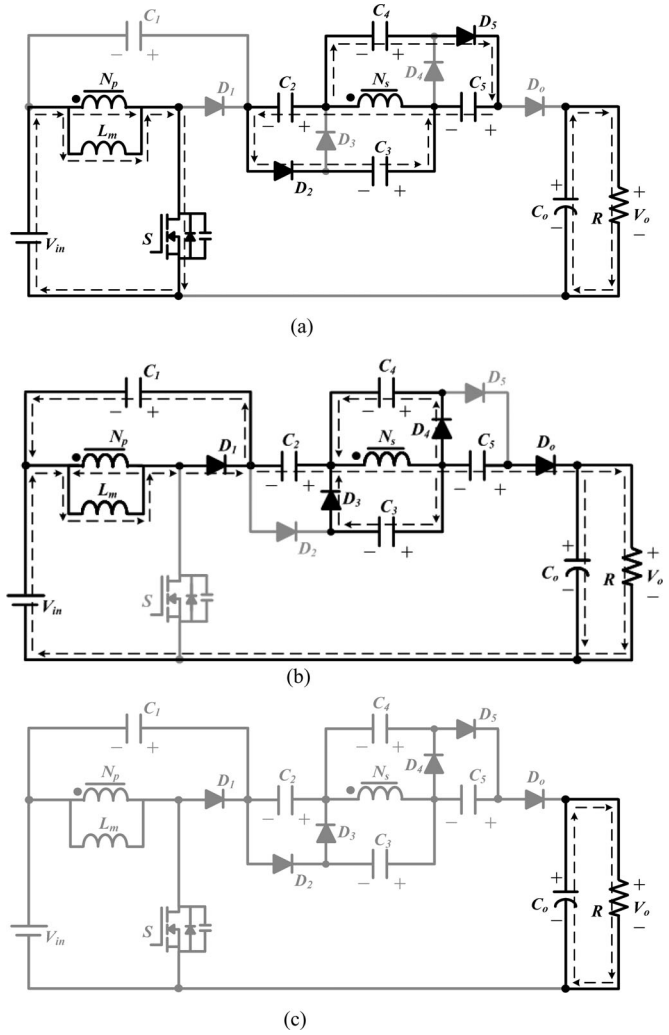

Fig. 5. Current-flow path of operating modes during one switching period at DCM operation. (a) Modes I. (b) Mode II. (c) Modes III.

1) *Mode I [t_0, t_1]:* During this time interval, *S* is turned ON to initiates this mode. The current-flow path is shown in Fig. 5(a). The energy of dc source $V_{\rm in}$ is transferred to magnetizing inductor L_m. Thus, i_{Lm} is increased linearly. Also, the secondary side of the coupled inductor is connected in series with capacitor C_3 or C_4 and releases their energies to charge capacitors C_2 and C_5 in parallel. The output capacitor C_o provides its energy to load *R*. This mode is ended when *S* is turned OFF at $t = t_1$.
2) *Mode II [t_1, t_2]:* During this time interval, *S* is turned OFF to initiates this mode. The current-flow path is shown in Fig. 5(b). The energies of dc source $V_{\rm in}$ and magnetizing inductor L_m are transferred to capacitors C_1, C_o, and load *R*. Similarly, capacitors C_2 and C_5 are discharged in series with dc source $V_{\rm in}$ and magnetizing inductor L_m to capacitor C_o and load *R*. The energy of magnetizing inductor L_m is transferred to capacitors C_3 and C_4 by coil N_s. This mode is ended when the energy stored in L_m is empty at $t = t_2$.
3) *Mode III [t_2, t_3]:* During this time interval, *S* remains OFF. The current-flow path is shown in Fig. 5(c). Since the energy stored in L_m is empty, the energy stored in C_o is discharged to load *R*. This mode is ended when S is turned ON at $t = t_3$.

III. Steady-State Analysis of the Proposed Converter

A. CCM Operation

At modes IV and V, the energy of the leakage inductor L_k is released to capacitor C_1. According to [19], the energy released duty cycle D_{c1} can be expressed as

$$D_{c1} = \frac{t_{c1}}{T_s} = \frac{2(1-D)}{n+1} \tag{1}$$

where t_{c1} is the time interval of the energy of a leakage inductor recycled by capacitor C_1.

By applying the volt-second balance principle of L_k, the voltage across capacitor C_1 can be expressed as

$$V_{c1} = \frac{D}{1-D} \cdot V_{\rm in} \cdot \frac{(1+k)+(1-k)n}{2}. \tag{2}$$

Since the time durations of modes I, III, and IV are significantly short, only modes II and V are considered at CCM operation for the steady-state analysis.

In the time duration of mode II, the following equations can be written based on Fig. 3(b):

$$v_{L1}^{\mathrm{II}} = \frac{L_m}{L_m + L_{k1}} V_{\mathrm{in}} = kV_{\mathrm{in}} \tag{3}$$

$$v_{L2}^{\mathrm{II}} = nv_{L1}^{\mathrm{II}} = nkV_{\mathrm{in}}. \tag{4}$$

Also, the voltage across capacitors C_2 and C_5 can be written as

$$V_{c2} = v_{L2}^{\mathrm{II}} + V_{c3} \tag{5}$$

$$V_{c5} = v_{L2}^{\mathrm{II}} + V_{c4}. \tag{6}$$

During the time duration of modes V, the following equations can be formulated based on Fig. 3(e):

$$v_{L2}^{\mathrm{V}} = V_{\mathrm{in}} + V_{c1} + V_{c2} + V_{c5} - V_o \tag{7}$$

$$v_{L2}^{V} = -V_{c3} = -V_{c4}. \tag{8}$$

The voltage across magnetizing inductor L_m can be derived from (6)

$$v_{L1}^{\mathrm{V}} = \frac{v_{L2}^{\mathrm{VI}}}{n} = \frac{V_{\mathrm{in}} + V_{c1} + V_{c2} + V_{c5} - V_o}{n}. \tag{9}$$

By applying the volt-second balance principle on N_s, the following equation is given:

$$\int_0^{DT_s} v_{L2}^{\mathrm{II}} dt + \int_{DT_s}^{T_s} v_{L2}^{\mathrm{V}} dt = 0. \tag{10}$$

Substituting (4) and (8) into (10), the voltages of capacitors C_2 and C_5 are obtained as

$$V_{c3} = V_{c4} = \frac{Dnk}{1-D} V_{\mathrm{in}}. \tag{11}$$

And substituting (11) into (5) and (6), the voltage across capacitors C_2 and C_5 can expressed as

$$V_{c2} = V_{c5} = \left(nk + \frac{Dnk}{1-D} \right) V_{\mathrm{in}}. \tag{12}$$

Also, using the volt-second balance principle on N_p, the following equation is given:

$$\int_0^{DT_s} v_{L1}^{\mathrm{II}} dt + \int_{DT_s}^{T_s} v_{L1}^{\mathrm{V}} dt = 0. \tag{13}$$

Substituting (2), (3), (9), (11), and (12) into (13), the voltage gain is obtained as

$$M_{\mathrm{CCM}} = \frac{1 + nk(2+D)}{1-D} + \frac{D}{1-D} \cdot \frac{(1-k)(n-1)}{2}. \tag{14}$$

The schematic of the voltage gain versus the duty ratio under various coupling coefficients of the coupled inductor is shown in Fig. 6. It illustrates that the coupling coefficient results in the decline of voltage gain. However, voltage gain is less sensitive to the coupling coefficient. When $k = 1$, the ideal voltage gain is written as

$$M_{\mathrm{CCM}} = \frac{1 + 2n + nD}{1-D}. \tag{15}$$

In Fig. 7, the curve shows the voltage gain versus the duty ratio of the proposed converter, and the converters in [26] and [27] at CCM operation under $k = 1$ and $n = 3$. Since the coupled inductor is worked as flyback and forward converters, voltage gain of the proposed converter is higher than that of the converters in [26] and [27]. Moreover, the utilization rate of the magnetic core of the coupled inductor can be improved.

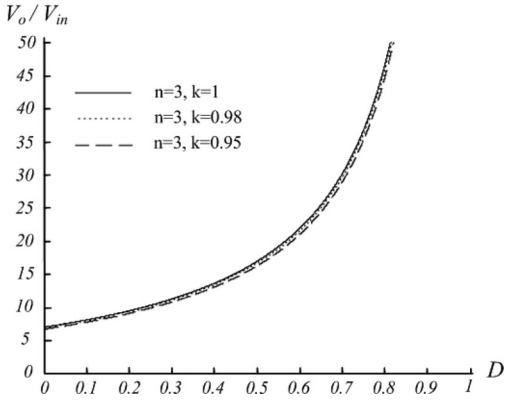

Fig. 6. Voltage gain versus duty ratio at CCM operation under $n = 3$ and various k.

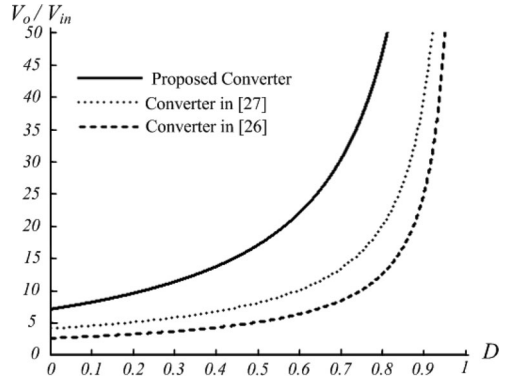

Fig. 7. Voltage gain versus duty ratio of the proposed converter, and the converters in [26] and [27] at CCM operation under $n = 3$ and $k = 1$.

B. DCM Operation

In DCM operation, three modes are discussed. The typical waveforms are shown in Fig. 4. In the time duration of mode I, switch *S* is turned ON. Thus, the following equations can be formulated based on Fig. 5(a):

$$v_{L1}^{\mathrm{I}} = V_{\mathrm{in}} \tag{16}$$

$$v_{L2}^{\mathrm{I}} = nV_{\mathrm{in}}. \tag{17}$$

The peak value of the magnetizing-inductor current is given as

$$I_{Lmp} = \frac{V_{\mathrm{in}}}{L_m} DT_s. \tag{18}$$

Furthermore, the voltage across capacitors C_2 and C_3 can be written as

$$V_{c2} = v_{L2}^{\mathrm{I}} + V_{c3} \tag{19}$$

$$V_{c5} = v_{L2}^{\mathrm{I}} + V_{c4}. \tag{20}$$

In the time interval of mode II, the following equations can be expressed based on Fig. 5(b):

$$v_{L1}^{\mathrm{II}} = -V_{c1} \tag{21}$$

$$v_{L2}^{\mathrm{II}} = V_{\mathrm{in}} + V_{c1} + V_{c2} + V_{c5} - V_o. \tag{22}$$

Also, the voltage across capacitors C_3 and C_4 is expressed as

$$V_{c3} = V_{c4} = -v_{L2}^{\mathrm{II}}. \tag{23}$$

During the time interval of mode III, the following equation can be derived from Fig. 5(c):

$$v_{L1}^{\mathrm{III}} = v_{L2}^{\mathrm{III}} = 0. \tag{24}$$

By applying the volt-second balance principle on the coupled inductor, the following equations are given as

$$\int_0^{DT_s} v_{L1}^{\mathrm{I}} dt + \int_{DT_s}^{(D+D_L)T_s} v_{L1}^{\mathrm{II}} dt + \int_{(D+D_L)T_s}^{T_s} v_{L1}^{\mathrm{III}} dt = 0 \tag{25}$$

$$\int_0^{DT_s} v_{L2}^{\mathrm{I}} dt + \int_{DT_s}^{(D+D_L)T_s} v_{L2}^{\mathrm{II}} dt + \int_{(D+D_L)T_s}^{T_s} v_{L2}^{\mathrm{III}} dt = 0. \tag{26}$$

Substituting (17), (23), and (24) into (26), the voltage is obtained as

$$V_{c3} = V_{c4} = \frac{nD}{D_L} V_{\mathrm{in}}. \tag{27}$$

Similarly, substituting (16), (19), (20), (21), (22), (24), and (27) into (25), the voltage across capacitors C_1, C_2, and C_5 is derived as

$$V_{c1} = \frac{D}{D_L} V_{\mathrm{in}} \tag{28}$$

$$V_{c2} = V_{c5} = \left(n + \frac{nD}{D_L} \right) V_{\mathrm{in}}. \tag{29}$$

Also, the voltage gain is expressed as

$$V_o = \left[\frac{D}{D_L}(3n+1) + (2n+1) \right] V_{\mathrm{in}}. \tag{30}$$

According to (30), the duty cycle D_L can be derived as

$$D_L = \frac{(1+3n)DV_{\mathrm{in}}}{V_o - (1+2n)V_{\mathrm{in}}}. \tag{31}$$

From Fig. 4, the average value of i_{co} is computed as

$$I_{co} = \frac{1}{2} D_L \frac{I_{Lmp}}{3n+1} - I_o. \tag{32}$$

Since I_{co} is equal to zero under steady state, (18), (31), and $I_{\mathrm{co}} = 0$ can be substituted to (32). Thus, (32) can be rewritten as follows:

$$\frac{D^2 V_{\mathrm{in}}^2 T_s}{2\left[V_o - (1+2n)V_{\mathrm{in}}\right] L_m} = \frac{V_o}{R}. \tag{33}$$

Then, the normalized magnetizing-inductor time constant is defined as

$$\tau_{Lm} \equiv \frac{L_m}{RT_s} = \frac{L_m f_s}{R} \tag{34}$$

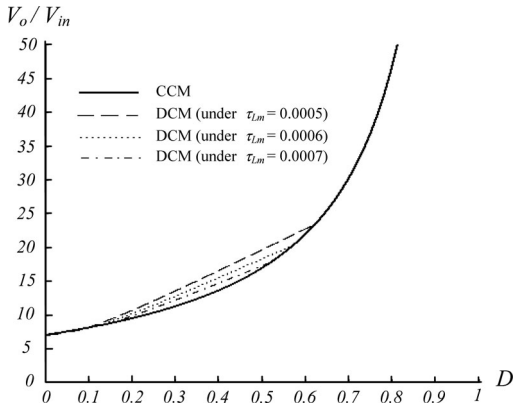

Fig. 8. Voltage gain versus duty ratio at DCM operation under various τ_{Lm} and at CCM operation under $n = 3$ and $k = 1$.

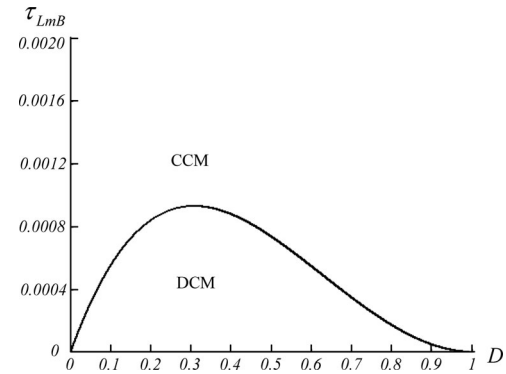

Fig. 9. Boundary condition of the proposed converter under $n = 3$.

where f_s is the switching frequency.

Substituting (34) into (33), the voltage gain is given by

$$M_{\mathrm{DCM}} = \frac{V_o}{V_{\mathrm{in}}} = \frac{1+2n}{2} + \sqrt{\frac{(1+2n)^2}{4} + \frac{D^2}{2\tau_{Lm}}}. \tag{35}$$

The curve of the voltage gain is shown in Fig. 8 which illustrates the voltage gain versus the duty ratio under various τ_{Lm}.

C. Boundary Operating Condition Between CCM and DCM

If the proposed converter is operated in boundary condition mode, the voltage gain of CCM operation is equal to the voltage gain of DCM operation. The boundary normalized magnetizing-inductor time constant τ_{LmB} can be derived from (15) and (35) as

$$\tau_{LmB} = \frac{D(1-D)^2}{2(1+3n)(1+2n+nD)}. \tag{36}$$

The curve of τ_{LmB} is plotted in Fig. 9. If τ_{Lm} is larger than τ_{LmB}, the proposed converter is operated in CCM.

D. Voltage Stress and Current Stress on Power Devices

Based on the description of operating modes in CCM, the voltage stresses of S is expressed as

$$V_{DS} = V_{\text{in}} + V_{c1} = \frac{1}{1-D}V_{\text{in}} = \frac{V_o + nV_{\text{in}}}{3n+1}. \quad (37)$$

Also, the voltage stress of diodes D_1–D_5 and D_o in Fig. 3(c) and (e) are expressed as

$$V_{D1} = V_{\text{in}} + V_{c1} = \frac{1}{1-D}V_{\text{in}} = \frac{V_o + nV_{\text{in}}}{3n+1} \quad (38)$$

$$V_{D3} = nV_{\text{in}} + V_{c3} = \frac{n}{1-D}V_{\text{in}} = \frac{n}{3n+1}(V_o + nV_{\text{in}}) \quad (39)$$

$$V_{D4} = nV_{\text{in}} + V_{c4} = \frac{n}{1-D}V_{\text{in}} = \frac{n}{3n+1}(V_o + nV_{\text{in}}) \quad (40)$$

$$V_{D2} = V_{c2} = \frac{n}{1-D}V_{\text{in}} = \frac{n}{3n+1}(V_o + nV_{\text{in}}) \quad (41)$$

$$V_{D5} = V_{c5} = \frac{n}{1-D}V_{\text{in}} = \frac{n}{3n+1}(V_o + nV_{\text{in}}) \quad (42)$$

$$V_{Do} = V_o - V_{\text{in}} - V_{c3} - V_{c5} = \frac{n}{1-D}V_{\text{in}} = \frac{n}{3n+1}(V_o + nV_{\text{in}}). \quad (43)$$

Under the BCM condition, the average current on the diode D_o is equal to output current I_o when switch S is OFF. The following equations can be derived as

$$\frac{(1-D)T_s i_{Do(\text{peak})}}{2}\frac{1}{T_s} = I_o \quad (44)$$

$$I_o = I_{c2(\text{off})} = I_{c5(\text{off})} \quad (45)$$

where I_o is the boundary current.

According to the current-balance principle on capacitors C_2 and C_5, the following equation can be derived as

$$\int_0^{DT_s} I_{c2(\text{on})}dt + \int_{DT_s}^{T_s} I_{c2(\text{off})}dt = 0 \quad (46)$$

$$\int_0^{DT_s} I_{c5(\text{on})}dt + \int_{DT_s}^{T_s} I_{c5(\text{off})}dt = 0. \quad (47)$$

Substituting (45) into (46) and (47), the following equation is derived as switch is ON:

$$I_{c2(\text{on})} = I_{c5(\text{on})} = \frac{1-D}{D}I_o. \quad (48)$$

Also, the energies of C_2 and C_5 are provided by capacitors C_3 and C_4. The following equation can be derived as

$$I_{c3(\text{on})} = I_{c2(\text{on})} = \frac{1-D}{D}I_o \quad (49)$$

$$I_{c4(\text{on})} = I_{c5(\text{on})} = \frac{1-D}{D}I_o. \quad (50)$$

Using the current-balance principle on capacitors C_3 and C_4, the current is derived as

$$I_{c3(\text{off})} = I_{c4(\text{off})} = I_o. \quad (51)$$

The average current of diodes D_2–D_5 can be derived from charged current of capacitors C_2–C_5. Thus, the following equations are given as

$$\frac{DT_s i_{D2(\text{peak})}}{2}\frac{1}{T_s} = I_{c2(\text{off})} \quad (52)$$

$$\frac{DT_s i_{D5(\text{peak})}}{2}\frac{1}{T_s} = I_{c5(\text{off})} \quad (53)$$

$$\frac{(1-D)T_s i_{D3(\text{peak})}}{2}\frac{1}{T_s} = I_{c3(\text{off})} \quad (54)$$

$$\frac{(1-D)T_s i_{D4(\text{peak})}}{2}\frac{1}{T_s} = I_{c4(\text{off})}. \quad (55)$$

Substituting (45) and (54) into (44), (52), (53), (54), and (55), the peak current of diodes is expressed as

$$i_{D2(\text{peak})} = i_{D5(\text{peak})} = \frac{2V_o}{DR} \quad (56)$$

$$i_{D3(\text{peak})} = i_{D4(\text{peak})} = i_{Do(\text{peak})} = \frac{2V_o}{(1-D)R}. \quad (57)$$

The current flow through the switch based on Fig. 3(b) is expressed as

$$i_{ds(\text{peak})} = n(I_{D2(\text{peak})} + I_{D5(\text{peak})}) + I_{Lmp}. \quad (58)$$

Also, when the switch is turned OFF, the peak current of the switch is equal to the current of diode D_1.

Substituting (32) and (56) into (58), the peak current values of the switch and diode D_1 are expressed as

$$i_{ds(\text{peak})} = i_{D1(\text{peak})} = \frac{2(D + Dn + 2n)V_o}{(1-D)DR}. \quad (59)$$

If the converter is operating at CCM, the current stress is modified to

$$i_{D2(\text{peak})} = i_{D5(\text{peak})} = \frac{2I_{o(\text{BCM})}}{D} + \frac{I_o - I_{o(\text{BCM})}}{1-D} \quad (60)$$

$$i_{D3(\text{peak})} = i_{D4(\text{peak})} = i_{Do(\text{peak})} = \frac{2I_{o(\text{BCM})}}{(1-D)} + \frac{I_o - I_{o(\text{BCM})}}{D} \quad (61)$$

$$i_{ds(\text{peak})} = i_{D1(\text{peak})} = \frac{2(D + Dn + 2n)I_{o(\text{BCM})}}{(1-D)D} + \frac{(2Dn + 1 - D)(I_o - I_{o(\text{BCM})})}{D(1-D)}. \quad (62)$$

IV. Design and Experiment of the Proposed Converter

To verify the performance of the proposed converter, a prototype circuit is implemented in the laboratory. The specifications are as follows:

1) input dc voltage V_{in}: 24 V
2) output dc voltage V_o: 400 V
3) maximum output power: 200 W
4) switching frequency: 50 kHz
5) MOSFET S: IRFB4410ZPBF

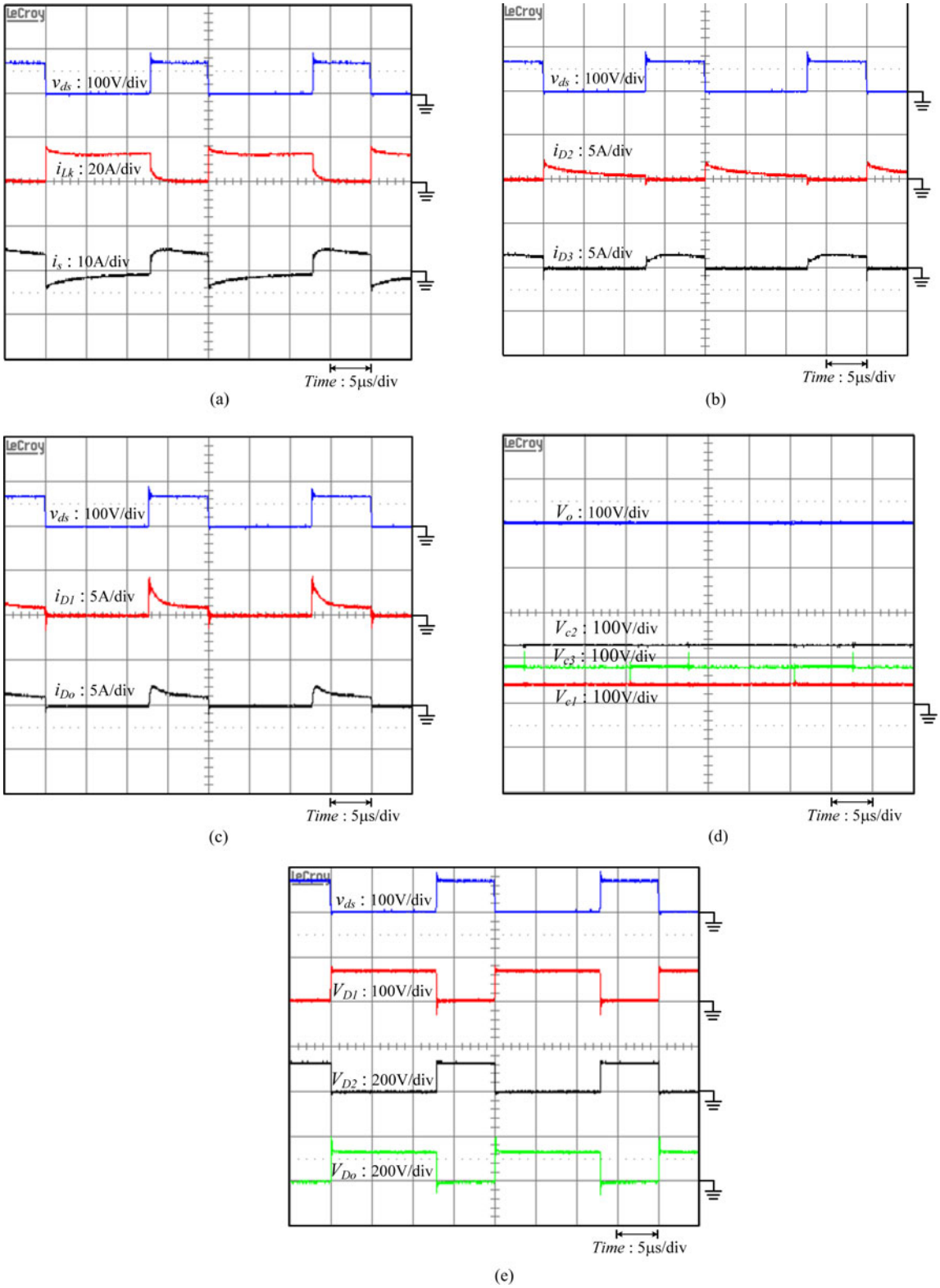

Fig. 10 Experiment results under full-load $P_o = 200$ W.

6) Diodes D_1: MBR30100CT, $D_2/D_3/D_4/D_5/D_o$: DESP30
7) Coupled inductor: ETD-59, core pc40, $N_p : N_s = 1{:}2$, $L_m = 100\ \mu$H; $L_k = 0.4\ \mu$H
8) Capacitors $C_1/C_2/C_3/C_4/C_5$: 22 μF/ 200 V, C_o : 150 μF/ 450 V.

Fig. 10 shows the measured waveforms for full-load $P_o = 200$ W and $V_{\rm in} = 24$ V. The proposed converter is operated in CCM under full-load condition. In the measured waveforms, $V_{\rm ds}$ is clamped at appropriately 93 V during the switch-off period. The waveforms demonstrate that the steady-state analysis is

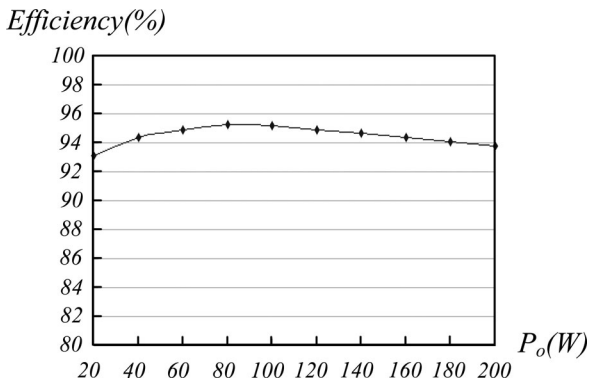

Fig. 11. Experimental conversion efficiency.

correct. Therefore, the low-voltage rated switch can be adopted to achieve high efficiency for the proposed converter.

The waveform of secondary-side current i_s in Fig. 10(a) shows that the proposed converter is operated in CCM because the current is not equal to zero when the switch is turned ON. In Fig. 10(b), the waveforms of i_{D2} and i_{D3} show that capacitors C_2 and C_3 are charged in different time durations. Capacitors C_2 and C_5 are charged in parallel when the switch is turned ON. Capacitors C_3 and C_4 are charged in parallel during the switch-off period and capacitors C_2 and C_5 are discharged in series at the same time. Fig. 10(c) shows that the energy of leakage inductor L_k is released to capacitor C_1 through diode D_1. Fig. 10(d) reveals that V_{c1}, V_{c2}, and V_{c3} satisfy (2), (11), and (12). In addition, output voltage V_o is consistent with (15). Fig. 10(e) shows the voltage stress of the main switch and diodes, and demonstrates the consistency of (38), (39), (41)–(43). The reverse-recovery problem is also alleviated by the coupled inductor. Fig. 11 shows the experimental conversion efficiency of the proposed converter. Maximum efficiency is around 95.28% at $P_o = 80$ W and $V_{\rm in} = 24$ V. The full-load efficiency is appropriately 93.8% at $P_o = 200$ W, $V_{\rm in} = 24$ V, and $V_{\rm out} = 400$ V.

V. Conclusion

This paper has proposed a novel high step-up dc–dc converter with the coupled inductor and switched capacitors. The proposed converter adds passive components without extra winding stage, and uses capacitors charged in parallel and discharged in series with a coupled inductor to achieve high step-up voltage gain and high efficiency. The steady-state analyses of voltage gain and boundary operating condition are discussed. Finally, a prototype circuit of the proposed converter is implemented in the laboratory. Experimental results verify the analysis. The conversion efficiency is 95.28%. Also, the reverse-recovery problem of diodes is alleviated by a coupled inductor. The voltage stress on the main switches is 93 V. Low voltage ratings and low on-state resistance levels $R_{\rm ds(on)}$ switch can be selected. The proposed converter is suitable for a low-voltage source to grid connection.

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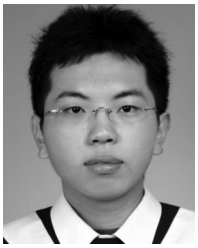

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