CLOCKED SEMI-FLOATING-GATE ULTRA LOW-VOLTAGE CURRENT MIRROR

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ABSTRACT

In this paper we present a low voltage current mirror based on clocked semi-floating-gate transistors used in low-voltage digital CMOS circuits [1]. By imposing offsets to semi-floating-gate nodes the current level may be increased while maintaining a very low supply voltage. The offset voltages are used to shift the effective threshold voltage of the evaluating transistors. The proposed current mirror can operate at supply voltages below 200mV. Two different current mirrors are described; the common gate- and the split gate current mirror. The simulated data presented are obtained using the *Spectre* simulator provided by *Cadence* and valid for a $90nm$ CMOS process.

I. INTRODUCTION

The operation of analog circuits at ultra low supply voltages (ULV) becomes necessary due to semiconductor technology scaling [2]. As supply voltages are forced down by digital constraints, new circuit techniques must evolve to preserve the precision of analog functions in a mixed-signal system. The gate oxide thickness becomes only a few nanometers and the supply voltage has to be reduced in order to ensure device reliability. In order to maintain maximum dynamic range, a low voltage analog circuit must be able to deal with signal voltages that extend from rail-to-rail. This requires traditional circuit solutions to be replaced by new circuit design strategies.

Low supply voltages put an upper limit on the number of gate-source voltages and saturation voltages which can be stacked. The lowest supply voltage can be obtained by biasing MOS transistors in weak inversion, since this gives the smallest gate-source voltage for a given transistor.

An important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not anticipated to decrease much below what is available today. It is necessary that the analog power supply be at least equal to the sum of the magnitudes of the n-channel and p-channel thresholds. This implies that low voltage analog circuits are incompatible with the CMOS technology trends of the future. The challenge is to develop circuit techniques that are compatible with future standard CMOS technology trends [3]. As CMOS process technologies improve, allowable supply voltages are reduced.

Floating-gate (FG) gates have been proposed for ultra low voltage (ULV) and low power (LP) logic [4]. However, in modern CMOS technologies there are significant gate leakages which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom [4]. There are several approaches to FG CMOS logic [5][6][7]. The gates proposed in this paper are influenced by ULV non-volatile FG circuits [8] and recharge logic [9].

Volatile ULV FG digital CMOS logic has been presented [1][10] and the initialization technique is used in this paper to explore ULV analog design. Although the recharge scheme was described for binary ULV logic the same scheme may be applied to analog ULV circuits as well. The current level may be increased compared to the current level determined directly by the supply voltage.

In section II the clocked semi floating gate (CSFG) transistors are presented. The CSFG common gate - and split gate current mirrors are described in section III. Simulated data for the current mirrors are included.

II. CSFG TRANSISTOR

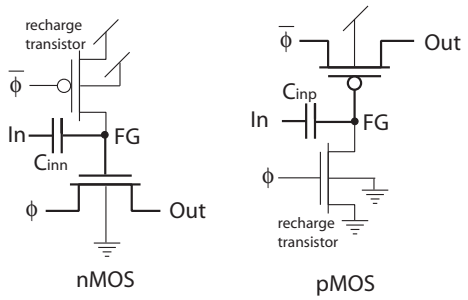

Fig. 1. *nMOS and pMOS clocked semi-floating-gate (CSFG) transistors. The recharge transistors are drawn vertically and the evaluate transistors are drawn horizontally.*

The clocked semi floating gate (CSFG) transistors are shown in Fig. 1. The recharge transistors are drawn vertically and the evaluate transistors are drawn horizontally. By powering up the gate to source voltages in an initialization phase we are able to reduce the supply voltage without decreasing the ON current provided by the enhanced transistors. The aim is to maintain a high current level combined with a very low supply voltage. The enhancement can be viewed as an active threshold voltage shift. Note that the recharge transistor and the evaluate transistor are clocked by inverse signals witch will, to some degree, reduce the capacitive noise imposed on the semi-floating-gate. In order to reduce the charge injection we may add a dummy recharge switch. The noise imposed through parasitic capacitances and charge injection may be reduced by a symmetrical, i.e. quasi differential, design approach.

The ULV logic, i.e. an inverter, in *recharge* and *evaluate* mode is shown in Fig. 2. The ulv gate operation is characterized by:

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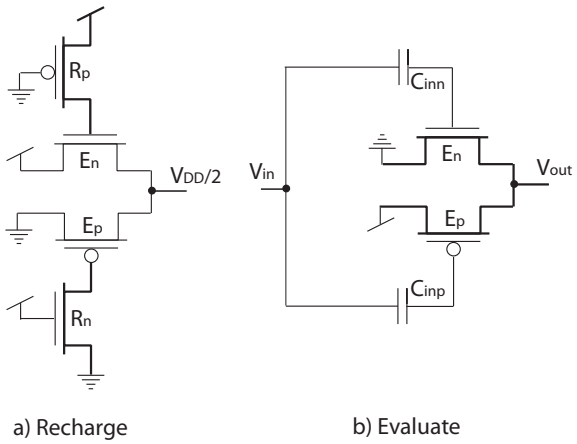

Fig. 2. *Simplified ultra low-voltage semi-floating-gate recharge logic in a) recharge mode and b) evaluate mode.*

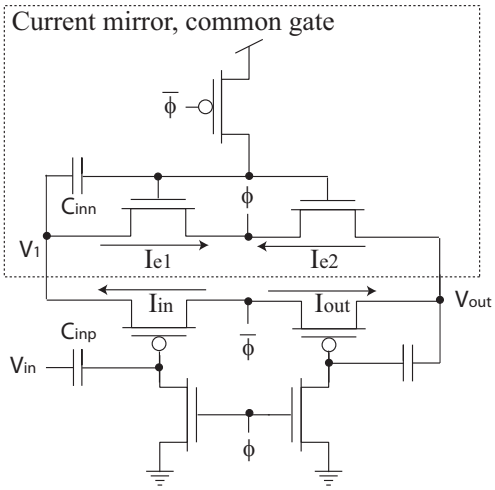

Fig. 3. *CSFG common gate current mirror with minimum sized transistors.*

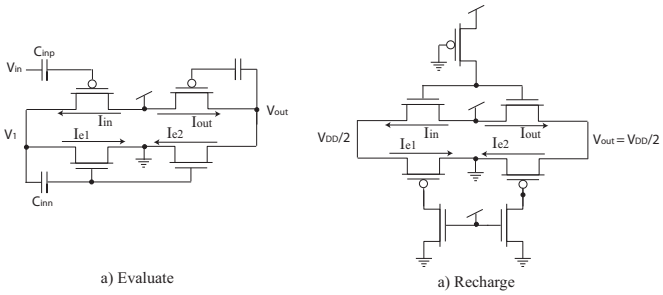

Fig. 4. *CSFG common gate current mirror in* **a** *evaluate mode and* **b** *recharge or initialization mode.*

• **Recharge.** The simplified ULV inverter in recharge mode is shown in Fig. 2 a). The nMOS floating-gate is recharged to V_{DD} and the pMOS floating-gate is recharged to $V_{SS} = gnd$ while the output and input are precharged to $V_{DD}/2 = (V_{DD} - V_{SS})/2$. The output will be forced to $V_{DD}/2$ due to a reversed biased inverter.

• **Evaluate.** The simplified ULV inverter in evaluate mode is shown in Fig. 2 b). The output will be pulled to V_{DD} if a negative transition, $\Delta V_{in} = -V_{DD}/2$, occurs and to V_{SS} if there is a positive transition, $\Delta V_{in} = V_{DD}/2$, applied at the input.

III. CSFG CURRENT MIRROR

In this section two ultra low-voltage CSFG current mirrors are presented.

III-A. Common gate current mirror

The CSFG current mirror is shown in Fig. 3 has a common semi floating-gate. In addition to the current mirror two CSFG pMOS transistors are included, one providing an input current and one pMOS acting as a typical load. Note that with the two CSFG pMOS transistors we obtain two ULV gates, as shown in Fig. 4 that will recharge close to $V_{DD}/2$. In a typical analog circuit the voltage headroom of the internal nodes, i.e. V_{in} and V_{out}, is limited by the supply voltage and the saturation voltage of the transistors. In practice this means that the voltage headroom may be expressed as

$$V_{limit} = V_{DD} - 2V_{sat}.$$

If $V_{sat} = 50mV$ and $V_{DD} = 250mV$ then $V_{limit} = 150mV$ which yields a dynamic voltage range of $50mV$ to $200mV$ and a dynamic range for the transistor currents equal to $1 \cdot 10^{-8}A$ to $3 \cdot 10^{-7}A$. The CSFG transistors offer a way to circumvent the limitation of the currents for ultra low supply voltages. By recharging the semi floating-gates to V_{DD} for the nMOS transistors and gnd for the pMOS transistors and assume a supply voltage equal to $250mV$ the dynamic current range is changed to $3 \cdot 10^{-7}A$ to $3 \cdot 10^{-6}A$.

In the initialization phase the floating-gate is recharged to V_{DD} while the input V_{in} and output V_{out} are recharged to $V_{DD}/2$. If the transistors are not matched the input and output voltages may be slightly different, which may give rise to different currents. The noise imposed, i.e. through parasitic capacitances and charge injection, will affect both evaluate transistors and the relative currents are not altered.

The two transistors constituting the current mirror shares a common input capacitor and the semi floating-gate. In this case the two transistors will be equally biased assuming that the drain voltages are equal. In the recharge phase (Fig. 2 b)) the output and input terminals will be driven to approximately $V_{DD}/2$ assuming a normal load of a pMOS CSFG transistor.

The CSFG common gate current mirror is simulated using $spectreS$ and the result is shown in Fig. 5. The supply voltage V_{DD} is equal to $175mV$ and the voltage range is $45mV$ to $130mV$. The input V_{in} is swept from $V_{DD}/2$ to gnd. The current range is $2 \cdot 10^{-8}A$ to $6 \cdot 10^{-7}A$ which offers a higher current level compared to an unbiased current mirror witch will be able to operate at a current level of $9 \cdot 10^{-9}A$ to $9 \cdot 10^{-8}A$. Note that the

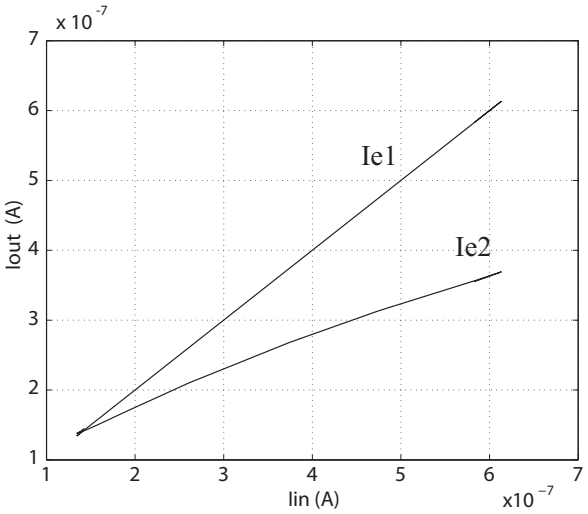

Fig. 5. *CSFG common gate current mirror with minimum sized transistors. The input V_{in} is swept from $V_{DD}/2$ to gnd. The supply voltage $V_{DD} = 175mV$ and the voltage range is $45mV$ to $130mV$. The current range is $2 \cdot 10^{-8}A$ to $6 \cdot 10^{-7}A$ which offers a higher current level compared to an unbiased current mirror witch will be able to operate at a current level of $9 \cdot 10^{-9}A$ to $9 \cdot 10^{-8}A$.*

recharge phase leaves all inputs close to $V_{DD}/2$, while the nMOS semi floating-gate node is equal to V_{DD} and the PMOS floating-gates are set to gnd. The recharge frequency is 100MHz which will secure a minimal leakage. It is evident that the leakage currents of the semi floating gates are neglectable due to the frequent recharge. However, the current mirror will not provide an output current equal to the input current due to the inherent finite input and output resistances or Early effect.

In the evaluation phase the currents can be approximated by the simple models, assuming weak inversion

$$\begin{aligned} I_{e1} &= I_r \cdot e^{k_1\left(V_1 - \frac{V_{DD}}{2}\right)} \cdot \left(1 + \lambda\left(V_1 - \frac{V_{DD}}{2}\right)\right) \\ I_{e2} &= I_r \cdot e^{k_1\left(V_1 - \frac{V_{DD}}{2}\right)} \cdot \left(1 + \lambda\left(V_{out} - \frac{V_{DD}}{2}\right)\right), \end{aligned}$$

where $k_1 = (C_{inn}/C_T) \cdot (1/nU_T)$, C_T is the total capacitance seen by the floating-gate, $C_{inn} = C_{inn1} = C_{inn2}$, U_T is the thermal voltage, n is the slope factor and I_r is the current running through the transistors when $V_1 = V_{DD}/2$. The current level, i.e. I_r is determined by the offset applied in the initialization phase. In this case the current level I_r is equal to the current running through a transistor assuming a gate to source voltage equal to the supply voltage. We may express the relative current, I_{e2}/I_{e1} or deviation assuming that $V_{out} \approx V_{DD} - V_1$

$$\frac{I_{e2}}{I_{e1}} = \frac{1 + \lambda \cdot \left(\frac{V_{DD}}{2} - V_1\right)}{1 + \lambda\left(V_1 - \frac{V_{DD}}{2}\right)}$$

The V_1 and V_{out} will be "inverse" due to the inverting property of CMOS gates. By maximizing the output resistance, assuming

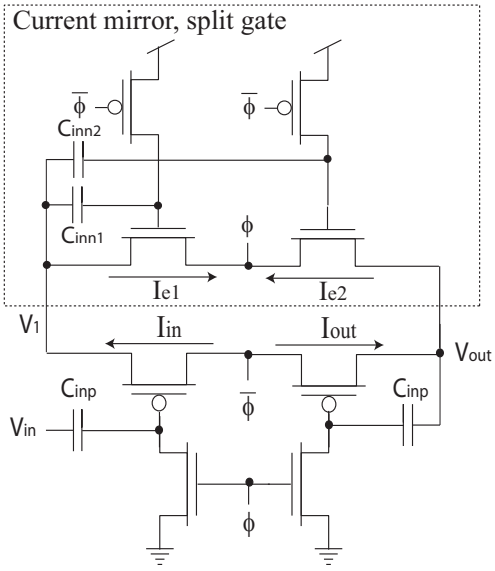

Fig. 6. *CSFG split gate current mirror with minimum sized transistors.*

long transistors, the inaccuracy may be reduced. More advanced current mirror configurations are not suitable for CSFG design. The large deviation between the input and output currents seen in Fig. 5 is due to a very large channel length modulation factor ($\lambda \approx 5.7$). The deviation may be reduced by increasing the transistor length at the expense of reduced current and increased capacitances.

III-B. Split gate current mirror

By separating the gate terminals of the transistors as shown in Fig. 6 we obtain the split gate CSFG current mirror. The gate terminals are recharged by two separate recharge transistors. More interestingly, the transistors do not share a common input capacitor. An advantage of the split gate approach is an increase in transconductance due to less capacitance associated with the floating gates.

The input capacitors may be exploited to compensate for the inaccuracy due to channel length modulation. By changing the relative capacitance of the input capacitors, C_{inn1} and C_{inn2} we may compensate for the inaccuracy due to the Early effect. Assuming that $V_2 \approx V_{DD} - V_1$ we may express the currents in the evaluation phase I_{e1} and I_{e2} as

$$\begin{aligned} I_{e1} &= I_r \cdot e^{k_1\left(V_1 - \frac{V_{DD}}{2}\right)} \cdot \left(1 + \lambda\left(V_1 - \frac{V_{DD}}{2}\right)\right) \\ I_{e2} &= I_r \cdot e^{k_2\left(V_1 - \frac{V_{DD}}{2}\right)} \cdot \left(1 + \lambda\left(\frac{V_{DD}}{2} - V_1\right)\right), \end{aligned}$$

We may exploit k_1 and k_2 to minimize the inaccuracy of the current mirror by solving the equation $I_{e2} = I_{e1}$

$$\begin{aligned} I_{e2} &= I_{e1} \\ k_2 &\approx k_1 + \frac{\ln\left(\frac{1+\lambda\cdot\frac{V_{DD}}{2}}{1-\lambda\cdot\frac{V_{DD}}{2}}\right)}{\frac{V_{DD}}{2}} \end{aligned}$$

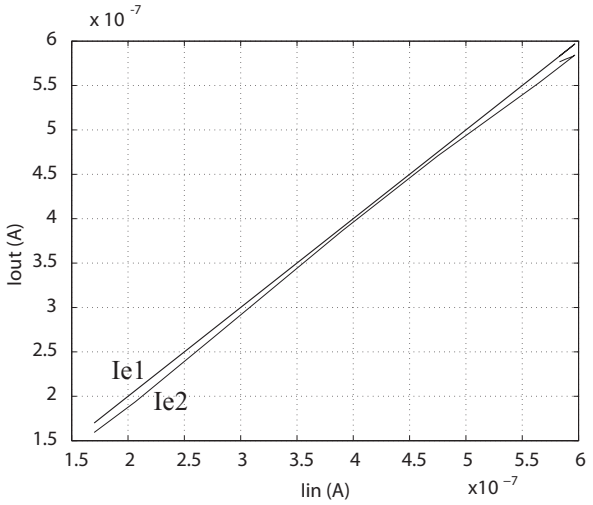

Fig. 7. *CSFG inverter with minimum sized transistors. The input V_{in} is swept from $V_{DD}/2$ to gnd. $C_{inn2} = 6fF$, and $C_{inn1} = 2fF$ and $V_{DD} = 0.175V$. Compared to the common gate the accuracy is significantly improved without increasing the transistor length.*

$$C_{inn2} \approx C_{inn1} + C_T n U_T \cdot \left(\frac{\ln\left(\frac{1+\lambda\cdot\frac{V_{DD}}{2}}{1-\lambda\cdot\frac{V_{DD}}{2}}\right)}{\frac{V_{DD}}{2}} \right),$$

which for $V_{DD} = 0.175V$, $\lambda = 5.7$, $C_{inn1} = 2fF$, $C_T = 6fF$ and $n = 2$ yields $C_{inn2} \approx 6fF$. The increased transconductance of the output transistor compensates for the output conductance of both transistors. If the current mirror operates in strong inversion the capacitance C_{inn2} needs to be increased furthermore due to the reduced relative transconductance g_m/I. The split-gate current mirror will be recharged or initialized in the same manner as the common gate current mirror shown in Fig. 4.

The CSFG split gate current mirror is simulated using $spectreS$ and the result is shown in Fig. 7. The input V_{in} is swept from $V_{DD}/2 = 88mV$ to gnd. Compared to the common gate the accuracy is significantly improved without increasing the transistor length. As expected the output current shows much less deviation from the input current. The actual precision is dependent on the matching of the capacitors.

IV. CONCLUSION

We have presented a ultra low-voltage current mirror based on a ultra low-voltage digital logic style. Clocked semi floating gate transistors are used to provide current mirrors operating at supply voltage close to or even below the inherent threshold voltage of a advanced CMOS process. The current mirror is recharged or initialized in the same way as ULV digital logic [1]. We have presented a split-gate current mirror which exploit relative capacitances to compensate for inaccuracy due to channel length modulation. Simulated data are provided valid for a $90nm$ CMOS process.

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