Substrate Effects in Monolithic RF Transformers on Silicon

Kiat T. Ng, Behzad Rejaei, and Joachim N. Burghartz, *Senior Member, IEEE*

***Abstract*—The effect of substrate RF losses on the characteristics of silicon-based integrated transformers is studied experimentally by using a substrate transfer technique. The maximum available gain is used to evaluate the quality of transformers similarly to that of active devices. The silicon substrate has a pronounced effect on the quality factor and mutual resistive coupling factor of the primary and secondary coils, thereby degrading the maximum available gain of the transformer. A highly structured patterned ground shield is shown to improve the maximum available gain of a transformer at high frequencies, while at low frequencies, it has little effect on the maximum available gain and even degrades the quality factors of the transformer coils. It is shown that the low-frequency degradation of the coil quality factors relates to local eddy currents in the patterned metal shield.**

***Index Terms*—Eddy-current losses, etching, ground shield, integrated transformer, maximum available gain, mutual coupling, periodic ground pattern, quality factor, substrate effect, substrate transfer.**

I. Introduction

THE demand for higher integration levels of RF functions on silicon has generated much interest in integrated RF transformers. Monolithic RF transformers can be used for on-chip impedance matching, balun implementation, and low-noise feedback. Even though transformers built over conductive silicon [1]–[5] are expected to be prone to substrate losses, like spiral inductors on silicon [6], this effect has not been discussed yet extensively. Means to suppress such substrate effects in monolithic transformers have not been discussed in detail either. In [7], we had indicated the significance of those substrate losses by using a substrate transfer technique to stress this issue. Metal ground pattern had been proposed to eliminate the effect of the substrate on the characteristics of spiral inductors [8] and transformers [2].

In this paper, we study experimentally and analyze the effect of the conductive silicon substrate and of metal ground pattern in monolithic RF transformers by using the maximum available gain as a figure-of-merit. The maximum available gain ($G_{\max}$) can be expressed in terms of the quality factors of the coils at the primary and secondary ports, as well as the mutual coupling between the ports. It is the aim of this paper to use $G_{\max}$ to evaluate the distinct impact of these parameters on the overall transformer characteristics. $G_{\max}$ will further be used to analyze the effect of the substrate and a metal ground pattern underneath the transformer coils on the transformer characteristics. Two experiments were carried out by using two different silicon fabrication processes. In process A, the effect of substrate losses on $G_{\max}$ is investigated by using a substrate transfer technique. Test devices to study the reduction of losses in the silicon substrate by using a patterned ground shield are fabricated in process B. An explanation for the effect of a patterned ground on the device will be given.

The organization of this paper is as follows. Section II introduces the $G_{\max}$ as a figure-of-merit to characterize transformers. Section III outlines the measurement procedure. In Section IV, we will present the effect of silicon removal underneath the transformer coils on $G_{\max}$ by using a substrate transfer technique. In Section V, we will present the effect of a metal ground pattern under the transformer coils on $G_{\max}$, and discuss the eddy-current losses of the patterned shield in Section VI. Section VII provides the conclusions of this study.

II. Figure-of-Merit for RF Transformers

The performance of an inductor with regard to its losses can be well described by its quality factor Q, i.e., the ratio of the (magnetic) energy stored in the device to the dissipated energy in a cycle. For transformers, however, no such simple figure-of-merit exists. In applications where the transfer of power is the primary objective, the transformer efficiency can be defined as the ratio of the power delivered to the load to the input power. In view of the dependence of this ratio on the termination impedances, a more favorable choice of a figure-of-merit for RF transformers is the maximum available gain $G_{\max}$, as used for passive RF components in [3], [9]. In terms of the S-parameters s_{ij} $(i, j = 1, 2)$, $G_{\max}$ is given by [10]

$$G_{\max} = \left|\frac{s_{21}}{s_{12}}\right|\left(k - \sqrt{k^2 - 1}\right) \tag{1a}$$

$$k = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} \tag{1b}$$

$$\Delta = s_{11}s_{22} - s_{12}s_{21}. \tag{1c}$$

However, instead of directly using (1a)–(1c), we use the alternative expression

$$G_{\max} = 1 + 2\left(x - \sqrt{x^2 + x}\right) \tag{2a}$$

$$x = \frac{\mathrm{Re}(z_{11})\mathrm{Re}(z_{22}) - [\mathrm{Re}(z_{12})]^2}{[\mathrm{Im}(z_{12})]^2 + [\mathrm{Re}(z_{12})]^2} \tag{2b}$$

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The authors are with the Microwave Components Group, Laboratory of Electronic Components, Technology, and Materials, Delft Institute of Microelectronics and Submicrontechnology, Delft University of Technology, 2628 CT Delft, The Netherlands (e-mail: t.kiat@dimes.tudelft.nl).

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where the components z_{ij} $(i, j = 1, 2)$ of the reciprocal impedance matrix of the transformer can be represented as

$$z_{11} = R_P + j\omega L_P$$
$$z_{22} = R_S + j\omega L_S$$
$$z_{12} = z_{21} = R_M + j\omega L_M. \quad (3)$$

Here, L_P, L_S, and L_M are the primary, secondary, and mutual inductances, respectively, and R_P, R_S, and R_M represent the primary, secondary, and mutual resistances of the device. Note that these quantities are all frequency dependent and cannot be considered as conventional lumped elements. Substitution of (3) into (2b) leads to

$$x = \frac{1 - k_{\mathrm{Re}}^2}{k_{\mathrm{Im}}^2 Q_P Q_S + k_{\mathrm{Re}}^2} \quad (4)$$

where $Q_P = j\omega L_P/R_P$ and $Q_S = j\omega L_S/R_S$ are the quality factors of the primary and secondary coils (with the other coil left open), respectively. The mutual reactive (k_{Im}) and mutual resistive (k_{Re}) coupling factors are given by

$$k_{\mathrm{Im}} = \sqrt{\frac{[\mathrm{Im}(z_{12})]^2}{\mathrm{Im}(z_{11})\,\mathrm{Im}(z_{22})}}$$
$$k_{\mathrm{Re}} = \sqrt{\frac{[\mathrm{Re}(z_{12})]^2}{\mathrm{Re}(z_{11})\,\mathrm{Re}(z_{22})}}. \quad (5)$$

The mutual reactive coupling factor k_{Im} equals the mutual magnetic coupling factor at low frequencies, but the earlier deviates from the latter at high frequencies due to the parasitic capacitances between the primary and secondary coils and between the coils and substrate. The mutual resistive coupling factor k_{Re} approaches zero at very low frequencies where the coupling between the inductors is predominantly inductive. At high frequencies, however, k_{Re} assumes a finite nonzero value because of the parasitic capacitances mentioned above and the eddy currents in the substrate.

Equations (2a) and (4) express the maximum available gain of a transformer in terms of the quality factors of its primary and secondary coils and their mutual coupling. Increasing the quality factors Q_P and Q_S or the mutual coupling factors k_{Im} and k_{Re} leads to a smaller x and, therefore, a higher $G_{\max}$. Therefore, an improvement of the transformer quality can be achieved by an optimization of the quality factors of the coils at the ports and maximization of the mutual coupling between the ports. In Sections IV and V, we experimentally study the effect of substrate RF losses and a patterned ground shield on each of these parameters and the overall transformer maximum available gain.

III. Measurement Procedure

On-wafer measurement was done using an HP-8510C network analyzer and Cascade Microtech air coplanar 200-μm-pitch ground–signal (G–S) and signal–ground (S–G) probes. A line-reflect-match (LRM) calibration procedure has been used so that measurement results can be taken directly from the probe tips. As the measurement pad size was small

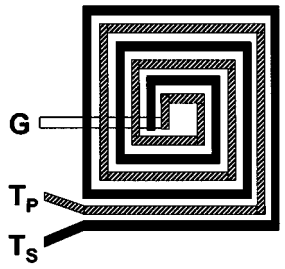

Fig. 1. Bifilar integrated spiral RF transformer, with three turns for both coils.

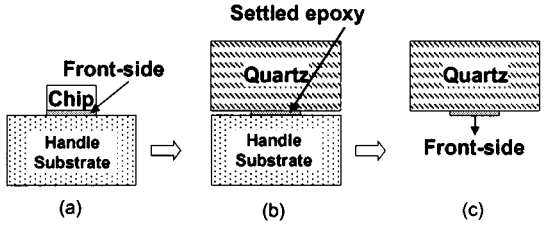

Fig. 2. Substrate transfer sequence. (a) Front side of chip is glued to handle substrate. (b) Silicon of chip is polished and etched, epoxy is settled on the etched surface to quartz. (c) Handle substrate, which have been glued to the front side of the chip is removed.

(50 μm $\times$ 50 μm), as compared to the transformer coil area, no deembedding of pad parasitic was done. The network analyzer was set to take averaged measurement readings. S-parameter measurements were carried out by using a two-port configuration, in which the inner terminations of the primary and secondary coils had been connected together and grounded.

IV. Effect of Substrate Loss on Transformer Characteristics

In order to study the effect of substrate RF losses on transformer characteristics, bifilar transformers (see Fig. 1) were fabricated on a 10-$\Omega\cdot$cm silicon substrate in process technology A. This process had four-level AlCu interconnects featuring nominal metal thickness of 0.85 and 0.63 μm at the metal levels $M2$–$M4$ and at $M1$, respectively, with a vertical dielectric separation of 1.2 μm between adjacent metals. Both coils of each three-turn transformer used in this experiment were built at $M4$.

Besides the integrated transformer structures on the lossy silicon substrate, identical structures were built on a lossless quartz substrate by using a substrate transfer technique. For the substrate transfer, silicon was removed completely by polishing and etching of the substrate silicon, and the transformer die was mounted onto a piece of insulating quartz by epoxy glue, as shown in Fig. 2. First, a quartz handle substrate was attached to the chip surface by using dissolvable glue. Mechanical polishing of silicon was then done by holding the chip-cum-handle substrate [see Fig. 2(a)] face down onto a rotating table with diamond sand paper until about 30-μm thickness of silicon remained. Removal of the remaining 30-μm silicon thickness was implemented by reactive plasma etching at room temperature until silicon end-point detection was observed. Epoxy was used to attach another piece of quartz [see Fig. 2(b)] onto the etched surface of the die. The handle substrate at the front side of the chip was then removed [see Fig. 2(c)] by dissolving the glue in

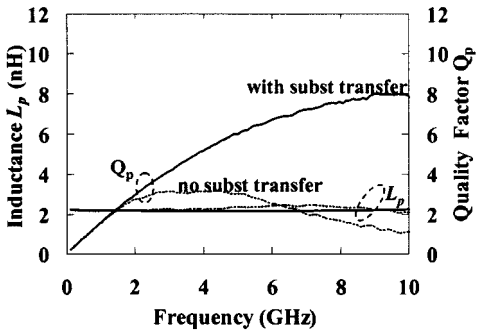

Fig. 3. Measured inductance (L_p) and quality factor (Q_p) of the primary coil of three-turn bifilar transformer with and without substrate transfer.

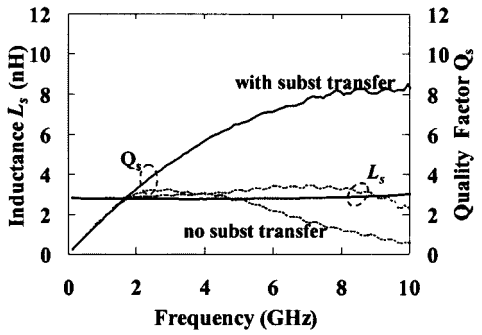

Fig. 4. Measured inductance (L_S) and quality factor (Q_S) of the secondary coil of three-turn bifilar transformer with and without substrate transfer.

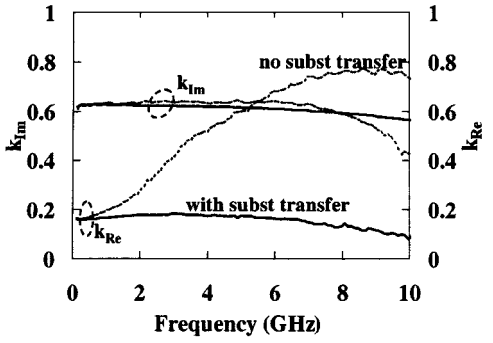

Fig. 5. Measured mutual reactive coupling k_{Im} and mutual resistive coupling k_{Rc} of three-turn bifilar transformer with and without substrate transfer.

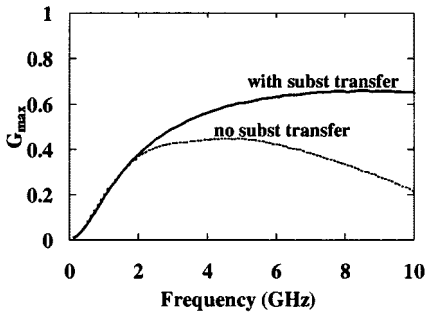

Fig. 6. Measured maximum available gain $G_{\max}$ of three-turn bifilar transformer with and without substrate transfer.

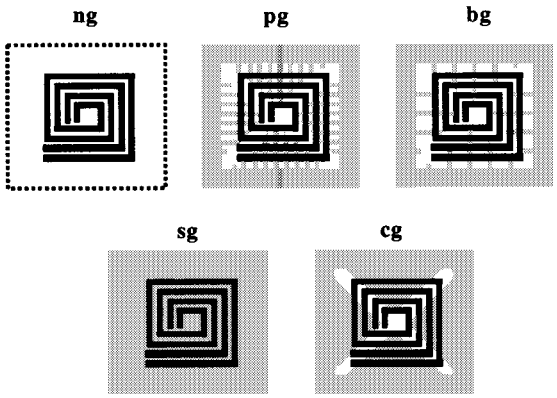

Fig. 7. Top view of two-turn bifilar transformers over various ground patterns: in the absence of ground pattern (ng), patterned ground (pg), bar ground (bg), solid ground (sg) and coarse ground (cg).

acetone. The measurements were done and results were compared with those of the control case, for which no removal of silicon was performed.

In Figs. 3 and 4, Q_P and Q_S are shown as a function of frequency for a 1 : 1-turn-ratio bifilar transformer with three primary and secondary turns each, an overall diameter of 300 μm, and a linewidth and spacing of 12.5 μm each. The removal of silicon yields significantly higher values for the quality factors of the primary and secondary coils, particularly at frequencies above 3 GHz where substrate losses dominate. The influence of the substrate on the mutual reactive coupling factor k_{Im}, however, is small (see Fig. 5). This is because below the resonant frequency of the transformer, the mutual reactive coupling k_{Im} approximately equals the mutual magnetic coupling. The latter only depends on the geometry of the coils if the magnetically induced eddy currents in the substrate are negligible. The mutual resistive coupling constant k_{Re}, however, decreases by the removal of silicon because of a larger reduction in the value of R_M compared to R_P or R_S. The overall effect on the maximum available gain of the transformer is shown in Fig. 6. The maximum attainable $G_{\max}$ increases from 0.4 to 0.6 with the application of the substrate transfer technique for silicon removal. Reduction of the substrate losses clearly leads to a higher $G_{\max}$ at high frequencies and, thus, to an increased bandwidth.

V. Effect of Ground Patterns on Transformer Characteristics

Although useful as a tool in the analysis of substrate effects, substrate transfer techniques cannot easily be applied for an improvement of integrated transformers on mass-produced RF integrated circuits (RFICs) due to presently nonstandard additional technological steps. A possible alternative is the use of a ground pattern to shield the integrated transformer from the silicon substrate. The ground shield prohibits the electromagnetic field from entering the conductive substrate. The flow of magnetically induced eddy currents in the metallic shield, however, leads to a significant decrease in the inductance of the transformer. This effect can be (partly) compensated by patterning the conductor [8], [11], [12].

In order to study the effectiveness of various ground patterns at metal level $M1$, the ground patterns were positioned beneath two-turn bifilar transformers (Fig. 7) by using process technology B. The "pg" ground pattern has metal strips with a 40-μm width and a 10-μm spacing. The "bg" ground pattern has

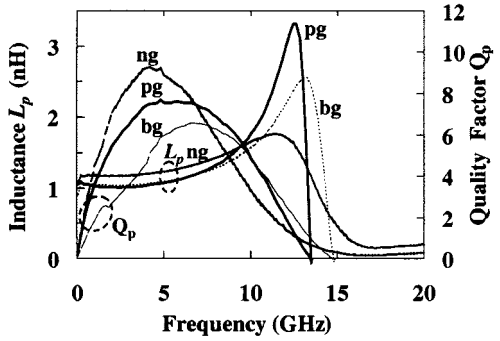

Fig. 8. Measured inductance (L_P) and quality factor (Q_P) of the primary coil of two-turn bifilar transformers over various ground patterns on 15-Ω·cm silicon substrate.

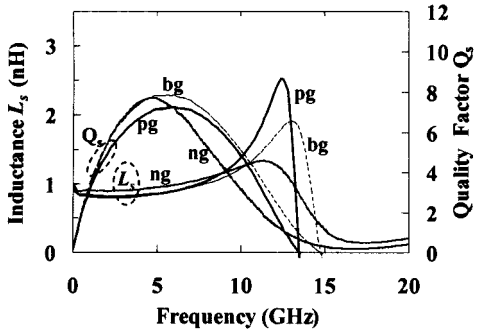

Fig. 9. Measured inductance (L_S) and quality factor (Q_S) of the secondary coil of two-turn bifilar transformers over various ground patterns on 15-$\Omega \cdot$ cm silicon substrate.

metal strips with a 40-μm and 60-μm spacing. The "cg" ground pattern has 30-μm wide openings.

The two-turn bifilar transformer coils used in this experiment were built at metal level $M3$ with underpasses at metal level $M2$. In process B, the nominal metal thickness at the metal levels $M3$, and $M2$ through $M1$, respectively, was 3 and 2 μm with a vertical silicon oxide separation of 1.4 μm between metals and with the silicon/silicon–dioxide interface. The contact to the ground pattern formed a closed loop (see Fig. 7), which, however, was spaced sufficiently away from the transformer coils to avoid any significant detrimental effect on the transformer characteristics. A square spiral coil with a 12.5-μm metal width and a 12.5-μm spacing and an inner free coil area of 50 $\times$ 50 μm^2 has been used in the design of the bifilar transformer. Experimental results were obtained on 15- and 3000-$\Omega \cdot$ cm silicon substrates for two-turn bifilar transformers.

From Figs. 8 and 9, it can be seen that, for the coils over the two ground patterns "pg" and "bg," essentially the same inductances were achieved as for those in case of an absent ground pattern ("ng"). However, although introduction of the patterned shield leads to higher Q's at frequencies above 4 GHz, it actually degrades Q at low frequencies. This effect was also observed in [12].

The improvement of quality factors of coils over a ground pattern as compared to coils without any ground pattern (see Figs. 8 and 9) above about 6 GHz can be attributed to the electric shielding of the silicon substrate. An integrated coil can be considered as a magnetic as well as an electric-field source. Current passing through the coil generates an ac magnetic field surrounding the device, while charges at the coil surface induce electric fields penetrating the substrate. However, the patterned ground is not an effective magnetic shield at frequencies below 10 GHz. This is because the dominant shielding mechanism for near-field magnetic sources is absorption loss, which becomes effective only when the thickness of the shield (2 μm) significantly exceeds the skin depth of the metal [13]. Furthermore, magnetic shielding requires the free flow of eddy currents in the shield, which is now suppressed by patterning.

By contrast, however, a patterned ground can effectively shield the electric field even when the metal thickness is much smaller than the skin depth, the main shielding mechanism here being reflection—rather than absorption loss [13]. If the conductivity of the silicon substrate is not too high, substrate RF losses are mainly caused by current flow along the electric-field lines in silicon induced by capacitive coupling between the coil and the substrate. By (partially) shielding this electric field, a patterned ground can, therefore, reduce substrate RF losses in medium resistivity silicon and, therefore, improve the quality factors of the coils.

At sufficiently low frequencies, the relative contribution of substrate RF losses to the total coil loss becomes insignificant as the quality factor is mainly determined by the ohmic losses in the metal. Therefore, although the patterned ground is still a good electrical shield, it does not enable a coil over it to have higher quality factors at low frequencies. In fact, it may degrade the performance of the device since local eddy currents flowing in the shield cause additional ohmic losses due to the finite metal conductivity. Patterning the ground shield substantially reduces this effect, but does not totally suppress it. In Section VI, we will return to this point by carrying out a model calculation. We will show that the observed reduction of the coil quality factors below about 6 GHz (see Figs. 8 and 9) by the introduction of the patterned shield can be attributed to the eddy currents in the shield.

Due to this behavior of the quality factors Q_P and Q_S of the primary and secondary coils, the introduction of the ground pattern (bg, pg) may increase the maximum available gain of integrated transformers only at sufficiently high frequencies (see Fig. 10). At low frequencies, it actually leads to lower values of $G_{\max}$. The k_{Im} and k_{Re} curves shown in Fig. 11 are not significantly affected by the use of the ground pattern, except near the self-resonant frequency of the transformer. Note that, for the solid ground pattern (sg) or with coarse patterning (cg), the detrimental effect of eddy currents on inductance is quite noticeable. In Fig. 12, we have also plotted $G_{\max}$ for the same transformers on a high-resistivity (3000 $\Omega \cdot$ cm) substrate. The use of the patterned ground again yields an improved $G_{\max}$ at higher frequencies. However, the improvement is less significant as compared to the results of the 15 $\Omega \cdot$ cm case, as the relative contribution of the substrate RF losses is reduced by the use of the higher resistivity substrate.

From Figs. 8, 9, and 11, it is further seen that the self-resonant frequencies of the transformers ng, pg, and bg were all about 14 GHz. In Fig. 13, the null frequencies for s_{21} of the transformers ng, pg, and bg are beyond 20 GHz. According to [14],

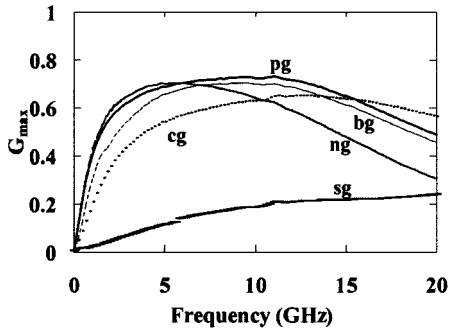

Fig. 10. Measured maximum available gain $G_{\max}$ of two-turn bifilar transformers over various ground patterns on 15-$\Omega \cdot$ cm silicon substrate.

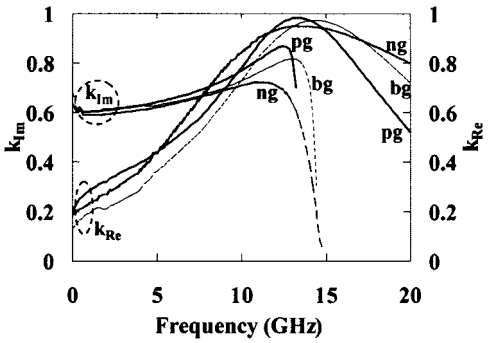

Fig. 11. Measured mutual reactive coupling k_{Im} and mutual resistive coupling k_{Re} of two-turn bifilar transformers over various ground patterns on 15-$\Omega \cdot$ cm silicon substrate.

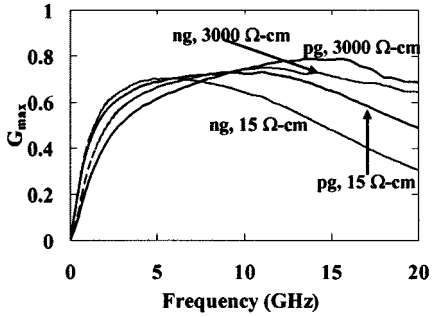

Fig. 12. Measured maximum available gain $G_{\max}$ of two-turn bifilar transformers over patterned ground (pg) on 15- and 3000-$\Omega \cdot$ cm silicon substrates.

the transformer power transfer is provided by classical magnetic coupling below the s_{21} null frequency. Thus, below 14 GHz, the transformers with ground shields pg and bg still behave as classical transformers, just like the transformer ng.

VI. Eddy-Current Losses in the Patterned Ground Shield

In order to see whether the ohmic losses caused by the local eddy currents in the patterned shield can explain the observed reduction of the low-frequency quality factor of coils, as compared to the case without a shield, we have considered the simplified model structure in Fig. 14. Here, a number of infinitely long parallel metal strips are placed on top of a periodic pattern of infinitely extended bars modeling a patterned shield. A total

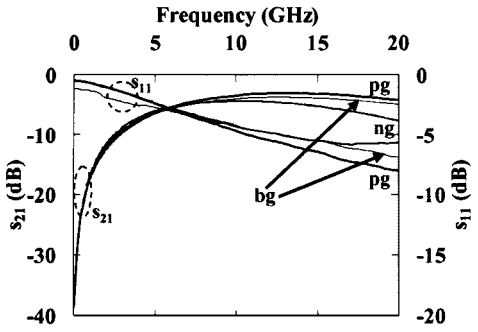

Fig. 13. Measured s-parameters of two-turn bifilar transformers over various ground patterns on 15-$\Omega \cdot$ cm silicon substrate.

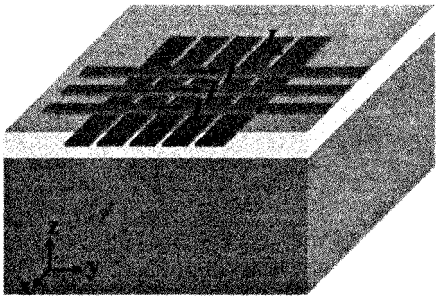

Fig. 14. Model structure of metal strips over periodic ground bars on silicon used for modeling eddy-current losses.

current I is conducted through each strip inducing a total magnetic field $\vec{B}$. The current density in the bars follows from the set of coupled integral equations [15]

$$\rho \vec{J}_i(\vec{r}) + j\omega\mu_0 \sum_k \int_{V_k} \frac{\vec{J}_k(\vec{r}\,')}{4\pi|\vec{r}-\vec{r}\,'|}\, d\vec{r}\,' = -j\omega\vec{A}(\vec{r}) - \vec{\nabla}\phi(\vec{r}) \tag{6}$$

where $\vec{J}_k$ denotes the current density in the kth bar, ρ is the resistivity of the metal, $\vec{A}$ is the vector potential associated with the magnetic field $\vec{B}$, and ϕ designates the electric potential. The integrals are taken over the volumes V_k of the bars. Since we are interested in the low-frequency behavior of the device, we separate the electric and magnetic problems by assuming that no local charges are induced in the metal bars, i.e.,

$$\vec{\nabla} \cdot \vec{J}_k = 0. \tag{7}$$

We have solved (6) and (7) within the planar approximation where the vertical component of current density is neglected and the current density is assumed to be uniform in the vertical (z) direction over the thickness of the bars. By taking advantage of the periodicity of the bar structure and applying a Fourier transform in the x-direction, we obtain a single integral equation involving one variable (y). The numerical solution of this equation is then used to compute the total eddy-current loss in each bar as follows:

$$P_k = \frac{\rho}{2} \int_{V_k} \vec{J}_k^{*}(\vec{r}) \cdot \vec{J}_k(\vec{r})\, d\vec{r} \tag{8}$$

where $P_1 = P_2 = P_3 = \cdots = P$ due to the periodicity of the structure.

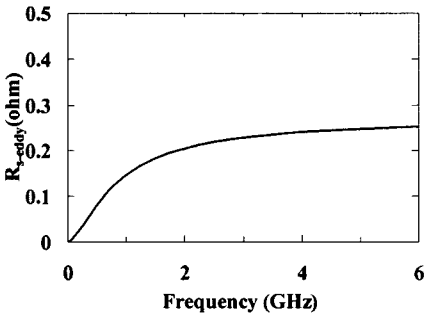

Fig. 15. Computed equivalent series resistance due to eddy-current losses.

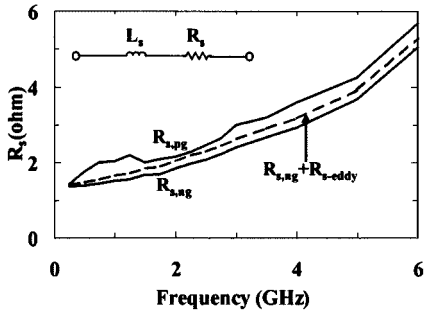

Fig. 16. Measured equivalent series resistances of coils over ground pattern (pg) and without ground pattern (ng), and measured series resistance of coil without ground pattern included with computed eddy-current losses.

Using the results obtained, we can estimate the ohmic shield losses for the square coils comprising the transformers by equating the width and spacing of each coil to those of the metal strips in the model. The width and spacing of the metal bars in the model are also chosen equal to that of the patterned ground. At sufficiently low frequencies, the effect of parasitic capacitances and substrate RF losses are negligible. The total eddy-current loss in the patterned ground can be represented as an effective equivalent resistance $R_{s\text{-eddy}}$ in series with the impedance of the coil in the absence of the shield. $R_{s\text{-eddy}}$ is computed from the equation

$$NP = \frac{1}{2} R_{s\text{-eddy}} |I|^2 \tag{9}$$

where N is the total number of bars underneath the coil, and I is the current flowing in the strips.

Fig. 15 shows the computed equivalent series resistance attributed to eddy-current loss $R_{s\text{-eddy}}$ as a function of frequency for the primary two-turn coil of the transformer over the patterned shield pg. It can be seen from Fig. 15 that eddy-current loss becomes already relatively significant at 1 GHz, but saturates rapidly beyond 3 GHz. Fig. 16 shows the equivalent series resistances of the primary coils over ground pattern (pg), without ground pattern (ng), and without ground pattern included with the modeled eddy-current losses. With the simplified model, we can account partially the higher equivalent series resistance due to eddy-current loss. We can, therefore, plausibly attribute the degradation of the quality factor of the coils at low frequencies due to the addition of a patterned shield to the ohmic loss caused by the flow of local eddy currents in the shield. This result suggests the importance of an optimal shield design, which not only serves its shielding functions, but also minimizes eddy-current losses.

VII. Conclusions

The maximum available gain $G_{\max}$ has been identified as a useful figure-of-merit for monolithic RF transformers. $G_{\max}$ has been expressed by the quality factors of the coils forming the transformer and the real and imaginary terms of the mutual coupling between the ports to relate the optimization of the individual coils to the optimum design of the transformer. Based on this detailed insight in the physics of the transformer, the following observations were made. The silicon substrate has a large effect on the coil quality factors at high frequencies and on the mutual resistive coupling factor, but not on the mutual reactive coupling factor. Thus, the substrate conductivity considerably influences the total loss of the transformer. A highly structured metal ground pattern may give a higher maximum available gain than that of a transformer without any ground pattern (ng), but this effect is pronounced only at high frequencies. This limitation is a result of the decrease in the quality factors of the transformer coils due to the ohmic losses in the coils and ground pattern. Our detailed analysis of the sources of loss in an integrated transformer on silicon, therefore, shows that $G_{\max}$ and the bandwidth can both be optimized by minimizing the ohmic losses in the coils by maximizing the mutual coupling between the ports and by minimizing the losses in the silicon substrate.

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Kiat T. Ng received the B.Eng. (with honors) degree and the M.Sc. degree from the National University of Singapore, Singapore, in 1995 and 1998 respectively, both in electrical engineering, and is currently working toward the Ph.D. degree in electrical engineering at the Delft University of Technology, Delft, The Netherlands.

Since 1998, he has been a Research Assistant with the Department of Electrical Engineering, Delft University of Technology.

Behzad Rejaei was born in Tehran, Iran, on May 15, 1965. He received the Ir. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1990, and the Ph.D. degree in theoretical condensed matter physics from the University of Leiden, Leiden, The Netherlands, in 1994.

From 1994 to 1995, he was a Post-Doctoral Research Fellow with the Theoretical Physics Department, University of Leiden. From 1995 to 1997, he was a Post-Doctoral Research Fellow with the Department of Applied Physics, Delft University of Technology. Since 1997, he has been with the Faculty of Information Technology and Systems, Delft University of Technology, where he is currently an Assistant Professor. His research interests are in the areas of electromagnetic modeling of integrated passive components and physics of ferromagnetic devices.

Joachim N. Burghartz (M'90–SM'92) received the Dipl. Ing. degree from the Technische Hochschule Aachen, Aachen, Germany, in 1982, and the Ph.D. degree from the University of Stuttgart, Stuttgart, Germany, in 1987, both in electrical engineering.

From 1982 to 1987, he was with the University of Stuttgart, where he developed sensors with integrated signal conversion and a special focus on magnetic-field sensors. From 1987 to 1998, he was with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY. His earlier research with IBM included applications of Si and SiGe epitaxial growth in high-speed transistor design and integration processes, in which he was a member of the pioneering team that invented and developed IBM's SiGe technology. From 1992 to 1994, he was a Project Leader involved with 0.15-μm CMOS development at IBM Microelectronics, East-Fishkill, NY. From 1994 to 1998, he concentrated on the design of circuit building blocks for SiGe RF front-ends, with a special interest in high-quality passive components in silicon technology. He has been driving the integration and optimization of spiral inductors on silicon substrates. In November 1998, he joined the Delft Institute of Microelectronics and Submicrontechnology (DIMES), Delft University of Technology, where he is currently a Full Professor with teaching responsibilities in electrical engineering and microelectronic research. With DIMES, he has extended his research in RF silicon technology to aspects ranging from novel materials to RF circuits. Since 1999, he has lead the DIMES research theme of "high-frequency silicon technologies for communications." In March 2001, he became the Scientific Director of the DIMES. He has authored or co-authored over 100 technical publications in refereed journals and conference proceedings. He holds 12 U.S. patents.

Prof. Burghartz has served as member of the program committees at the technical conferences of the International Electron Devices Meeting (IEDM), European Solid-State Device Research Conference (ESSDERC), and Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). He was the BCTM general chairman in 2000.