A 1-VOLT, HIGH PSRR, CMOS BANDGAP VOLTAGE REFERENCE

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Abstract- *A low voltage bandgap reference (BGR) in CMOS technology, with high power supply rejection ratio (PSRR) is presented. The proposed circuit uses a regulated current mode structure and some feedback loops to reach a low voltage, low power and high PSRR voltage reference.*
The circuit was designed and simulated in 0.25um CMOS technology, with a power supply of 1 volt. The results show PSRR is below -70dB at 1MHz and the output voltage variation versus temperature (0-70) is less than 0.3%. This circuit shows robustness against process variation.

Index Terms- CMOS analog circuit design, Bandgap reference, High PSRR, Low voltage.

1. INTRODUCTION

Reference circuits are necessarily used in many applications, from analog mixed-mode circuits to digital ones, and bandgap voltage references (BGR) have been the most popular solution, since they were first introduced in 80's.
The growing trend for low voltage circuit design is especially appeared in battery operated systems such as cellular phones, pagers, laptops and etc. consequently low voltage and low power are required characteristics to increase battery efficiency and life time.
The supply noise injected to the output of Bandgap reference circuit is the most significant noise, regarding to other sources [1]. Thus a high PSRR bandgap voltage reference is desired to achieve a high performance analog and digital system, particularly in wireless communications. In order to meet the goals of low power supply and low power dissipation, it is necessary to avoid using complex architecture and circuits. On the other hand, it is necessary to choose a structure to achieve high PSRR, over a broad frequency range to reject noise coupled from high-speed digital circuit on the chip [4].
The bandgap voltage reference presented here, has a simple architecture to achieve high PSRR, with low power dissipation and voltage supply as low as 1 volt.

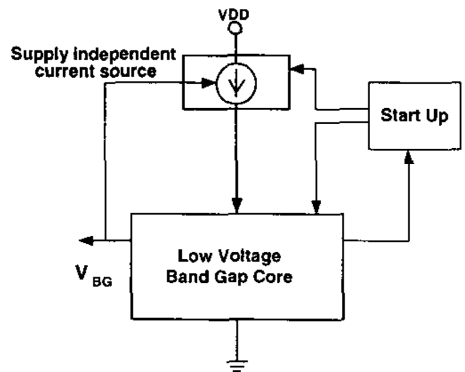

Fig 1. Top view on proposed BGR

In next section the basic operations of this bandgap are described.

2. Regulated Low Voltage Bandgap Reference

Bandgap voltage reference is quite challenging due to power consumption, noise of power supply, low power supply, temperature dependency and etc. In the BGR, the temperature dependence of the BG voltage obtained from a positive temperature coefficient (PTC) of a PTAT current and a negative temperature coefficient of a VBE. Fig.1 illustrates a low voltage, supply independent bandgap voltage reference, and to achieve high PSRR, bandgap core is supplied from a current source instead of voltage supply. The bandgap core is a widely used BGR [2]. The current source receives a feedback signal from bandgap core to have less dependency on power supply.

2.1. Improved Bandgap Core

The basic operating principle of Bandgap voltage reference is presented in Fig.2.a. The feedback loop amplifier (OP1) sets the voltage of nodes X and Y equal and the PTAT current is made. Supply independent current source (Fig.2.b), sources current to main branch (Vb2) and M4 transistor sinks the reminder.

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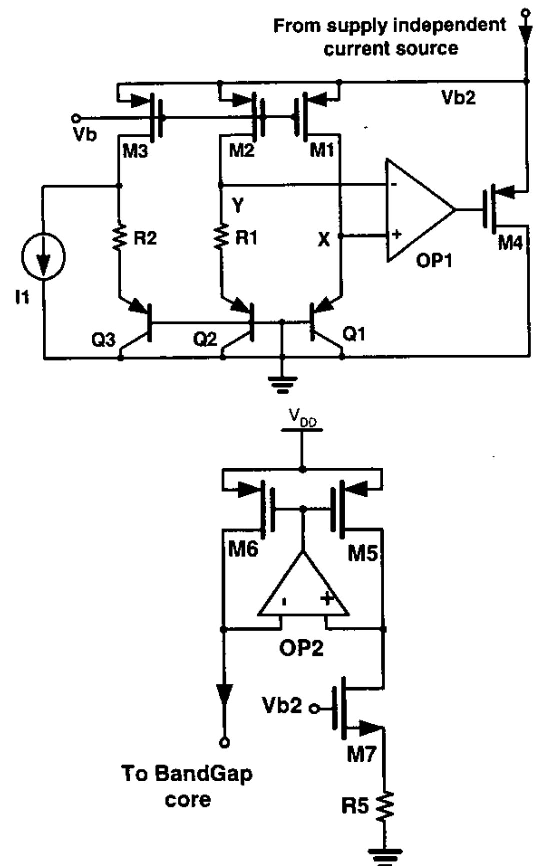

Fig 2. (a) Bandgap core. (b) Current reference

Due to low voltage design, resistor division of output Bandgap voltage provides the bias voltage of M1 and M2. These Match resistors (R2, R3, R4) provide the output voltage from the bandgap core. The M3 transistor is responsible to provide the regulated voltage (vb2) for bandgap current source. (Fig.3)

The most important point to be considered in the circuit is the stability of frequent loops [3].

2.2. Stability of the Loop

From stability point of view the worst loop is the loop including OP1 and M4, whose stability will be discussed here. According to Fig.2.a, the Loop gain of this loop can be determined as,

$$LG = A_V(s)\frac{g_{M4}}{g_{M4}+g_{Meq}}\left(\frac{g_{M1}}{g_{q1}}-\frac{g_{M2}}{g_{R1}+g_{q2}}\right) \quad (1)$$

While:

$$g_{Meq} = g_{M1}+g_{M2}+g_{M3}+g_o \quad (2)$$

Since M1 and M2 have the same voltage gate and the Q1 and Q2 have the same base voltage, so we have

$$g_{M1} \approx g_{M2} = g_M,\ g_{q1} \approx g_{q2} = g_q \quad (3)$$

Then, following expression can be written for Loop gain,

$$LG = A_V(s)\frac{g_M}{g_q}\frac{g_{R1}}{g_{R1}+g_q}\frac{g_{M4}}{g_{M4}+g_{Meq}} \quad (4)$$

Assuming:

$$g_M < g_q,\ \frac{g_M}{g_q}\frac{g_{R1}}{g_{R1}+g_q}\frac{g_{M4}}{g_{M4}+g_{Meq}} < 1 \quad (5)$$

To guarantee the stability of this loop,

$$F_u(LG) < F_u(op1) \quad (6)$$

Where LG is loop gain and Fu is unity gain bandwidth. Discussion shows that the loop is unconditionally stable if the amplifier in the loop (op1) has enough phase margins.

2.3. Reference Current Module

Fig2.b illustrates the supply independent current source applied to bandgap core, which is controlled by the bandgap output voltage. OP2 amplifier has been used to increase output resistance of current mirror by boosting mechanism. As it will be discussed in the next section, using this method will increase The PSRR.

2.4. High PSRR Mechanism

Assume Vs as the AC part of V_{DD} and I_S, as the AC part of reference current, then

$$\frac{v_{out}}{v_s} = \frac{v_{out}}{i_s}\frac{i_s}{v_s} \quad (7)$$

$$\Rightarrow \frac{v_{out}}{v_s} \approx \frac{R_2 \| (R_3+R_4)}{A_1 A_2 (g_{M4} r_{o6}) R_1} \quad (8)$$

This equation shows what parameters are of high importance to increase PSRR. So high PSRR is obtained by applying these strategies:

1) The bandgap core is supplied from regulated voltage made with a feedback loop including OP1 and M4. [1]
2) The current reference that supplies the bandgap core is designed wideband to have high PSRR, because the PSRR of this block is proportional to gain and bandwidth of OP1.
3) The current reference of bandgap core is made from regulated supply voltage and resistor R5, matched with other resistors.

2.5. Low Voltage Structure

However this circuit uses stacking to provide the regulated voltage, it works with 1-V power supply, using some techniques, which will be discussed here.

According to Fig.3:

$$(V_{T,M3}+\Delta V_{T,M3}+V_{R4})+\Delta V_{M3} < (V_{BG})+\Delta V_{M3} \quad (9)$$

So:

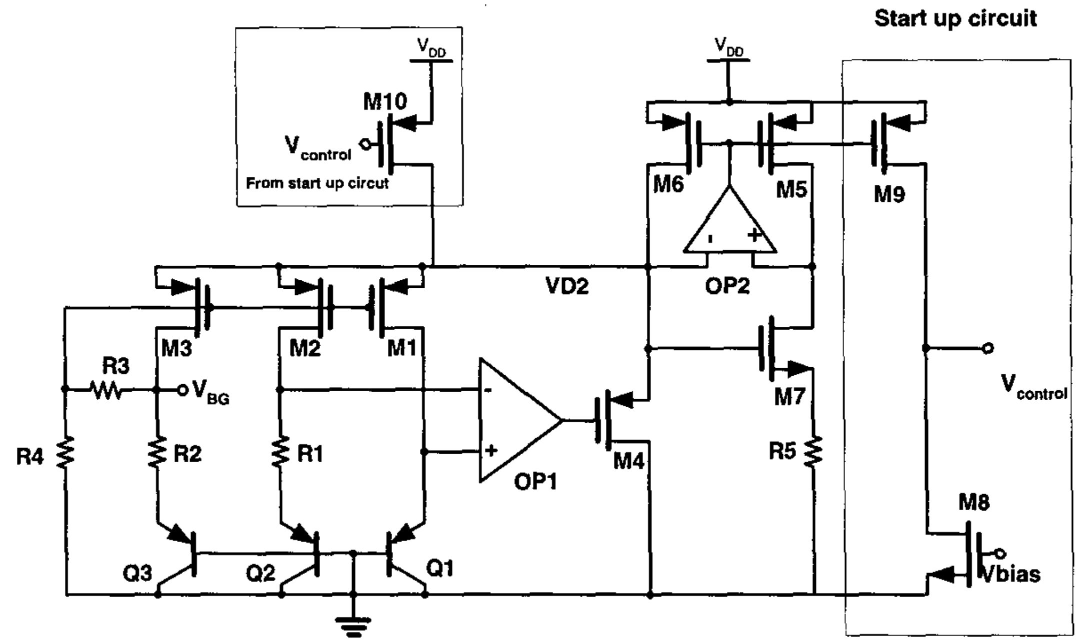

Fig 3. Low voltage, High PSRR Bandgap voltage reference

$$V_{ddMIN} = V_{BG} + \Delta V_{M6} + \Delta V_{M3} \qquad (10)$$

With using R3 and R4 resistors shown in fig 4 the V_{BG} voltage can be decreased as follow:

Assume the V_{BG} voltage before connection of R3, R4 V_{BGP}, so,

$$V_{BGP} = V_{BEQ3} + \frac{R2}{R1}\left(\frac{KT}{q}\right)Ln(N) \qquad (11)$$

Where N is aspect ratio of Q1 and Q2, then it can be shown that:

$$V_{BG} = \frac{V_{BGP}}{1 + \frac{R2}{R3 + R4}} \qquad (12)$$

By choosing the proper values for R2, R3 and R4, V_{BG} can be reduced to about 0.7 volt, which is the minimum possible voltage can keep Q3 on, in all corner cases .So,

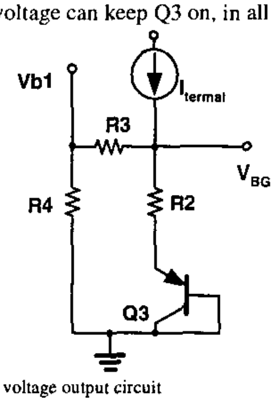

Fig 4. Low voltage output circuit

$$V_{ddMIN} = 0.7 + 2\Delta V \le 1 \qquad (13)$$

Then supply voltage can be reduced to as low as 1-volt.

2.6. Start-up Circuit

Due to multiple loops, the Bandgap reference needs a start up circuitry. A simple start up for proposed circuit has been designed that Fig.3 presents it. First, M8 transistor that is biased through V_{DD}, is on and force M10 transistor to source current to the Bandgap core. When circuit started, M9 that its current is larger than M8 current, pushes the $V_{control}$ to V_{DD} and makes M10 to be off.

2.7. Amplifiers

The input-referred noise and offset of OP1 amplifier are inserted directly in the current of IPTAT, So OP1 must be designed to be a low noise and low offset op-amp, In addition to having a high frequency bandwidth.

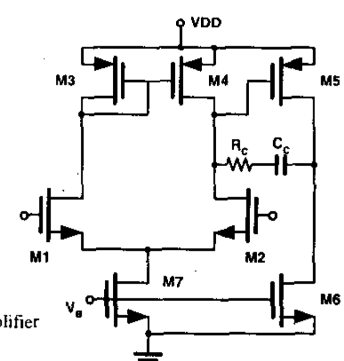

Fig 5. Amplifier

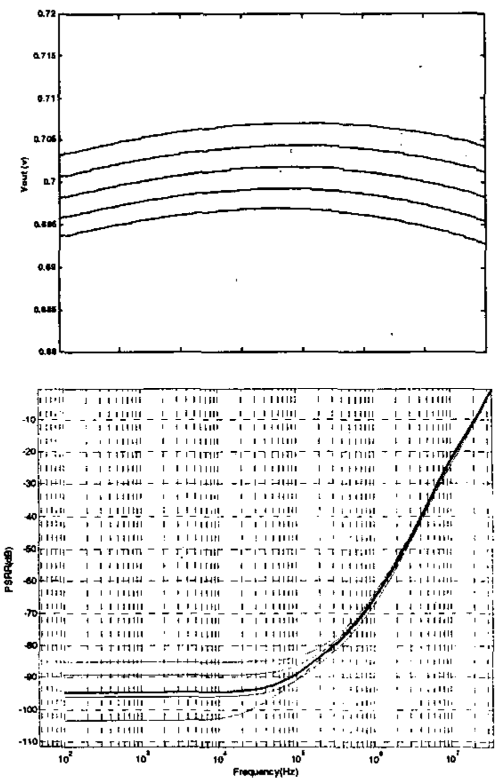

Fig 6. (a) Temperature dependence of Bandgap output. (b) Variation of PSRR versus frequency in different cases.

According to what was mentioned above, a simple low voltage op-amp with NMOS input transistors was designed for OP1 and OP2 op-amps. (Fig.5)

3. RESULTS

Table I summarizes the bandgap voltage reference characteristics extracted from simulations. The curve of PSRR versus frequency is shown in Fig.6.a and Fig 6.b shows the temperature variation curve.

4. CONCLUSION

An ultra low voltage, low power, high PSRR bandgap voltage reference has been developed in a standard CMOS 0.25Um technology. The circuit operated down to minimum power supply voltage 1-volt and it consumes only 0.22mw at minimum supply.

The regulated structure, multiple feedback loops and additional circuitry required for high PSRR, were designed which lead to the PSRR more than 110 dB at low frequencies and more than 70 dB at 1 MHz.

TABLE I
BANDGAP REFERENCE CHARACTERISTICS

Parameter	Value
Power supply Range (V)	1 to 2.5
Power dissipation (μW) @V_{DD}=1V	220
I_{DD} (μA)	220
V_{BG} (V)	0.7
Standard deviation (mV)	18
Temperature Variation	0.3%
PSRR	
Dc frequency (dB)	-110
1MHz (dB)	-70

5. ACKNOWLEDGEMENT

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