Figure 3.55, assumes an evenly interdigitated device ($m = 2$, 4, 6, 8, etc.) where the drain perimeter and area are minimized. If interdigitation is not used ($m = 1$), C_{DBO} is twice the value considered, reducing f_{diode}/f_{Ti} and the associated value of f_{diode}.

Figure 3.59 shows the bandwidth reduction from f_{Ti} present in a single device as a result of the extrinsic capacitances, C_{GSO} and C_{DBO}. The bandwidth reduction is greater for multiple devices, for example for a unity-gain current mirror where two units of C_{gsi}, C_{gbi}, C_{GSO}, and C_{GBO} (again, excluded in Figure 3.59) load the circuit from the gate of input and output devices along with one unit of C_{DB} from the drain of the input device alone. As a rough estimate, the -3 dB frequency associated with the input impedance of a unity-gain current mirror is $f_{diode}/2$, which assumes an additional unit of C_{DB} not present at the input while neglecting C_{GBO} from both input and output devices [11]. Layout capacitances, of course, reduce operating bandwidth further.

As mentioned in the previous section, f_{Ti} has a universal characteristic across CMOS processes. f_T and f_{diode}, however, depend on f_{Ti} and the extrinsic, gate-overlap and drain–body capacitances described in Sections 3.9.3 and 3.9.4. These depend strongly on the process, giving a strong process dependence on f_T and f_{diode}. Extrinsic device and layout capacitances can be expected to continue to lower bandwidth from the intrinsic bandwidth in smaller-geometry processes.

3.10 NOISE

The prediction and trends of MOS noise are important since noise determines the minimum AC signal that can be processed by an analog circuit. This section describes MOS thermal noise in both the ohmic and saturation regions. Following this, low-frequency flicker noise is described, including a review of reported flicker-noise factors. The section then describes channel avalanche noise and thermal noise from the gate, substrate, and source resistances. Finally, the section concludes by describing induced gate noise current caused by channel thermal noise, and gate noise current caused by gate resistance noise and DC leakage current.

Figure 3.60 shows MOS drain-referred noise current and gate-referred noise voltage sources that are added to the small-signal model shown earlier in Figure 3.21 in Section 3.8.1. As described in this section, the sources model thermal and low-frequency flicker noise where the drain-referred or gate-referred sources are used separately for circuit analysis. Figure 3.60 describes the conversion

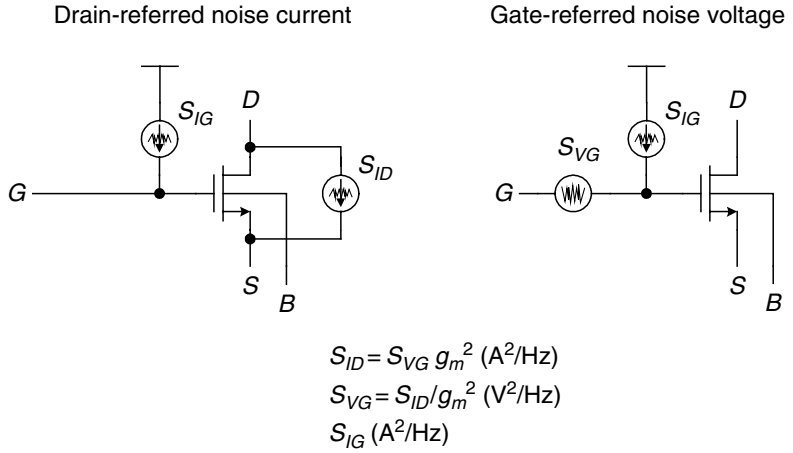

Figure 3.60 MOS noise model showing drain-referred noise current and gate-referred noise voltage sources along with a gate noise current source. The drain-referred and gate-referred noise sources are used separately and are added to the small-signal model shown in Figure 3.21 along with the gate noise current source that is always present. Expressions are given showing the PSD conversion between drain-referred and gate-referred noise sources