Design of Fully Differential Folded Cascode Operational Amplifier by the g_m/I_D Methodology

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Abstract - This paper presents the design of a fully differential folded cascode operational amplifier by using the g_m/I_D methodology. The g_m/I_D curves have been computed for a 0.35-µm CMOS process and the g_m/I_D methodology is applied to computing the transistor aspect ratios W/L for the specified operational amplifier requirements, such as open-loop gain, unity-gain frequency and slew rate. The output stage is designed to drive a 20-kΩ resistive load. The amplifier performance is simulated over wide process and temperature variations to determine the worst case behaviour.

I. INTRODUCTION

Growing complexity of integrated circuits makes hand analysis and design of analogue circuits difficult. It is often very hard to find a good starting point for the circuit design because the circuit specification is based on several, usually contradictory requirements, such as gain, speed, power dissipation, offset voltage, etc.

First, a designer must choose a suitable architecture for the given circuit specification. Once an appropriate topology is selected, the design develops through the tuning of component values and transistor sizes. Although the numerical optimisation routines coupled with circuit simulation tools like Spice or Spectre can be used to tune transistor dimensions [1], an analytical or hand synthesizing methodology gives better insight into the circuit design. In this paper the g_m/I_D methodology is used as a tool for hand calculations.

The g_m/I_D methodology [2-4] is a good approach to select the starting point of the design in the small-signal circuit analysis. The methodology is chosen because it is strongly related to the performance of analogue circuits and it can be used for the calculation of the transistor dimensions. It is based on the unique g_m/I_D curve versus the normalised current $I_D/(W/L)$.

The target of this work is to design a fully differential folded cascode (FDFC) operational amplifier. Fully differential output operational amplifiers are widely used because they provide a large output voltage swing and they are less susceptible to common-mode noise than the single-ended versions [5-7]. Fully differential amplifiers are used in a noisy environment when external noise can mask low input signals. Also, the differential operation in switched-capacitor analogue circuits is a good way to minimize the influence of clock feedthrough and charge injection. A disadvantage of fully differential operational amplifiers is the fact that they require the use of a common mode feedback (CMFB) circuit to control the common-mode output voltage.

Section II describes and analyses the fully differential folded cascode operational amplifier. The amplifier specifications are presented in Section III, while section IV describes the design methodology. In Section V the simulation results are presented.

II. AMPLIFIER STRUCTURE

The designed amplifier can be divided into three main parts: basic FDFC amplifier, common mode feedback (CMFB) amplifier and biasing circuit.

Fig. 1 presents a basic fully differential folded cascode operational amplifier [8]. It is a two stage amplifier. The input stage is a differential output differential folded cascode amplifier with the transistors M_1-M_{12}. The high gain of this stage is a result of the cascode current mirrors M_5-M_8 and M_9-M_{12}. The nMOS devices M_1 and M_2 are chosen as the input differential pair because of larger transconductance compared to pMOS devices. The output stage is a common source amplifier with the transistors M_{13}-M_{16}. It is designed to drive resistive loads. Special attention is dedicated to the design of the output transistors in order to obtain a high voltage swing. The frequency compensation network consists of the compensation capacitors C_{cp} and C_{cm} and zero-nulling resistors R_{cp} and

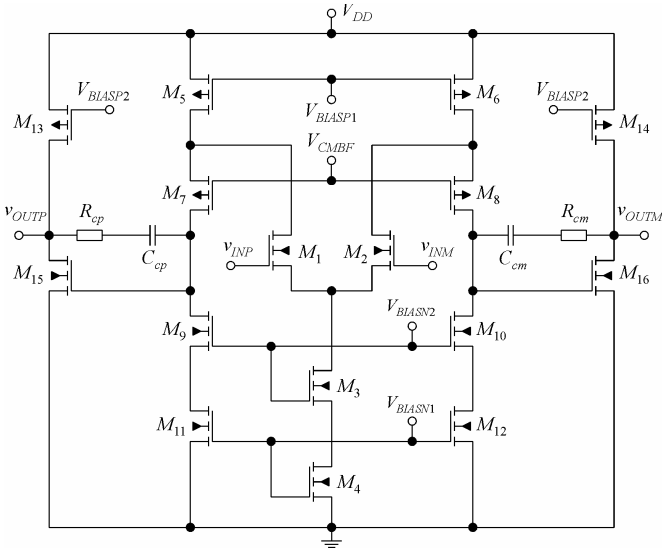

Figure 1. - Fully differential folded cascade (FDFC) operational amplifier.

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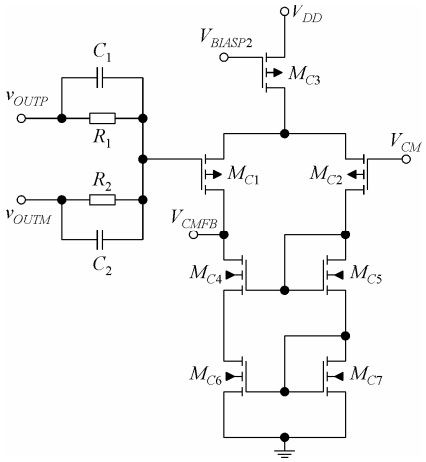

Figure 2. - Common mode feedback (CMFB) amplifier.

R_{cm}.

The common mode feedback (CMFB) circuit is used in a fully differential operational amplifier to keep the operational amplifier outputs balanced around a known voltage V_{CM}. The common mode feedback (CMFB) amplifier is shown in Fig. 2. The common mode output voltage is detected by the resistive divider R_1 and R_2. One side of the large and equal resistors R_1 and R_2 is connected at the gate of M_{C1}, where the common voltage is detected, while the other side of the resistors is connected to the basic FDFC amplifier output nodes v_{OUTP} and v_{OUTM} (Fig. 1), respectively. The resistors R_1 and R_2 have to be large to prevent the gain loss of the output stage of the basic FDFC amplifier.

On the other hand, the large resistances R_1 and R_2 and the parasitic gate-source capacitance of M_{C1} form the *RC* network that slows down the common mode detection. From the stability consideration, the common mode detection must be fast enough in order to ensure the stability of the whole amplifier. To ensure that the balance is maintained at high speed, two equal capacitors C_1 and C_2 are added in parallel with the resistors R_1 and R_2. At high frequencies the impedance of the capacitors becomes dominant, lowering down the total impedance. The value of the resistors is a trade-off between the fast common voltage detection and the gain of the output stage.

The CMFB amplifier must have enough gain to ensure good tracking between the common voltage V_{CM} and the detected common voltage at the outputs, which is equal to $(v_{OUTP} + v_{OUTM})/2$. High gain is achieved by cascode connected active loads. The CMFB amplifier output is V_{CMFB}. This common mode voltage regulation is applied to the gates of the transistors M_7 and M_8 of the FDFC amplifier in Fig. 1. This is the best point for the regulation with respect to the stability of the circuit.

The biasing circuit is shown in Fig. 3. The voltages V_{BIASP2}, V_{BIASP1}, V_{BIASN1} and V_{BIASN2} determine all biasing currents for the FDFC operational amplifier in Fig. 1 and the CMFB amplifier in Fig. 2. The biasing current is controlled by the current source I_{BIAS}. The transistors M_{B9}-M_{B11} with transistors M_{B14} and M_{B15} form a low-voltage wide-swing current source [7-8]. This type of source, that mirrors currents in input stage of basic amplifier, is necessary because of the stack of the transistors M_3, M_4 and M_9-M_{12} in Fig 1. The series connection of the transistors M_{B9}-M_{B11} is used instead of a

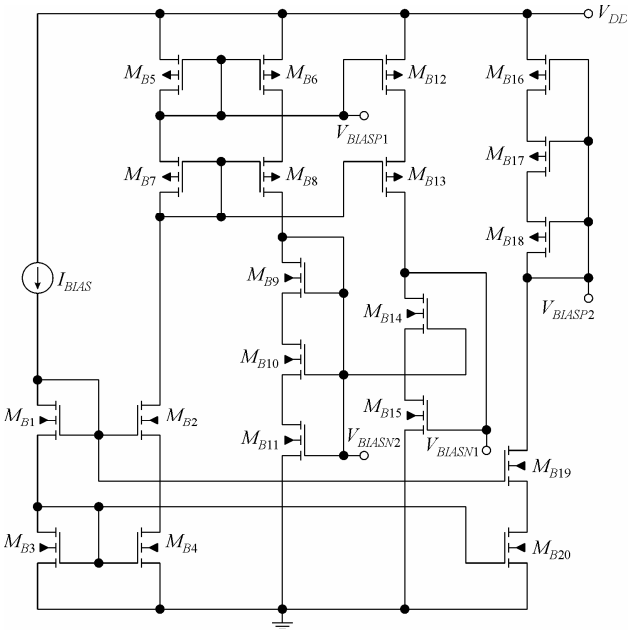

Figure 3. - Biasing circuit.

single nMOS transistor with longer channel. The usage of the series connection is also applied to the transistors M_{B16}-M_{B18}.

III. AMPLIFIER SPECIFICATION AND SMALL SIGNAL ANALYSIS

A. Amplifier Specification

The amplifier is designed in the AMS 0.35-µm CMOS technology and it must satisfy the following specifications:

- open-loop gain $A_{V0} > 120$ dB,
- slew rate $SR > 4$ V/µs,
- unity gain frequency $f_T > 10$ MHz,
- differential output voltage swing 2.8 V_{PP},
- resistive load ≥ 20 kΩ,
- power supply from 3.3 V to 3.6 V,
- operating temperature range from – 40ºC to 85ºC.

These are the worst case specifications that must be fulfilled over all temperature and process variations.

B. Small Signal Analysis

The operational amplifier from Fig. 1 has two stages. The total gain of 120 dB is distributed among the input differential folded cascode stage ($A_{V1} = 80$ dB) and the output the stage ($A_{V2} = 40$ dB).

The gain A_{V1} of the input differential folded cascode stage is

$$A_{V1} = g_{m1}\left(R_{d7} \| R_{d9}\right), \tag{1}$$

where R_{d7} and R_{d9} are the small signal output resistances as seen from the drain of M_7 and M_9

$$R_{d7} = r_{d7}\left[1 + g_{m7}\left(r_{d1} \| r_{d5}\right)\right], \tag{2}$$

$$R_{d9} = r_{d9}\left(1 + g_{m9}\, r_{d11}\right). \quad (3)$$

In (1)-(3) g_{mi} and r_{di} are the transconductance and small signal output resistance of the transistor M_i, respectively.

The gain of the output stage A_{V2} is

$$A_{V2} = g_{m15}\left(r_{d13} \| r_{d15} \| R_1\right), \quad (4)$$

where R_1 is the resistor used for common mode detection in the CMFB amplifier. The open-loop gain A_{V0} of the operational amplifier is

$$A_{V0} = A_{V1}\, A_{V2}. \quad (5)$$

The unity frequency f_T is determined by the compensation capacitance C_{cp}

$$f_T = \frac{1}{2\pi}\frac{g_{m1}}{C_{cp}}. \quad (6)$$

The compensation capacitance C_{cp} is also the key parameter for the slew rate SR

$$SR = \frac{I}{C_{cp}}, \quad (7)$$

where I is the current that flows through the capacitor C_{cp} when a large differential input signal is applied.

IV. AMPLIFIER DESIGN

A. g_m/I_D Methodology

The g_m/I_D methodology is a unified synthesis methodology for all regions of operation of the MOS transistors. The fundamental design parameter is the relationship between the ratio g_m/I_D and the normalized drain current $I_D/(W/L)$. Since it is the function of the normalized drain current, i.e. not depended on the transistor size, the ratio g_m/I_D is a unique characteristic for each nMOS and pMOS transistor in a given technology. When the values of g_m and I_D for a particular transistor are chosen in the design process, the aspect ratio W/L can be determined from the g_m/I_D curve.

The g_m/I_D versus $I_D/(W/L)$ curves are determined for the AMS 0.35-µm CMOS technology by Spectre simulations. Fig. 4 presents the calculated g_m/I_D curves for both nMOS and pMOS transistors.

The additional transistor parameter needed for small signal analysis is the output resistance r_d. It is defined as

$$r_d = \frac{1}{\lambda I_D}, \quad (8)$$

where the channel length modulation parameter λ determines the slope of the transistor characteristic in the saturation region. The parameter λ is also computed from the simulated characteristics.

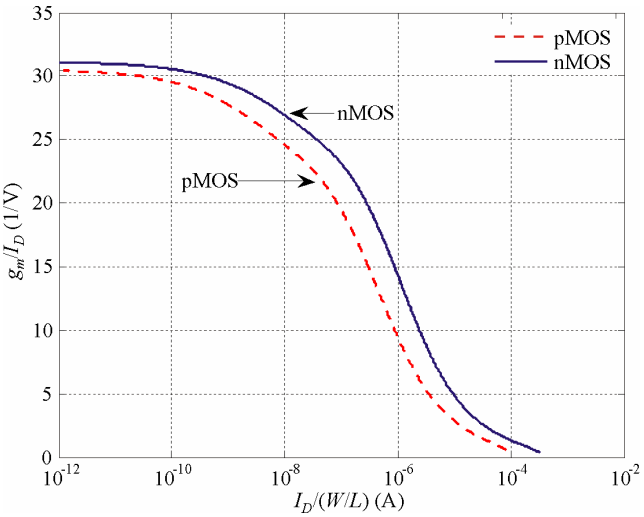

Figure 4. - Calculated g_m/I_D versus $I_D/(W/L)$ curves for nMOS and pMOS transistors in the AMS CMOS 0.35-µm technology.

B. Amplifier Design

The g_m/I_D methodology is used to determine the initial dimensions of transistors in order to satisfy the design relations (1)-(7).

It is assumed that the compensation capacitance C_{cp} is equal to 10 pF. To obtain the required unity gain frequency of 10 MHz, the transconductance g_{m1} should be 0.6 mA/V, according to (6). For the slew rate requirements (7) current I through the capacitor C_{cp} must be at least 40 µA. This current flows through the transistor M_1 in the differential pair so its drain current I_{D1} should be 40 µA. Based on known parameters I_{D1} and g_{m1}, the aspect ratio W/L of the transistor M_1 is determined from the g_m/I_D versus $I_D/(W/L)$ curve.

The parameters of other transistors are determined through the following reasoning:

- The current of transistors M_5, M_7, M_9 and M_{11} is calculated from the static condition $I_{D5} = I_{D7} + I_{D1}$, and the required small signal output resistances.
- Transconductances of transistors M_7 and M_9 are calculated by combining equations (1)-(3) and (8) to obtain the input stage gain $A_{V1} = 80$ dB.
- By using the calculated currents and transconductances the aspect ratios W/L of transistors M_7 and M_9 is read from the g_m/I_D versus $I_D/(W/L)$ curve.

The transistors M_3, M_4, M_5 and M_{11} in Fig. 1 belong to the current sources and their transconductances are of no importance for the small signal gain. The aspect ratios W/L of these transistors are chosen to satisfy the static conditions and to ensure their operation in the saturation region. The transistor parameters for the input differential folded cascode amplifier are presented in Table I.

TABLE I - COMPUTED TRANSISTOR PARAMETERS
FOR INPUT DIFFERENTIAL FOLDED CASCODE AMPLIFIER

Transistor	I_D (µA)	g_m (mA/V)	W/L
M_1, M_2	40	0.6	40
M_3, M_4	80		48
M_5, M_6	90		45
M_7, M_8	50	0.23	12
M_9, M_{10}	50	0.6	31
M_{11}, M_{12}	50		30

The primary concern in the design of the output stage in Fig. 1 is the rail to rail voltage swing and driving capability. The current which provides the required voltage swing of 2.8 V on the 20 kΩ resistive load is 140 µA. The current source transistors M_{13} and M_{14} and the active transistors M_{15} and M_{16} have to deliver and sink required currents. To keep these transistors in the saturation region and to overcome process and temperature variations of the output stage, the current through these transistors is increased to 210 µA. Additionally, the specified gain of the output stage should be 40 dB. These requirements can be achieved with the aspect ratios W/L of 70 for pMOS and 25 for nMOS transistors.

The CMFB amplifier in Fig. 2 is a simple one stage amplifier. As the required gain is achieved by using the cascode current source, the only requirement is the stability of the basic FDFC amplifier. So we have a freedom in determining the W/L ratio for the CMFB amplifier. The transistor dimensions are chosen so that the sizes of M_{C4}-M_{C7} are the same as for M_9-M_{12}, and the sizes of M_{C1} and M_{C2} are the same as for M_7 and M_8.

The transistor dimensions in the biasing circuit from Fig. 3 are determined to ensure proper biasing of both the basic and CMFB amplifier. Special care is devoted to the aspect ratios W/L of the transistors M_{B9}-M_{B11} and M_{B14}-M_{B18} to ensure the proper mirroring coefficient. The bias current I_{BIAS} is chosen to be 10 µA so that all static currents in both amplifiers (50 µA, 80 µA, 90 µA and 210 µA) can be obtained by multiplying this bias current by a whole number.

The determined transistor dimensions are used as the starting point in circuit simulations. These dimensions are verified and confirmed by Cadence Spectre simulations [9]. Almost all initially determined transistor dimensions have remained the same, except for the dimensions of the transistors M_7 and M_8. The aspect ratio W/L of 12 for these transistors has been determined for the standalone basic FDFC amplifier. When the CMFB amplifier output V_{CMFB} is connected to the gates of the transistors M_7 and M_8, Spectre simulations have shown that the amplifier is not stable. The amplifier stability is insured by the increased aspect ratio W/L of 60 for these two transistors.

C. Layout Design

After the verification of the design by circuit simulations, the amplifier layout is drawn in Cadence Virtuoso [10]. Fig 5 shows the layout of the complete amplifier. In the layout design the topological symmetry of the basic FDFC amplifier is essential for the good overall amplifier characteristics, such as e.g. low offset. Each transistor from both sides of the basic amplifier is split into several parallel transistors to ensure symmetry and matching. Additionally, parallel transistor dummy structures are also used, especially for the input differential pair. The layout of the operational amplifier occupies 0.06 mm^2.

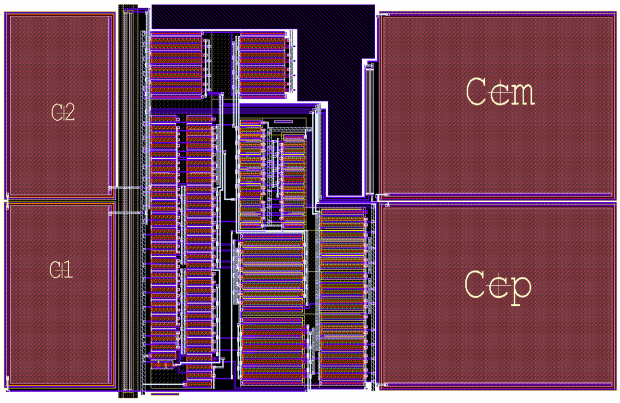

Figure 5. - Complete operational amplifier layout.

V. SIMULATION RESULTS

Post-layout extraction of parasitics and simulations are performed in order to verify the design. The amplifier dissipates 3.3 mW for the supply voltage of 3.3 V.

A. Open-loop frequency response

The simulated open-loop frequency response is shown in Fig. 6 and the numerical results are presented in Table II. In addition to the nominal case results, Table II also shows the worst case results, where the process and temperature variations are considered. In the nominal case the open-loop gain A_{V0} is 134 dB and the unity gain

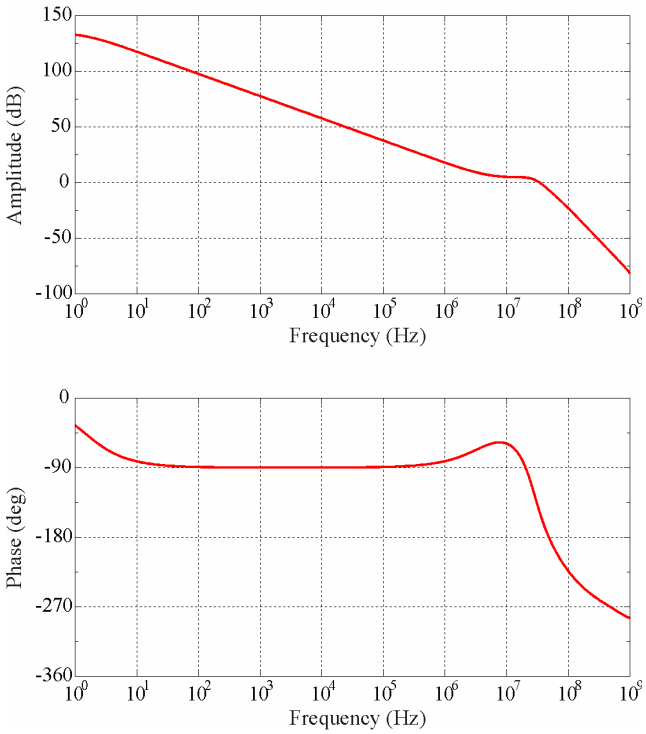

Figure 6. - Open-loop frequency response.

TABLE II - OPEN-LOOP GAIN AND UNITY GAIN FREQUENCY

	Nominal case	Worst case
A_{V0} (dB)	134	119
f_T (MHz)	44	34

frequency f_T is 44 MHz. The increase of the frequency f_T is obtained by using the resistors R_{cp} and R_{cm} in the FDFC operational amplifier (Fig. 1) to compensate a zero in the transfer function [7]. The specified requirements are satisfied in the nominal and in the worst case. The worst case values are obtained for the process variation "worst power" and the temperature of 85ºC.

B. Step response

The simulation test bench for the transient simulations is shown in Fig. 7. The closed loop voltage gain is

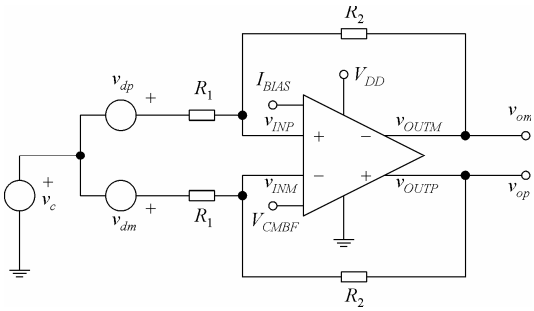

Figure 7. - Simulation test banch.

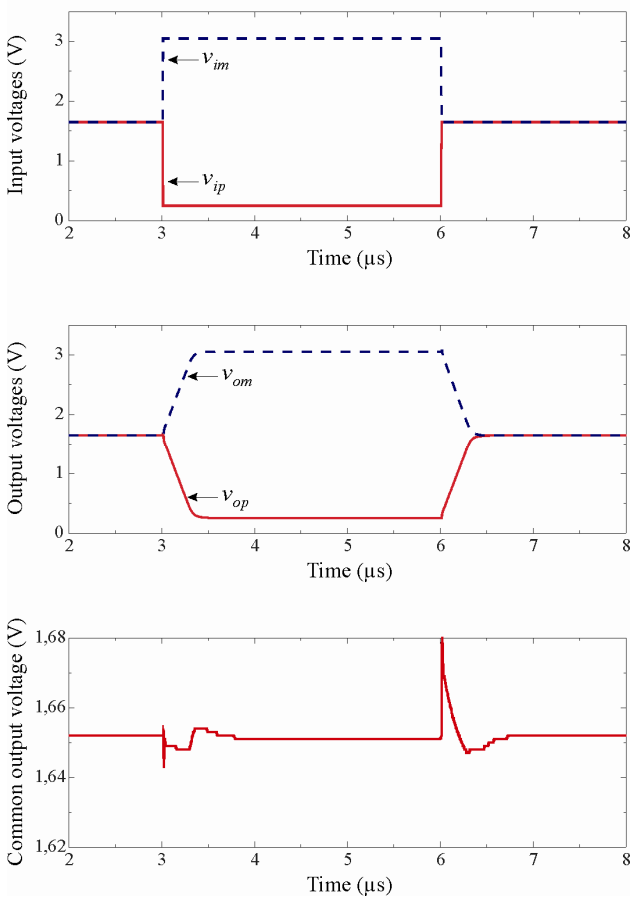

Figure 8. - Step response.

TABLE III - STEP RESPONSE RESULTS

	Gain × 1		Gain × 10	
	Nominal case	Worst case	Nominal case	Worst case
t_r (ns)	280	322	480	655
t_f (ns)	270	312	472	641

determined by the input and feedback resistors R_1 and R_2, $A_V = R_2/R_1$. In Fig 7 the resistances R_1 and R_2 have the same value equal to 20 kΩ, so that the gain A_V is 1. In the transient simulations, each output is additionally resistively loaded by the next stage input resistances of 20 kΩ. Fig. 8 shows the step response for the full voltage swing. The rise time t_r and the fall time t_f of the output differential voltage are presented in Table III for the nominal and worst case. The worst case values in Table III are obtained for the process variation "worst speed" and the temperature of 85ºC. The differential output voltage rises from 0 V to 2.8 V in less than 1 µs without overshoots. The transient simulations have confirmed that the operational amplifier is stable and very fast. Since a slewing occurs when the input voltage swing is high, the slew rate is estimated from the results of transient simulations in Table III for the case when the voltage gain is 1. The estimated slew rate of 8 V/µs in the nominal case and 7 V/ µs in the worst case are larger than the design requirement.

Fig. 8 also shows the common mode regulation. The output common voltage follows the input common mode voltage within the range of ±3 mV in the worst case. Transient simulations have been also carried out for the closed loop gain of 10 and the results are included in Table III.

C. DC transfer characteristic

The amplifier driving capability is checked by DC simulations. For the circuit with the closed loop gain of 1 and for the resistive load of 20 kΩ the input voltage is swept from 0 V to ± 2.8 V. The linear transfer characteristic, shown in Fig. 9, proves that the amplifier output stage is capable of driving a resistive load of 20 kΩ for the required output voltage swing.

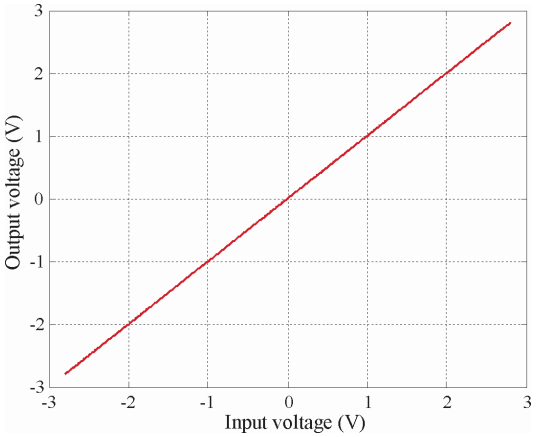

Figure 9. - DC transfer characteristic.

VI. CONCLUSION

Complexity of analogue integrated circuits makes hand analysis difficult. The design methodology based on the g_m/I_D curve is a good approach for hand calculations of transistor dimensions. The g_m/I_D methodology is applied to the design of a folded cascode fully differential operational amplifier. Once the transistor dimensions are estimated they have been optimised by circuit simulations to meet required specifications regarding process and temperature variations, and amplifier stability. The simulation results confirm that the amplifier specifications (high gain, bandwidth, slew rate and voltage swing) are satisfied.

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