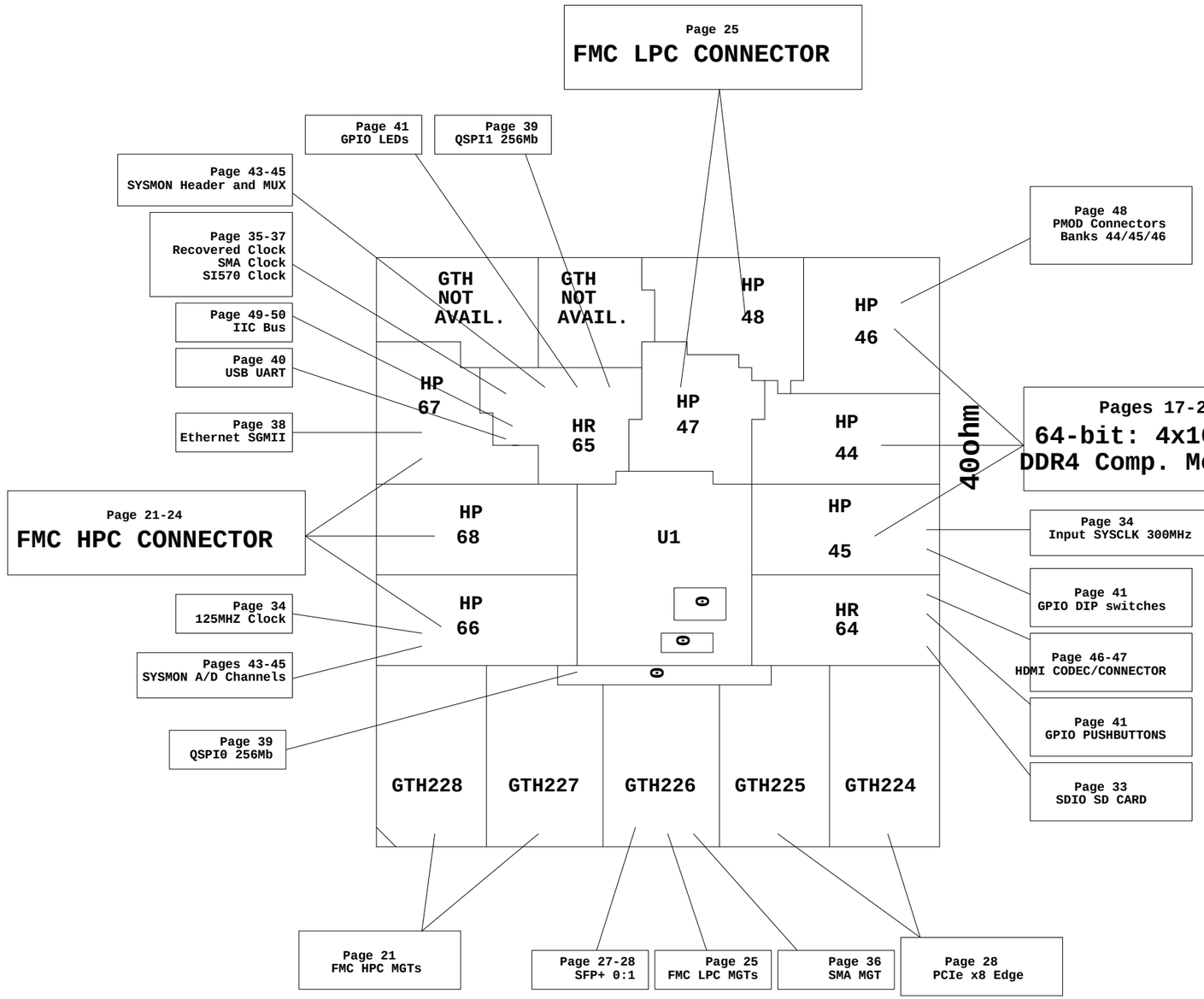
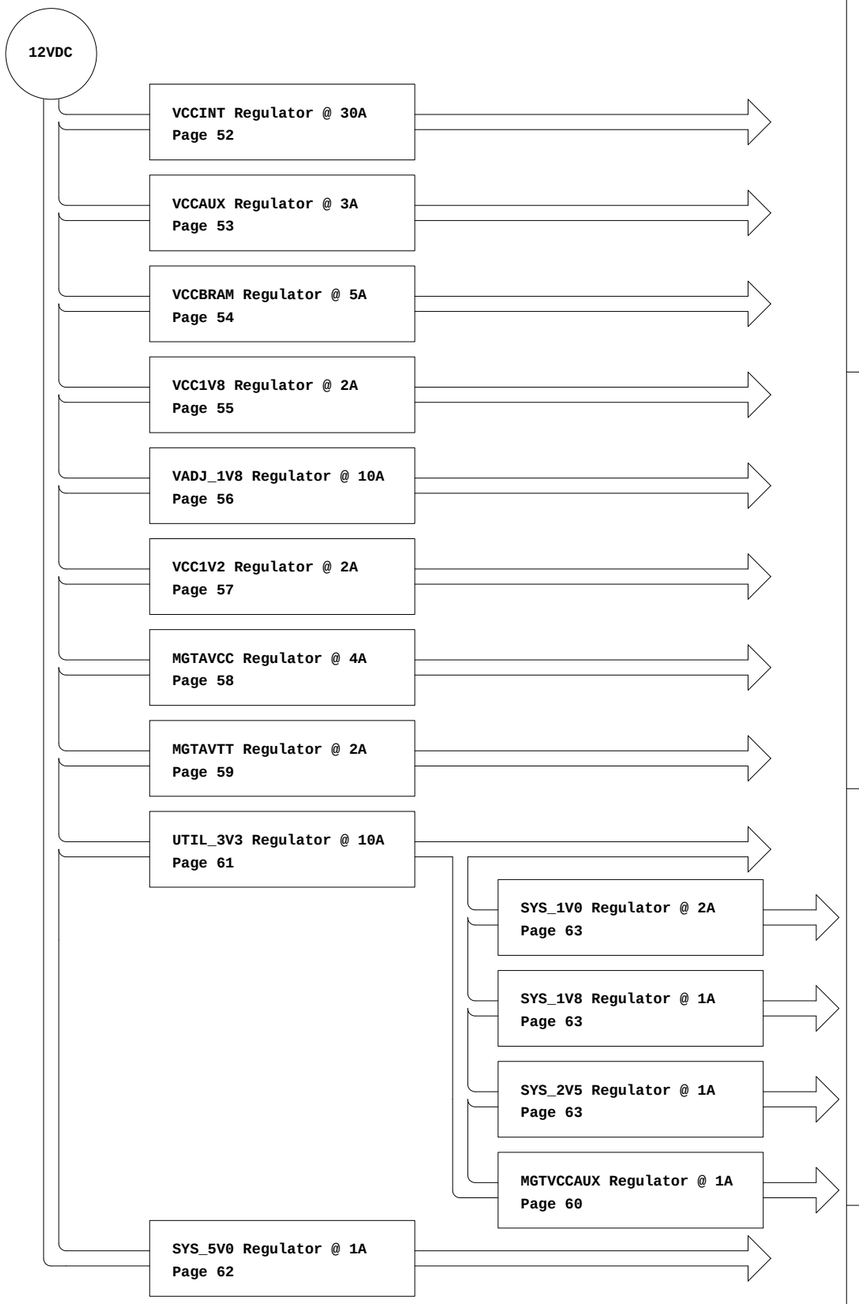
KCU105 EVALUATION PLATFORM HW-U1-KCU105 (KU040-FFVA1156)

XILINX

TITLE: Title Page SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 1 OF 66	DRAWN BY: BF





SMT, 14-pin JTAG Buffers

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System Controller IIC, JTAG, SD

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BANK#	PAGE#	BANK#	PAGE#
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BANK 44	4	BANK 67	8
BANK 45	4	BANK 68	9
BANK 46	5	MGT225-228	10
BANK 47	6		
BANK 48	6		
BANK 64	7	PWR/GND BANKS	11-13
BANK 65	7	PWR CONNECTORS	50-51

MECHANICALS

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XILINX

TITLE: Block Diagram
SCHEM, ROHS COMPLIANT
HW-U1-KCU105_REV1_1

ASSY P/N: 0431811
PCB P/N: 1280723
SCH P/N: 0381556
TEST P/N: TSS0165

DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 2 OF 66	DRAWN BY: BF

POR_OVERRIDE select
Default: 2-3 GND

PCIe Test Header

Bank 0 HR

SOC_KU040_FFVA1156_IRON_REVD

BANK 0
XCKU040FFVA1156

U1

SOC_IRONWOOD_FF1156

VCCINT_FPGA

J5 HDR_1X3

J78 HDR_1X4

GND

SYS_1V8

C542 0.1UF 25V

UTIL_3V3

C541 0.1UF 25V

SN74AVC1T45

U84

SC70_6

COMBINED_PGOOD_LS

COMBINED_PGOOD

R554 200 1/10W 1%

R553 200 1/10W 1%

VCC1V8_FPGA

R953 1.00K 1/16W 1%

R418 DNP DNP DNP

PUDC_B_0_R7
POR_OVERRIDE_P7
RDWR_FCS_B_0_U7
DXP_Y12
DXN_Y11
VCCADC_U12
GNDADC_U11
VREFN_V11
VREFP_W12
VP_V12
VN_W11
VBATT_AD7
CCLK_0_AA9
TCK_0_AC9
TMS_0_W9
TDO_0_U9
TDI_0_V9
INIT_B_0_V7
PROGRAM_B_0_T7
CFGBVS_0_W7
DONE_0_N7
D03_0_Y7
D02_0_AA7
D01_DIN_0_AB7
D00_MOSI_0_AC7
M2_0_M7
M1_0_L7
M0_0_K7

R7 P7 U7 Y12 Y11 U12 U11 V11 W12 V12 W11 AD7 AA9 AC9 W9 U9 V9 V7 T7 W7 N7 Y7 AA7 AB7 AC7 M7 L7 K7

QSPI0_CS_B
SYSMON_DXP
SYSMON_DXN
SYSMON_VCC
SYSMON_VREFP
SYSMON_VP_R
SYSMON_VN_R
FPGA_VBATT
FPGA_CCLK
JTAG_TCK
JTAG_TMS
FPGA_TDO_FMC_TDI
JTAG_TDI
FPGA_INIT_B
FPGA_PROG_B
FPGA_DONE
QSPI0_IO3
QSPI0_IO2
QSPI0_IO1
QSPI0_IO0
FPGA_M2

C2 0.1UF 25V

C1 0.1UF 25V

SYSMON_AGND

VCC1V8_FPGA

AB9 Y9 VCCO_0_AB9 VCCO_0_Y9

VCC1V8

R807 1.00K 1/16W 1%

R116 4.70K 1/16W 1%

R806 1.00K 1/16W 1%

R339 DNP DNP DNP

C357 DNP DNP DNP

LAYOUT: Place CCLK termination pads after last QSPI device

VCCAUX_FPGA

R547 DNP DNP DNP

J80 HDR_1X2

SYSMON_VP_R_I2C

SYSMON_VP_R

R548 20.5K 1/10W 1%

J81 HDR_1X2

SYSMON_VN_R_I2C

SYSMON_VN_R

R560 20.5K 1/10W 1%

SYSMON I2C Address jumpers

D15 200MW 40V BAS40-04

NC

SYS_1V8

R115 4.70K 1/16W 1%

FPGA_VBATT

TS518FE_FL35E

B1 BAT_TS518_TS621_DUAL

VCC1V8

R6 4.7K 1/10W 5%

C540 0.1UF 25V

SN74AVC1T45

U53

SC70_6

FPGA_INIT_B

C633 0.1UF 25V

R473 261 1/10W 1%

DS2 RED GRN LED-GRN-RED

R472 261 1/10W 1%

VCC1V8

R236 4.70K 1/16W 1%

C642 0.1UF 25V

SN74AVC1T45

U90

SC70_6

FPGA_DONE

C643 0.1UF 25V

R598 261 1/10W 1%

DS34

FPGA Bank 0

XILINX

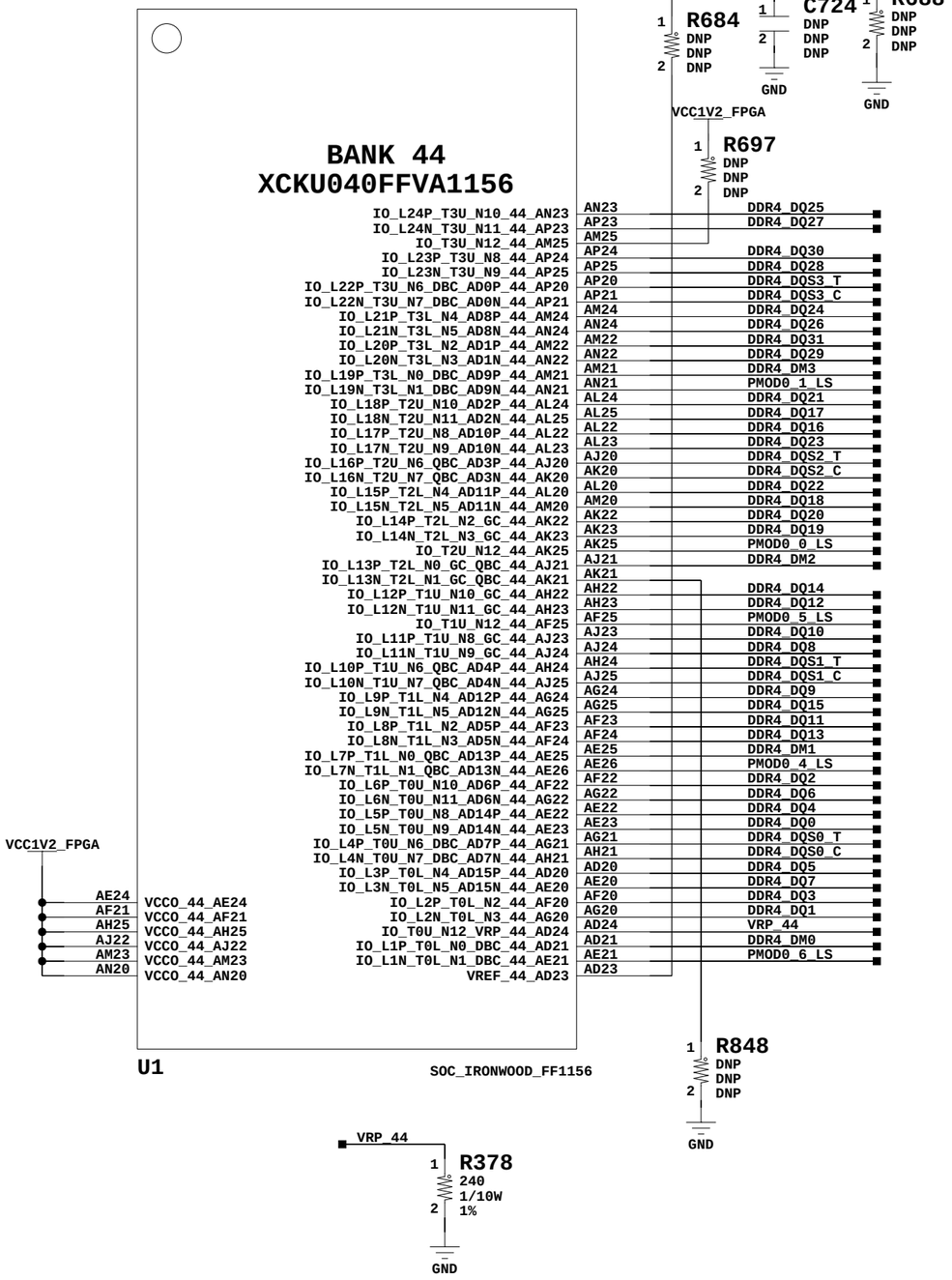
TITLE: FPGA Bank 0 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 3 OF 66	DRAWN BY: BF

Layout: Place resistor and capacitor for VREF

Underneath the FPGA via array
right next to the via

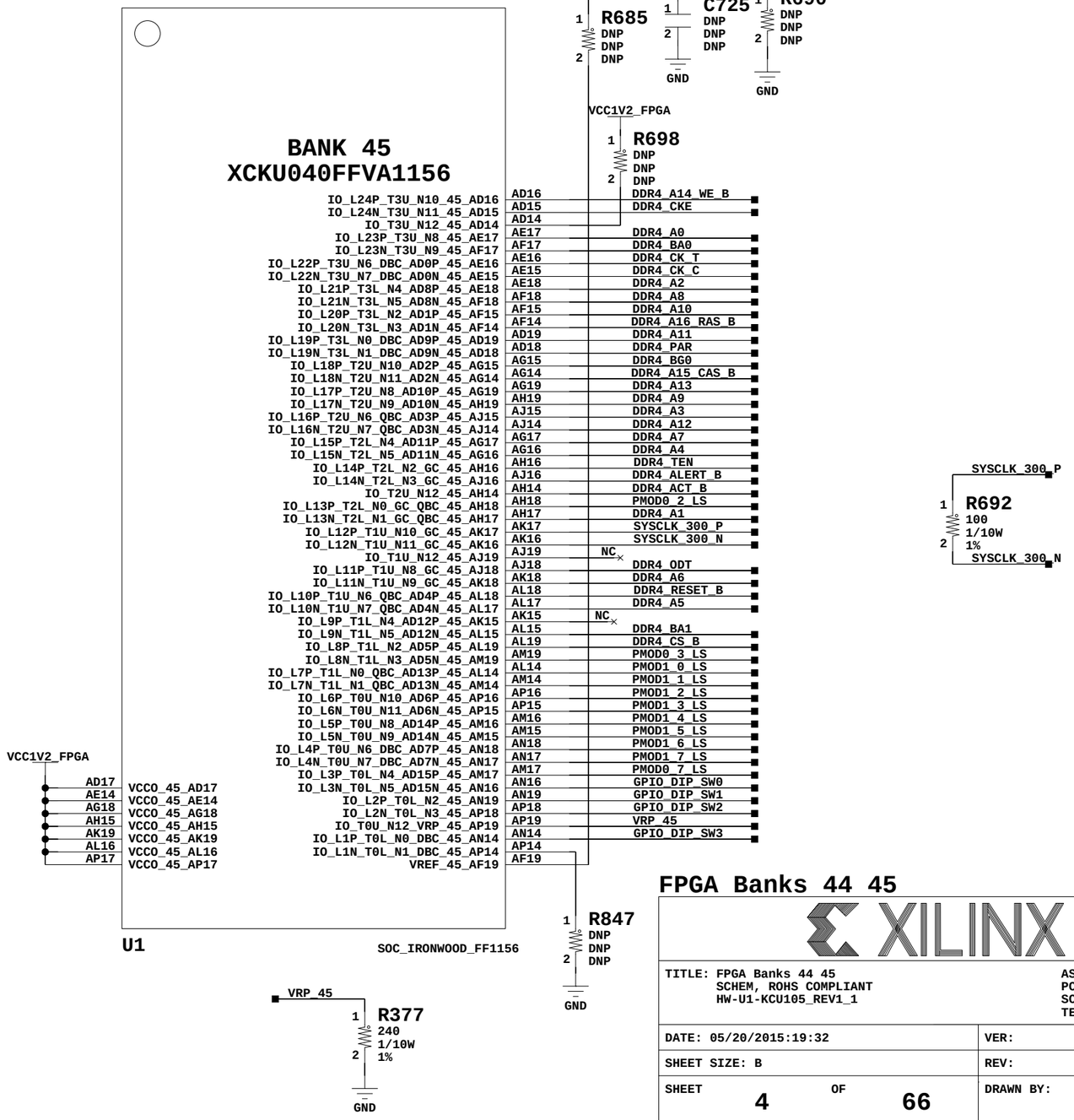
Bank 44 HP

SOC_KU040_FFVA1156_IRON_REVD



Bank 45 HP

SOC_KU040_FFVA1156_IRON_REVD



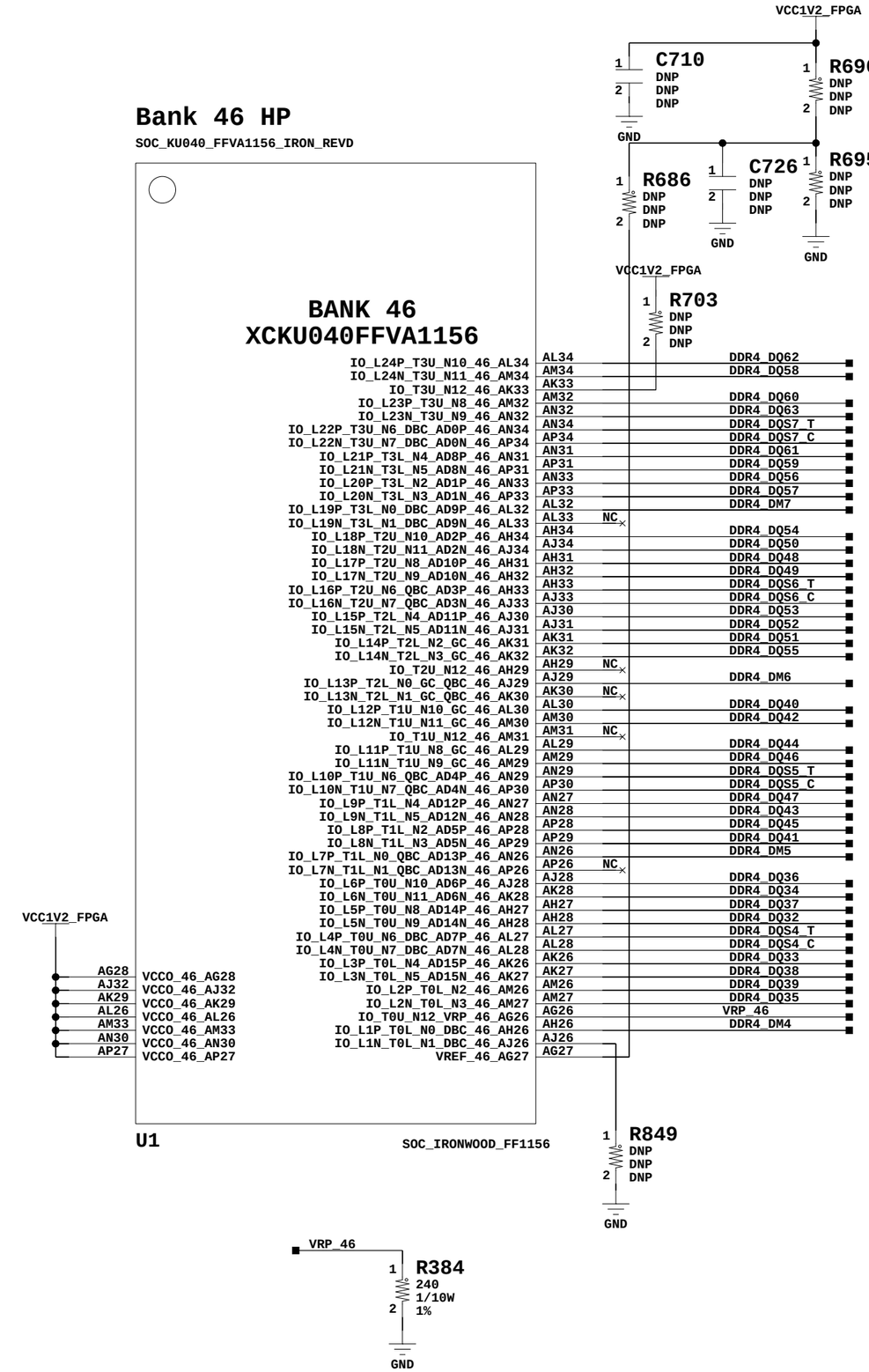
FPGA Banks 44 45

XILINX

TITLE: FPGA Banks 44 45 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 4 OF 66	DRAWN BY: BF

Bank 46 HP

SOC_KU040_FFVA1156_IRON_REVD



Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

FPGA Bank 46

XILINX

TITLE: FPGA Bank 46 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 5 OF 66	DRAWN BY: BF

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

Bank 47 HP

SOC_KU040_FFVA1156_IRON_REVD

FMC_LPC_VREF_A_M2C

R794 DNP DNP DNP

C854 DNP DNP DNP

GND

VADJ_1V8_FPGA

R699 DNP DNP DNP

BANK 47
XCKU040FFVA1156

IO_L24P_T3U_N10_47_V26	V26	FMC_LPC_LA09_P
IO_L24N_T3U_N11_47_W26	W26	FMC_LPC_LA09_N
IO_T3U_N12_47_U29	U29	
IO_L23P_T3U_N8_47_V29	V29	FMC_LPC_LA06_P
IO_L23N_T3U_N9_47_W29	W29	FMC_LPC_LA06_N
IO_L22P_T3U_N6_DBC_AD0P_47_U26	U26	FMC_LPC_LA04_P
IO_L22N_T3U_N7_DBC_AD0N_47_U27	U27	FMC_LPC_LA04_N
IO_L21P_T3L_N4_AD8P_47_W28	W28	FMC_LPC_LA03_P
IO_L21N_T3L_N5_AD8N_47_Y28	Y28	FMC_LPC_LA03_N
IO_L20P_T3L_N2_AD1P_47_U24	U24	FMC_LPC_LA08_P
IO_L20N_T3L_N3_AD1N_47_U25	U25	FMC_LPC_LA08_N
IO_L19P_T3L_N0_DBC_AD9P_47_V27	V27	FMC_LPC_LA05_P
IO_L19N_T3L_N1_DBC_AD9N_47_V28	V28	FMC_LPC_LA05_N
IO_L18P_T2U_N10_AD2P_47_V21	V21	FMC_LPC_LA11_P
IO_L18N_T2U_N11_AD2N_47_W21	W21	FMC_LPC_LA11_N
IO_L17P_T2U_N8_AD10P_47_T22	T22	FMC_LPC_LA10_P
IO_L17N_T2U_N9_AD10N_47_T23	T23	FMC_LPC_LA10_N
IO_L16P_T2U_N6_QBC_AD3P_47_V22	V22	FMC_LPC_LA07_P
IO_L16N_T2U_N7_QBC_AD3N_47_V23	V23	FMC_LPC_LA07_N
IO_L15P_T2L_N4_AD11P_47_U21	U21	FMC_LPC_LA14_P
IO_L15N_T2L_N5_AD11N_47_U22	U22	FMC_LPC_LA14_N
IO_L14P_T2L_N2_GC_47_W25	W25	FMC_LPC_LA01_CC_P
IO_L14N_T2L_N3_GC_47_Y25	Y25	FMC_LPC_LA01_CC_N
IO_T2U_N12_47_Y21	Y21	ROTARY_INCA
IO_L13P_T2L_N0_GC_QBC_47_W23	W23	FMC_LPC_LA00_CC_P
IO_L13N_T2L_N1_GC_QBC_47_W24	W24	FMC_LPC_LA00_CC_N
IO_L12P_T1U_N10_GC_47_AA24	AA24	FMC_LPC_CLK0_M2C_P
IO_L12N_T1U_N11_GC_47_AA25	AA25	FMC_LPC_CLK0_M2C_N
IO_T1U_N12_47_Y22	Y22	NC
IO_L11P_T1U_N8_GC_47_Y23	Y23	NC
IO_L11N_T1U_N9_GC_47_AA23	AA23	NC
IO_L10P_T1U_N6_QBC_AD4P_47_AB21	AB21	FMC_LPC_LA16_P
IO_L10N_T1U_N7_QBC_AD4N_47_AC21	AC21	FMC_LPC_LA16_N
IO_L9P_T1L_N4_AD12P_47_AA20	AA20	FMC_LPC_LA13_P
IO_L9N_T1L_N5_AD12N_47_AB20	AB20	FMC_LPC_LA13_N
IO_L8P_T1L_N2_AD5P_47_AC22	AC22	FMC_LPC_LA12_P
IO_L8N_T1L_N3_AD5N_47_AC23	AC23	FMC_LPC_LA12_N
IO_L7P_T1L_N0_QBC_AD13P_47_AA22	AA22	FMC_LPC_LA02_P
IO_L7N_T1L_N1_QBC_AD13N_47_AB22	AB22	FMC_LPC_LA02_N
IO_L6P_T0U_N10_AD6P_47_AB25	AB25	FMC_LPC_LA15_P
IO_L6N_T0U_N11_AD6N_47_AB26	AB26	FMC_LPC_LA15_N
IO_L5P_T0U_N8_AD14P_47_AA27	AA27	NC
IO_L5N_T0U_N9_AD14N_47_AB27	AB27	NC
IO_L4P_T0U_N6_DBC_AD7P_47_AC26	AC26	NC
IO_L4N_T0U_N7_DBC_AD7N_47_AC27	AC27	NC
IO_L3P_T0L_N4_AD15P_47_AB24	AB24	NC
IO_L3N_T0L_N5_AD15N_47_AC24	AC24	NC
IO_L2P_T0L_N2_47_AD25	AD25	NC
IO_L2N_T0L_N3_47_AD26	AD26	ROTARY_INCB
IO_T0U_N12_VRP_47_AA28	AA28	VRP_47
IO_L1P_T0L_N0_DBC_47_Y26	Y26	NC
IO_L1N_T0L_N1_DBC_47_Y27	Y27	NC
VREF_47_V24	V24	

VADJ_1V8_FPGA

T21	VCCO_47_T21
U28	VCCO_47_U28
V25	VCCO_47_V25
W22	VCCO_47_W22
AA26	VCCO_47_AA26
AB23	VCCO_47_AB23
AC20	VCCO_47_AC20

U1

SOC_IRONWOOD_FF1156

VRP_47

R379 240 1/10W 1%

GND

Bank 48 HP

SOC_KU040_FFVA1156_IRON_REVD

FMC_LPC_VREF_A_M2C

R795 DNP DNP DNP

C855 DNP DNP DNP

GND

VADJ_1V8_FPGA

R583 DNP DNP DNP

BANK 48
XCKU040FFVA1156

IO_L24P_T3U_N10_48_V31	V31	FMC_LPC_LA28_P
IO_L24N_T3U_N11_48_W31	W31	FMC_LPC_LA28_N
IO_T3U_N12_48_V32	V32	
IO_L23P_T3U_N8_48_U34	U34	FMC_LPC_LA29_P
IO_L23N_T3U_N9_48_V34	V34	FMC_LPC_LA29_N
IO_L22P_T3U_N6_DBC_AD0P_48_Y31	Y31	FMC_LPC_LA30_P
IO_L22N_T3U_N7_DBC_AD0N_48_Y32	Y32	FMC_LPC_LA30_N
IO_L21P_T3L_N4_AD8P_48_V33	V33	FMC_LPC_LA31_P
IO_L21N_T3L_N5_AD8N_48_W34	W34	FMC_LPC_LA31_N
IO_L20P_T3L_N2_AD1P_48_W30	W30	FMC_LPC_LA32_P
IO_L20N_T3L_N3_AD1N_48_Y30	Y30	FMC_LPC_LA32_N
IO_L19P_T3L_N0_DBC_AD9P_48_W33	W33	FMC_LPC_LA33_P
IO_L19N_T3L_N1_DBC_AD9N_48_Y33	Y33	FMC_LPC_LA33_N
IO_L18P_T2U_N10_AD2P_48_AC33	AC33	FMC_LPC_LA21_P
IO_L18N_T2U_N11_AD2N_48_AD33	AD33	FMC_LPC_LA21_N
IO_L17P_T2U_N8_AD10P_48_AA34	AA34	FMC_LPC_LA20_P
IO_L17N_T2U_N9_AD10N_48_AB34	AB34	FMC_LPC_LA20_N
IO_L16P_T2U_N6_QBC_AD3P_48_AA29	AA29	FMC_LPC_LA19_P
IO_L16N_T2U_N7_QBC_AD3N_48_AB29	AB29	FMC_LPC_LA19_N
IO_L15P_T2L_N4_AD11P_48_AC34	AC34	FMC_LPC_LA22_P
IO_L15N_T2L_N5_AD11N_48_AD34	AD34	FMC_LPC_LA22_N
IO_L14P_T2L_N2_GC_48_AB30	AB30	FMC_LPC_LA18_CC_P
IO_L14N_T2L_N3_GC_48_AB31	AB31	FMC_LPC_LA18_CC_N
IO_T2U_N12_48_AA33	AA33	NC
IO_L13P_T2L_N0_GC_QBC_48_AA32	AA32	FMC_LPC_LA17_CC_P
IO_L13N_T2L_N1_GC_QBC_48_AB32	AB32	FMC_LPC_LA17_CC_N
IO_L12P_T1U_N10_GC_48_AC31	AC31	FMC_LPC_CLK1_M2C_P
IO_L12N_T1U_N11_GC_48_AC32	AC32	FMC_LPC_CLK1_M2C_N
IO_T1U_N12_48_AE31	AE31	NC
IO_L11P_T1U_N8_GC_48_AD30	AD30	FMC_LPC_LA23_P
IO_L11N_T1U_N9_GC_48_AD31	AD31	FMC_LPC_LA23_N
IO_L10P_T1U_N6_QBC_AD4P_48_AE33	AE33	FMC_LPC_LA25_P
IO_L10N_T1U_N7_QBC_AD4N_48_AF34	AF34	FMC_LPC_LA25_N
IO_L9P_T1L_N4_AD12P_48_AE32	AE32	FMC_LPC_LA24_P
IO_L9N_T1L_N5_AD12N_48_AF32	AF32	FMC_LPC_LA24_N
IO_L8P_T1L_N2_AD5P_48_AF33	AF33	FMC_LPC_LA26_P
IO_L8N_T1L_N3_AD5N_48_AG34	AG34	FMC_LPC_LA26_N
IO_L7P_T1L_N0_QBC_AD13P_48_AG31	AG31	FMC_LPC_LA27_P
IO_L7N_T1L_N1_QBC_AD13N_48_AG32	AG32	FMC_LPC_LA27_N
IO_L6P_T0U_N10_AD6P_48_AF30	AF30	NC
IO_L6N_T0U_N11_AD6N_48_AG30	AG30	NC
IO_L5P_T0U_N8_AD14P_48_AD29	AD29	NC
IO_L5N_T0U_N9_AD14N_48_AE30	AE30	NC
IO_L4P_T0U_N6_DBC_AD7P_48_AF29	AF29	NC
IO_L4N_T0U_N7_DBC_AD7N_48_AG29	AG29	NC
IO_L3P_T0L_N4_AD15P_48_AC28	AC28	NC
IO_L3N_T0L_N5_AD15N_48_AD28	AD28	NC
IO_L2P_T0L_N2_48_AE28	AE28	NC
IO_L2N_T0L_N3_48_AF28	AF28	ROTARY_PUSH
IO_T0U_N12_VRP_48_AC29	AC29	VRP_48
IO_L1P_T0L_N0_DBC_48_AE27	AE27	NC
IO_L1N_T0L_N1_DBC_48_AF27	AF27	NC
VREF_48_AA30	AA30	

VADJ_1V8_FPGA

W32	VCCO_48_W32
Y29	VCCO_48_Y29
AB33	VCCO_48_AB33
AC30	VCCO_48_AC30
AD27	VCCO_48_AD27
AE34	VCCO_48_AE34
AF31	VCCO_48_AF31

U1

SOC_IRONWOOD_FF1156

VRP_48

R380 240 1/10W 1%

GND

FPGA Banks 47 48

XILINX

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DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 6 OF 66	DRAWN BY: BF

Bank 64 HR

SOC_KU040_FFVA1156_IRON_REVD

BANK 64
XCKU040FFVA1156

IO_L24P_T3U_N10_64_AK8	AK8	HDMI_R_D17
IO_L24N_T3U_N11_64_AL8	AL8	SFP0_TX_DISABLE
IO_T3U_N12_64_AM9	AM9	SFP1_LOS_LS
IO_L23P_T3U_N8_64_AJ9	AJ9	SM_FAN_PWM
IO_L23N_T3U_N9_64_AJ8	AJ8	SM_FAN_TACH
IO_L22P_T3U_N6_DBC_AD0P_64_AN8	AN8	CPU_RESET
IO_L22N_T3U_N7_DBC_AD0N_64_AP8	AP8	GPIO_LED_0_LS
IO_L21P_T3L_N4_AD8P_64_AK10	AK10	PMBUS_ALERT_FPGA
IO_L21N_T3L_N5_AD8N_64_AL9	AL9	MAXIM_CABLE_B_FPGA
IO_L20P_T3L_N2_AD1P_64_AN9	AN9	SDIO_DATA1_FPGA
IO_L20N_T3L_N3_AD1N_64_AP9	AP9	SDIO_DATA0_FPGA
IO_L19P_T3L_N0_DBC_AD9P_64_AL10	AL10	SDIO_CLK_FPGA
IO_L19N_T3L_N1_DBC_AD9N_64_AM10	AM10	SDIO_CD_FPGA
IO_L18P_T2U_N10_AD2P_64_AH9	AH9	SDIO_DATA2_FPGA
IO_L18N_T2U_N11_AD2N_64_AH8	AH8	SDIO_DATA3_FPGA
IO_L17P_T2U_N8_AD10P_64_AD9	AD9	SDIO_CMD_FPGA
IO_L17N_T2U_N9_AD10N_64_AD8	AD8	NC
IO_L16P_T2U_N6_QBC_AD3P_64_AD10	AD10	GPIO_SW_N
IO_L16N_T2U_N7_QBC_AD3N_64_AE10	AE10	GPIO_SW_C
IO_L15P_T2L_N4_AD11P_64_AE8	AE8	GPIO_SW_E
IO_L15N_T2L_N5_AD11N_64_AF8	AF8	GPIO_SW_S
IO_L14P_T2L_N2_GC_64_AF9	AF9	GPIO_SW_W
IO_L14N_T2L_N3_GC_64_AG9	AG9	SYSCTLR_GPIO_6
IO_T2U_N12_64_AJ10	AJ10	SYSCTLR_GPIO_5
IO_L13P_T2L_N0_GC_QBC_64_AF10	AF10	SYSCTLR_GPIO_7
IO_L13N_T2L_N1_GC_QBC_64_AG10	AG10	HDMI_R_D16
VREF_64_AD13	AD13	NC
IO_L12P_T1U_N10_GC_64_AG11	AG11	REC_CLOCK_C_P
IO_L12N_T1U_N11_GC_64_AH11	AH11	REC_CLOCK_C_N
IO_T1U_N12_64_AJ11	AJ11	HDMI_R_D15
IO_L11P_T1U_N8_GC_64_AG12	AG12	HDMI_R_D14
IO_L11N_T1U_N9_GC_64_AH12	AH12	HDMI_R_D13
IO_L10P_T1U_N6_QBC_AD4P_64_AD11	AD11	HDMI_R_D12
IO_L10N_T1U_N7_QBC_AD4N_64_AE11	AE11	HDMI_R_DE
IO_L9P_T1L_N4_AD12P_64_AE12	AE12	HDMI_R_SPDIF
IO_L9N_T1L_N5_AD12N_64_AF12	AF12	HDMI_SPDIF_OUT_LS
IO_L8P_T1L_N2_AD5P_64_AH13	AH13	HDMI_R_VSYNC
IO_L8N_T1L_N3_AD5N_64_AJ13	AJ13	HDMI_INT
IO_L7P_T1L_N0_QBC_AD13P_64_AE13	AE13	HDMI_R_HSYNC
IO_L7N_T1L_N1_QBC_AD13N_64_AF13	AF13	HDMI_R_CLK
IO_L6P_T0U_N10_AD6P_64_AK13	AK13	HDMI_R_D11
IO_L6N_T0U_N11_AD6N_64_AL13	AL13	HDMI_R_D10
IO_L5P_T0U_N8_AD14P_64_AK12	AK12	HDMI_R_D9
IO_L5N_T0U_N9_AD14N_64_AL12	AL12	HDMI_R_D8
IO_L4P_T0U_N6_DBC_AD7P_64_AM12	AM12	HDMI_R_D7
IO_L4N_T0U_N7_DBC_AD7N_64_AN12	AN12	HDMI_R_D6
IO_L3P_T0L_N4_AD15P_64_AM11	AM11	HDMI_R_D5
IO_L3N_T0L_N5_AD15N_64_AN11	AN11	HDMI_R_D4
IO_L2P_T0L_N2_64_AN13	AN13	HDMI_R_D3
IO_L2N_T0L_N3_64_AP13	AP13	HDMI_R_D2
IO_T0U_N12_64_AK11	AK11	HDMI_R_D0
IO_L1P_T0L_N0_DBC_64_AP11	AP11	HDMI_R_D1
IO_L1N_T0L_N1_DBC_64_AP10	AP10	IIC_MUX_RESET_B_LS

VCC1V8_FPGA

AF11	VCCO_64_AF11
AG8	VCCO_64_AG8
AJ12	VCCO_64_AJ12
AK9	VCCO_64_AK9
AM13	VCCO_64_AM13
AN10	VCCO_64_AN10

U1

SOC_IRONWOOD_FF1156

Bank 65 HR

SOC_KU040_FFVA1156_IRON_REVD

BANK 65
XCKU040FFVA1156

IO_L24P_T3U_N10_EMCCLK_65_K20	K20	FPGA_EMCCLK
IO_L24N_T3U_N11_DOUT_CSO_B_65_K21	K21	SFP0_LOS_LS
IO_T3U_N12_PERSTN0_65_K22	K22	PCIE_PERST_LS
IO_L23P_T3U_N8_I2C_SCLK_65_N21	N21	SYSMON_SCL_LS
IO_L23N_T3U_N9_I2C_SDA_65_M21	M21	SYSMON_SDA_LS
IO_L22P_T3U_N6_DBC_AD0P_D04_65_M20	M20	QSPI1_IO0
IO_L22N_T3U_N7_DBC_AD0N_D05_65_L20	L20	QSPI1_IO1
IO_L21P_T3L_N4_AD8P_D06_65_R21	R21	QSPI1_IO2
IO_L21N_T3L_N5_AD8N_D07_65_R22	R22	QSPI1_IO3
IO_L20P_T3L_N2_AD1P_D08_65_P20	P20	GPIO_LED_2_LS
IO_L20N_T3L_N3_AD1N_D09_65_P21	P21	GPIO_LED_3_LS
IO_L19P_T3L_N0_DBC_AD9P_D10_65_N22	N22	GPIO_LED_4_LS
IO_L19N_T3L_N1_DBC_AD9N_D11_65_M22	M22	GPIO_LED_5_LS
IO_L18P_T2U_N10_AD2P_D12_65_R23	R23	GPIO_LED_6_LS
IO_L18N_T2U_N11_AD2N_D13_65_P23	P23	GPIO_LED_7_LS
IO_L17P_T2U_N8_AD10P_D14_65_R25	R25	NC
IO_L17N_T2U_N9_AD10N_D15_65_R26	R26	NC
IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65_T24	T24	NC
IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65_T25	T25	NC
IO_L15P_T2L_N4_AD11P_A02_D18_65_T27	T27	SYSMON_MUX_ADDR0_LS
IO_L15N_T2L_N5_AD11N_A03_D19_65_R27	R27	SYSMON_MUX_ADDR1_LS
IO_L14P_T2L_N2_GC_A04_D20_65_P24	P24	SGMII_RX_P
IO_L14N_T2L_N3_GC_A05_D21_65_P25	P25	SGMII_RX_N
IO_T2U_N12_CSI_ADV_B_65_N27	N27	SYSMON_MUX_ADDR2_LS
IO_L13P_T2L_N0_GC_QBC_A06_D22_65_P26	P26	SGMIICLK_P
IO_L13N_T2L_N1_GC_QBC_A07_D23_65_N26	N26	SGMIICLK_N
VREF_65_J21	J21	NC
IO_L12P_T1U_N10_GC_A08_D24_65_N24	N24	SGMII_TX_P
IO_L12N_T1U_N11_GC_A09_D25_65_M24	M24	SGMII_TX_N
IO_T1U_N12_PERSTN1_65_N23	N23	PCIE_WAKE_B_LS
IO_L11P_T1U_N8_GC_A10_D26_65_M25	M25	USER_SI570_CLOCK_P
IO_L11N_T1U_N9_GC_A11_D27_65_M26	M26	USER_SI570_CLOCK_N
IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65_L22	L22	SI5328_INT_ALM_LS
IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65_K23	K23	SI5328_RST_LS
IO_L9P_T1L_N4_AD12P_A14_D30_65_L25	L25	PHY_MDC_LS
IO_L9N_T1L_N5_AD12N_A15_D31_65_K25	K25	PHY_INT_LS
IO_L8P_T1L_N2_AD5P_A16_65_L23	L23	USB_UART_CTS
IO_L8N_T1L_N3_AD5N_A17_65_L24	L24	FMC_VADJ_ON_LS
IO_L7P_T1L_N0_QBC_AD13P_A18_65_M27	M27	VADJ_1V8_PGOOD_LS
IO_L7N_T1L_N1_QBC_AD13N_A19_65_L27	L27	FMC_HPC_PG_M2C_LS
IO_L6P_T0U_N10_AD6P_A20_65_J23	J23	PHY_RESET_LS
IO_L6N_T0U_N11_AD6N_A21_65_H24	H24	FMC_HPC_PRSNT_M2C_B_LS
IO_L5P_T0U_N8_AD14P_A22_65_J26	J26	FMC_LPC_PRSNT_M2C_B_LS
IO_L5N_T0U_N9_AD14N_A23_65_H26	H26	PHY_MDIO_LS
IO_L4P_T0U_N6_DBC_AD7P_A24_65_J24	J24	IIC_MAIN_SCL_LS
IO_L4N_T0U_N7_DBC_AD7N_A25_65_J25	J25	IIC_MAIN_SDA_LS
IO_L3P_T0L_N4_AD15P_A26_65_K26	K26	USB_UART_RX
IO_L3N_T0L_N5_AD15N_A27_65_K27	K27	USB_UART_RTS
IO_L2P_T0L_N2_FOE_B_65_G25	G25	USB_UART_TX
IO_L2N_T0L_N3_FWE_FCS2_B_65_G26	G26	QSPI1_CS_B
IO_T0U_N12_A28_65_H23	H23	GPIO_LED_1_LS
IO_L1P_T0L_N0_DBC_RS0_65_H27	H27	USER_SMA_GPIO_P
IO_L1N_T0L_N1_DBC_RS1_65_G27	G27	USER_SMA_GPIO_N

VCC1V8_FPGA

H25	VCCO_65_H25
J22	VCCO_65_J22
L26	VCCO_65_L26
M23	VCCO_65_M23
N20	VCCO_65_N20
P27	VCCO_65_P27
R24	VCCO_65_R24

U1

SOC_IRONWOOD_FF1156

SGMIICLK_P — R865 (100, 1/10W, 1%) — SGMIICLK_N

SGMII_RX_P — R888 (100, 1/10W, 1%) — SGMII_RX_N

USER_SI570_CLOCK_P — R866 (100, 1/10W, 1%) — USER_SI570_CLOCK_N

FPGA Banks 64 65

XILINX

TITLE: FPGA Banks 64 65 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 7 OF 66	DRAWN BY: BF

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

Bank 66 HP

SOC_KU040_FFVA1156_IRON_REVD

FMC_HPC_VREF_A_M2C

R796 DNP DNP DNP — C856 DNP DNP DNP — GND

VADJ_1V8_FPGA

R701 DNP DNP DNP

CLK_125MHZ_P — R150 100 1/10W 1% — CLK_125MHZ_N

BANK 66
XCKU040FFVA1156

IO_L24P_T3U_N10_66_D13	D13	FMC_HPC_LA06_P
IO_L24N_T3U_N11_66_C13	C13	FMC_HPC_LA06_N
IO_T3U_N12_66_E12	E12	
IO_L23P_T3U_N8_66_A13	A13	FMC_HPC_LA03_P
IO_L23N_T3U_N9_66_A12	A12	FMC_HPC_LA03_N
IO_L22P_T3U_N6_DBC_AD0P_66_F13	F13	SYSMON_AD0_R_P
IO_L22N_T3U_N7_DBC_AD0N_66_E13	E13	SYSMON_AD0_R_N
IO_L21P_T3L_N4_AD8P_66_C11	C11	SYSMON_AD8_R_P
IO_L21N_T3L_N5_AD8N_66_B11	B11	SYSMON_AD8_R_N
IO_L20P_T3L_N2_AD1P_66_C12	C12	NC
IO_L20N_T3L_N3_AD1N_66_B12	B12	NC
IO_L19P_T3L_N0_DBC_AD9P_66_E11	E11	NC
IO_L19N_T3L_N1_DBC_AD9N_66_D11	D11	NC
IO_L18P_T2U_N10_AD2P_66_J13	J13	SYSMON_AD2_R_P
IO_L18N_T2U_N11_AD2N_66_H13	H13	SYSMON_AD2_R_N
IO_L17P_T2U_N8_AD10P_66_L12	L12	FMC_HPC_LA04_P
IO_L17N_T2U_N9_AD10N_66_K12	K12	FMC_HPC_LA04_N
IO_L16P_T2U_N6_QBC_AD3P_66_L13	L13	FMC_HPC_LA05_P
IO_L16N_T2U_N7_QBC_AD3N_66_K13	K13	FMC_HPC_LA05_N
IO_L15P_T2L_N4_AD11P_66_K11	K11	FMC_HPC_LA11_P
IO_L15N_T2L_N5_AD11N_66_J11	J11	FMC_HPC_LA11_N
IO_L14P_T2L_N2_GC_66_H12	H12	FMC_HPC_CLK0_M2C_P
IO_L14N_T2L_N3_GC_66_G12	G12	FMC_HPC_CLK0_M2C_N
IO_T2U_N12_66_F12	F12	SI570_CLK_SEL_LS
IO_L13P_T2L_N0_GC_QBC_66_H11	H11	FMC_HPC_LA00_CC_P
IO_L13N_T2L_N1_GC_QBC_66_G11	G11	FMC_HPC_LA00_CC_N
IO_L12P_T1U_N10_GC_66_G10	G10	CLK_125MHZ_P
IO_L12N_T1U_N11_GC_66_F10	F10	CLK_125MHZ_N
IO_T1U_N12_66_L9	L9	NC
IO_L11P_T1U_N8_GC_66_G9	G9	FMC_HPC_LA01_CC_P
IO_L11N_T1U_N9_GC_66_F9	F9	FMC_HPC_LA01_CC_N
IO_L10P_T1U_N6_QBC_AD4P_66_K10	K10	FMC_HPC_LA02_P
IO_L10N_T1U_N7_QBC_AD4N_66_J10	J10	FMC_HPC_LA02_N
IO_L9P_T1L_N4_AD12P_66_J8	J8	FMC_HPC_LA08_P
IO_L9N_T1L_N5_AD12N_66_H8	H8	FMC_HPC_LA08_N
IO_L8P_T1L_N2_AD5P_66_J9	J9	FMC_HPC_LA09_P
IO_L8N_T1L_N3_AD5N_66_H9	H9	FMC_HPC_LA09_N
IO_L7P_T1L_N0_QBC_AD13P_66_L8	L8	FMC_HPC_LA10_P
IO_L7N_T1L_N1_QBC_AD13N_66_K8	K8	FMC_HPC_LA10_N
IO_L6P_T0U_N10_AD6P_66_E10	E10	FMC_HPC_LA12_P
IO_L6N_T0U_N11_AD6N_66_D10	D10	FMC_HPC_LA12_N
IO_L5P_T0U_N8_AD14P_66_D9	D9	FMC_HPC_LA13_P
IO_L5N_T0U_N9_AD14N_66_C9	C9	FMC_HPC_LA13_N
IO_L4P_T0U_N6_DBC_AD7P_66_B10	B10	FMC_HPC_LA14_P
IO_L4N_T0U_N7_DBC_AD7N_66_A10	A10	FMC_HPC_LA14_N
IO_L3P_T0L_N4_AD15P_66_D8	D8	FMC_HPC_LA15_P
IO_L3N_T0L_N5_AD15N_66_C8	C8	FMC_HPC_LA15_N
IO_L2P_T0L_N2_66_B9	B9	FMC_HPC_LA16_P
IO_L2N_T0L_N3_66_A9	A9	FMC_HPC_LA16_N
IO_T0U_N12_VRP_66_A8	A8	VRP_66
IO_L1P_T0L_N0_DBC_66_F8	F8	FMC_HPC_LA07_P
IO_L1N_T0L_N1_DBC_66_E8	E8	FMC_HPC_LA07_N
VREF_66_L10	L10	

VADJ_1V8_FPGA

B13	VCCO_66_B13
C10	VCCO_66_C10
F11	VCCO_66_F11
G8	VCCO_66_G8
J12	VCCO_66_J12
K9	VCCO_66_K9

U1

SOC_IRONWOOD_FF1156

VRP_66 — R700 240 1/10W 1% — GND

Bank 67 HP

SOC_KU040_FFVA1156_IRON_REVD

FMC_HPC_VREF_A_M2C

R797 DNP DNP DNP — C857 DNP DNP DNP — GND

VADJ_1V8_FPGA

R584 DNP DNP DNP

BANK 67
XCKU040FFVA1156

IO_L24P_T3U_N10_67_H21	H21	FMC_HPC_LA27_P
IO_L24N_T3U_N11_67_G21	G21	FMC_HPC_LA27_N
IO_T3U_N12_67_H22	H22	
IO_L23P_T3U_N8_67_G22	G22	FMC_HPC_LA23_P
IO_L23N_T3U_N9_67_F22	F22	FMC_HPC_LA23_N
IO_L22P_T3U_N6_DBC_AD0P_67_G20	G20	FMC_HPC_LA26_P
IO_L22N_T3U_N7_DBC_AD0N_67_F20	F20	FMC_HPC_LA26_N
IO_L21P_T3L_N4_AD8P_67_F23	F23	FMC_HPC_LA21_P
IO_L21N_T3L_N5_AD8N_67_F24	F24	FMC_HPC_LA21_N
IO_L20P_T3L_N2_AD1P_67_E20	E20	FMC_HPC_LA24_P
IO_L20N_T3L_N3_AD1N_67_E21	E21	FMC_HPC_LA24_N
IO_L19P_T3L_N0_DBC_AD9P_67_G24	G24	FMC_HPC_LA22_P
IO_L19N_T3L_N1_DBC_AD9N_67_F25	F25	FMC_HPC_LA22_N
IO_L18P_T2U_N10_AD2P_67_D20	D20	FMC_HPC_LA25_P
IO_L18N_T2U_N11_AD2N_67_D21	D21	FMC_HPC_LA25_N
IO_L17P_T2U_N8_AD10P_67_B20	B20	FMC_HPC_LA29_P
IO_L17N_T2U_N9_AD10N_67_A20	A20	FMC_HPC_LA29_N
IO_L16P_T2U_N6_QBC_AD3P_67_C21	C21	FMC_HPC_LA19_P
IO_L16N_T2U_N7_QBC_AD3N_67_C22	C22	FMC_HPC_LA19_N
IO_L15P_T2L_N4_AD11P_67_B21	B21	FMC_HPC_LA28_P
IO_L15N_T2L_N5_AD11N_67_B22	B22	FMC_HPC_LA28_N
IO_L14P_T2L_N2_GC_67_E22	E22	FMC_HPC_LA18_CC_P
IO_L14N_T2L_N3_GC_67_E23	E23	FMC_HPC_LA18_CC_N
IO_T2U_N12_67_A22	A22	NC
IO_L13P_T2L_N0_GC_QBC_67_D23	D23	USER_SMA_CLOCK_P
IO_L13N_T2L_N1_GC_QBC_67_C23	C23	USER_SMA_CLOCK_N
IO_L12P_T1U_N10_GC_67_D24	D24	FMC_HPC_LA17_CC_P
IO_L12N_T1U_N11_GC_67_C24	C24	FMC_HPC_LA17_CC_N
IO_T1U_N12_67_A23	A23	NC
IO_L11P_T1U_N8_GC_67_E25	E25	FMC_HPC_CLK1_M2C_P
IO_L11N_T1U_N9_GC_67_D25	D25	FMC_HPC_CLK1_M2C_N
IO_L10P_T1U_N6_QBC_AD4P_67_B24	B24	FMC_HPC_LA20_P
IO_L10N_T1U_N7_QBC_AD4N_67_A24	A24	FMC_HPC_LA20_N
IO_L9P_T1L_N4_AD12P_67_C26	C26	FMC_HPC_LA30_P
IO_L9N_T1L_N5_AD12N_67_B26	B26	FMC_HPC_LA30_N
IO_L8P_T1L_N2_AD5P_67_B25	B25	FMC_HPC_LA31_P
IO_L8N_T1L_N3_AD5N_67_A25	A25	FMC_HPC_LA31_N
IO_L7P_T1L_N0_QBC_AD13P_67_E26	E26	FMC_HPC_LA32_P
IO_L7N_T1L_N1_QBC_AD13N_67_D26	D26	FMC_HPC_LA32_N
IO_L6P_T0U_N10_AD6P_67_A27	A27	FMC_HPC_LA33_P
IO_L6N_T0U_N11_AD6N_67_A28	A28	FMC_HPC_LA33_N
IO_L5P_T0U_N8_AD14P_67_D28	D28	SFP1_TX_DISABLE
IO_L5N_T0U_N9_AD14N_67_C28	C28	NC
IO_L4P_T0U_N6_DBC_AD7P_67_B29	B29	NC
IO_L4N_T0U_N7_DBC_AD7N_67_A29	A29	NC
IO_L3P_T0L_N4_AD15P_67_E28	E28	NC
IO_L3N_T0L_N5_AD15N_67_D29	D29	NC
IO_L2P_T0L_N2_67_C27	C27	NC
IO_L2N_T0L_N3_67_B27	B27	NC
IO_T0U_N12_VRP_67_C29	C29	VRP_67
IO_L1P_T0L_N0_DBC_67_F27	F27	NC
IO_L1N_T0L_N1_DBC_67_E27	E27	NC
VREF_67_J20	J20	

VADJ_1V8_FPGA

A26	VCCO_67_A26
B23	VCCO_67_B23
C20	VCCO_67_C20
D27	VCCO_67_D27
E24	VCCO_67_E24
F21	VCCO_67_F21

U1

SOC_IRONWOOD_FF1156

USER_SMA_CLOCK_P — R896 100 1/10W 1% — USER_SMA_CLOCK_N

VRP_67 — R382 240 1/10W 1% — GND

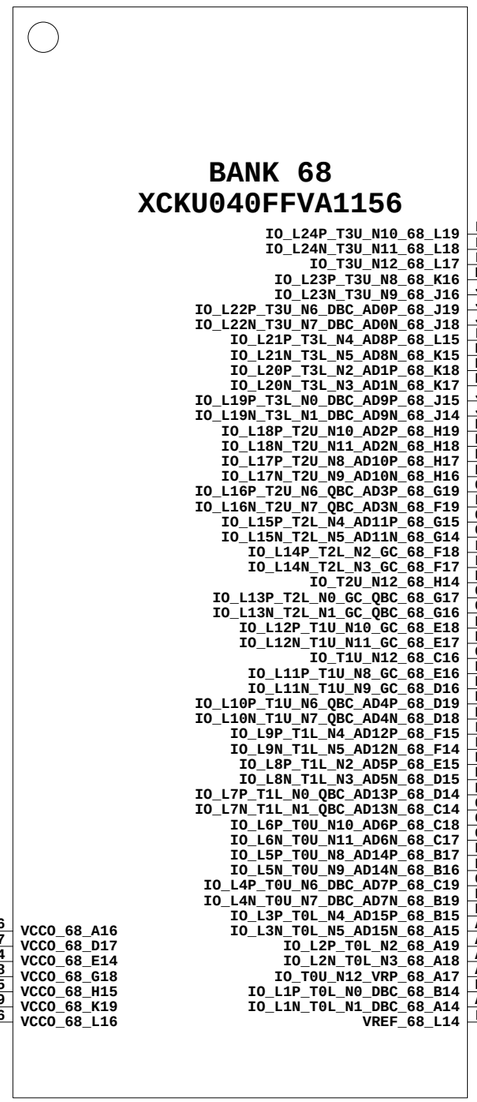
FPGA Banks 66 67

XILINX

TITLE: FPGA Banks 66 67 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 8 OF 66	DRAWN BY: BF

Bank 68 HP

SOC_KU040_FFVA1156_IRON_REVD



FMC_HPC_VREF_A_M2C

R798 DNP DNP DNP

C858 DNP DNP DNP

GND

VADJ_1V8_FPGA

R702 DNP DNP DNP

VRP_68

R383 240 1/10W 1%

GND

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

FPGA Bank 68

XILINX

TITLE: FPGA Bank 68 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 9 OF 66	DRAWN BY: BF

SOC_KU040_FFVA1156_IRON_REVD

BANK 224
XCKU040FFVA1156

MGTHTXP0_224_AN4	AN4	PCIE_TX7_P
MGTHTXN0_224_AN3	AN3	PCIE_TX7_N
MGTHRXP0_224_AP2	AP2	PCIE_RX7_P
MGTHRXN0_224_AP1	AP1	PCIE_RX7_N
MGTHTXP1_224_AM6	AM6	PCIE_TX6_P
MGTHTXN1_224_AM5	AM5	PCIE_TX6_N
MGTHRXP1_224_AM2	AM2	PCIE_RX6_P
MGTHRXN1_224_AM1	AM1	PCIE_RX6_N
MGTHTXP2_224_AL4	AL4	PCIE_TX5_P
MGTHTXN2_224_AL3	AL3	PCIE_TX5_N
MGTHRXP2_224_AK2	AK2	PCIE_RX5_P
MGTHRXN2_224_AK1	AK1	PCIE_RX5_N
MGTHTXP3_224_AK6	AK6	PCIE_TX4_P
MGTHTXN3_224_AK5	AK5	PCIE_TX4_N
MGTHRXP3_224_AJ4	AJ4	PCIE_RX4_P
MGTHRXN3_224_AJ3	AJ3	PCIE_RX4_N
MGTREFCLK0P_224_AF6	AF6	NC
MGTREFCLK0N_224_AF5	AF5	NC
MGTREFCLK1P_224_AD6	AD6	NC
MGTREFCLK1N_224_AD5	AD5	NC

U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REVD

BANK 225
XCKU040FFVA1156

MGTHTXP0_225_AH6	AH6	PCIE_TX3_P
MGTHTXN0_225_AH5	AH5	PCIE_TX3_N
MGTHRXP0_225_AH2	AH2	PCIE_RX3_P
MGTHRXN0_225_AH1	AH1	PCIE_RX3_N
MGTHTXP1_225_AG4	AG4	PCIE_TX2_P
MGTHTXN1_225_AG3	AG3	PCIE_TX2_N
MGTHRXP1_225_AF2	AF2	PCIE_RX2_P
MGTHRXN1_225_AF1	AF1	PCIE_RX2_N
MGTHTXP2_225_AE4	AE4	PCIE_TX1_P
MGTHTXN2_225_AE3	AE3	PCIE_TX1_N
MGTHRXP2_225_AD2	AD2	PCIE_RX1_P
MGTHRXN2_225_AD1	AD1	PCIE_RX1_N
MGTHTXP3_225_AC4	AC4	PCIE_TX0_P
MGTHTXN3_225_AC3	AC3	PCIE_TX0_N
MGTHRXP3_225_AB2	AB2	PCIE_RX0_P
MGTHRXN3_225_AB1	AB1	PCIE_RX0_N
MGTREFCLK0P_225_AB6	AB6	PCIE_CLK_QO_P
MGTREFCLK0N_225_AB5	AB5	PCIE_CLK_QO_N
MGTREFCLK1P_225_Y6	Y6	NC
MGTREFCLK1N_225_Y5	Y5	NC
MGTRREF_225_AP5	AP5	
MGTAVTTRCAL_225_AP6	AP6	

R265 100 1/10W 1% — MGTAVTT_FPGA

U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REVD

BANK 226
XCKU040FFVA1156

MGTHTXP0_226_AA4	AA4	FMC_LPC_DP0_C2M_P
MGTHTXN0_226_AA3	AA3	FMC_LPC_DP0_C2M_N
MGTHRXP0_226_Y2	Y2	FMC_LPC_DP0_M2C_P
MGTHRXN0_226_Y1	Y1	FMC_LPC_DP0_M2C_N
MGTHTXP1_226_W4	W4	SFP1_TX_P
MGTHTXN1_226_W3	W3	SFP1_TX_N
MGTHRXP1_226_V2	V2	SFP1_RX_P
MGTHRXN1_226_V1	V1	SFP1_RX_N
MGTHTXP2_226_U4	U4	SFP0_TX_P
MGTHTXN2_226_U3	U3	SFP0_TX_N
MGTHRXP2_226_T2	T2	SFP0_RX_P
MGTHRXN2_226_T1	T1	SFP0_RX_N
MGTHTXP3_226_R4	R4	SMA_MGT_TX_P
MGTHTXN3_226_R3	R3	SMA_MGT_TX_N
MGTHRXP3_226_P2	P2	SMA_MGT_RX_C_P
MGTHRXN3_226_P1	P1	SMA_MGT_RX_C_N
MGTREFCLK0P_226_V6	V6	SMA_MGT_REFCLK_C_P
MGTREFCLK0N_226_V5	V5	SMA_MGT_REFCLK_C_N
MGTREFCLK1P_226_T6	T6	FMC_LPC_GBTCLK0_M2C_C_P
MGTREFCLK1N_226_T5	T5	FMC_LPC_GBTCLK0_M2C_C_N

U1

SOC_IRONWOOD_FF1156

C18 0.1UF 25V — FMC_LPC_GBTCLK0_M2C_C_P → FMC_LPC_GBTCLK0_M2C_P
C17 0.1UF 25V — FMC_LPC_GBTCLK0_M2C_C_N → FMC_LPC_GBTCLK0_M2C_N
C655 0.1UF 25V — SMA_MGT_REFCLK_C_P → SMA_MGT_REFCLK_P
C654 0.1UF 25V — SMA_MGT_REFCLK_C_N → SMA_MGT_REFCLK_N

SOC_KU040_FFVA1156_IRON_REVD

BANK 227
XCKU040FFVA1156

MGTHTXP0_227_N4	N4	FMC_HPC_DP4_C2M_P
MGTHTXN0_227_N3	N3	FMC_HPC_DP4_C2M_N
MGTHRXP0_227_M2	M2	FMC_HPC_DP4_M2C_P
MGTHRXN0_227_M1	M1	FMC_HPC_DP4_M2C_N
MGTHTXP1_227_L4	L4	FMC_HPC_DP6_C2M_P
MGTHTXN1_227_L3	L3	FMC_HPC_DP6_C2M_N
MGTHRXP1_227_K2	K2	FMC_HPC_DP6_M2C_P
MGTHRXN1_227_K1	K1	FMC_HPC_DP6_M2C_N
MGTHTXP2_227_J4	J4	FMC_HPC_DP5_C2M_P
MGTHTXN2_227_J3	J3	FMC_HPC_DP5_C2M_N
MGTHRXP2_227_H2	H2	FMC_HPC_DP5_M2C_P
MGTHRXN2_227_H1	H1	FMC_HPC_DP5_M2C_N
MGTHTXP3_227_G4	G4	FMC_HPC_DP7_C2M_P
MGTHTXN3_227_G3	G3	FMC_HPC_DP7_C2M_N
MGTHRXP3_227_F2	F2	FMC_HPC_DP7_M2C_P
MGTHRXN3_227_F1	F1	FMC_HPC_DP7_M2C_N
MGTREFCLK0P_227_P6	P6	MGT_SI570_CLOCK_C_P
MGTREFCLK0N_227_P5	P5	MGT_SI570_CLOCK_C_N
MGTREFCLK1P_227_M6	M6	SI5328_OUT_C_P
MGTREFCLK1N_227_M5	M5	SI5328_OUT_C_N

U1

SOC_IRONWOOD_FF1156

C9 0.1UF 25V — MGT_SI570_CLOCK_C_P → MGT_SI570_CLOCK_P
C10 0.1UF 25V — MGT_SI570_CLOCK_C_N → MGT_SI570_CLOCK_N

SOC_KU040_FFVA1156_IRON_REVD

BANK 228
XCKU040FFVA1156

MGTHTXP0_228_F6	F6	FMC_HPC_DP0_C2M_P
MGTHTXN0_228_F5	F5	FMC_HPC_DP0_C2M_N
MGTHRXP0_228_E4	E4	FMC_HPC_DP0_M2C_P
MGTHRXN0_228_E3	E3	FMC_HPC_DP0_M2C_N
MGTHTXP1_228_D6	D6	FMC_HPC_DP1_C2M_P
MGTHTXN1_228_D5	D5	FMC_HPC_DP1_C2M_N
MGTHRXP1_228_D2	D2	FMC_HPC_DP1_M2C_P
MGTHRXN1_228_D1	D1	FMC_HPC_DP1_M2C_N
MGTHTXP2_228_C4	C4	FMC_HPC_DP2_C2M_P
MGTHTXN2_228_C3	C3	FMC_HPC_DP2_C2M_N
MGTHRXP2_228_B2	B2	FMC_HPC_DP2_M2C_P
MGTHRXN2_228_B1	B1	FMC_HPC_DP2_M2C_N
MGTHTXP3_228_B6	B6	FMC_HPC_DP3_C2M_P
MGTHTXN3_228_B5	B5	FMC_HPC_DP3_C2M_N
MGTHRXP3_228_A4	A4	FMC_HPC_DP3_M2C_P
MGTHRXN3_228_A3	A3	FMC_HPC_DP3_M2C_N
MGTREFCLK0P_228_K6	K6	FMC_HPC_GBTCLK0_M2C_P
MGTREFCLK0N_228_K5	K5	FMC_HPC_GBTCLK0_M2C_N
MGTREFCLK1P_228_H6	H6	FMC_HPC_GBTCLK1_M2C_P
MGTREFCLK1N_228_H5	H5	FMC_HPC_GBTCLK1_M2C_N

U1

SOC_IRONWOOD_FF1156

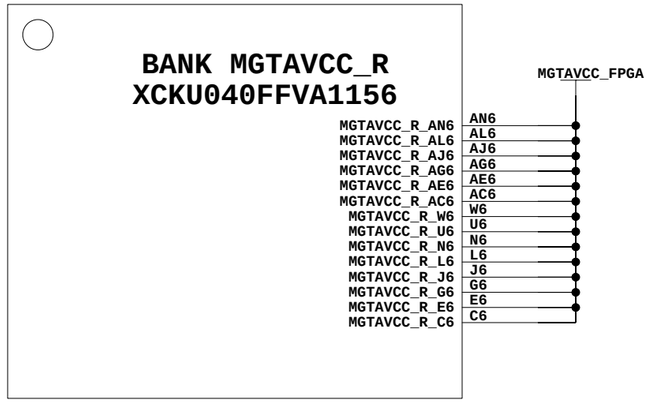
C13 0.1UF 25V — FMC_HPC_GBTCLK0_M2C_C_P → FMC_HPC_GBTCLK0_M2C_P
C14 0.1UF 25V — FMC_HPC_GBTCLK0_M2C_C_N → FMC_HPC_GBTCLK0_M2C_N
C15 0.1UF 25V — FMC_HPC_GBTCLK1_M2C_C_P → FMC_HPC_GBTCLK1_M2C_P
C16 0.1UF 25V — FMC_HPC_GBTCLK1_M2C_C_N → FMC_HPC_GBTCLK1_M2C_N

FPGA Banks 224 225 226 227 228

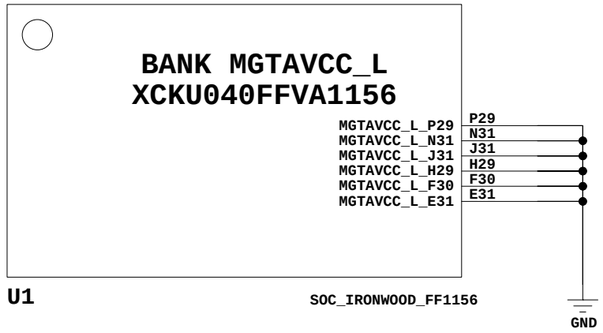
XILINX

TITLE: FPGA Banks 224 225 226 227 228 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 10 OF 66	DRAWN BY: BF

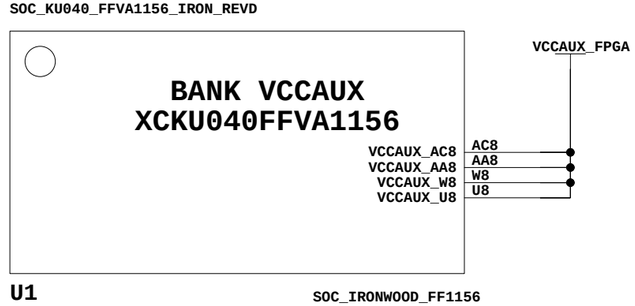
SOC_KU040_FFVA1156_IRON_REVD



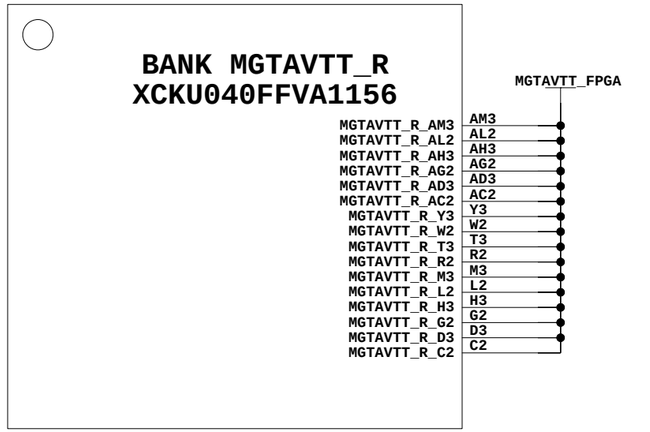
SOC_KU040_FFVA1156_IRON_REVD



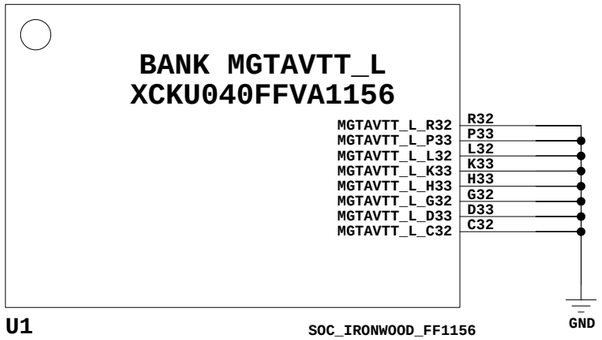
SOC_KU040_FFVA1156_IRON_REVD



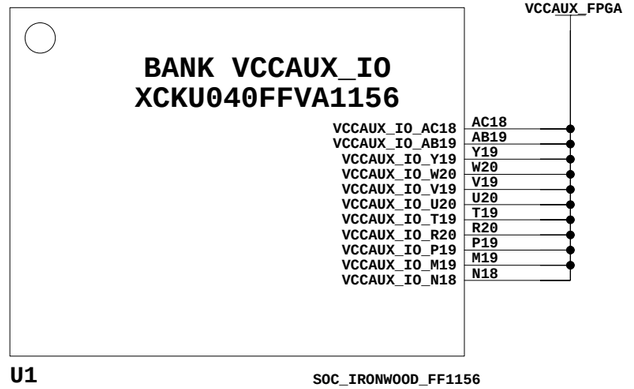
SOC_KU040_FFVA1156_IRON_REVD



SOC_KU040_FFVA1156_IRON_REVD



SOC_KU040_FFVA1156_IRON_REVD



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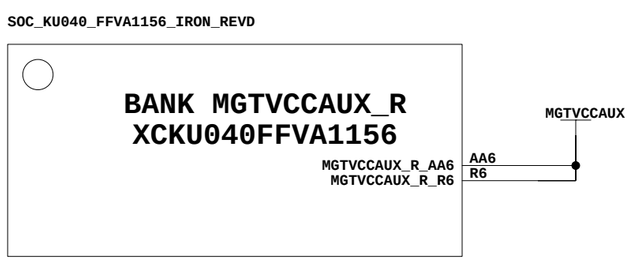
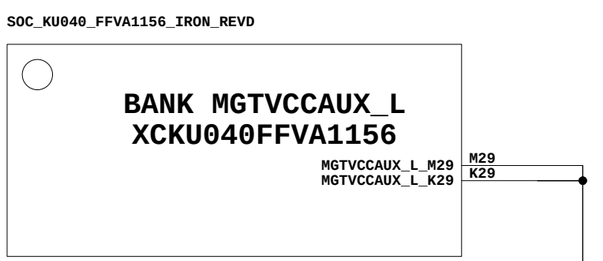
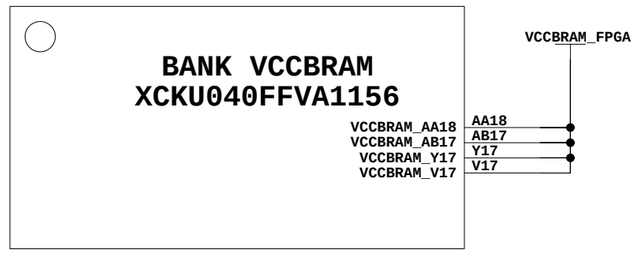


SOC_KU040_FFVA1156_IRON_REVD



SOC_KU040_FFVA1156_IRON_REVD

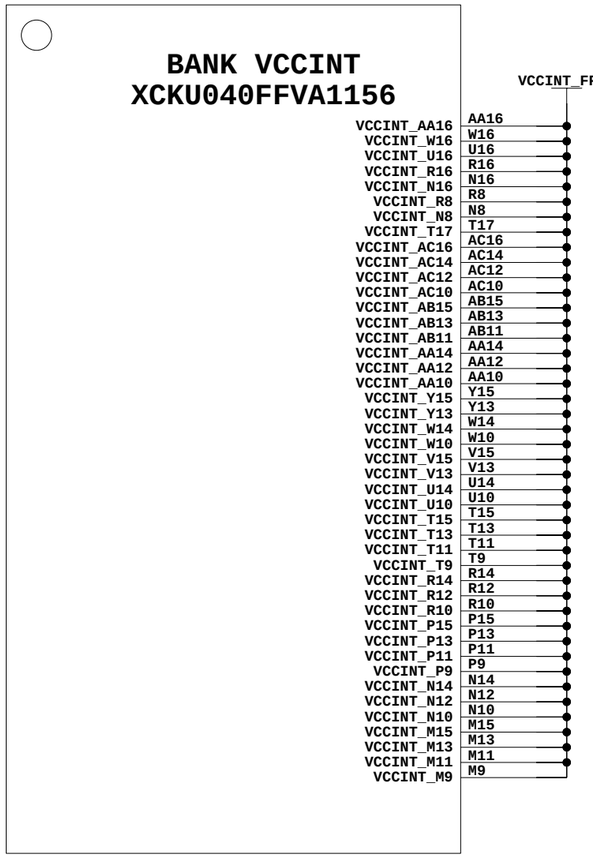


FPGA Power 1

XILINX

TITLE: FPGA Power 1 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 11 OF 66	DRAWN BY: BF

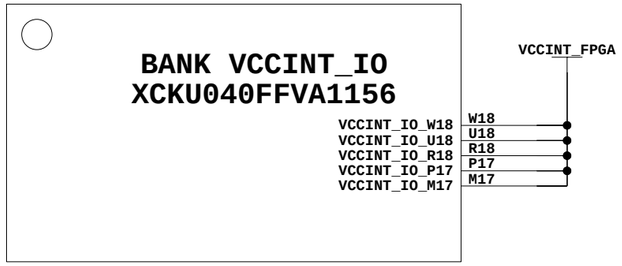
SOC_KU040_FFVA1156_IRON_REVD



U1

SOC_IRONWOOD_FF1156

SOC_KU040_FFVA1156_IRON_REVD



U1

SOC_IRONWOOD_FF1156

FPGA Power 2

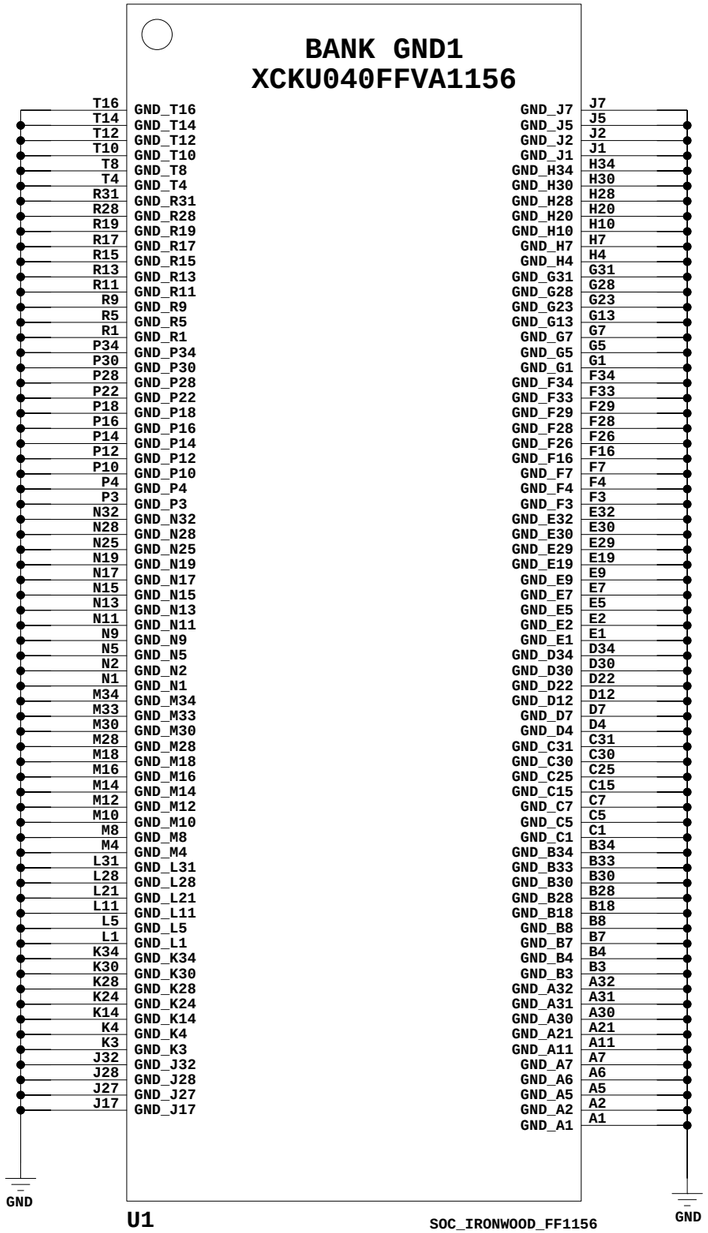
XILINX

TITLE: FPGA Power 2
SCHEM, ROHS COMPLIANT
HW-U1-KCU105_REV1_1

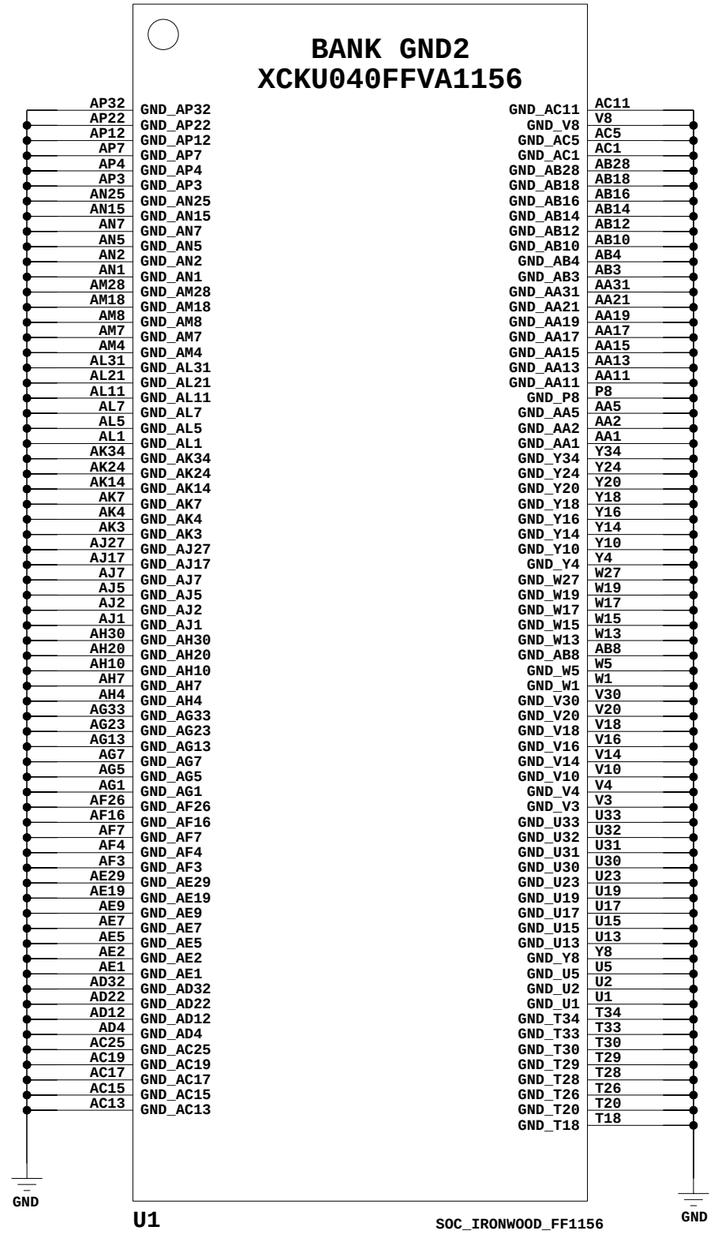
ASSY P/N: 0431811
PCB P/N: 1280723
SCH P/N: 0381556
TEST P/N: TSS0165

DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 12 OF 66	DRAWN BY: BF

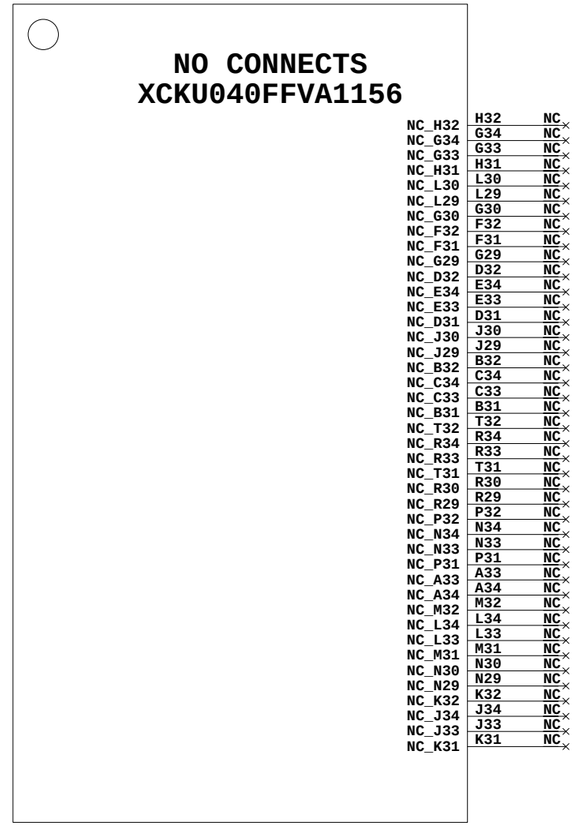
SOC_KU040_FFVA1156_IRON_REVD



SOC_KU040_FFVA1156_IRON_REVD



SOC_KU040_FFVA1156_IRON_REVD

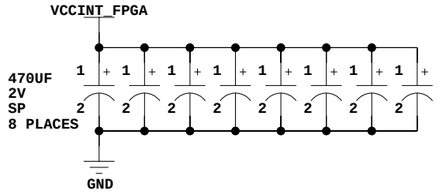


FPGA GND NC

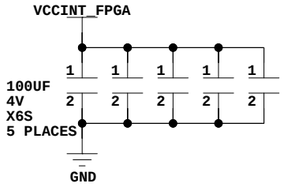
XILINX

TITLE: FPGA GND NC SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 13 OF 66	DRAWN BY: BF

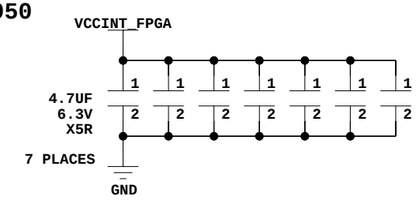
C461 C915
C460 C916
C462 C917
C911 C918



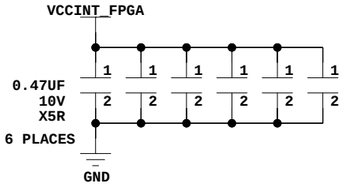
C906 C914
C907
C908
C909



C657C948
C658C949
C659C950
C947

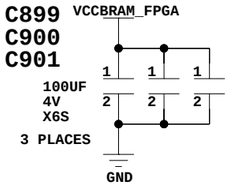


C660 C661 C662 C663 C664 C665

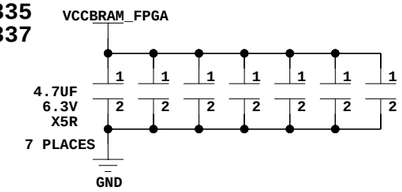


VCCINT

C899
C900
C901

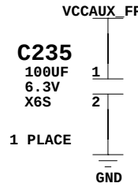


C330 C334 C338
C331 C335
C336 C337

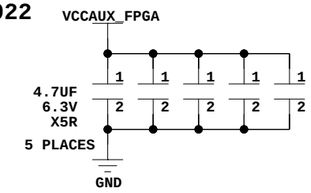


VCCBRAM

C235



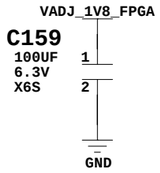
C919 C921
C920 C922
C923



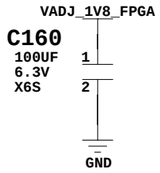
VCCAUX / VCCAUX_IO

VCCO_47 / VCCO_48 / VCCO_66 / VCCO_67 / VCCO_68

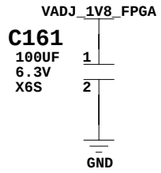
C159



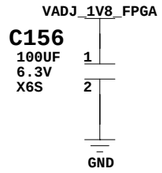
C160



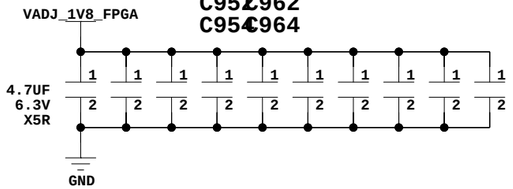
C161



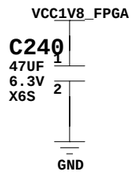
C156



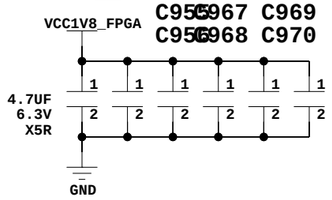
C951 C961 C965
C953 C963 C966
C952 C962
C954 C964



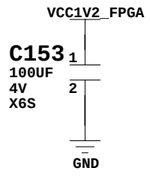
VCCO_0 / VCCO_64 / VCCO_65



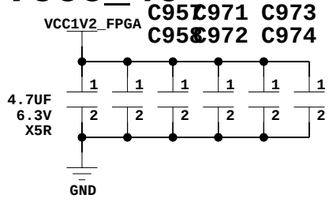
C955 C967 C969
C956 C968 C970



VCCO_44 / VCCO_45 / VCCO_46



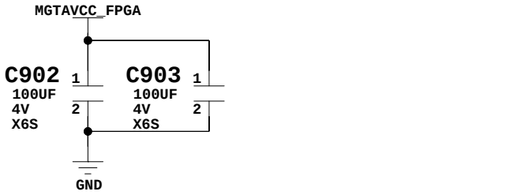
C957 C971 C973
C958 C972 C974

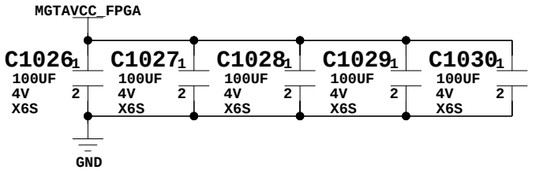


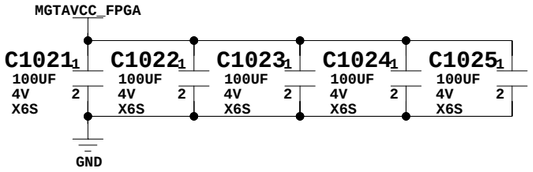
FPGA Decoupling 1

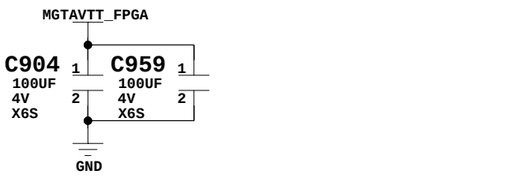
XILINX

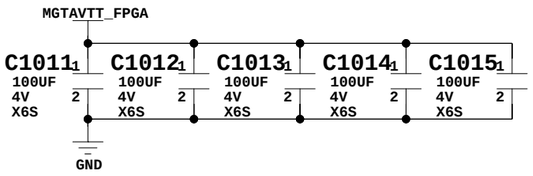
TITLE: FPGA Decoupling 1 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 14 OF 66	DRAWN BY: BF

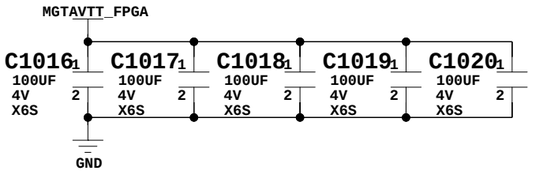


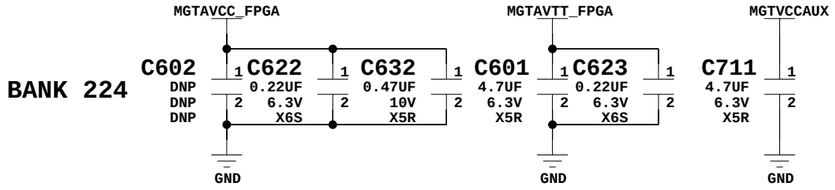


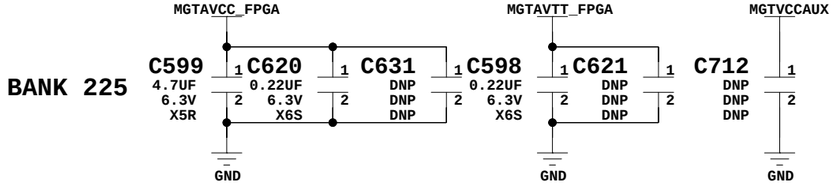


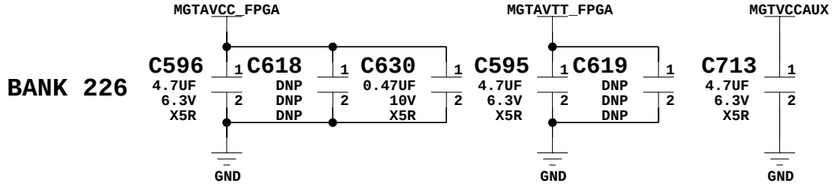


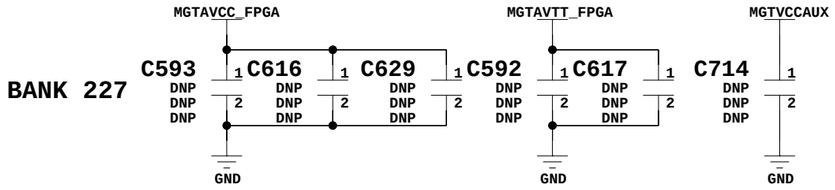


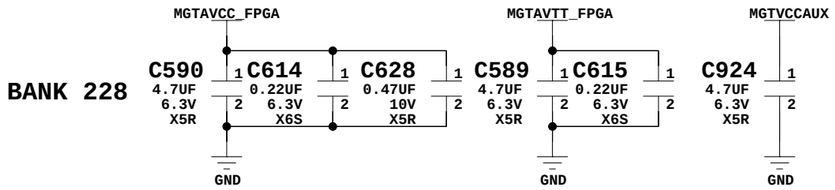








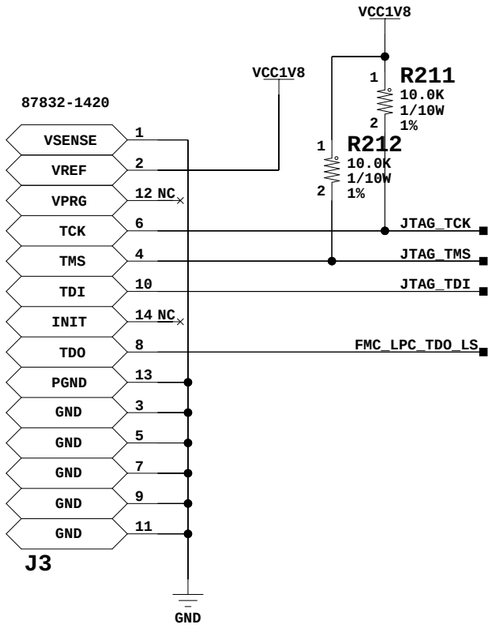


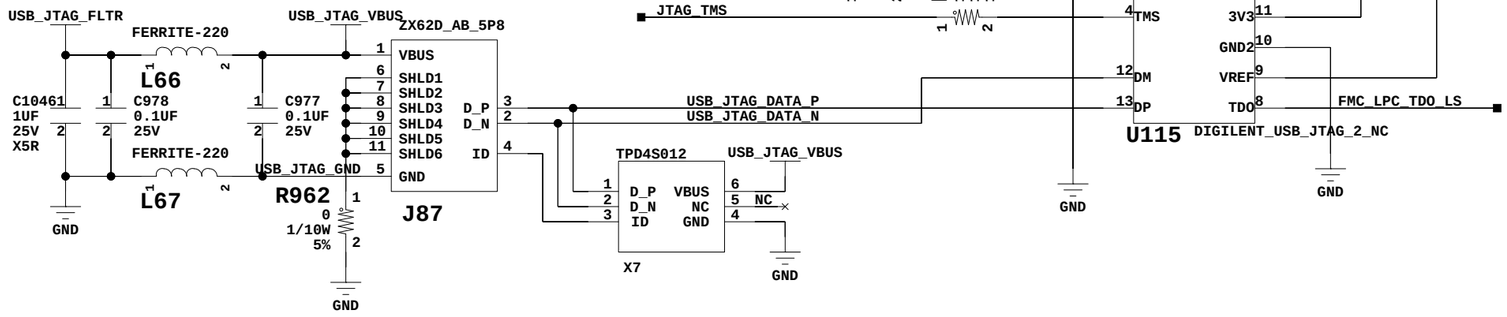


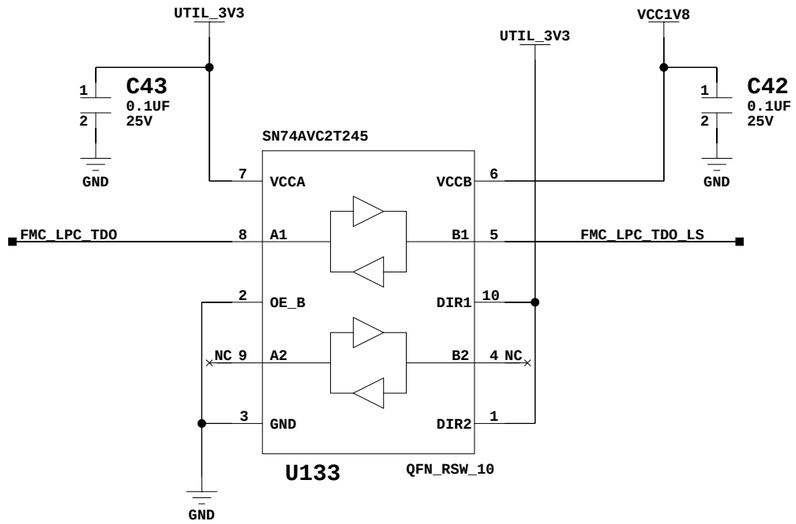
FPGA Decoupling 2

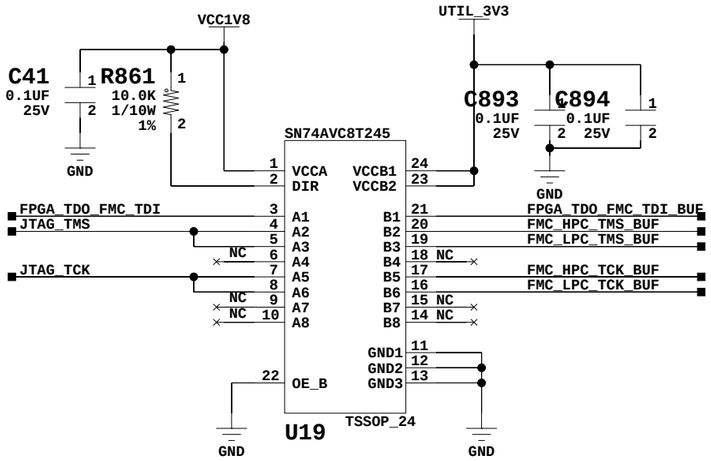
XILINX

TITLE: FPGA Decoupling 2 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 15 OF 66	DRAWN BY: BF







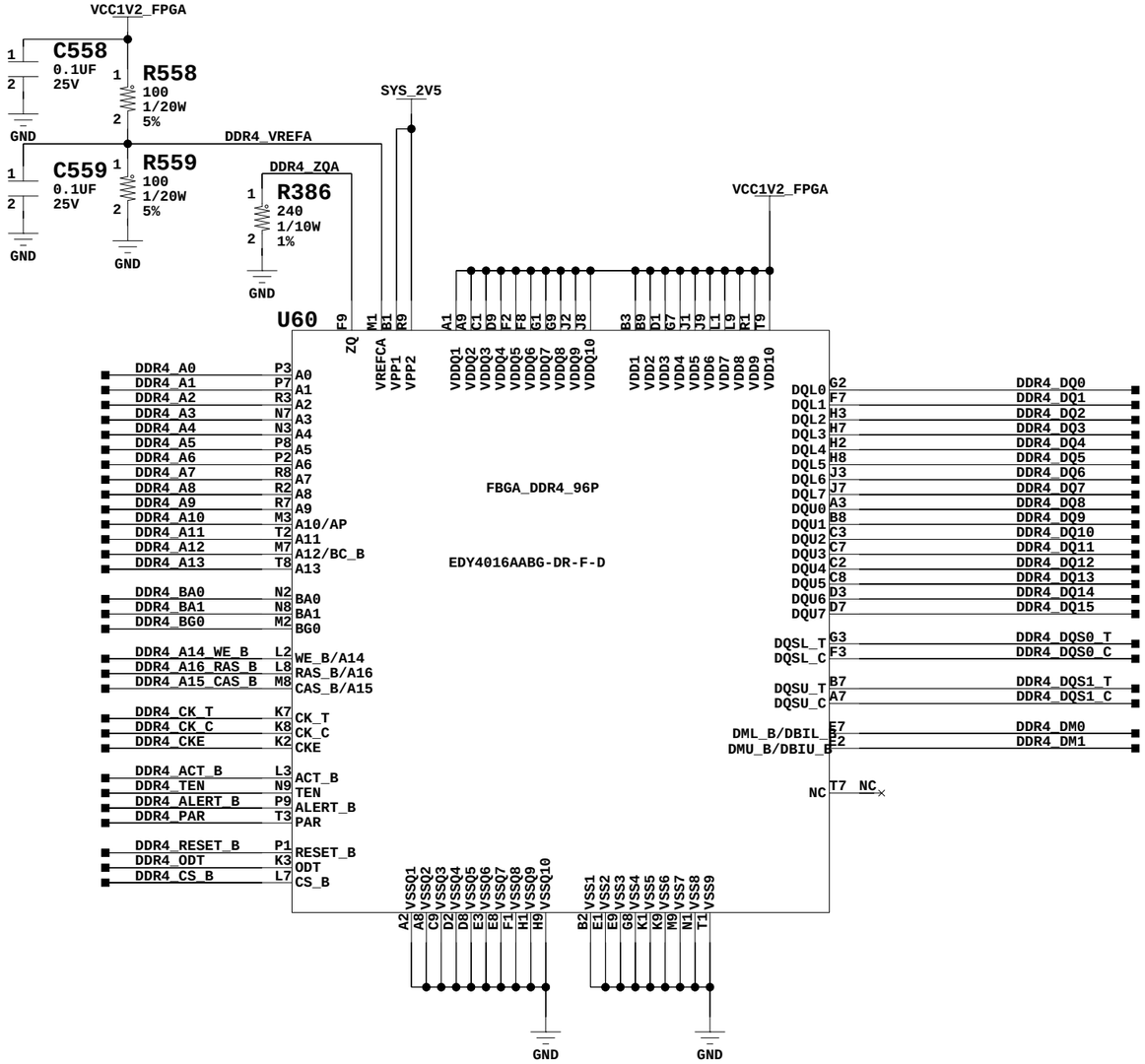


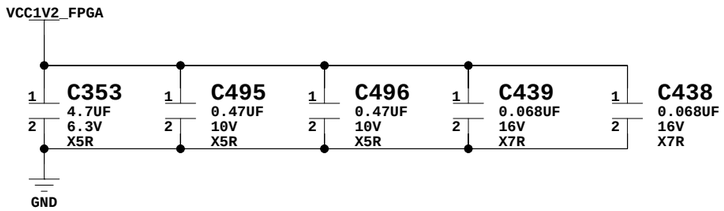
JTAG Buffer - USB Module - JTAG Header

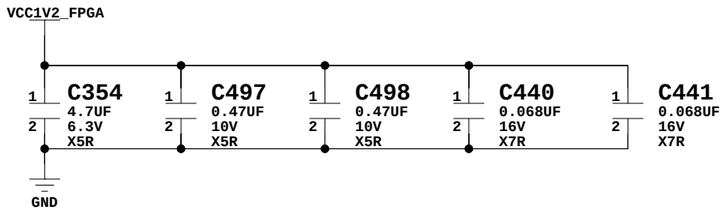
XILINX

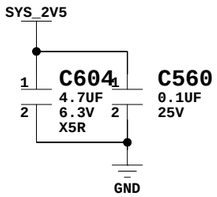
TITLE: JTAG Buffer - USB Module - JTAG Header SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 16 OF 66	DRAWN BY: BF

Layout: Place 0.1UF cap in via matrix at M1





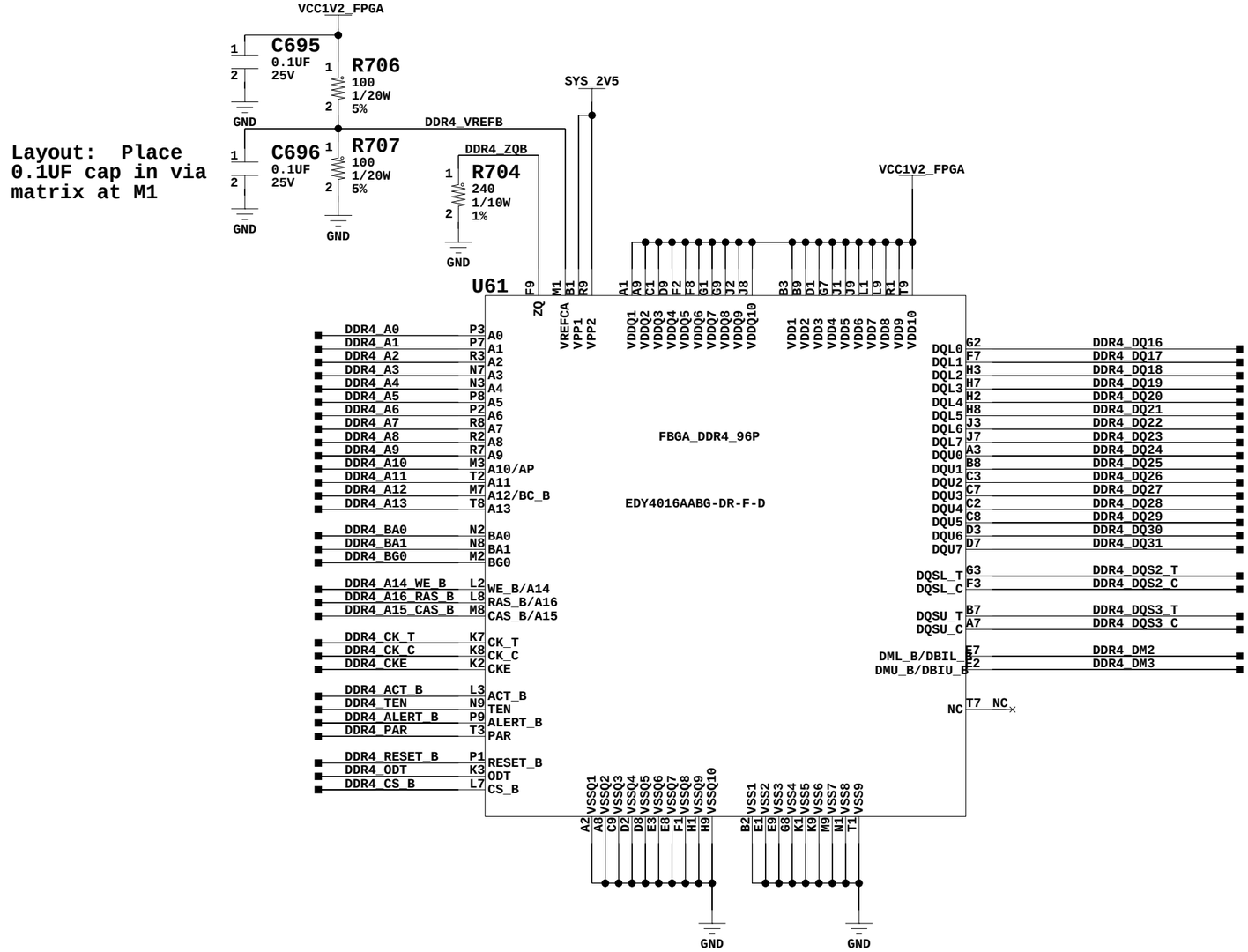


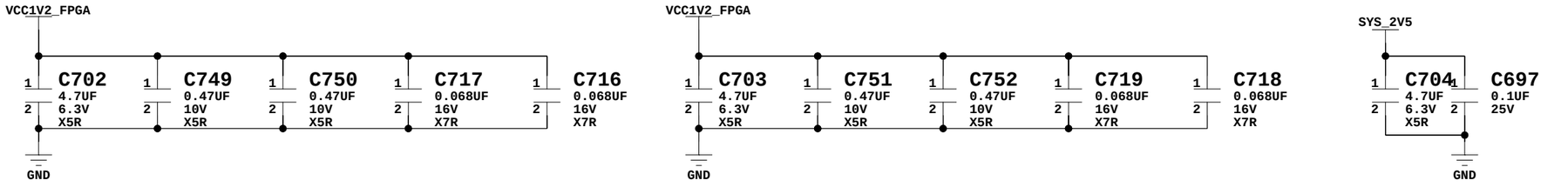


DDR4 Data [15-0]

TITLE: DDR4 Data [15-0] SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 17 OF 66	DRAWN BY: BF

Layout: Place 0.1UF cap in via matrix at M1



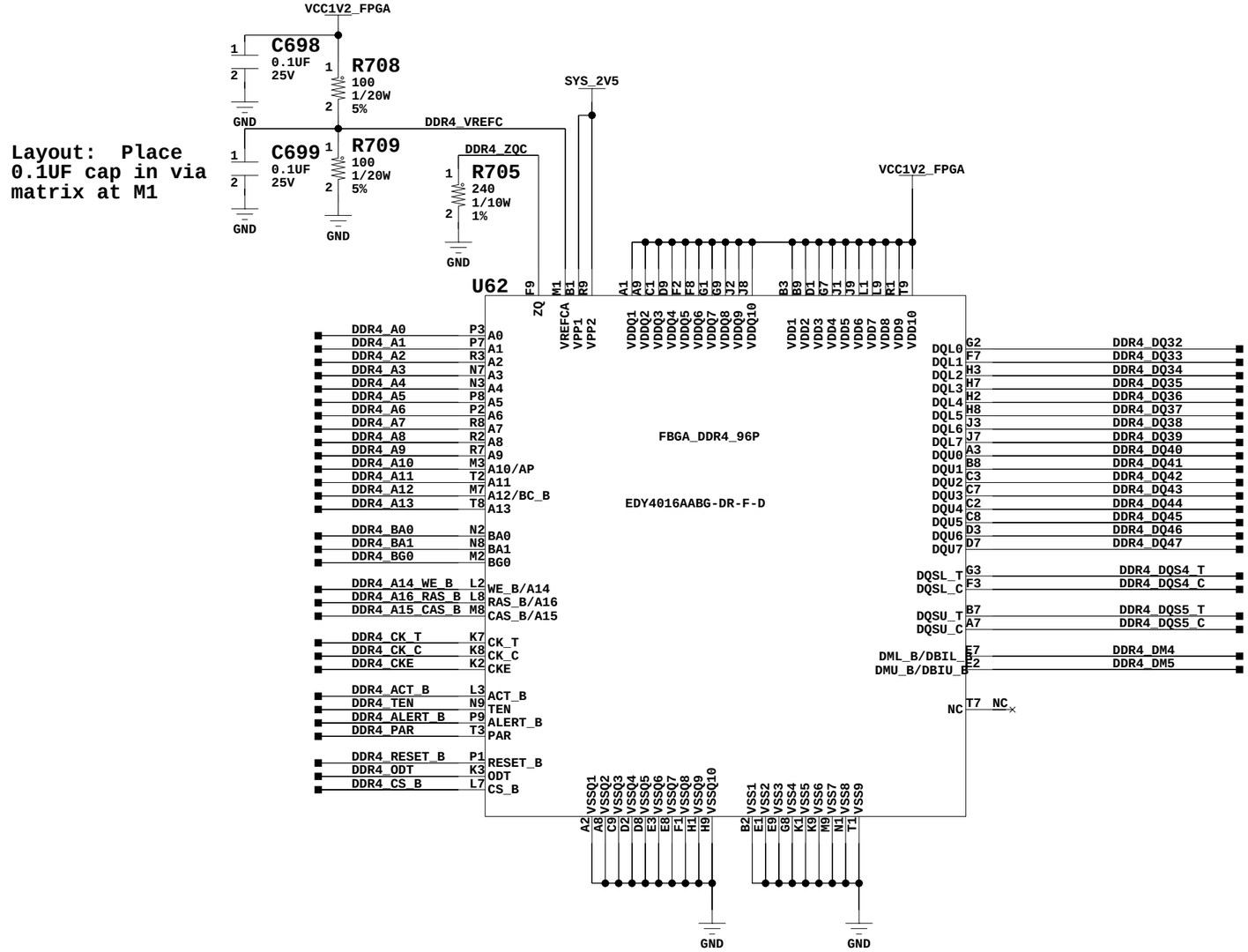


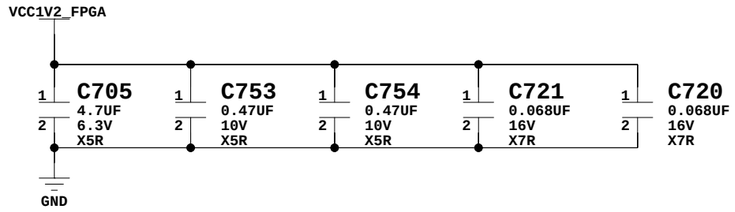
DDR4 Data [31-16]

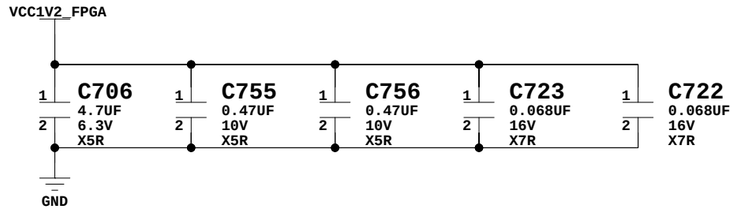
XILINX

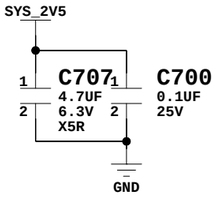
TITLE: DDR4 Data [31-16] SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 18 OF 66	DRAWN BY: BF

Layout: Place 0.1UF cap in via matrix at M1









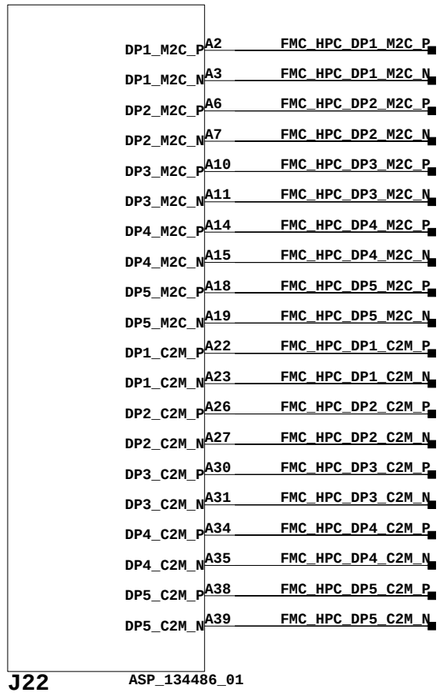
DDR4 Data [47-31]

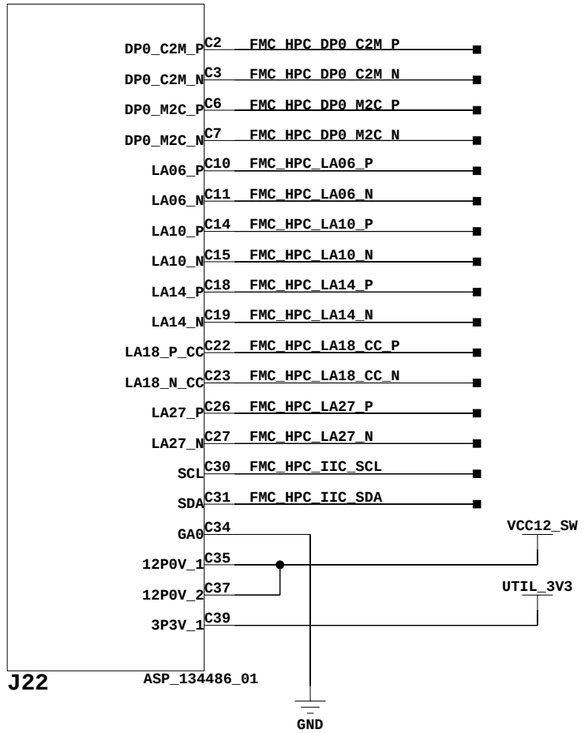
TITLE: DDR4 Data [47-31] SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 19 OF 66	DRAWN BY: BF

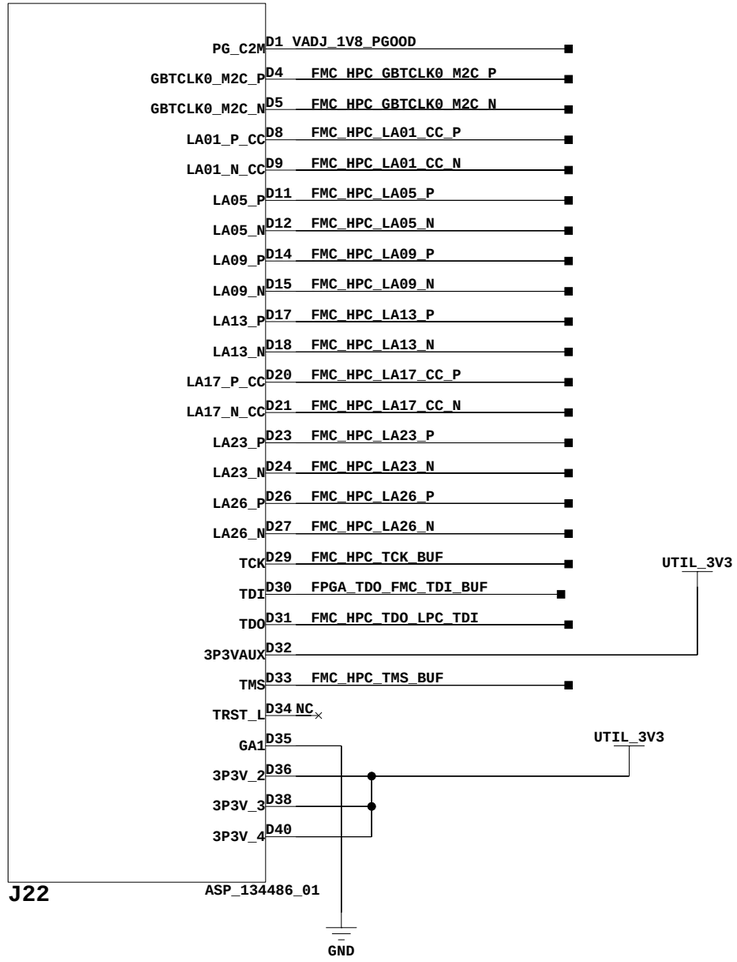
Layout: Place 0.1UF cap in via matrix at M1

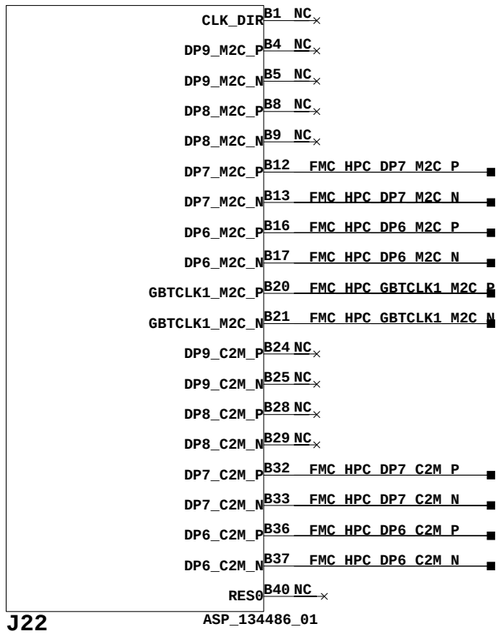
DDR4 Data [63-48]

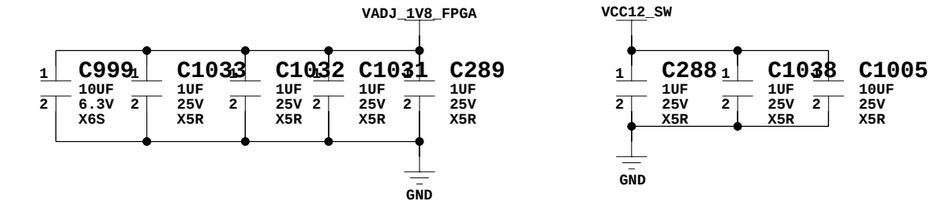
TITLE: DDR4 Data [63-48] SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 20 OF 66	DRAWN BY: BF

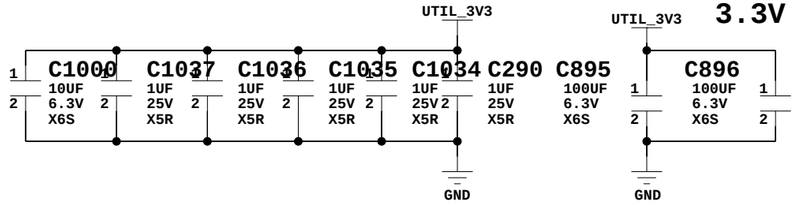




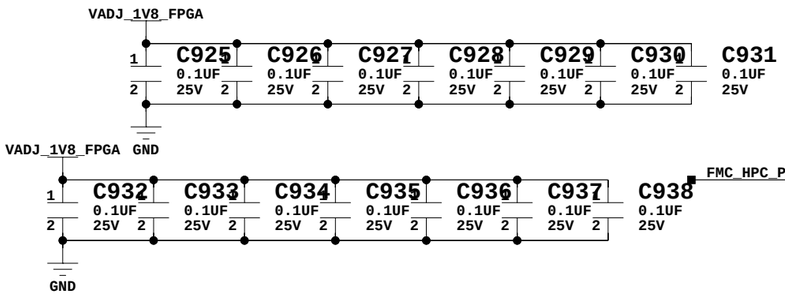


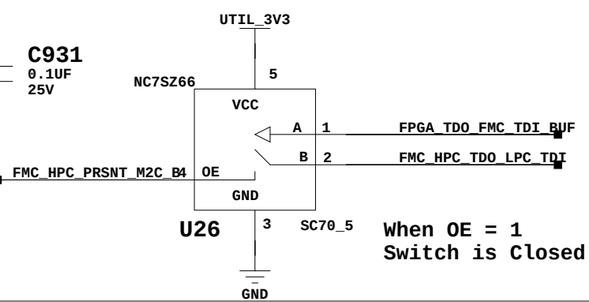






3.3V Bulk



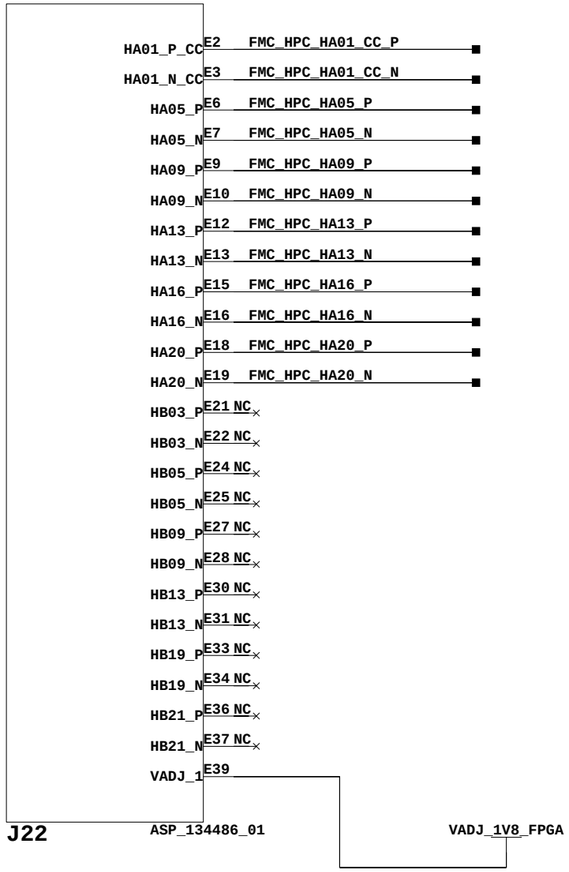


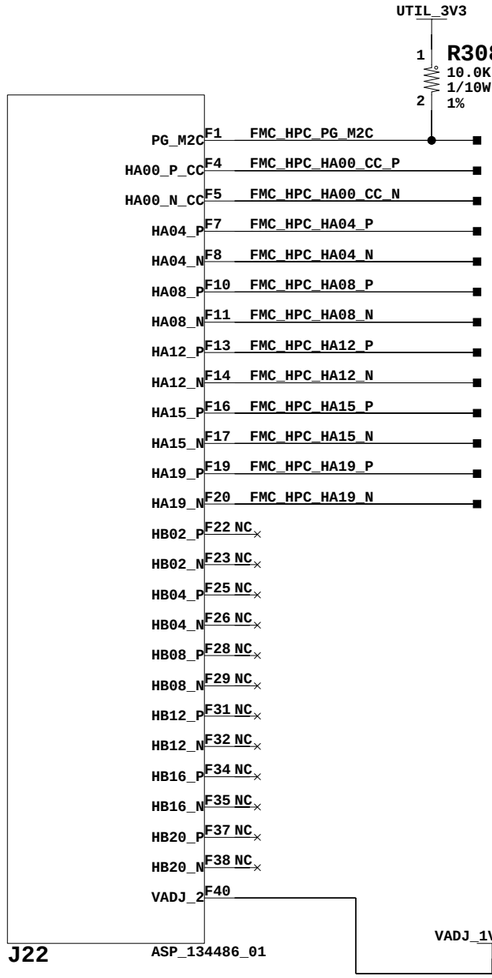
When OE = 1
Switch is Closed

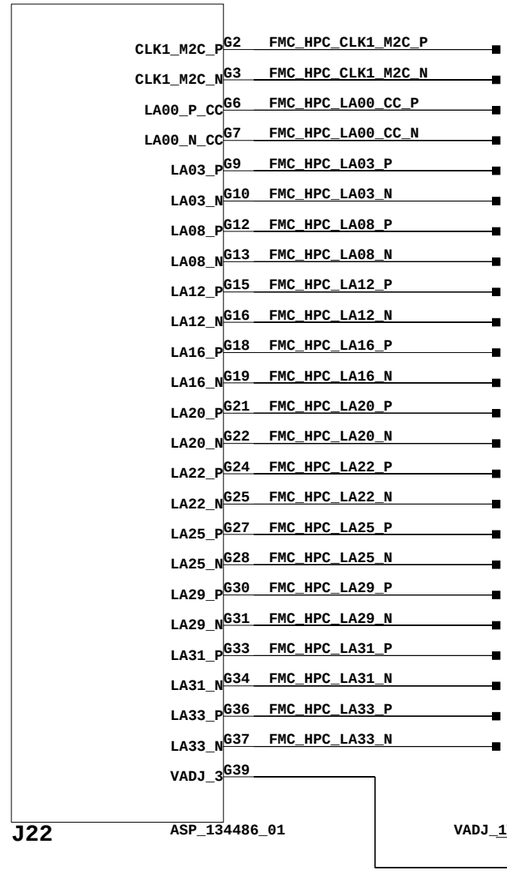
ANSI/VITA 57.1 - Revised 2010
FMC HPC Header Rows A B C D

XILINX

TITLE: FMC HPC Header Rows A B C D SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 21 OF 66	DRAWN BY: BF



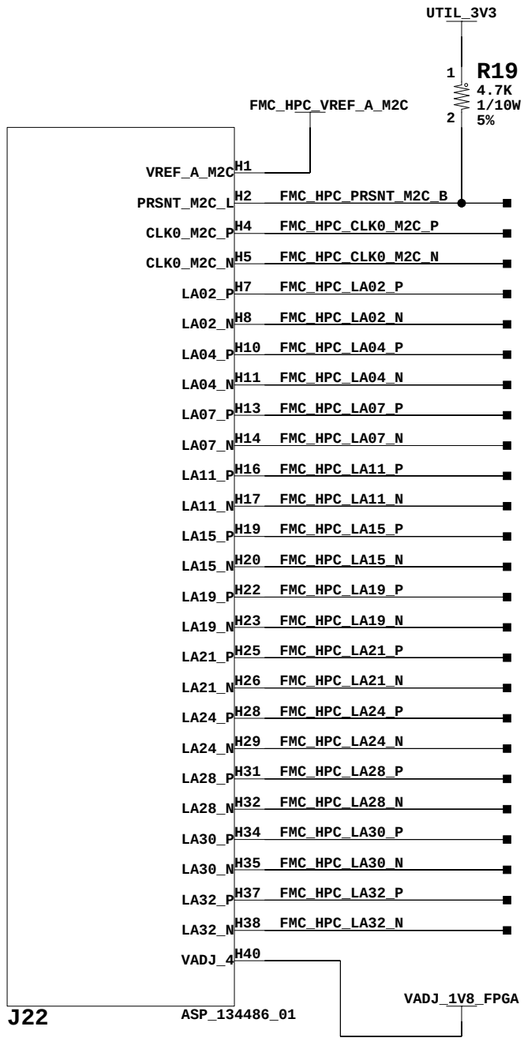


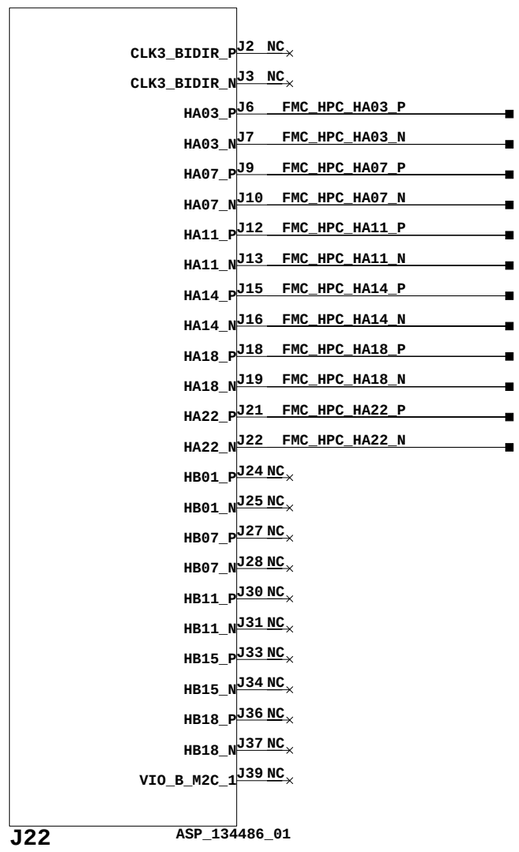


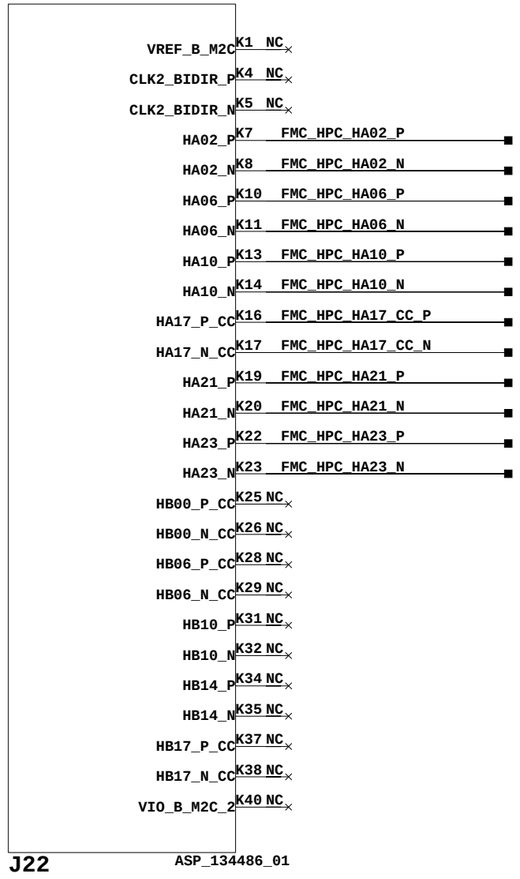
ANSI/VITA 57.1 - Revised 2010
FMC HPC Header Rows E F G

XILINX

TITLE: FMC HPC Header Rows E F G SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 22 OF 66	DRAWN BY: BF



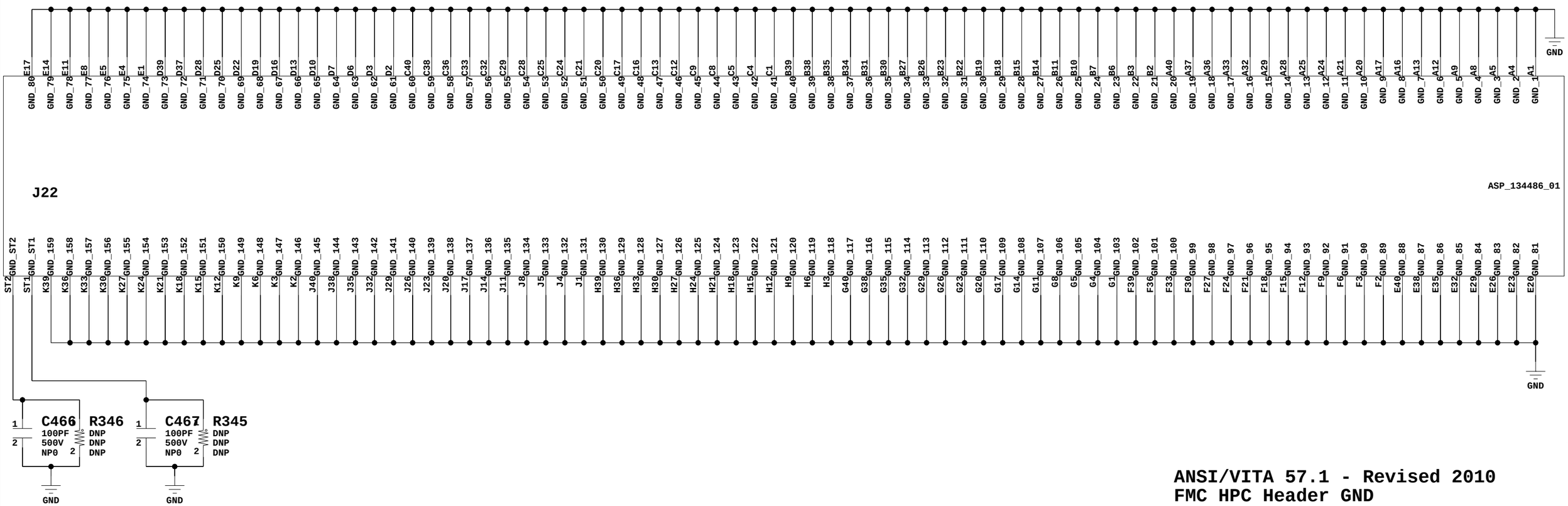




ANSI/VITA 57.1 - Revised 2010
FMC HPC Header Rows H J K

XILINX

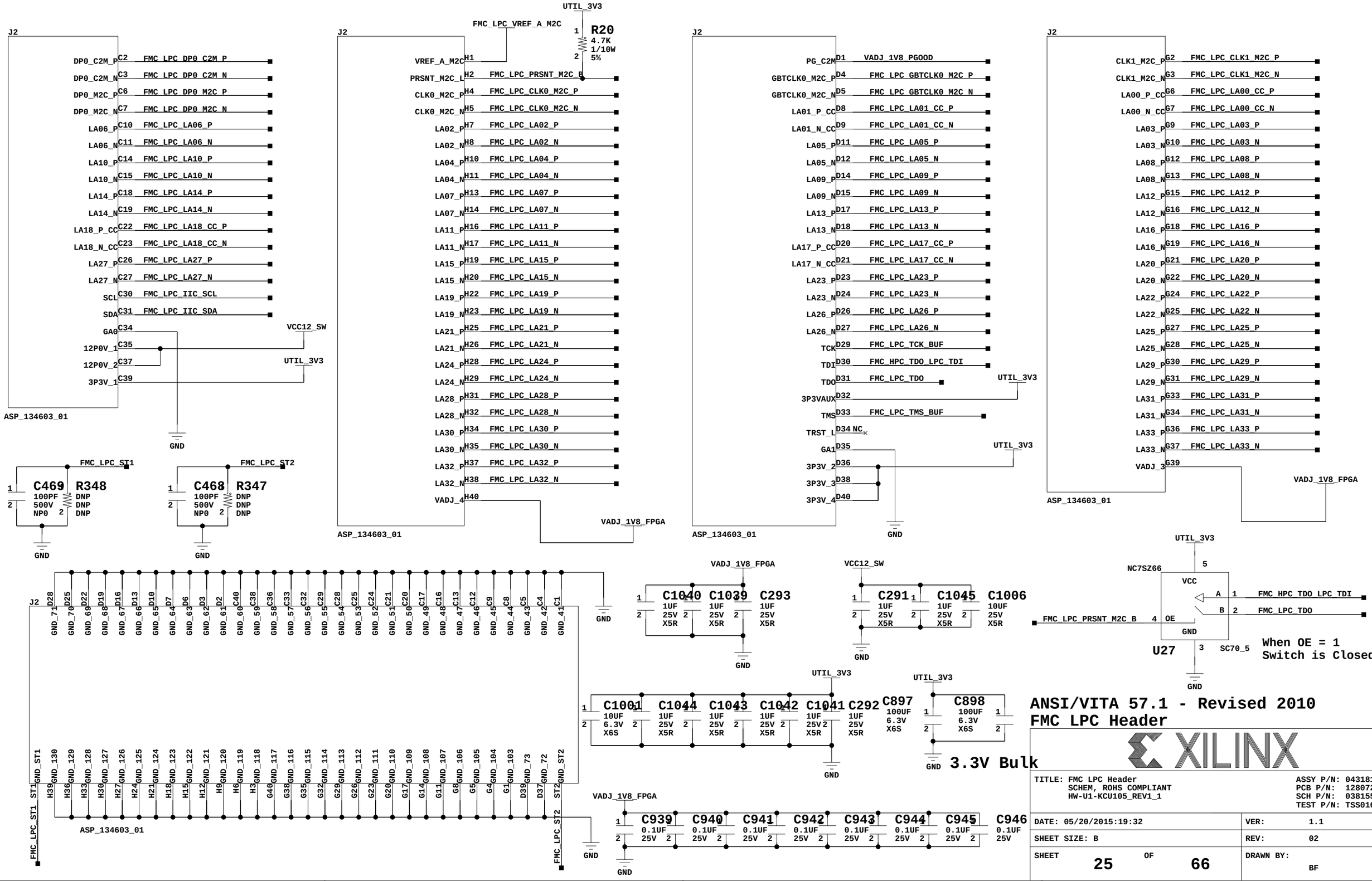
TITLE: FMC HPC Header Rows H J K SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 23 OF 66	DRAWN BY: BF

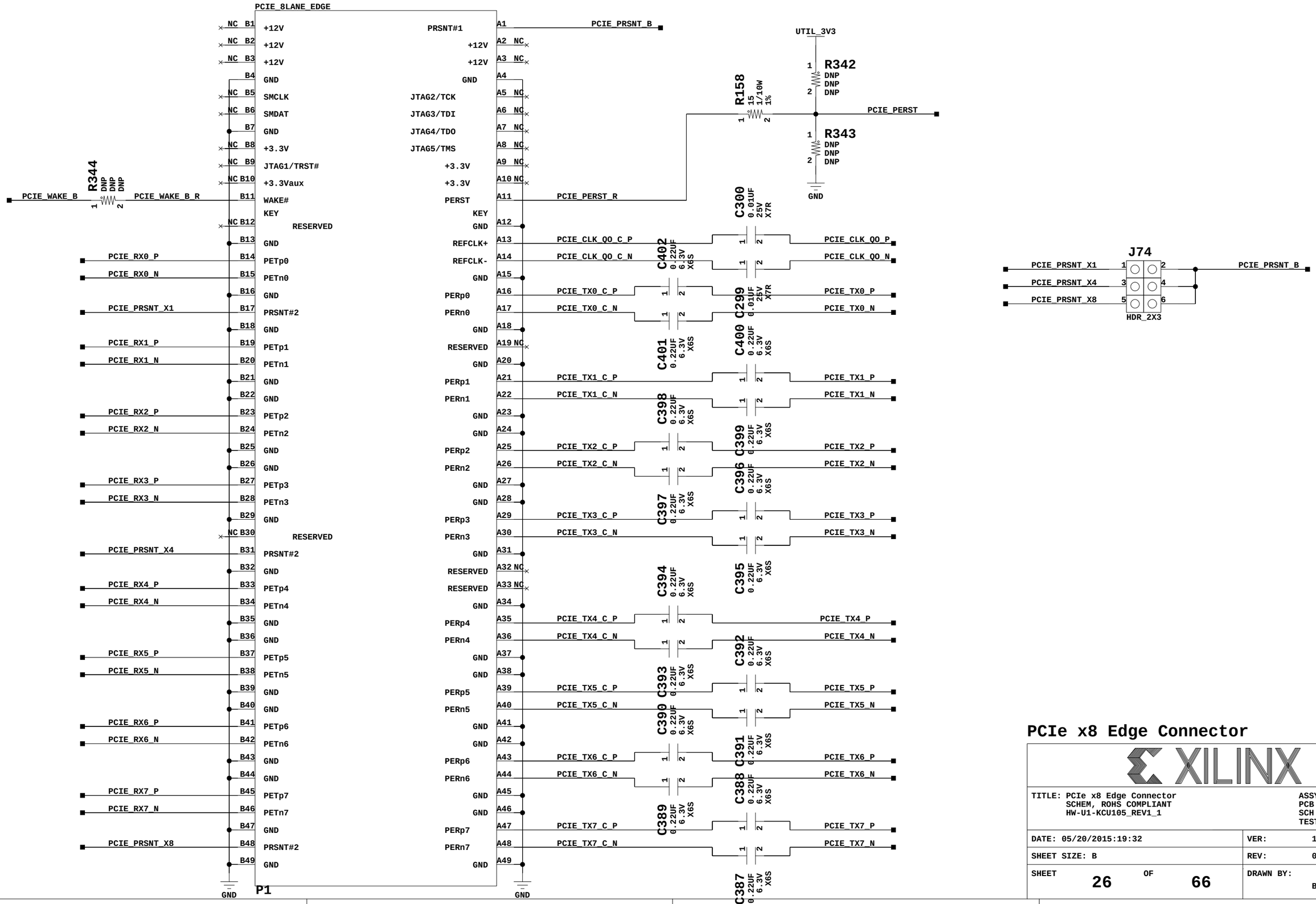


ANSI/VITA 57.1 - Revised 2010
FMC HPC Header GND

XILINX

TITLE: FMC HPC Header GND SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 24 OF 66	DRAWN BY: BF


J2
DP0_C2M_P C2 FMC_LPC_DP0_C2M_P
DP0_C2M_M C3 FMC_LPC_DP0_C2M_N
DP0_M2C_P C6 FMC_LPC_DP0_M2C_P
DP0_M2C_N C7 FMC_LPC_DP0_M2C_N
LA06_P C10 FMC_LPC_LA06_P
LA06_N C11 FMC_LPC_LA06_N
LA10_P C14 FMC_LPC_LA10_P
LA10_N C15 FMC_LPC_LA10_N
LA14_P C18 FMC_LPC_LA14_P
LA14_N C19 FMC_LPC_LA14_N
LA18_P_CC C22 FMC_LPC_LA18_CC_P
LA18_N_CC C23 FMC_LPC_LA18_CC_N
LA27_P C26 FMC_LPC_LA27_P
LA27_N C27 FMC_LPC_LA27_N
SCL C30 FMC_LPC_IIC_SCL
SDA C31 FMC_LPC_IIC_SDA
GA0 C34
12P0V_1 C35
12P0V_2 C37
3P3V_1 C39
VCC12_SW
UTIL_3V3
GND
ASP_134603_01
FMC_LPC_ST1
C469 100PF 500V NP0 R348 DNP DNP DNP
FMC_LPC_ST2
C468 100PF 500V NP0 R347 DNP DNP DNP
UTIL_3V3
R20 4.7K 1/10W 5%
FMC_LPC_VREF_A_M2C
VREF_A_M2C H1
PRSNT_M2C_L H2 FMC_LPC_PRSNT_M2C_B
CLK0_M2C_P H4 FMC_LPC_CLK0_M2C_P
CLK0_M2C_N H5 FMC_LPC_CLK0_M2C_N
LA02_P H7 FMC_LPC_LA02_P
LA02_N H8 FMC_LPC_LA02_N
LA04_P H10 FMC_LPC_LA04_P
LA04_N H11 FMC_LPC_LA04_N
LA07_P H13 FMC_LPC_LA07_P
LA07_N H14 FMC_LPC_LA07_N
LA11_P H16 FMC_LPC_LA11_P
LA11_N H17 FMC_LPC_LA11_N
LA15_P H19 FMC_LPC_LA15_P
LA15_N H20 FMC_LPC_LA15_N
LA19_P H22 FMC_LPC_LA19_P
LA19_N H23 FMC_LPC_LA19_N
LA21_P H25 FMC_LPC_LA21_P
LA21_N H26 FMC_LPC_LA21_N
LA24_P H28 FMC_LPC_LA24_P
LA24_N H29 FMC_LPC_LA24_N
LA28_P H31 FMC_LPC_LA28_P
LA28_N H32 FMC_LPC_LA28_N
LA30_P H34 FMC_LPC_LA30_P
LA30_N H35 FMC_LPC_LA30_N
LA32_P H37 FMC_LPC_LA32_P
LA32_N H38 FMC_LPC_LA32_N
VADJ_4 H40
VADJ_1V8_FPGA
PG_C2M D1 VADJ_1V8_PGOOD
GBTCLK0_M2C_P D4 FMC_LPC_GBTCLK0_M2C_P
GBTCLK0_M2C_N D5 FMC_LPC_GBTCLK0_M2C_N
LA01_P_CC D8 FMC_LPC_LA01_CC_P
LA01_N_CC D9 FMC_LPC_LA01_CC_N
LA05_P D11 FMC_LPC_LA05_P
LA05_N D12 FMC_LPC_LA05_N
LA09_P D14 FMC_LPC_LA09_P
LA09_N D15 FMC_LPC_LA09_N
LA13_P D17 FMC_LPC_LA13_P
LA13_N D18 FMC_LPC_LA13_N
LA17_P_CC D20 FMC_LPC_LA17_CC_P
LA17_N_CC D21 FMC_LPC_LA17_CC_N
LA23_P D23 FMC_LPC_LA23_P
LA23_N D24 FMC_LPC_LA23_N
LA26_P D26 FMC_LPC_LA26_P
LA26_N D27 FMC_LPC_LA26_N
TCK D29 FMC_LPC_TCK_BUF
TDI D30 FMC_HPC_TDO_LPC_TDI
TDO D31 FMC_LPC_TDO
3P3VAUX D32
TMS D33 FMC_LPC_TMS_BUF
TRST_L D34 NC
GA1 D35
3P3V_2 D36
3P3V_3 D38
3P3V_4 D40
CLK1_M2C_P G2 FMC_LPC_CLK1_M2C_P
CLK1_M2C_N G3 FMC_LPC_CLK1_M2C_N
LA00_P_CC G6 FMC_LPC_LA00_CC_P
LA00_N_CC G7 FMC_LPC_LA00_CC_N
LA03_P G9 FMC_LPC_LA03_P
LA03_N G10 FMC_LPC_LA03_N
LA08_P G12 FMC_LPC_LA08_P
LA08_N G13 FMC_LPC_LA08_N
LA12_P G15 FMC_LPC_LA12_P
LA12_N G16 FMC_LPC_LA12_N
LA16_P G18 FMC_LPC_LA16_P
LA16_N G19 FMC_LPC_LA16_N
LA20_P G21 FMC_LPC_LA20_P
LA20_N G22 FMC_LPC_LA20_N
LA22_P G24 FMC_LPC_LA22_P
LA22_N G25 FMC_LPC_LA22_N
LA25_P G27 FMC_LPC_LA25_P
LA25_N G28 FMC_LPC_LA25_N
LA29_P G30 FMC_LPC_LA29_P
LA29_N G31 FMC_LPC_LA29_N
LA31_P G33 FMC_LPC_LA31_P
LA31_N G34 FMC_LPC_LA31_N
LA33_P G36 FMC_LPC_LA33_P
LA33_N G37 FMC_LPC_LA33_N
VADJ_3 G39
VADJ_1V8_FPGA
J2 D28 D25 D22 D19 D16 D13 D10 D7 D6 D3 D2 C40 C38 C36 C33 C32 C29 C28 C25 C24 C21 C20 C17 C16 C13 C12 C9 C8 C5 C4 C1
GND_71 GND_70 GND_69 GND_68 GND_67 GND_66 GND_65 GND_64 GND_63 GND_62 GND_61 GND_60 GND_59 GND_58 GND_57 GND_56 GND_55 GND_54 GND_53 GND_52 GND_51 GND_50 GND_49 GND_48 GND_47 GND_46 GND_45 GND_44 GND_43 GND_42 GND_41
GND
FMC_LPC_ST1 GND_ST1 GND_130 GND_129 GND_128 GND_127 GND_126 GND_125 GND_124 GND_123 GND_122 GND_121 GND_120 GND_119 GND_118 GND_117 GND_116 GND_115 GND_114 GND_113 GND_112 GND_111 GND_110 GND_109 GND_108 GND_107 GND_106 GND_105 GND_104 GND_103 GND_73 GND_72 GND_ST2 FMC_LPC_ST2
H39 H36 H33 H30 H27 H24 H21 H18 H15 H12 H9 H6 H3 G40 G38 G35 G32 G29 G26 G23 G20 G17 G14 G11 G8 G5 G4 G1 D39 D37
ASP_134603_01
C1040 1UF 25V X5R
C1039 1UF 25V X5R
C293 1UF 25V X5R
C291 1UF 25V X5R
C1045 1UF 25V X5R
C1006 10UF 25V X5R
C1001 10UF 6.3V X6S
C1044 1UF 25V X5R
C1043 1UF 25V X5R
C1042 1UF 25V X5R
C1041 1UF 25V X5R
C292 1UF 25V X5R
C897 100UF 6.3V X6S
C898 100UF 6.3V X6S
3.3V Bulk
C939 0.1UF 25V
C940 0.1UF 25V
C941 0.1UF 25V
C942 0.1UF 25V
C943 0.1UF 25V
C944 0.1UF 25V
C945 0.1UF 25V
C946 0.1UF 25V
NC7SZ66
VCC
A 1 FMC_HPC_TDO_LPC_TDI
B 2 FMC_LPC_TDO
FMC_LPC_PRSNT_M2C_B 4 OE
GND
U27 3 SC70_5
When OE = 1
Switch is Closed
ANSI/VITA 57.1 - Revised 2010
FMC LPC Header
XILINX
TITLE: FMC LPC Header
SCHEM, ROHS COMPLIANT
HW-U1-KCU105_REV1_1
ASSY P/N: 0431811
PCB P/N: 1280723
SCH P/N: 0381556
TEST P/N: TSS0165
DATE: 05/20/2015:19:32
VER: 1.1
SHEET SIZE: B
REV: 02
SHEET 25 OF 66
DRAWN BY: BF



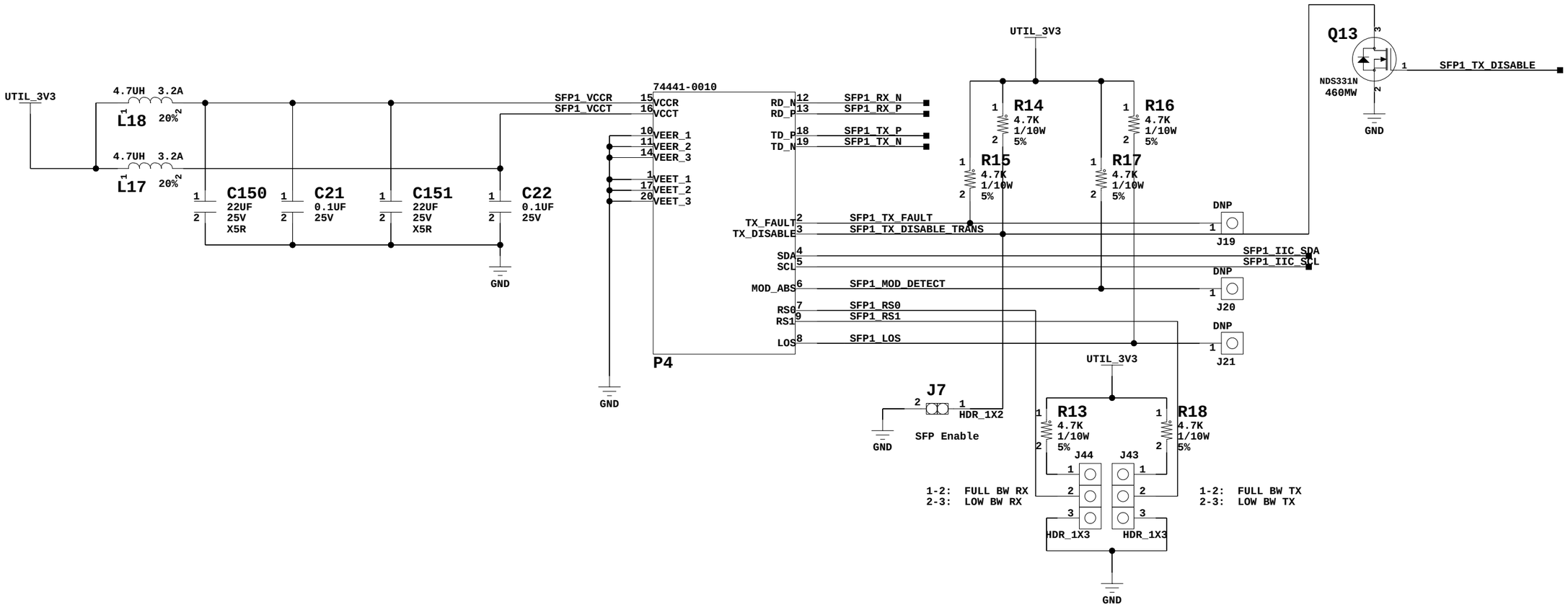
PCIe x8 Edge Connector

TITLE: PCIe x8 Edge Connector SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 26 OF 66	DRAWN BY: BF

SFP0 - SFP+ Connector and Dual Cage

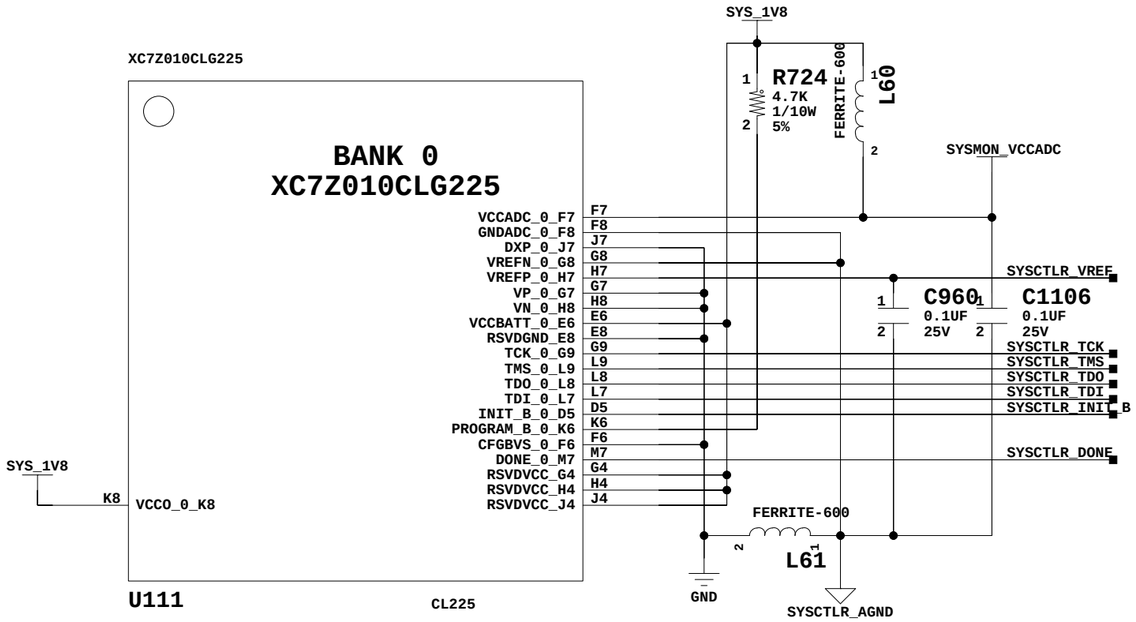
XILINX

TITLE: SFP0 - SFP+ Connector and Dual Cage SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 27 OF 66	DRAWN BY: BF



SFP1 - SFP+ Connector

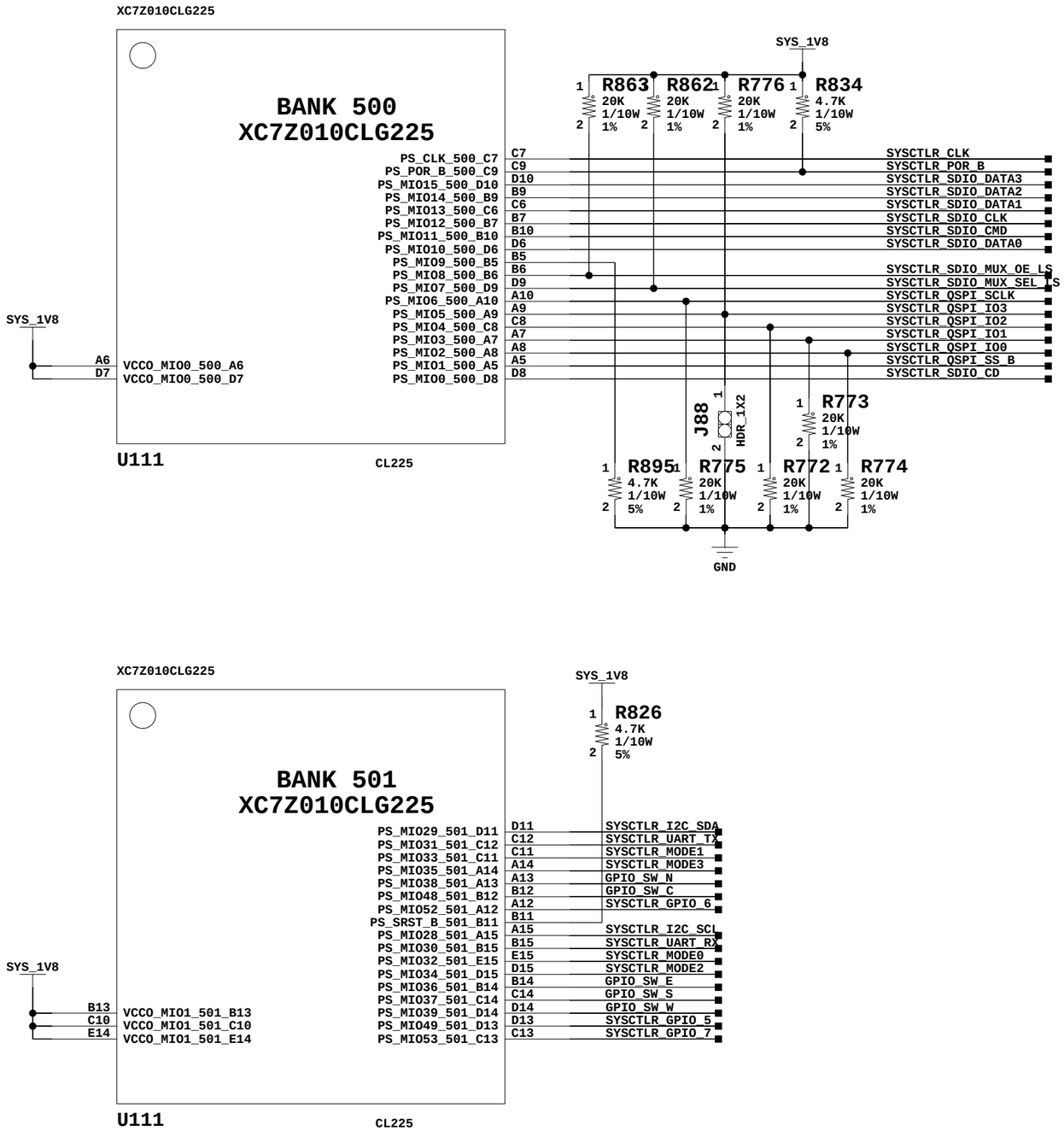
TITLE: SFP1 - SFP+ Connector SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 28 OF 66	DRAWN BY: BF

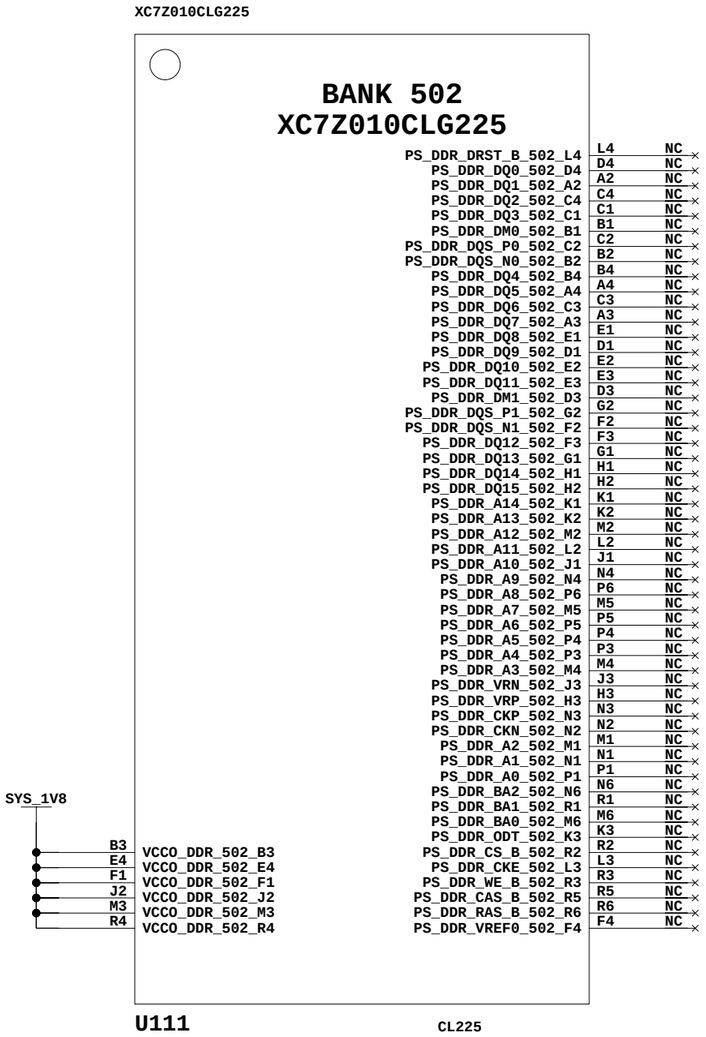


System Controller 1

XILINX

TITLE: System Controller 1 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 29 OF 66	DRAWN BY: BF





System Controller 2

XILINX

TITLE: System Controller 2 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 30 OF 66	DRAWN BY: BF

XC7Z010CLG225

BANK VCCPINT
XC7Z010CLG225

VCCPINT_K5 K5
VCCPINT_H5 H5
VCCPINT_G6 G6

SYS_1V0

U111 CL225

XC7Z010CLG225

BANK VCCINT
XC7Z010CLG225

VCCINT_L10 L10
VCCINT_J10 J10
VCCINT_G10 G10
VCCINT_F9 F9
VCCINT_E10 E10

SYS_1V0

U111 CL225

XC7Z010CLG225

BANK GND
XC7Z010CLG225

GND_R9 R9
GND_P2 P2
GND_P12 P12
GND_N5 N5
GND_N15 N15
GND_M8 M8
GND_L5 L5
GND_L11 L11
GND_L1 L1
GND_K7 K7
GND_K4 K4
GND_K14 K14
GND_K10 K10
GND_J9 J9
GND_J5 J5
GND_H6 H6
GND_H10 H10
GND_G5 G5
GND_G3 G3
GND_G13 G13
GND_F10 F10
GND_E9 E9
GND_E7 E7
GND_E5 E5
GND_D2 D2
GND_D12 D12
GND_C5 C5
GND_C15 C15
GND_B8 B8
GND_A11 A11
GND_A1 A1

GND

U111 CL225

XC7Z010CLG225

BANK VCCPAUX
XC7Z010CLG225

VCCPAUX_L6 L6
VCCPAUX_J6 J6

SYS_1V8

U111 CL225

XC7Z010CLG225

BANK VCCAUX
XC7Z010CLG225

VCCAUX_K9 K9
VCCAUX_J8 J8
VCCAUX_H9 H9

SYS_1V8

U111 CL225

XC7Z010CLG225

BANK VCCPLL
XC7Z010CLG225

VCCPLL_F5 F5

U111 CL225

SYS_1V8
VCCPLL
FERRITE-120
L62 H 3A N
C835 1 2 0.47UF 10V X5R
C794 1 2 10UF 4V X5R
GND

VCCINT/VCCBRAM

SYS_1V0
C816 1 2 100UF 4V X6S
C806 1 2 4.7UF 6.3V X5R
C833 1 2 0.47UF 10V X5R
C834 1 2 0.47UF 10V X5R
GND

Bank 0

SYS_1V8
C795 1 2 47UF 6.3V X6S
GND

VCCAUX

SYS_1V8
C796 1 2 47UF 6.3V X6S
C808 1 2 4.7UF 6.3V X5R
C837 1 2 0.47UF 10V X5R
GND

Bank 34

SYS_1V8
C792 1 2 47UF 6.3V X6S
C810 1 2 4.7UF 6.3V X5R
C811 1 2 4.7UF 6.3V X5R
C843 1 2 0.47UF 10V X5R
C844 1 2 0.47UF 10V X5R
C841 1 2 0.47UF 10V X5R
C842 1 2 0.47UF 10V X5R
GND

VCCPINT

SYS_1V0
C788 1 2 100UF 4V X6S
C798 1 2 4.7UF 6.3V X5R
C821 1 2 0.47UF 10V X5R
C822 1 2 0.47UF 10V X5R
C820 1 2 0.47UF 10V X5R
GND

VCCPAUX

SYS_1V8
C789 1 2 100UF 4V X6S
C801 1 2 4.7UF 6.3V X5R
C825 1 2 0.47UF 10V X5R
GND

VCCO_MIO0

SYS_1V8
C790 1 2 100UF 4V X6S
C803 1 2 4.7UF 6.3V X5R
C828 1 2 0.47UF 10V X5R
GND

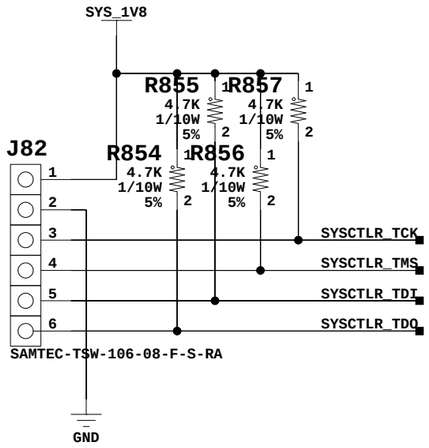
VCCO_MIO1

SYS_1V8
C791 1 2 100UF 4V X6S
C805 1 2 4.7UF 6.3V X5R
C830 1 2 0.47UF 10V X5R
GND

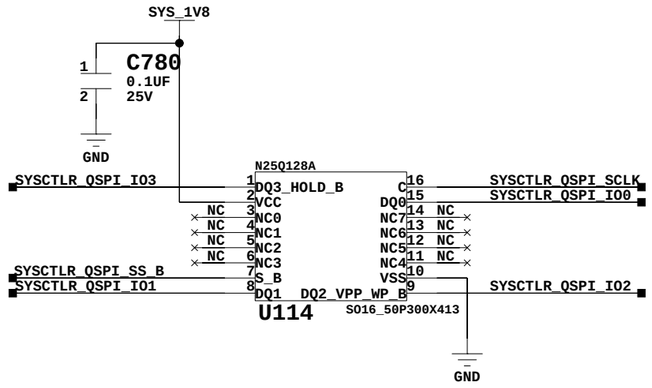
System Controller 3

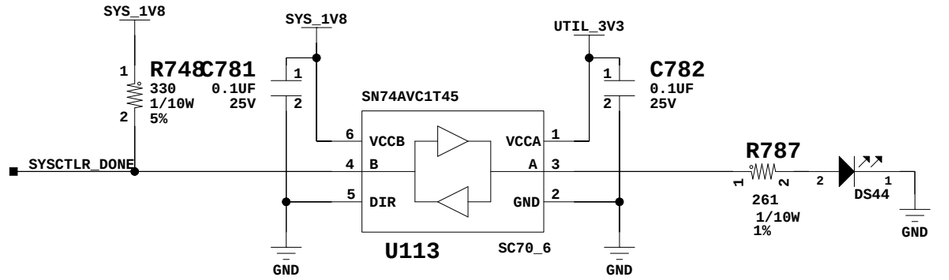
XILINX

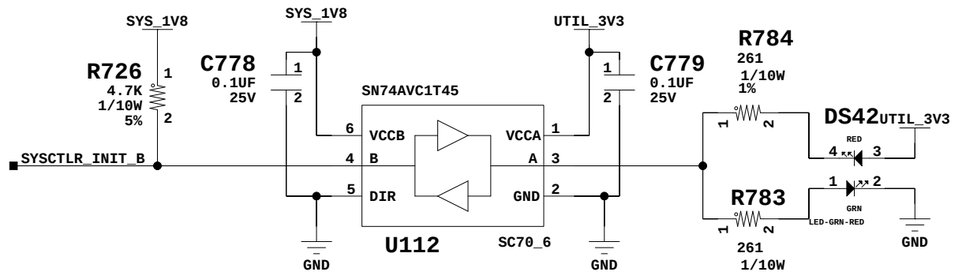
TITLE: System Controller 3 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 31 OF 66	DRAWN BY: BF



System Controller JTAG header







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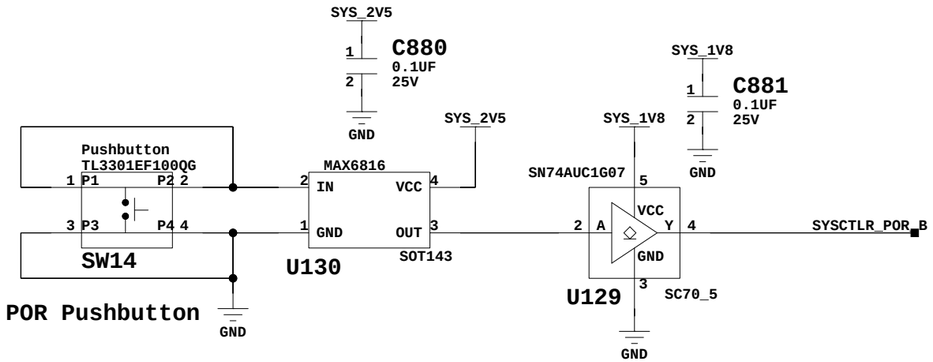
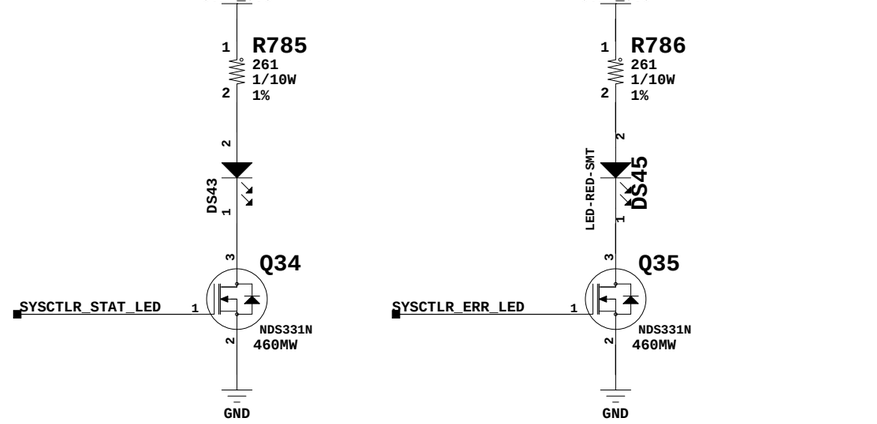
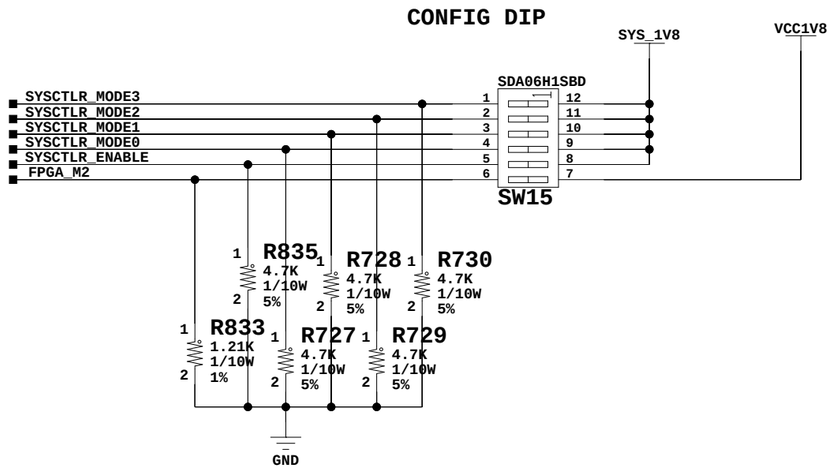




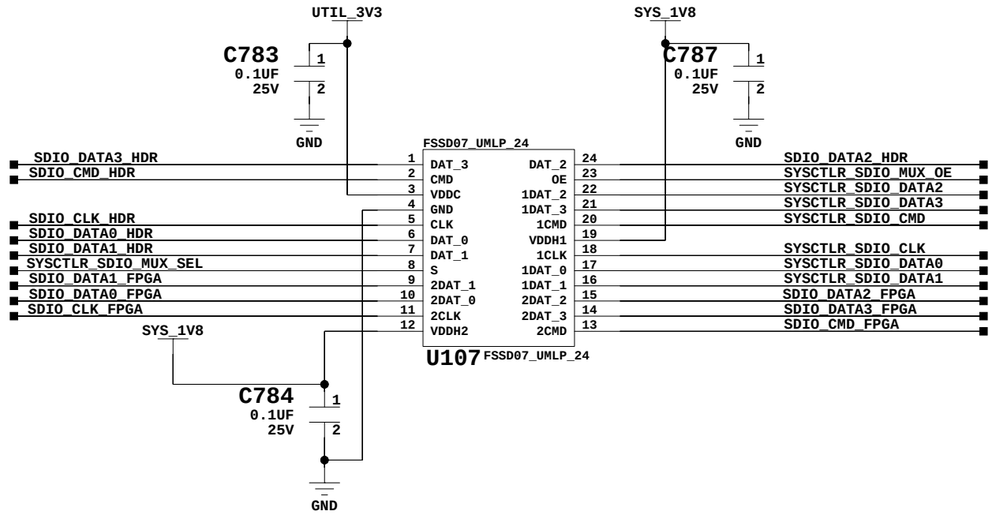


System Controller 4 - Config DIP

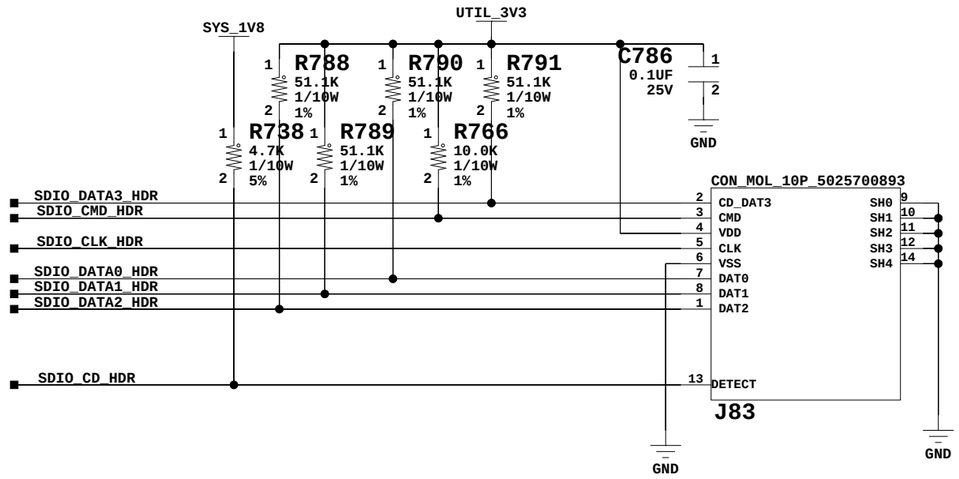
XILINX

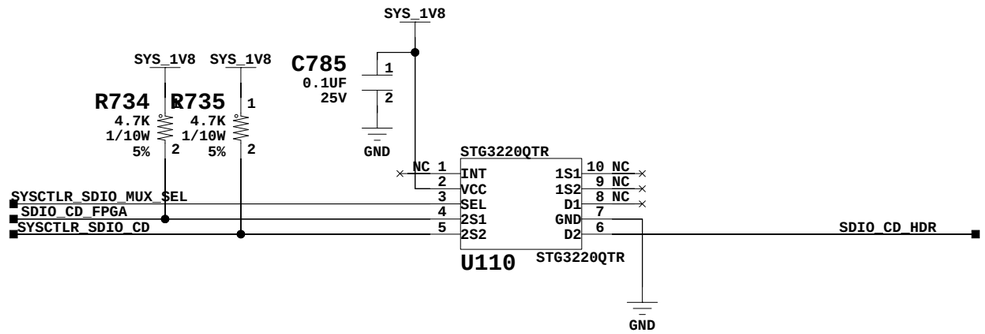
TITLE: System Controller 4 - Config DIP SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 32 OF 66	DRAWN BY: BF

SD MUX



Micro SD CONNECTOR

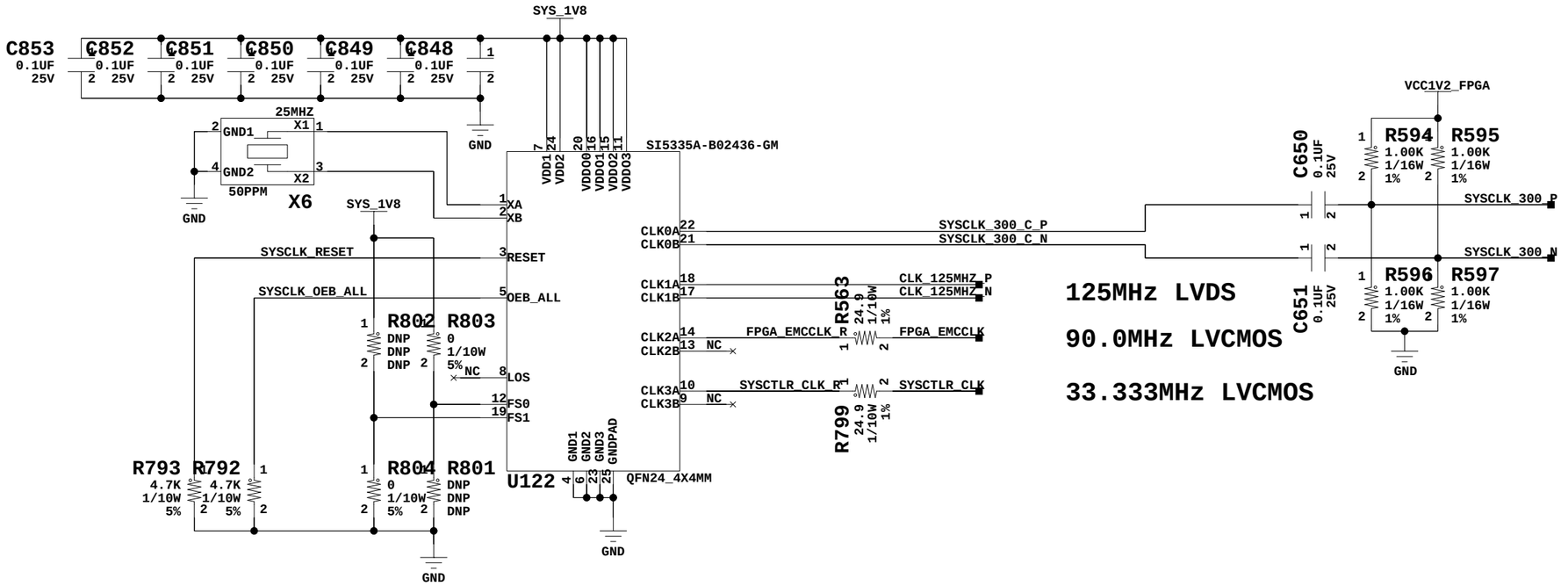




System Controller 5

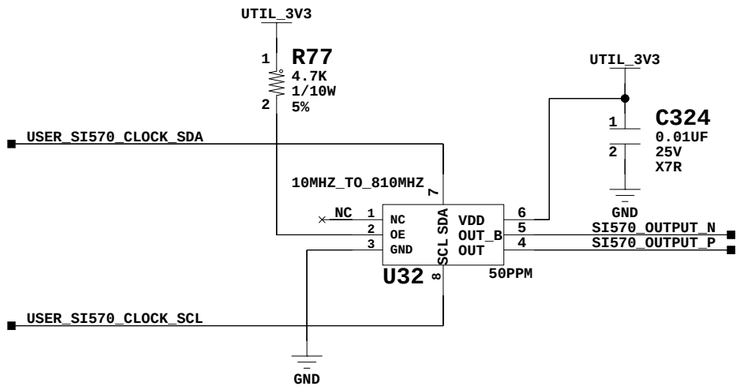
XILINX

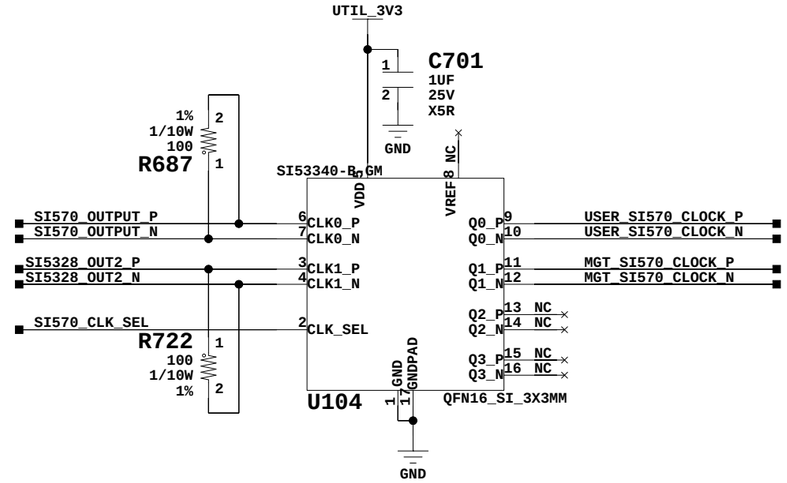
TITLE: System Controller 5 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 33 OF 66	DRAWN BY: BF



EMCCLK and System Clocks

TITLE: EMCCLK and System Clocks SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 34 OF 66	DRAWN BY: BF

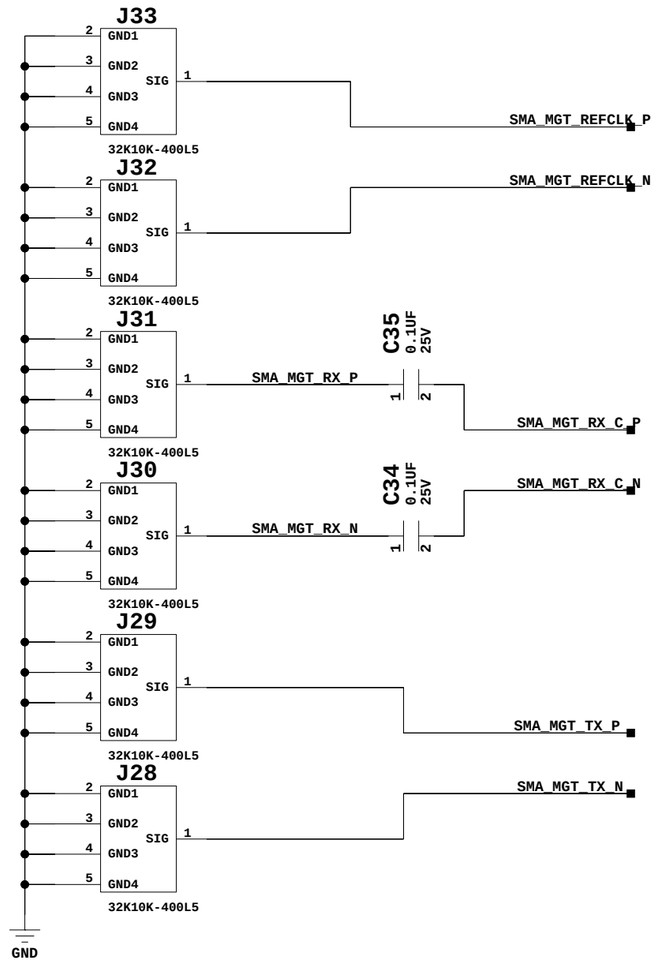


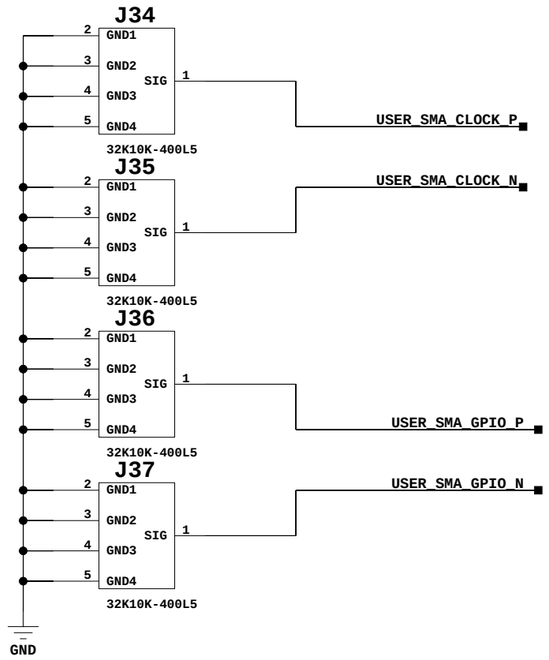


Programmable Clocks and Buffer

XILINX

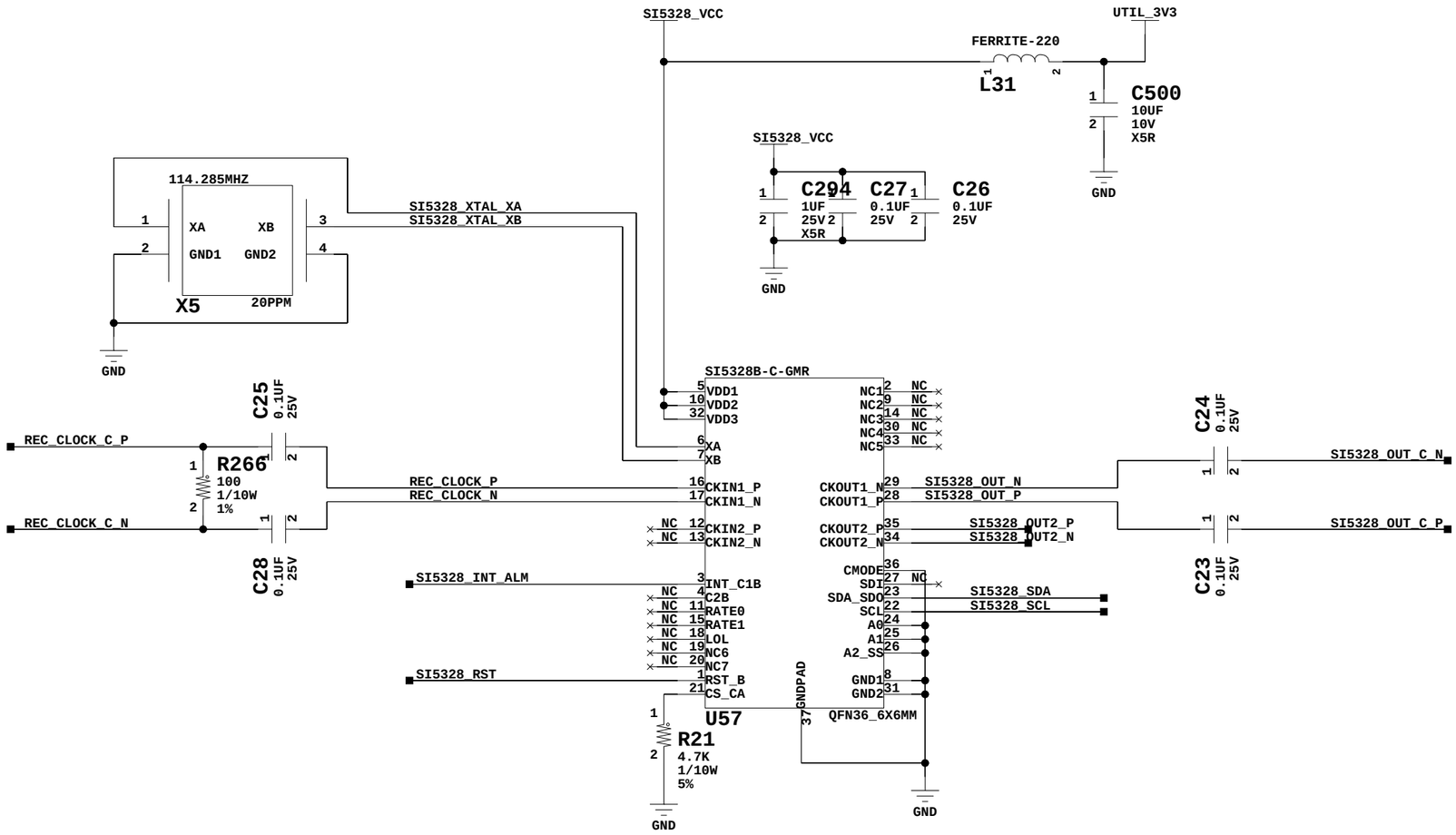
TITLE: Programmable Clocks and Buffer SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 35 OF 66	DRAWN BY: BF





SMA Connectors

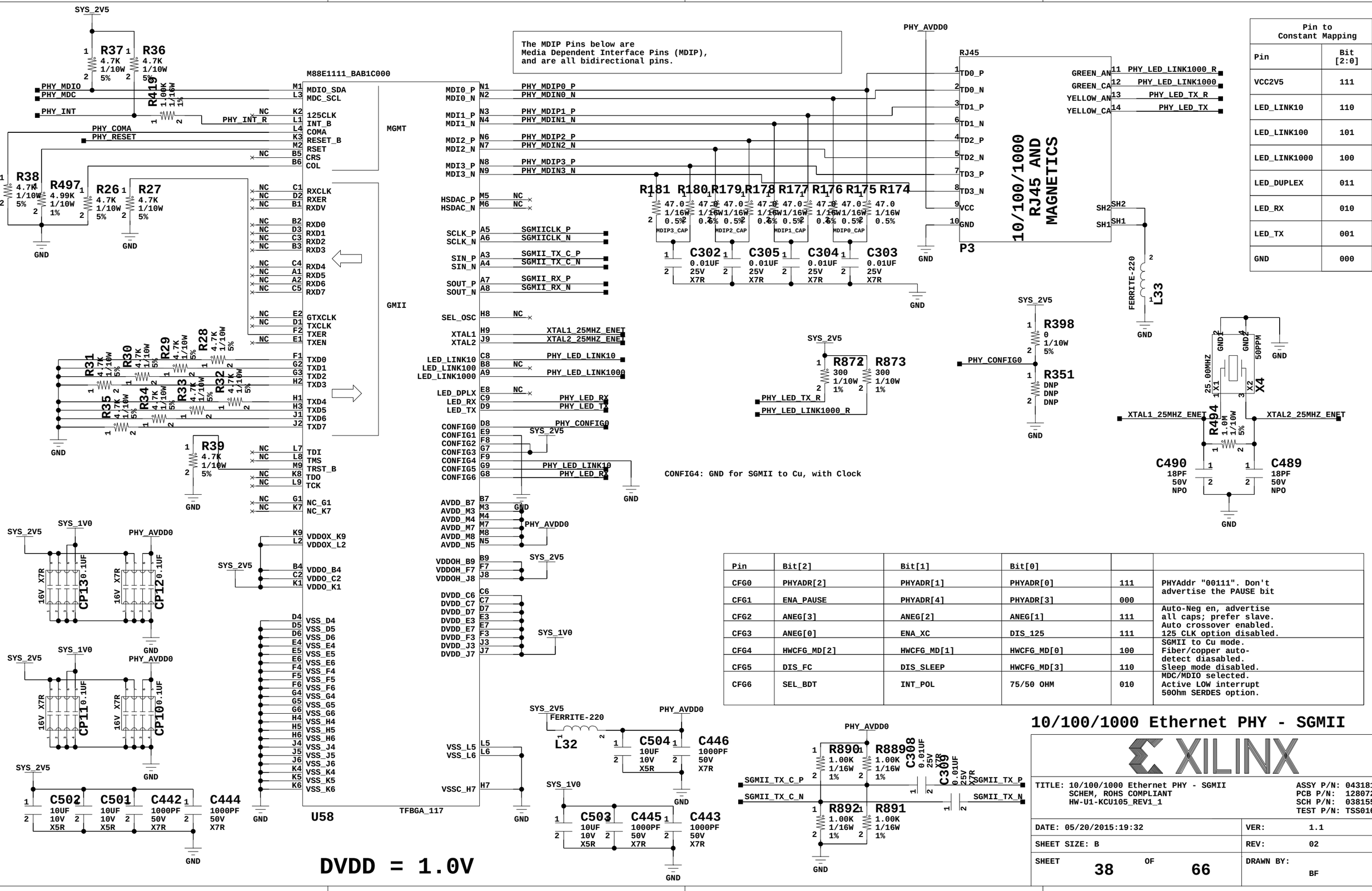
TITLE: SMA Connectors SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 36 OF 66	DRAWN BY: BF



5328 Clock Recovery

XILINX

TITLE: 5328 Clock Recovery SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 37 OF 66	DRAWN BY: BF



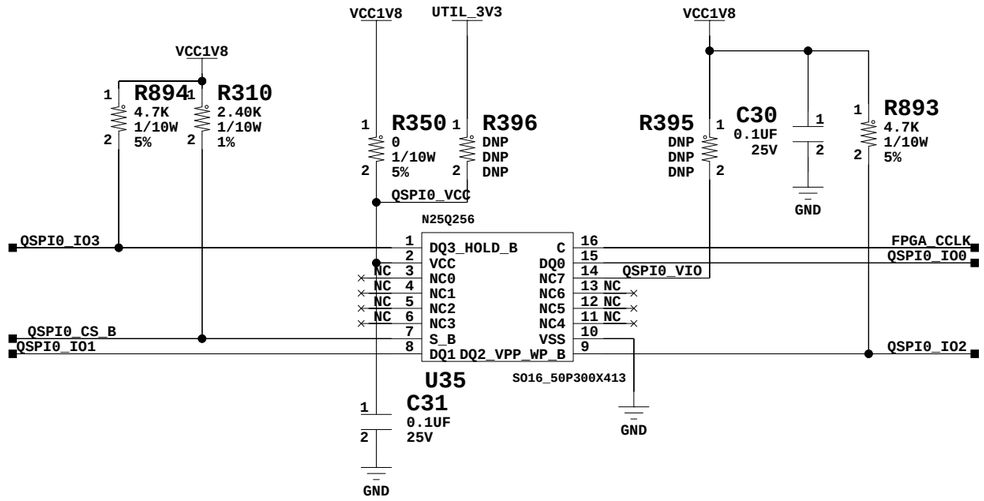
Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

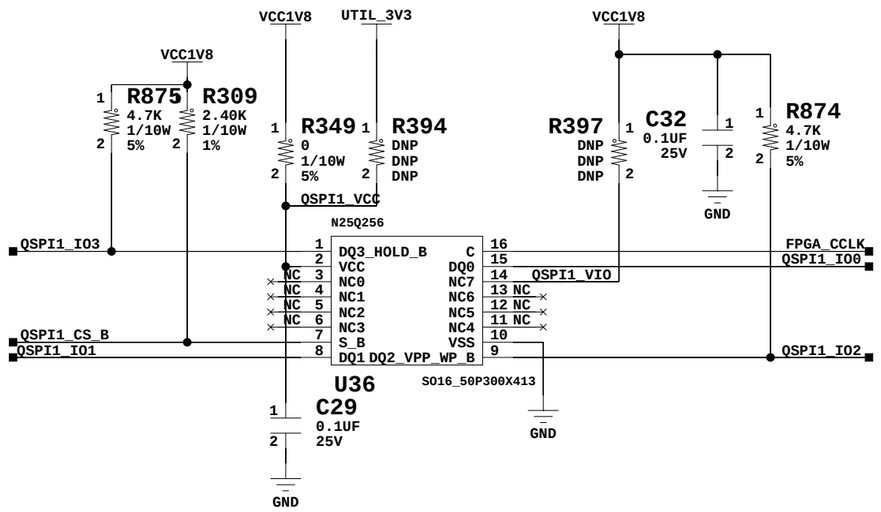
Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	100	SGMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	110	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

10/100/1000 Ethernet PHY - SGMII

XILINX

TITLE: 10/100/1000 Ethernet PHY - SGMII SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 38 OF 66	DRAWN BY: BF

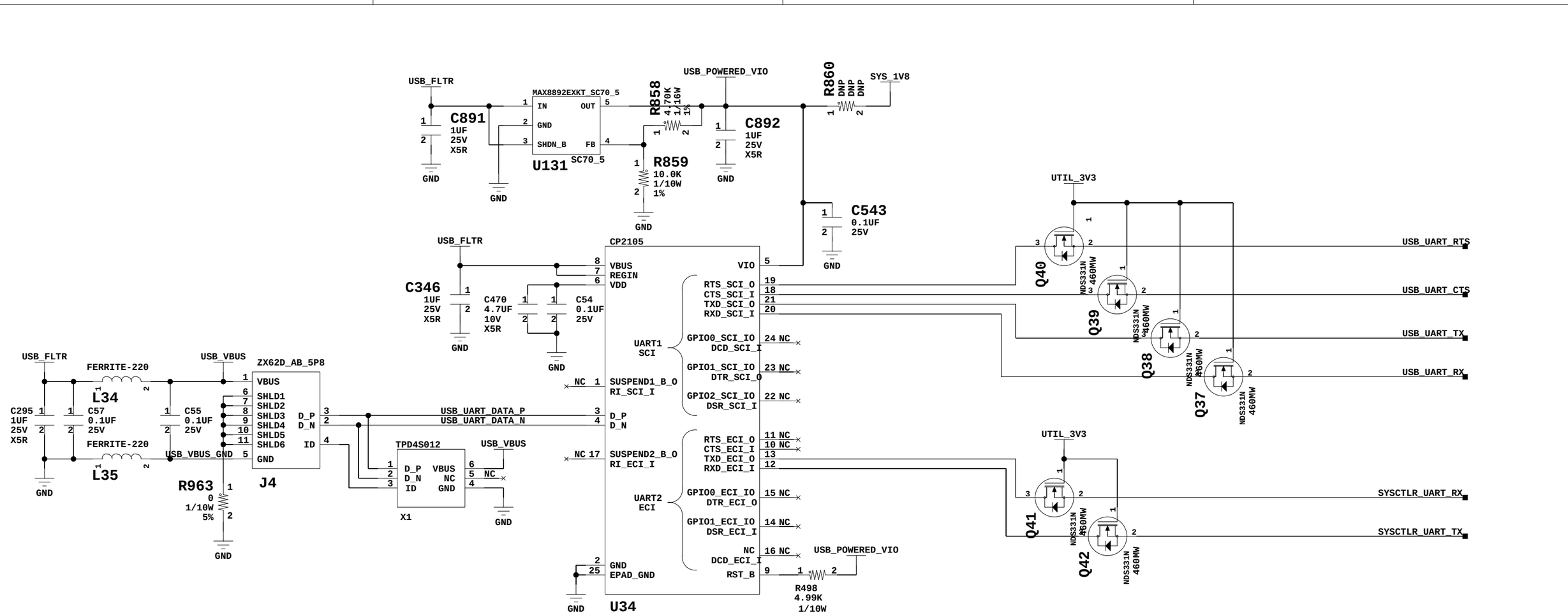


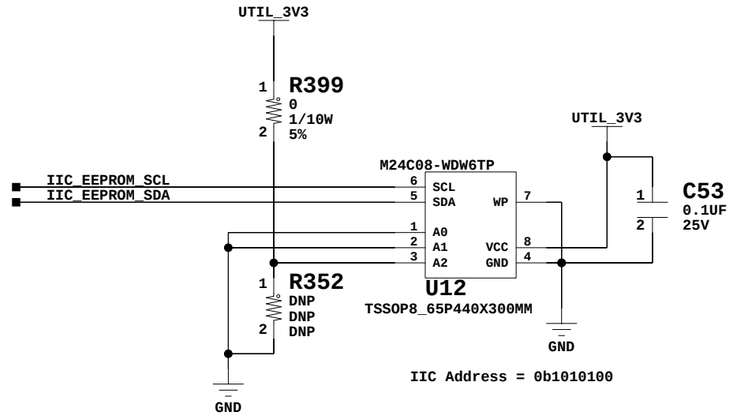


Dual Quad SPIs

XILINX

TITLE: Dual Quad SPIs SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 39 OF 66	DRAWN BY: BF

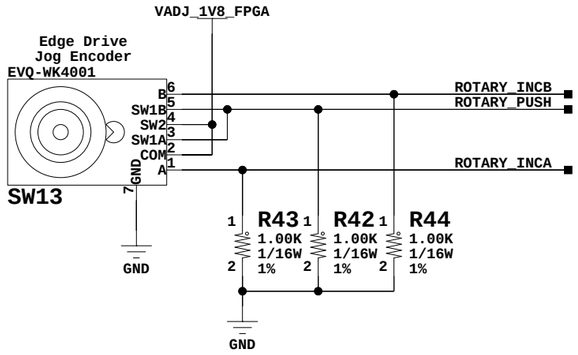




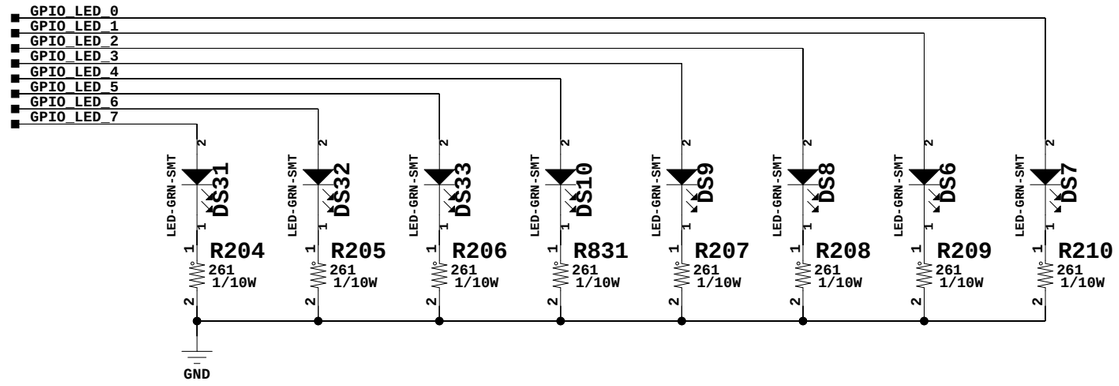
Dual USB UART - EEPROM

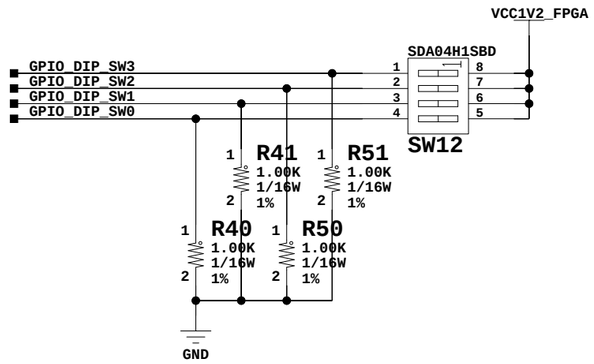
XILINX

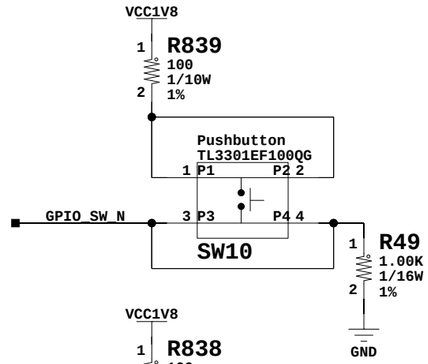
TITLE: Dual USB UART - EEPROM SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 40 OF 66	DRAWN BY: BF

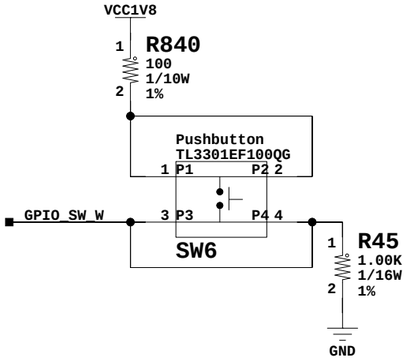


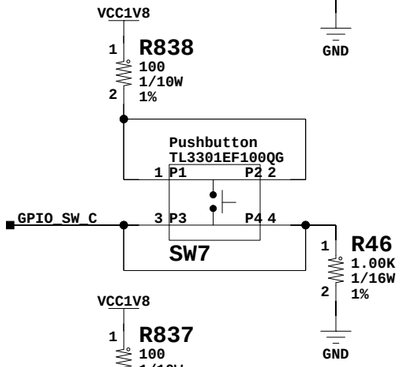
LEDs near top right edge

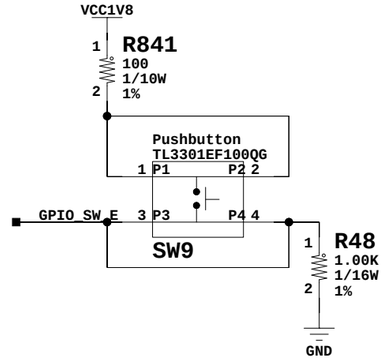


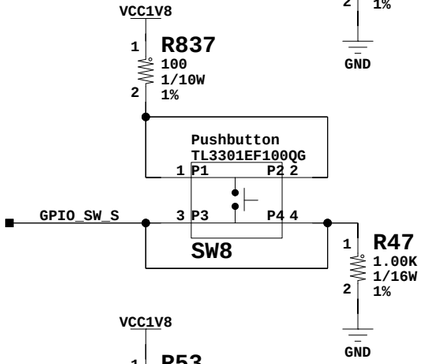


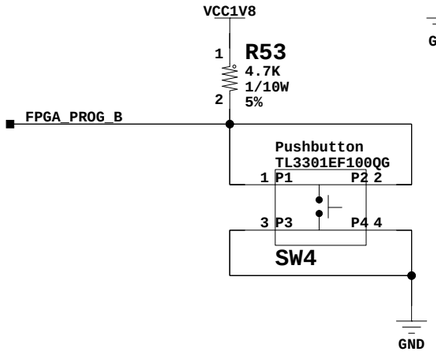


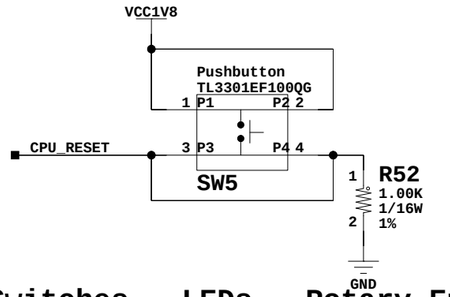






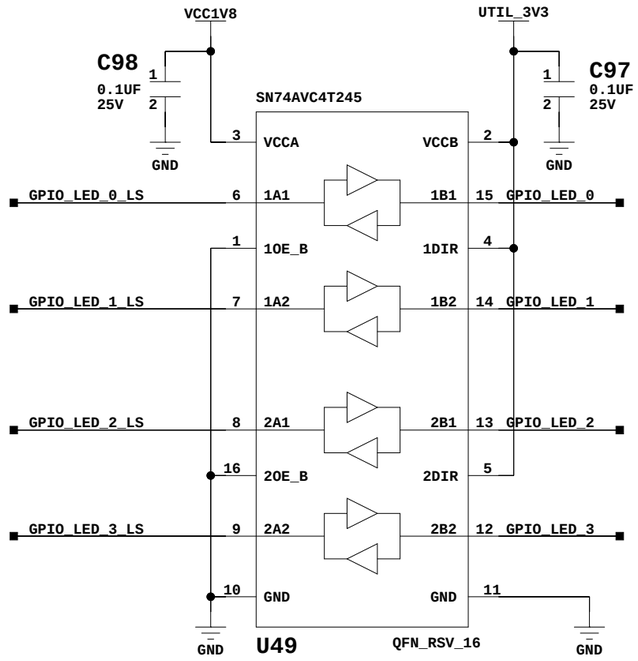


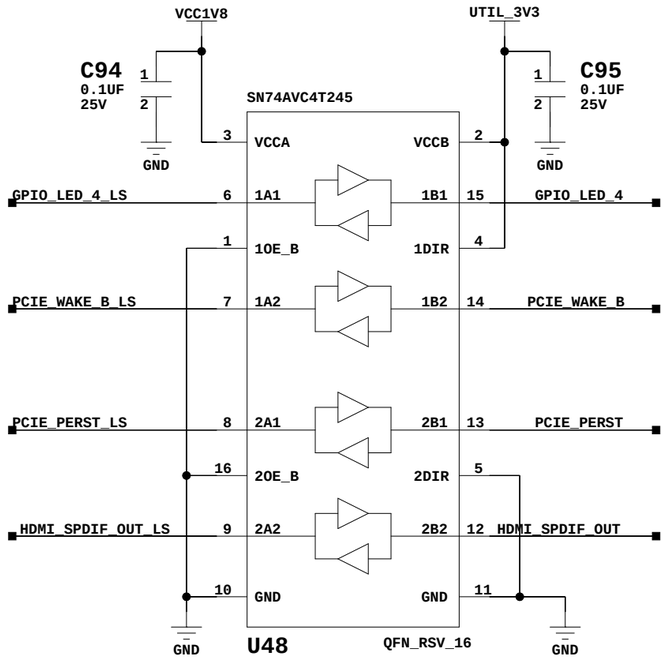


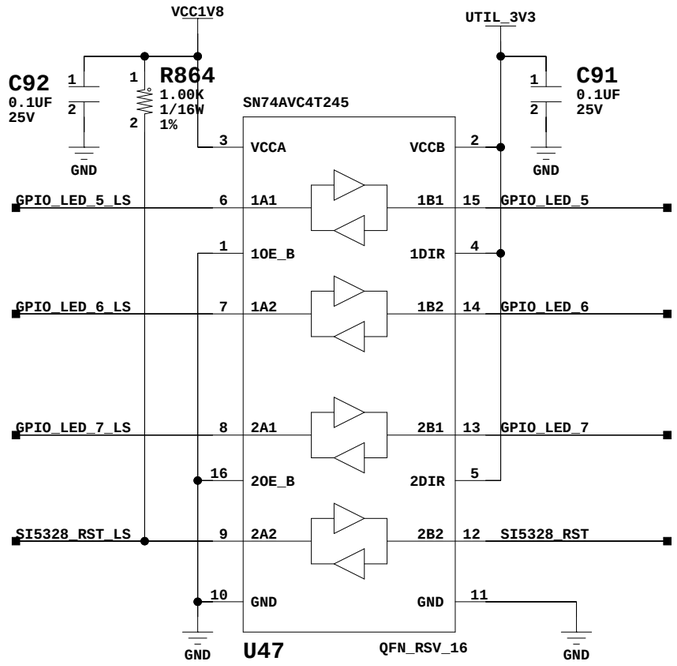


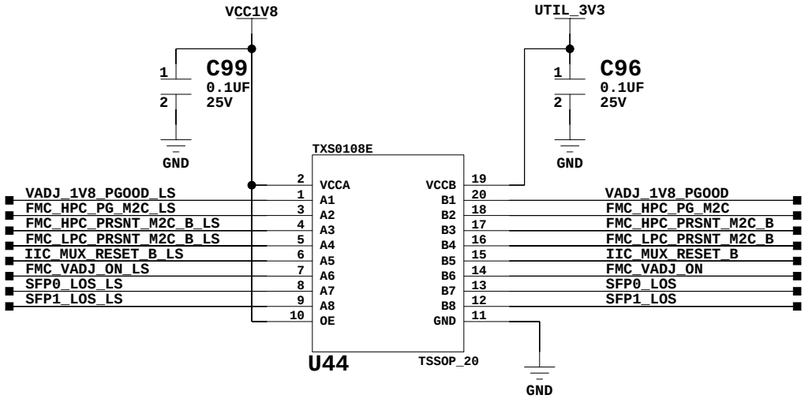
Buttons - Switches - LEDs - Rotary Encoder

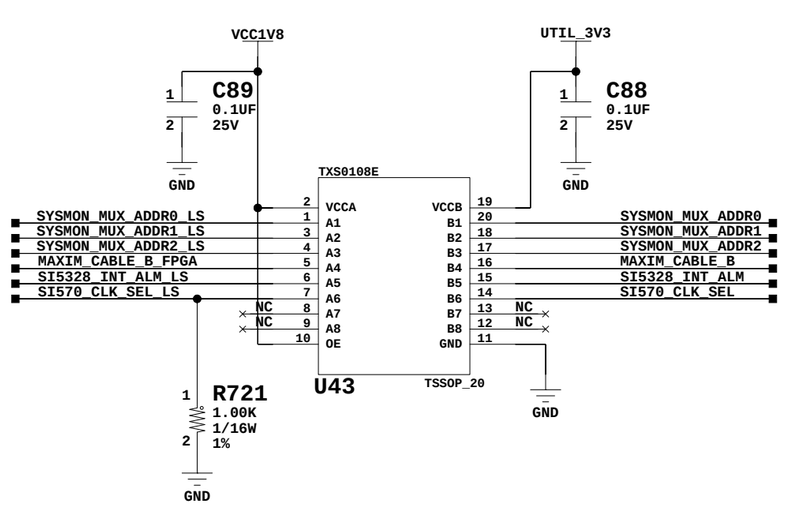
TITLE: Buttons - Switches - LEDs - Rotary Encoder SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 41 OF 66	DRAWN BY: BF







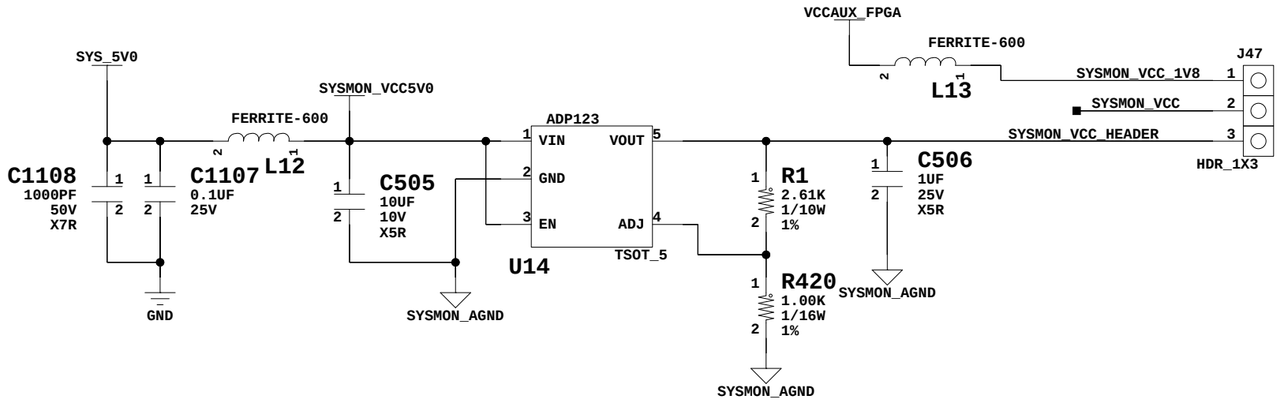


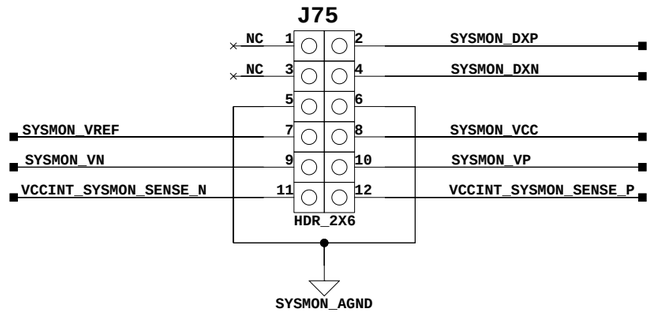


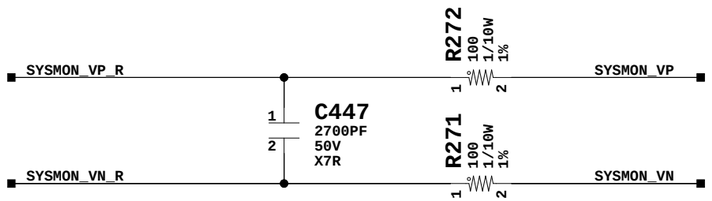
Level Shifters

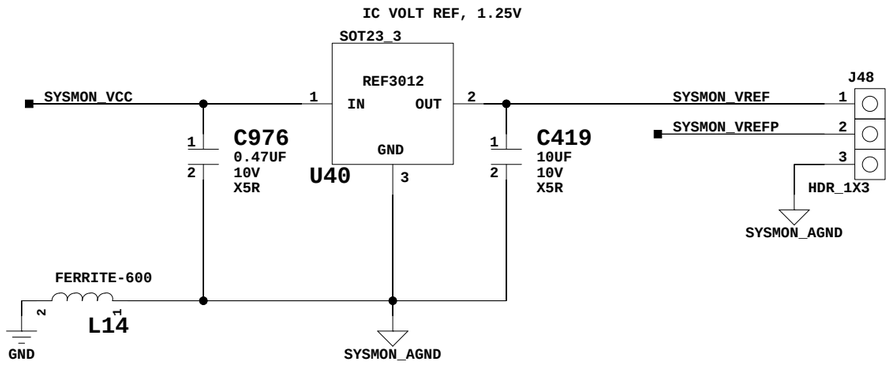
XILINX

TITLE: Level Shifters SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 42 OF 66	DRAWN BY: BF









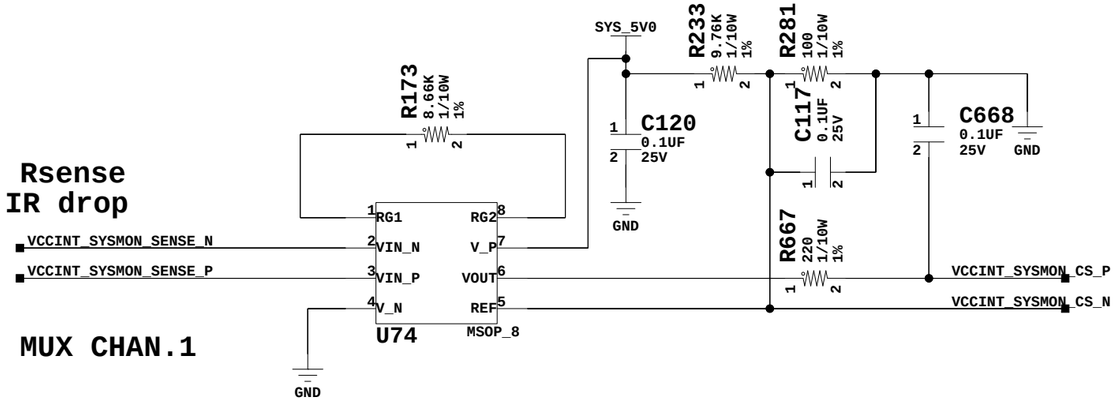
SYSMON Header and Reference

XILINX

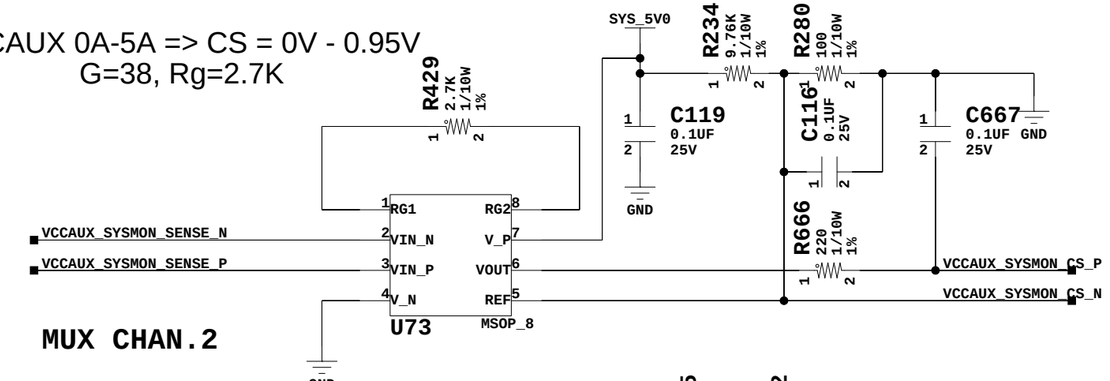
TITLE: SYSMON Header and Reference SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 43 OF 66	DRAWN BY: BF

VCCINT 0A-40A => CS = 0V - 1V G=12.5, Rg=8.66K

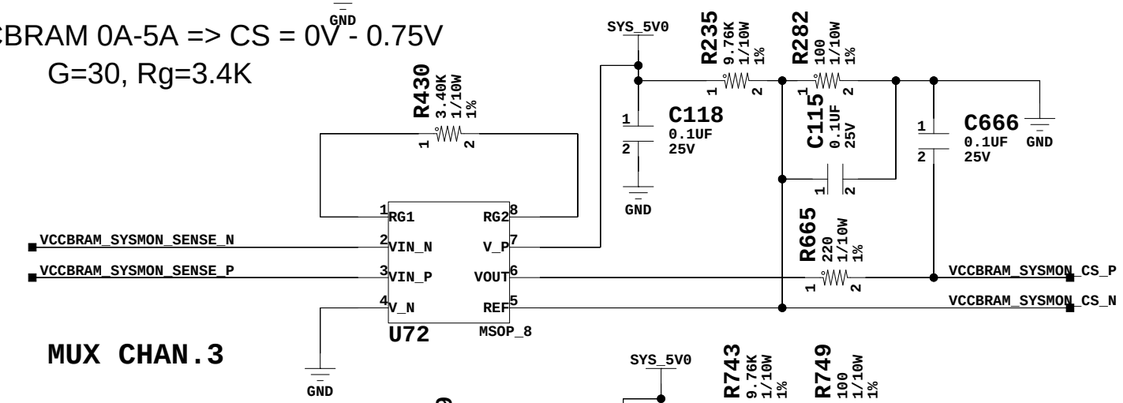
NOTE: VCCINT sense resistor is 0.002ohms



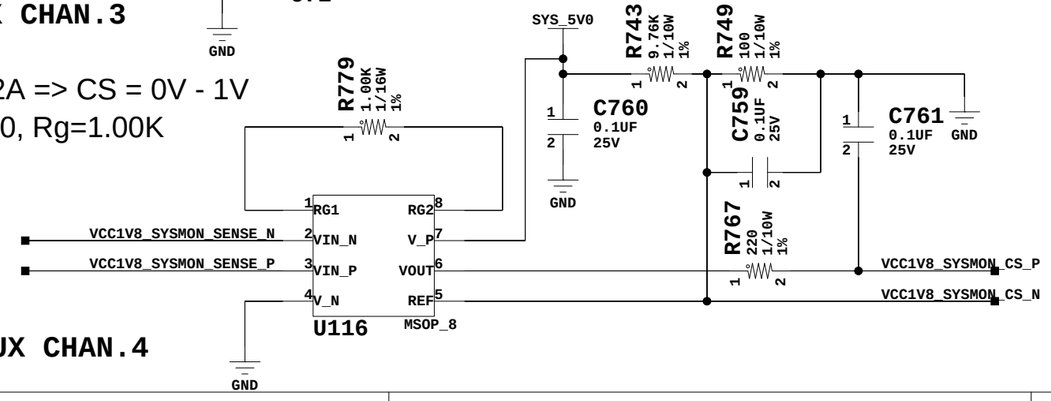
VCCAUX 0A-5A => CS = 0V - 0.95V
G=38, Rg=2.7K



VCCBRAM 0A-5A => CS = 0V - 0.75V
G=30, Rg=3.4K



VCC1V8 0A-2A => CS = 0V - 1V
G=100, Rg=1.00K

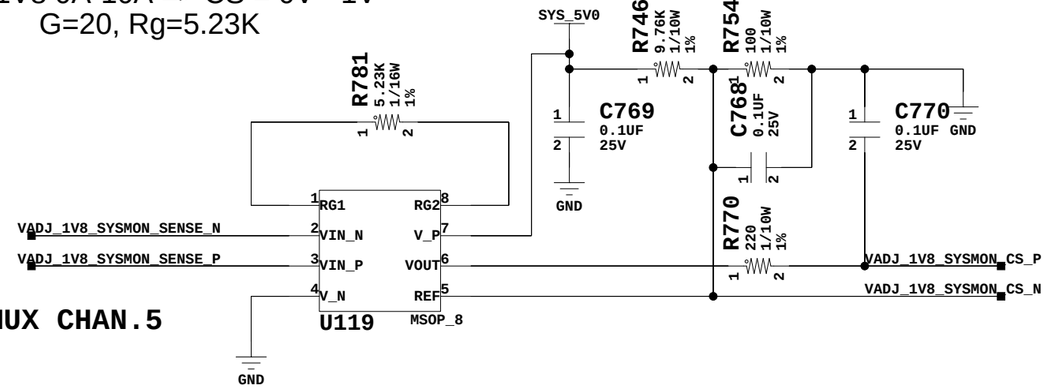


SYSMON Monitoring 1

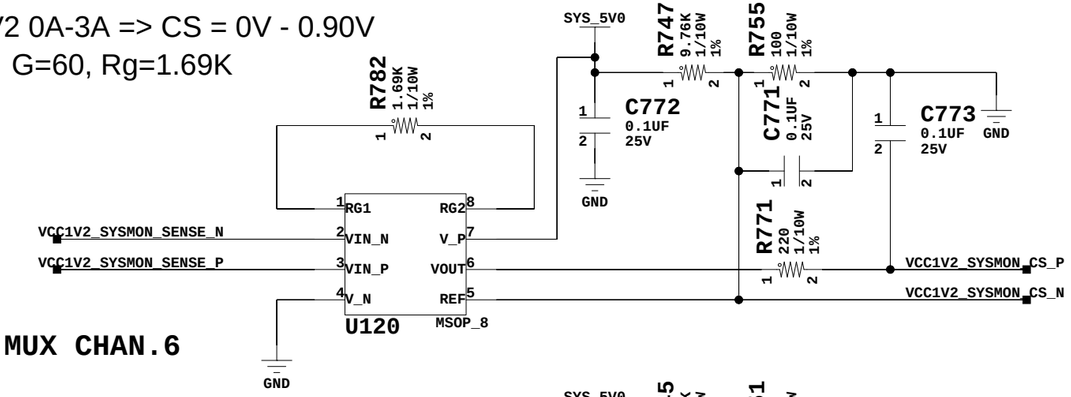
XILINX

TITLE: SYSMON Monitoring 1 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 44 OF 66	DRAWN BY: BF

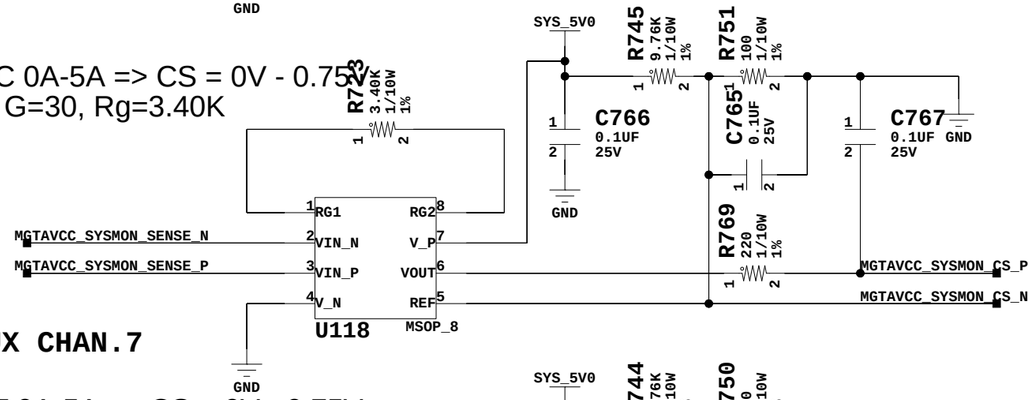
VADJ_1V8 0A-10A => CS = 0V - 1V
G=20, Rg=5.23K



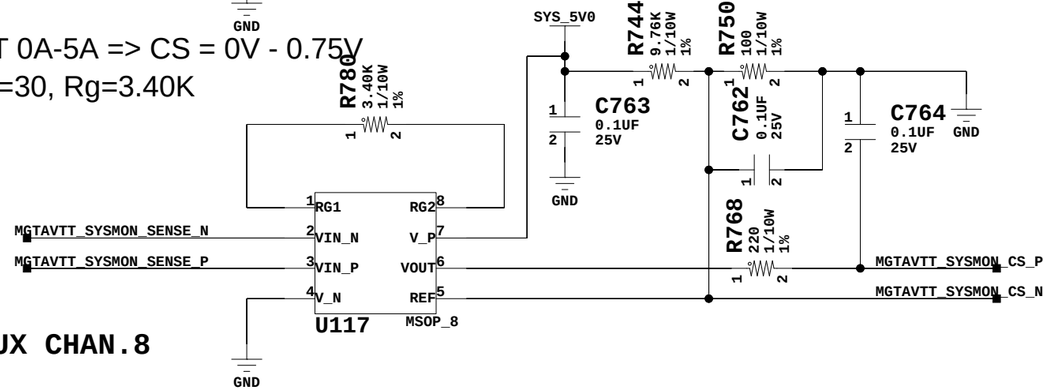
VCC1V2 0A-3A => CS = 0V - 0.90V
G=60, Rg=1.69K

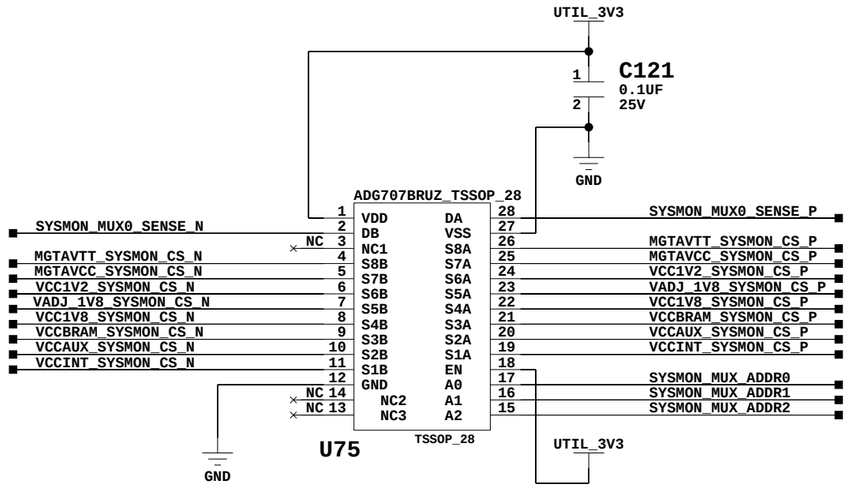


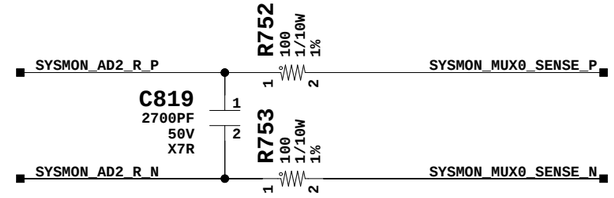
MGTAVCC 0A-5A => CS = 0V - 0.75V
G=30, Rg=3.40K



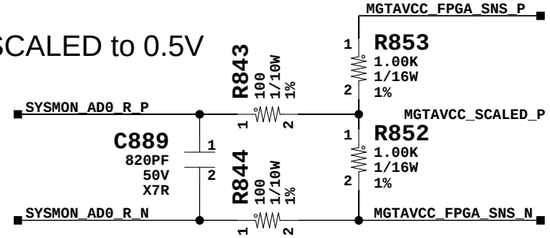
MGTAVTT 0A-5A => CS = 0V - 0.75V
G=30, Rg=3.40K



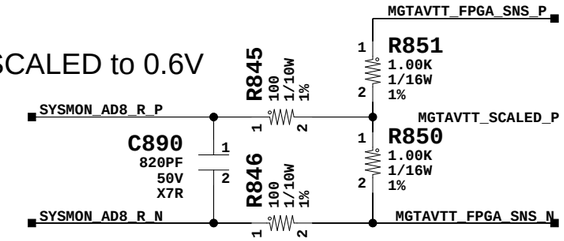




MGTAVCC 1.0V SCALED to 0.5V

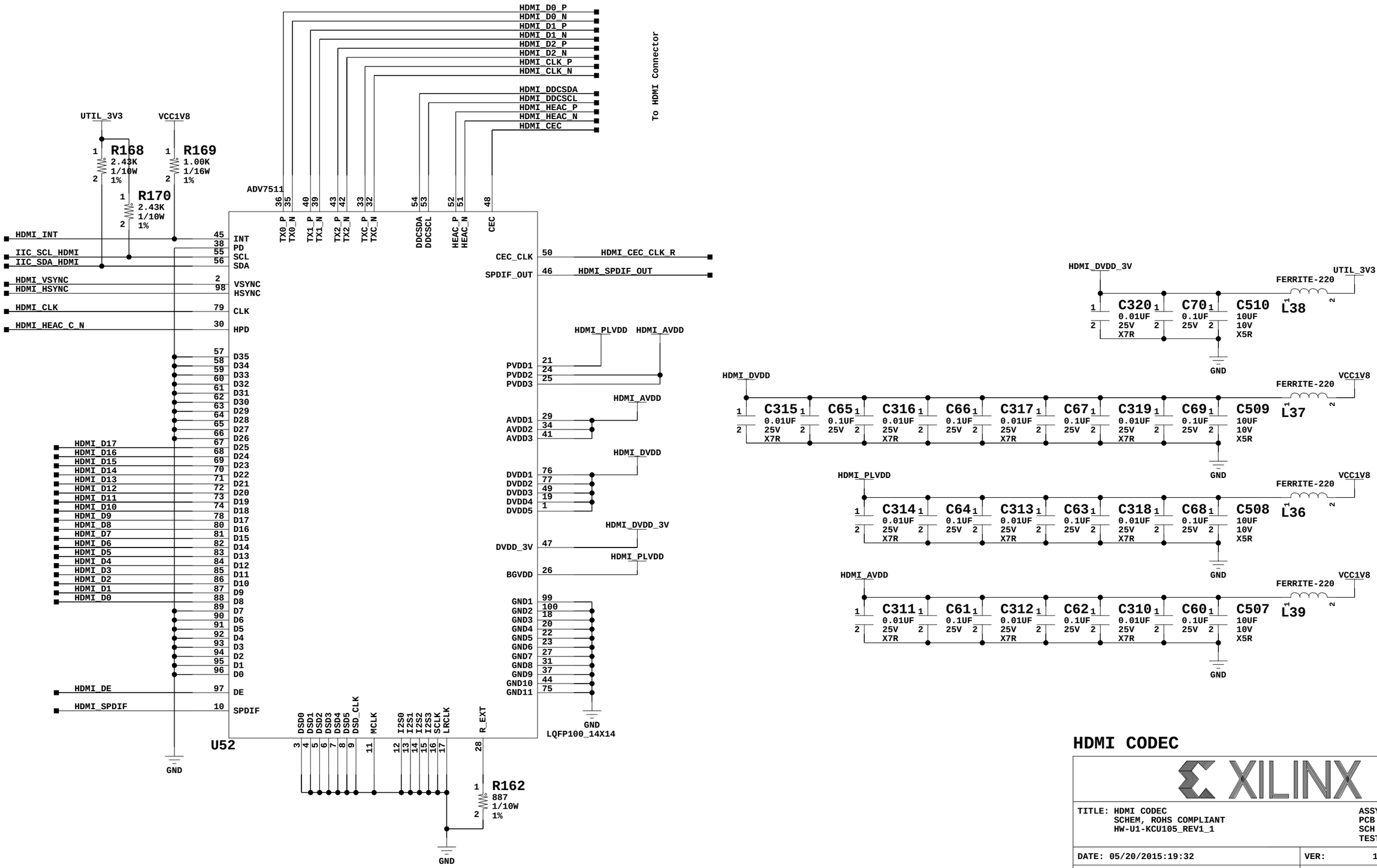


MGTAVTT 1.2V SCALED to 0.6V



SYSMON Monitoring 2

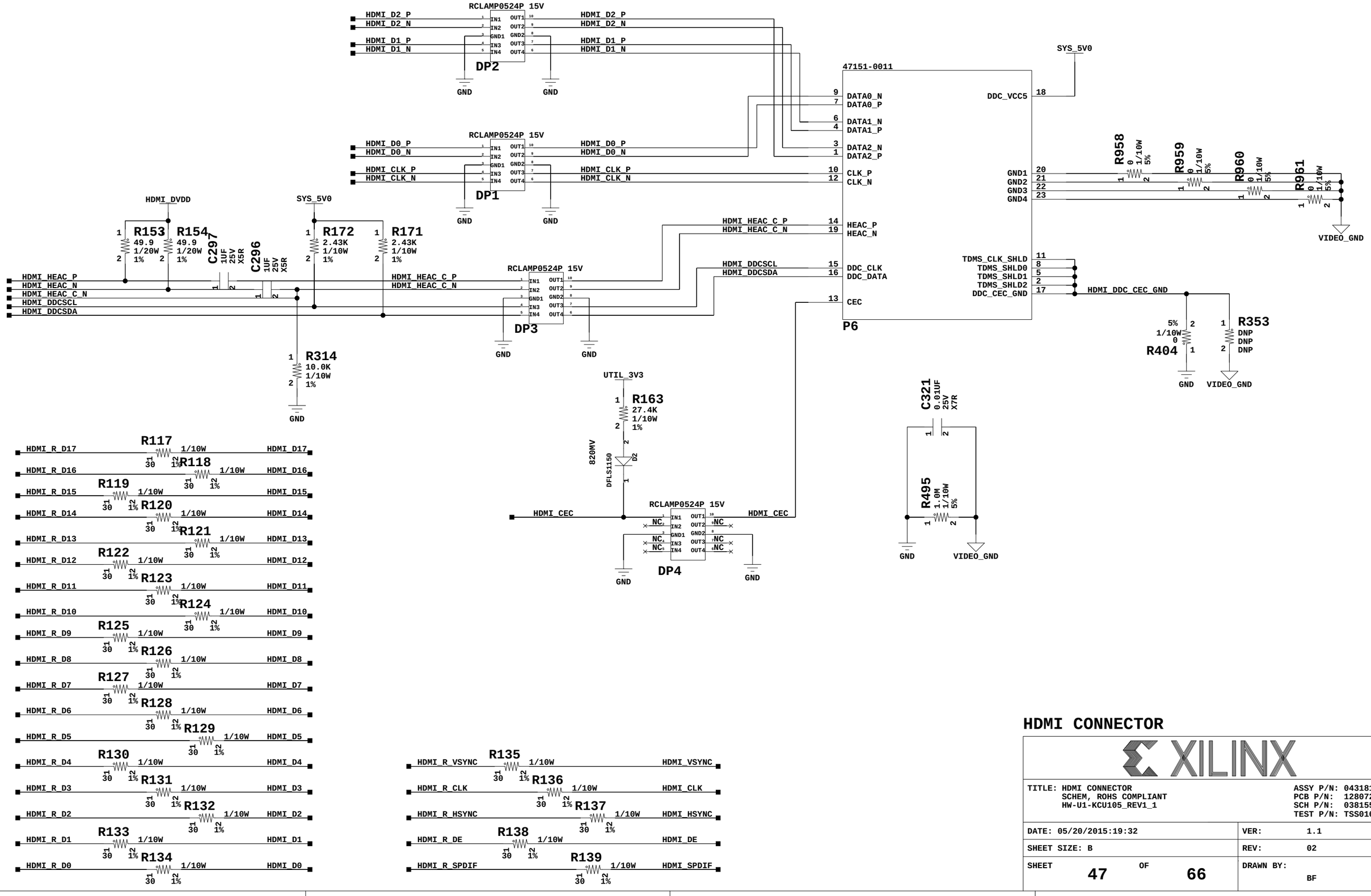
TITLE: SYSMON Monitoring 2 SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 45 OF 66	DRAWN BY: BF



HDMI CODEC

XILINX

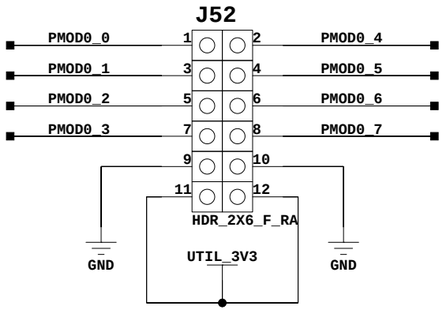
TITLE: HDMI CODEC SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 46 OF 66	DRAWN BY: BF

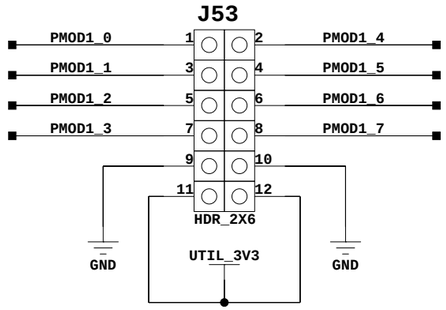


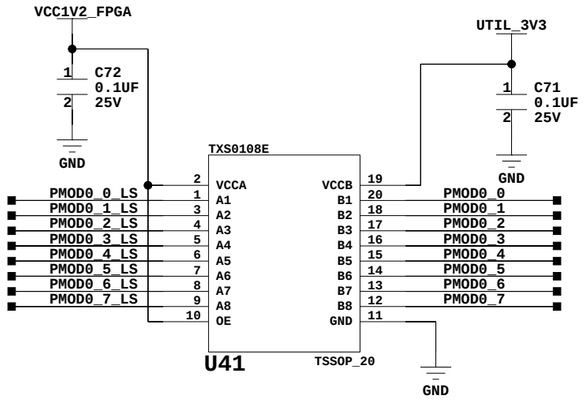
HDMI CONNECTOR

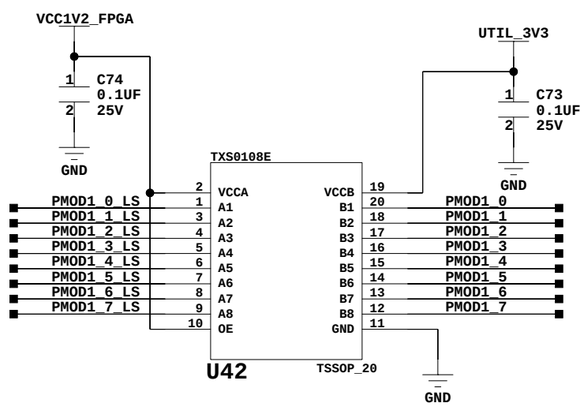
XILINX

TITLE: HDMI CONNECTOR SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 47 OF 66	DRAWN BY: BF



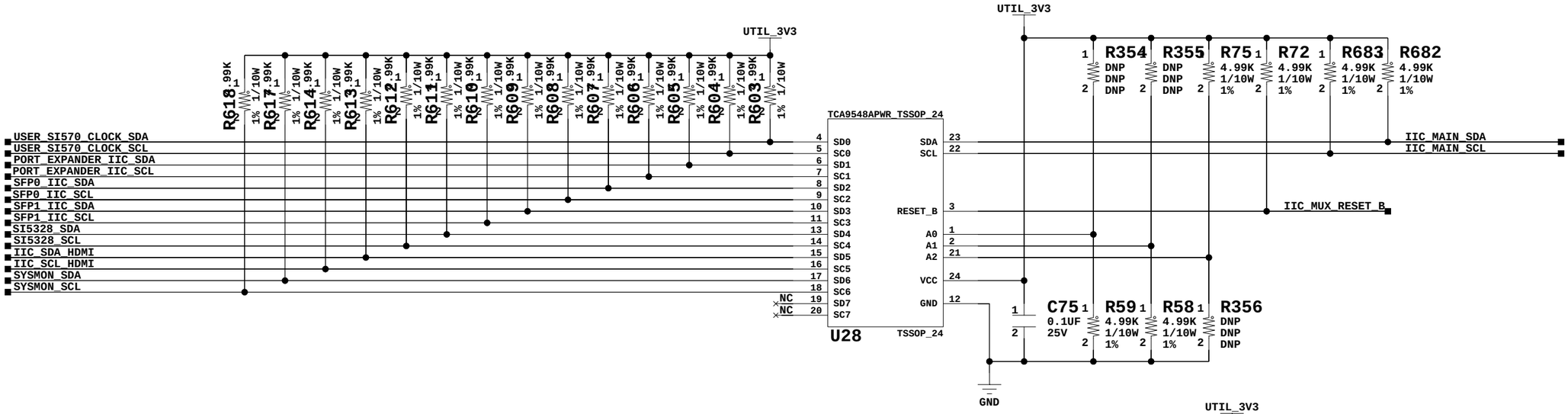


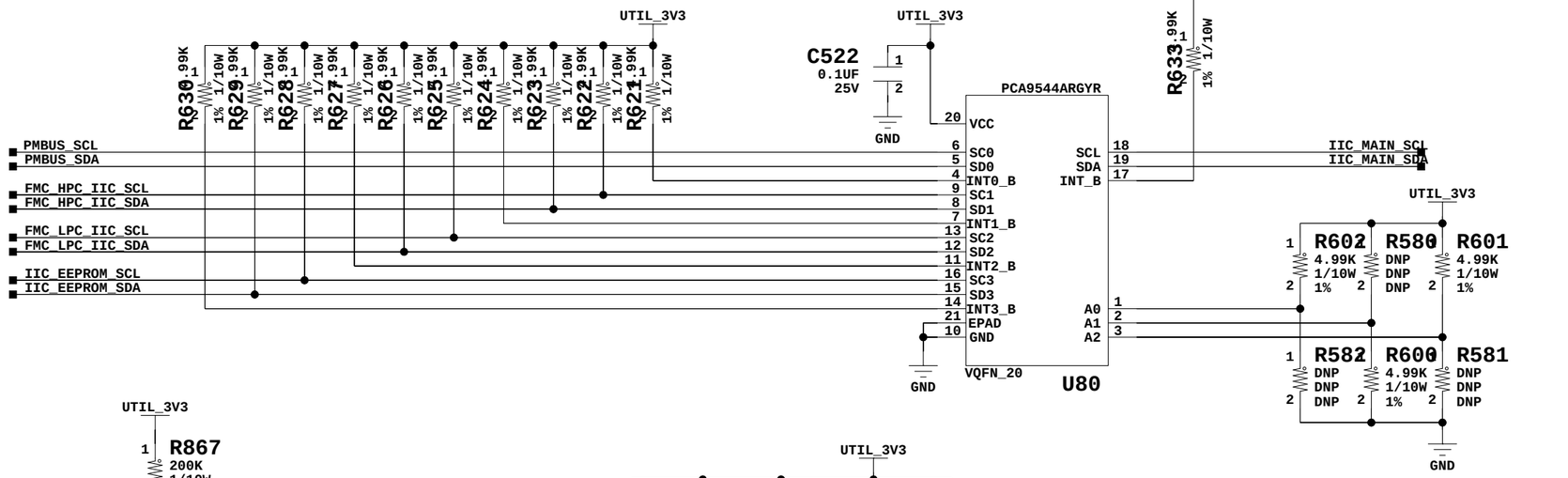


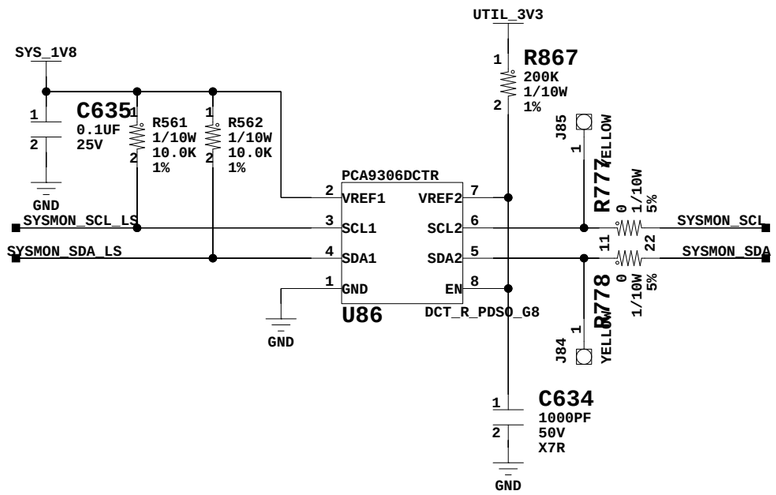


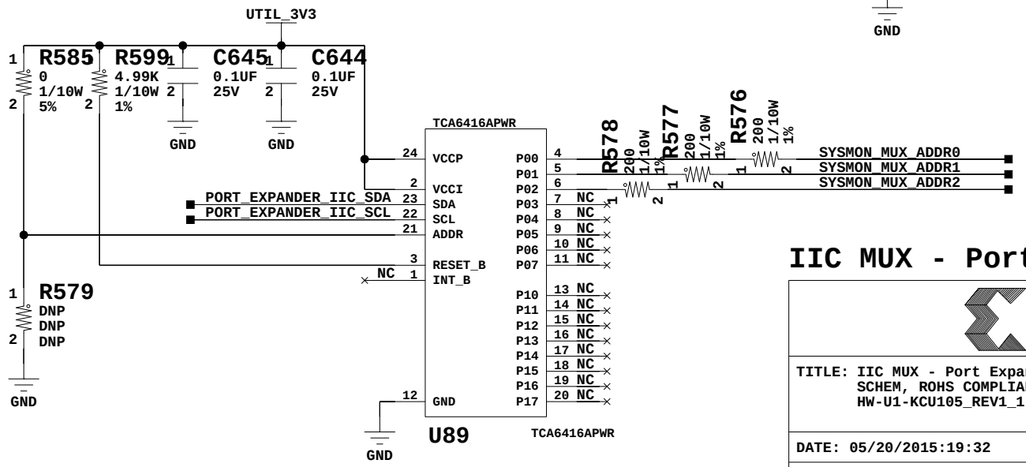
PMODs and Level Shifters

TITLE: PMODs and Level Shifters SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 48 OF 66	DRAWN BY: BF







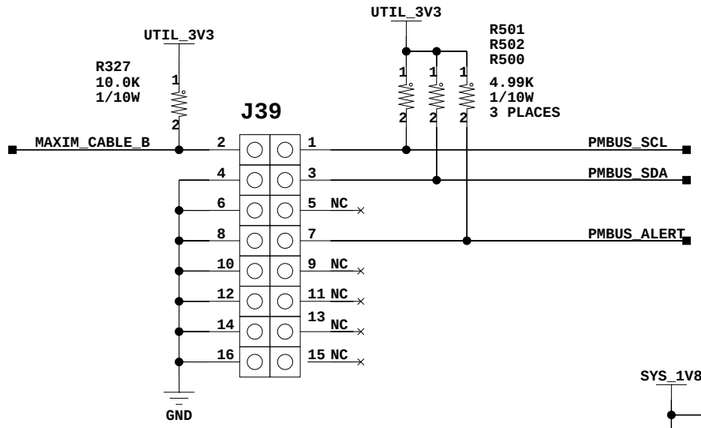


IIC MUX - Port Expander

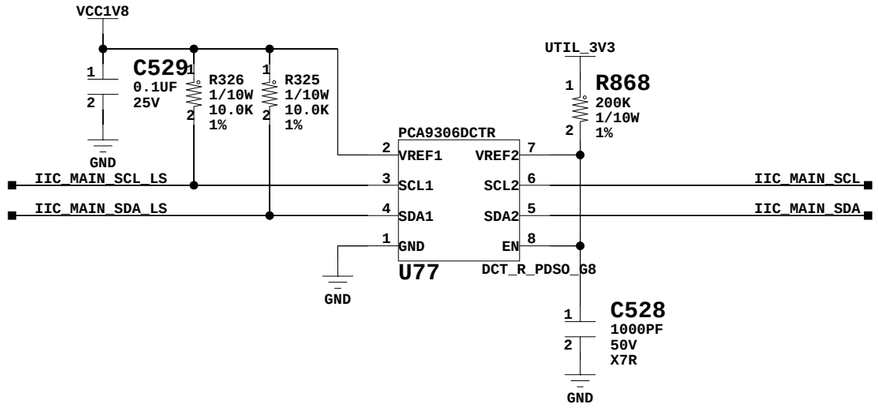
XILINX

TITLE: IIC MUX - Port Expander SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 49 OF 66	DRAWN BY: BF

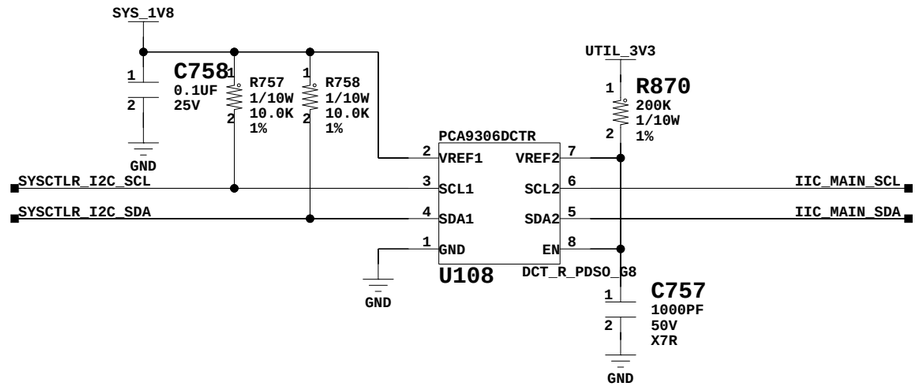
MAXIM PMBUS PROGRAMMING CABLE



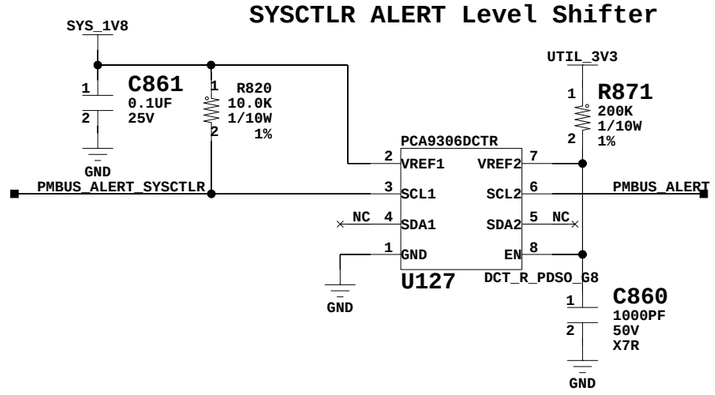
FPGA I2C Level Shifter



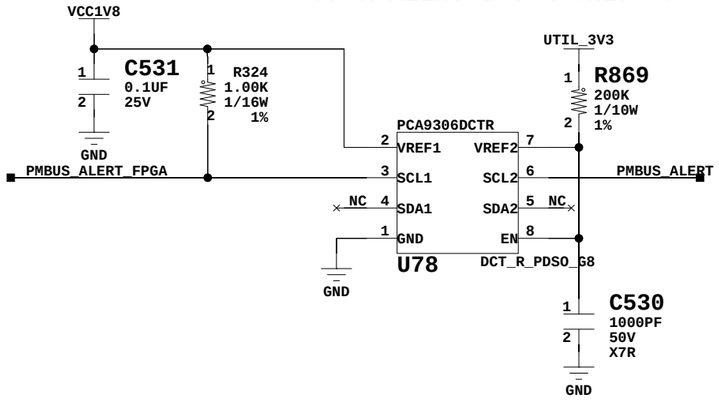
SYSCTLR I2C Level Shifter



SYSCTLR ALERT Level Shifter



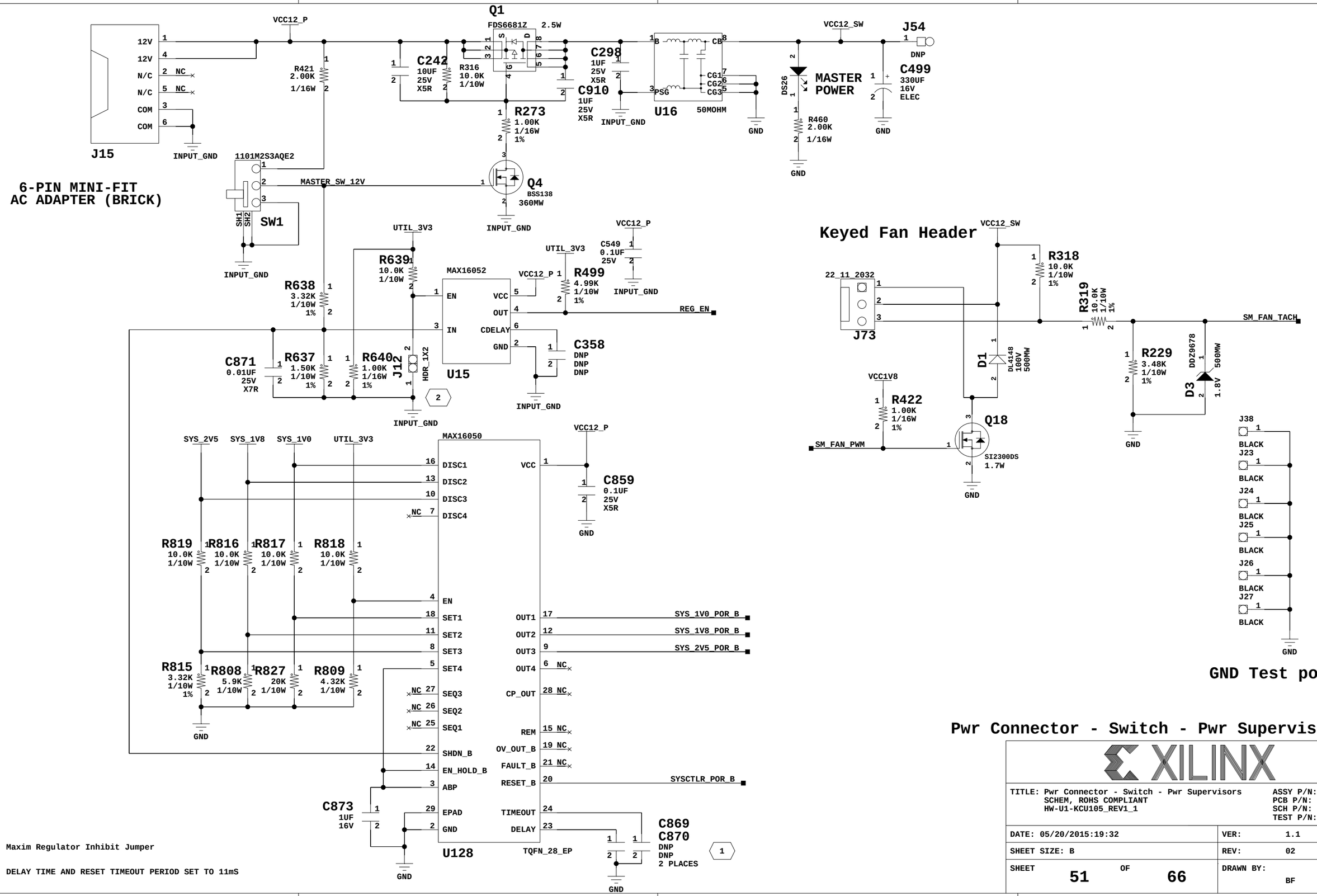
FPGA ALERT Level Shifter



PMBUS Header - I2C Level Shifters

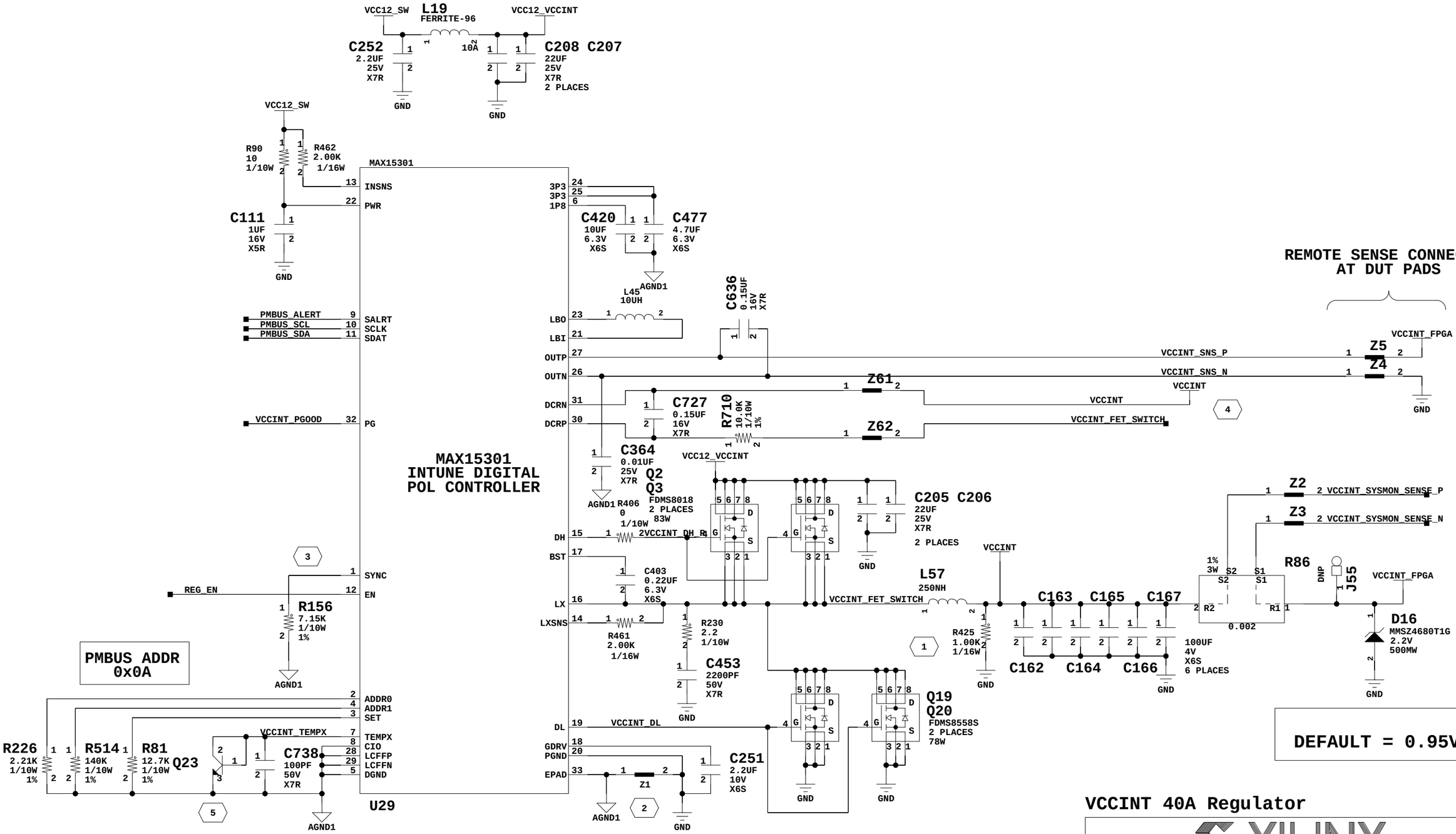
XILINX

TITLE: PMBUS Header - I2C Level Shifters SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 50 OF 66	DRAWN BY: BF



Pwr Connector - Switch - Pwr Supervisors

TITLE: Pwr Connector - Switch - Pwr Supervisors SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 51 OF 66	DRAWN BY: BF



3 VCCINT RAIL SWITCHING FREQUENCY IS 400kHz AND SHOULD NOT BE SYNCHRONIZED TO OTHER LOWER CURRENT RAILS OPERATING AT 600 kHZ.

2 CONNECT AGND TO GND AT OUTPUT CAPACITORS

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

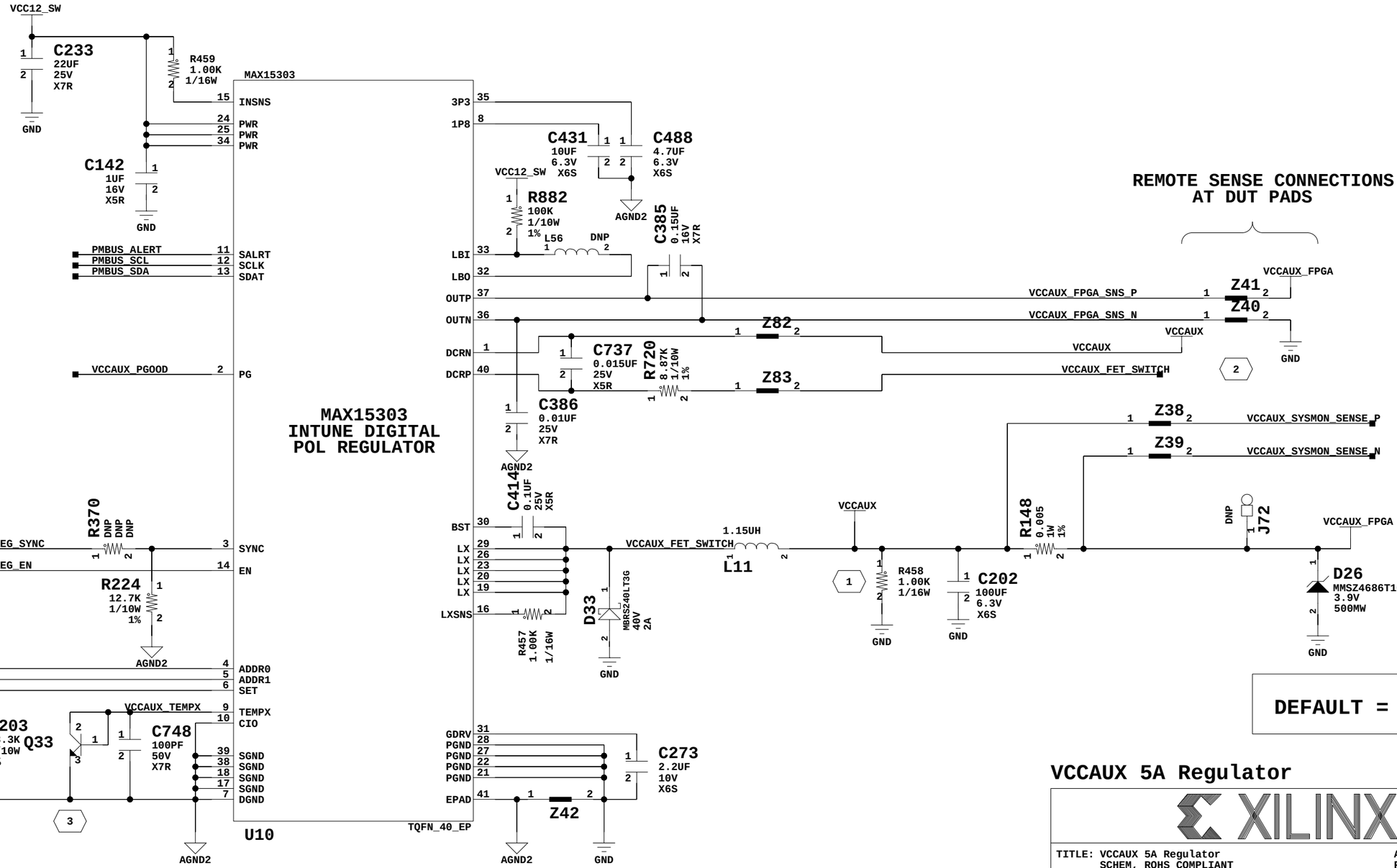
5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

VCCINT 40A Regulator

XILINX

TITLE: VCCINT 40A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 52 OF 66	DRAWN BY: BF



VCCAUX 5A Regulator

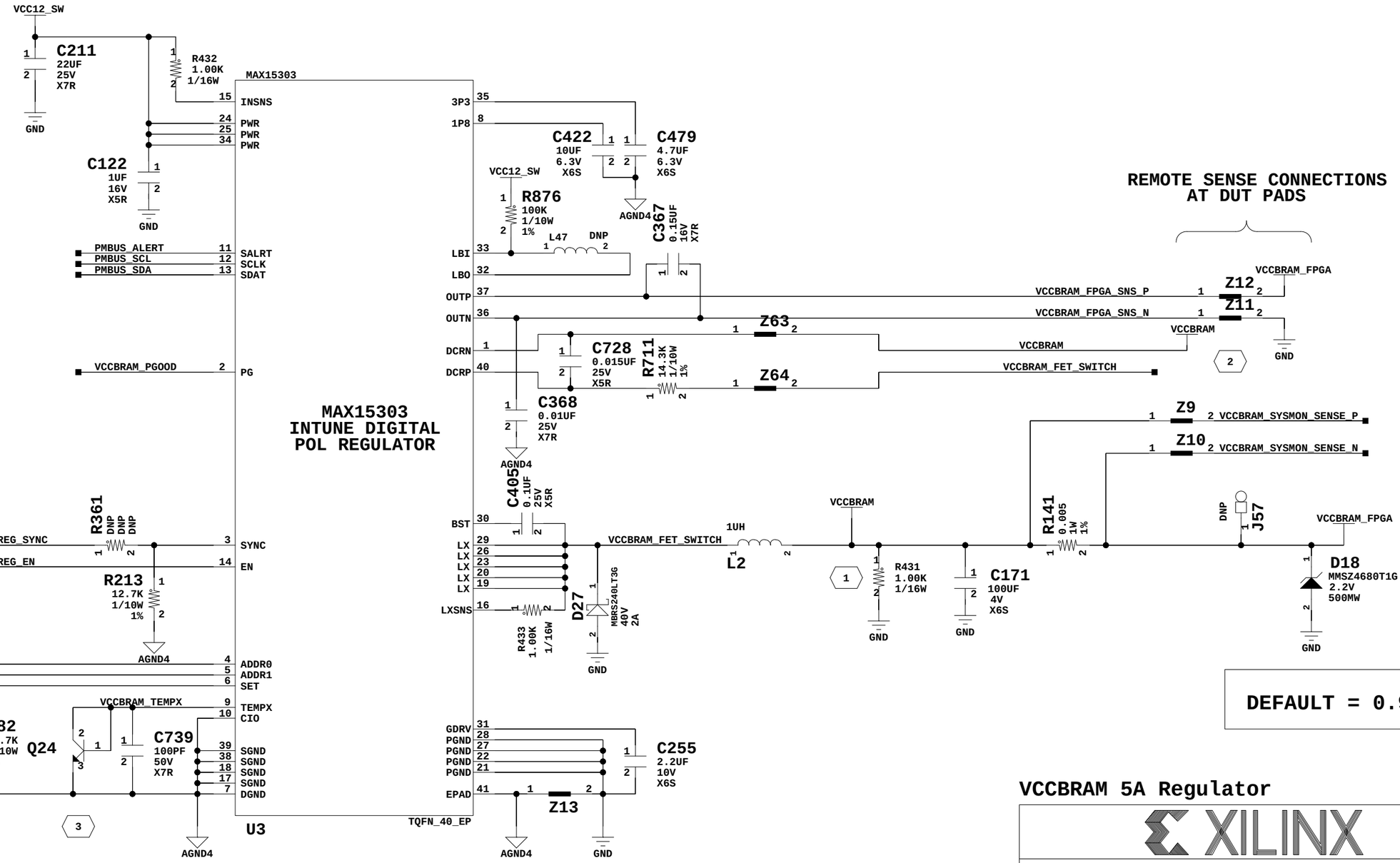
3 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

2 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

XILINX

TITLE: VCCAUX 5A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 53 OF 66	DRAWN BY: BF



3 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

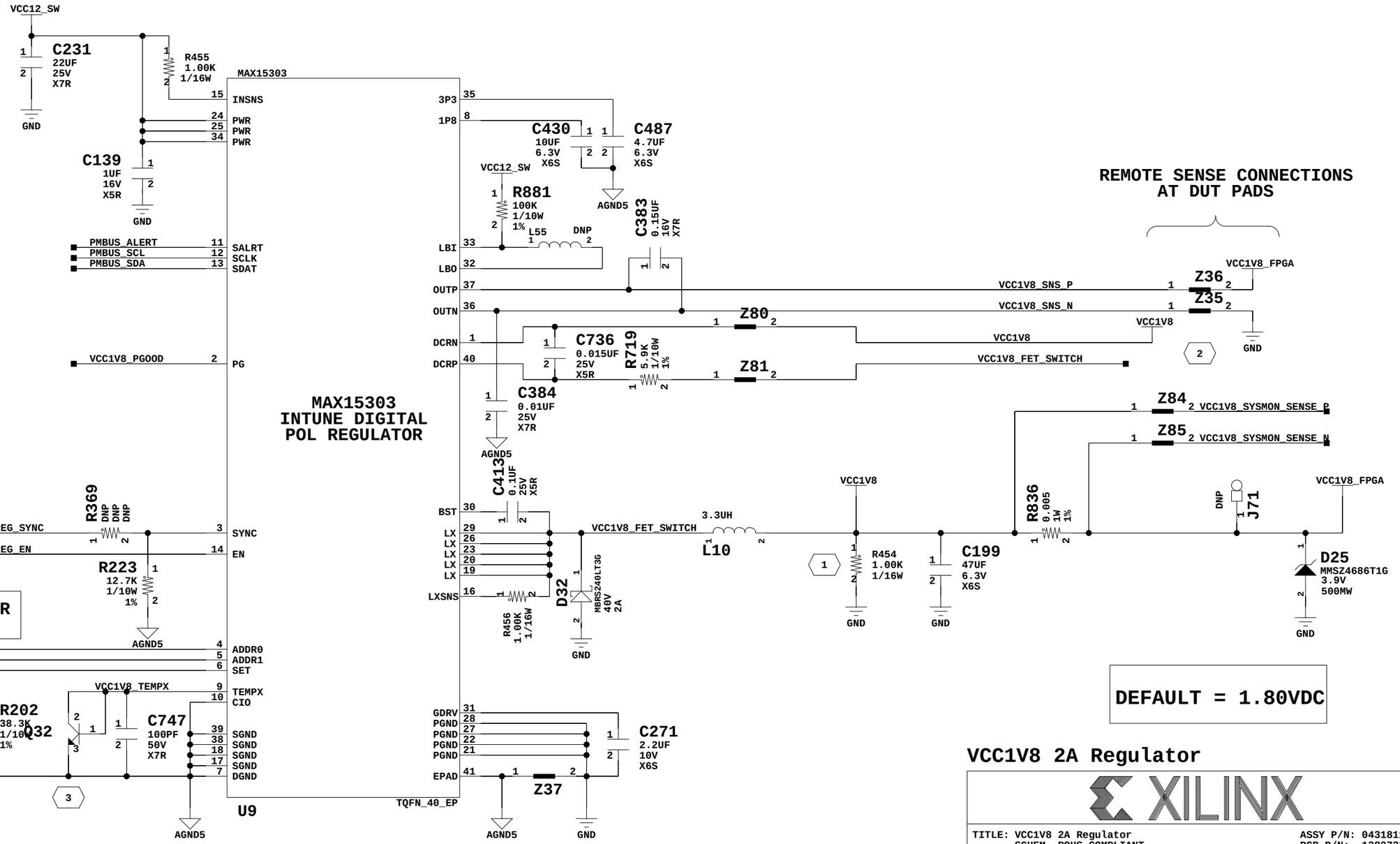
2 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VCCBRAM 5A Regulator

XILINX

TITLE: VCCBRAM 5A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 54 OF 66	DRAWN BY: BF



3 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

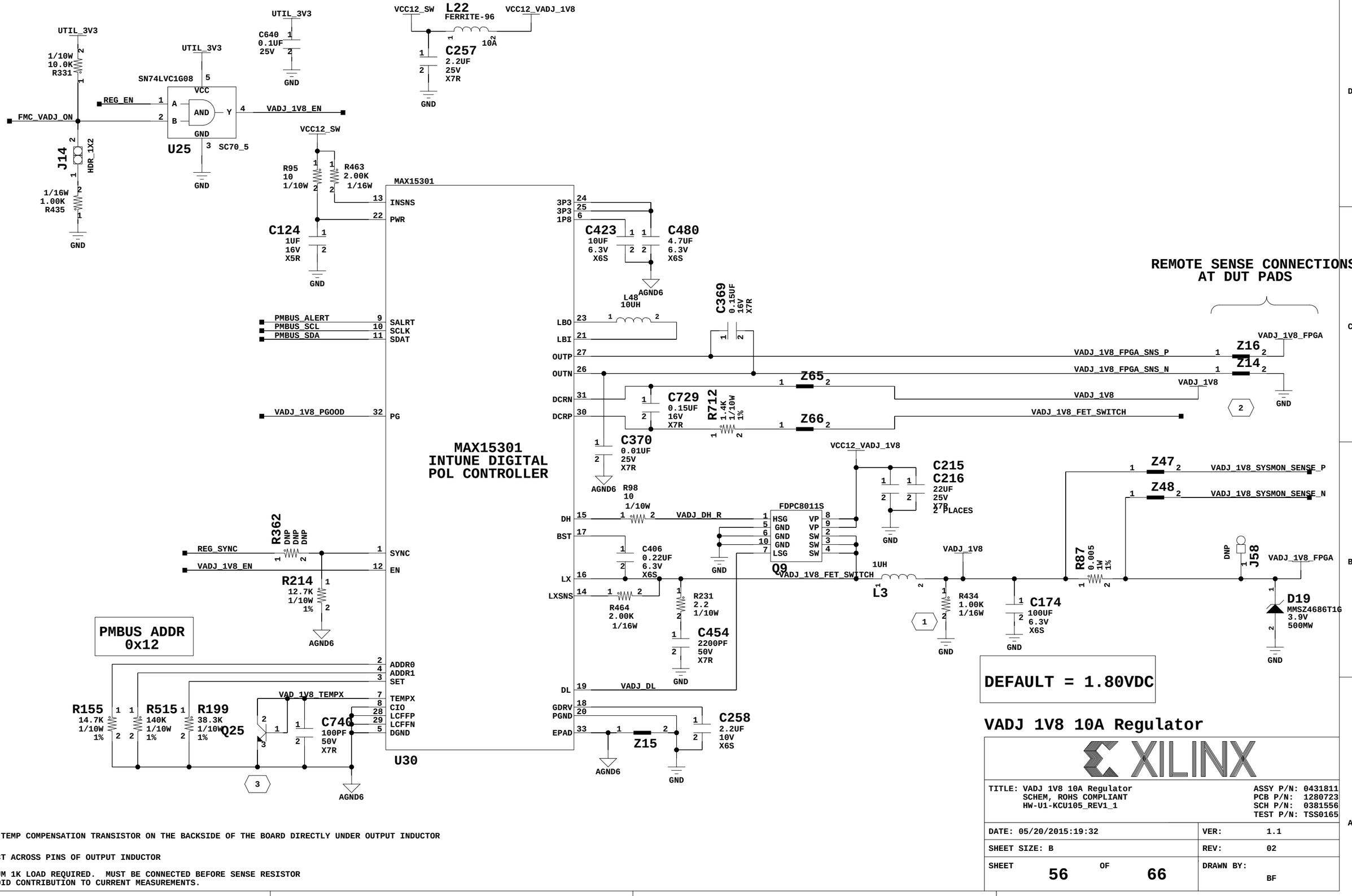
2 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VCC1V8 2A Regulator

XILINX

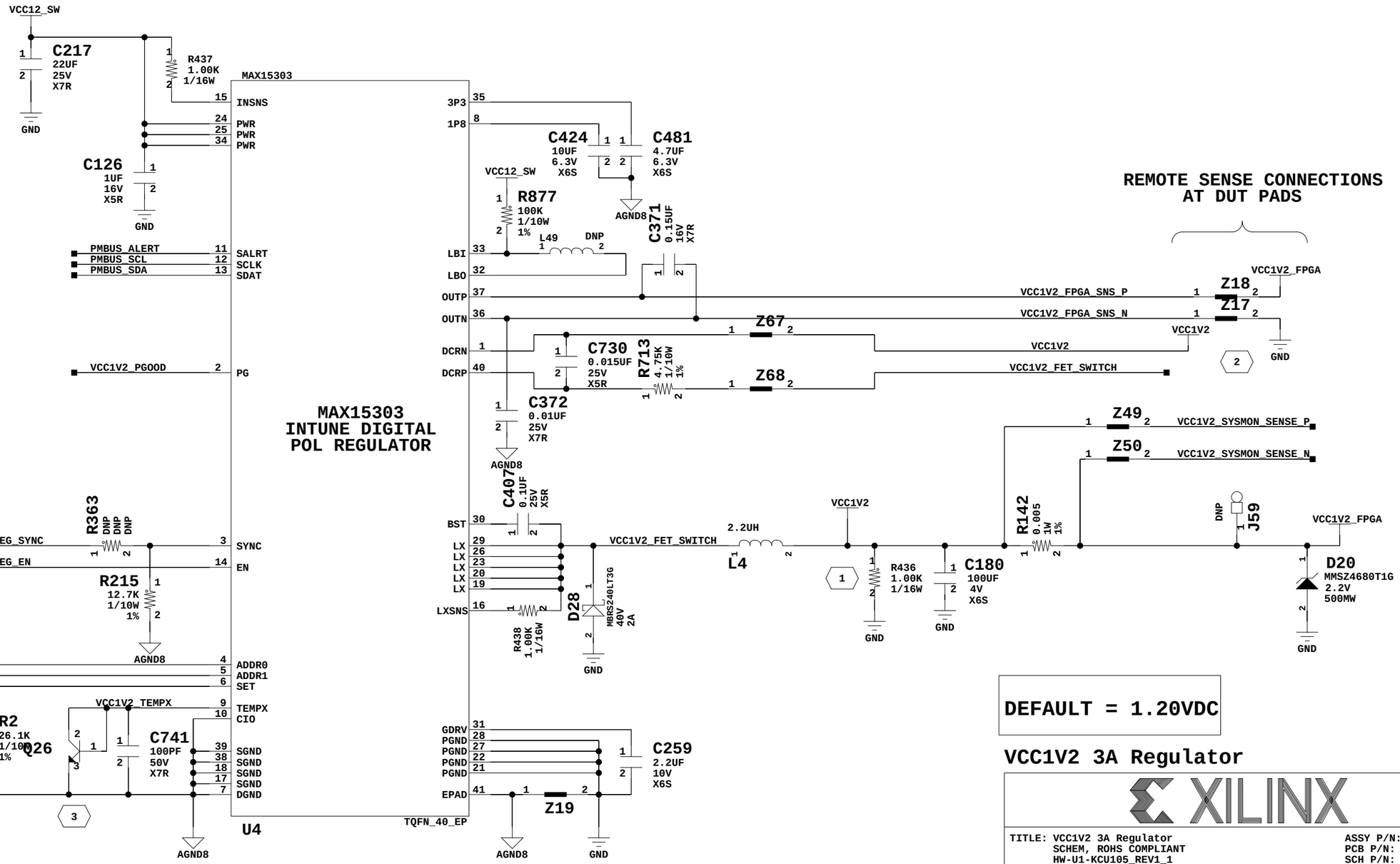
TITLE: VCC1V8 2A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 55 OF 66	DRAWN BY: BF



3 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

2 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

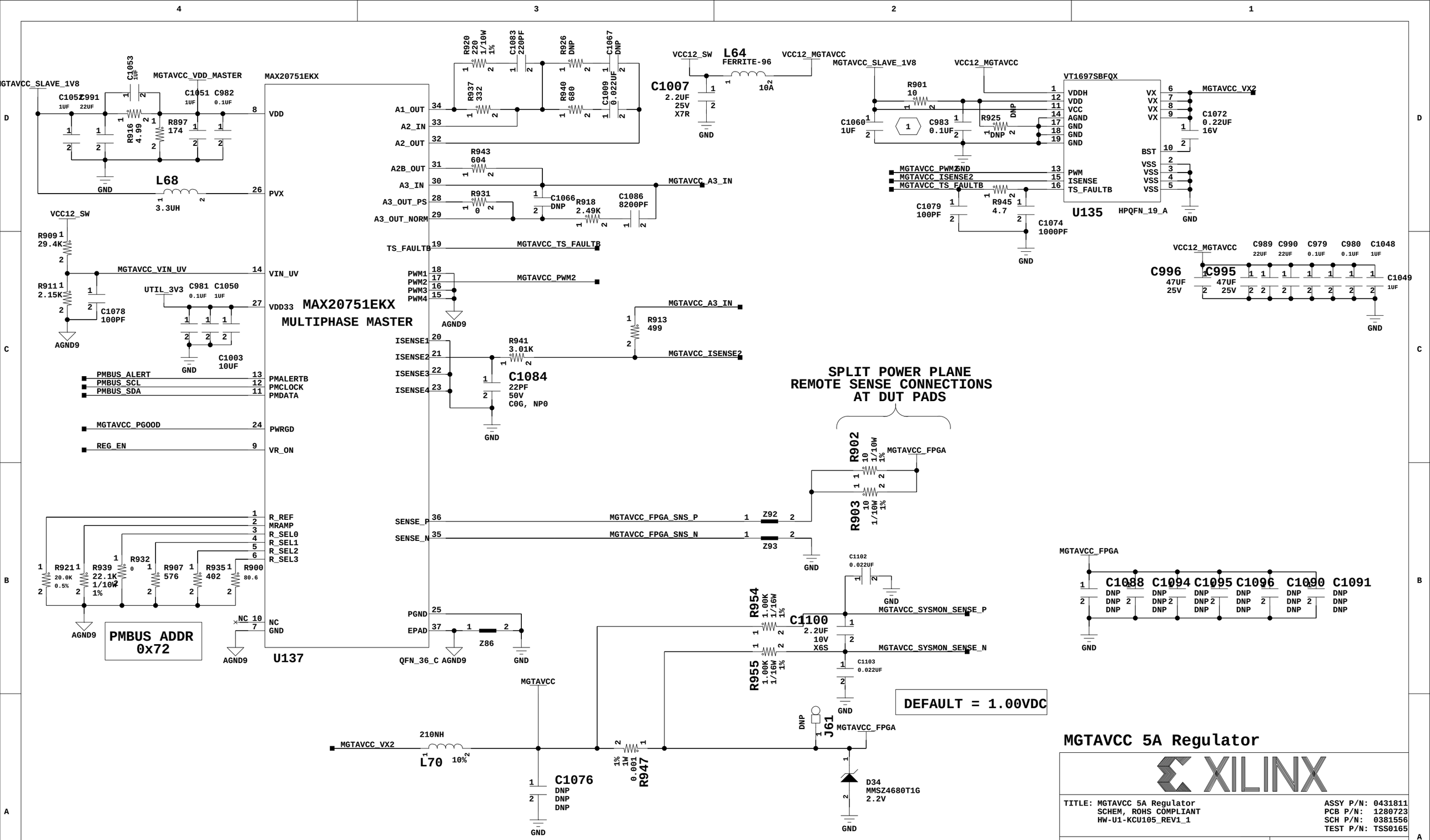
1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.



3 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

2 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.



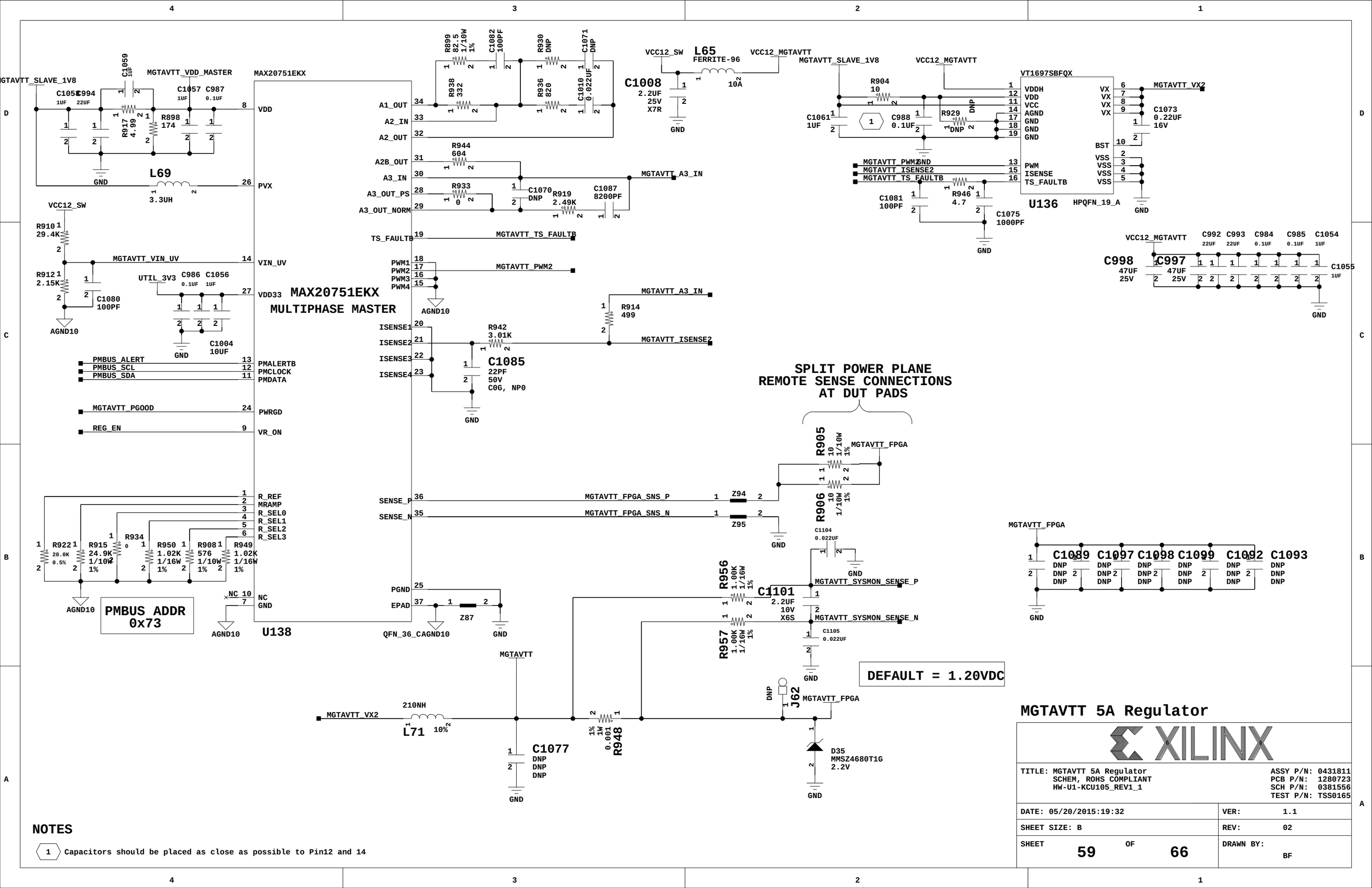
NOTES

1. Capacitors should be placed as close as possible to Pin12 and 14

MGTAVCC 5A Regulator

XILINX

TITLE: MGTAVCC 5A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 58 OF 66	DRAWN BY: BF



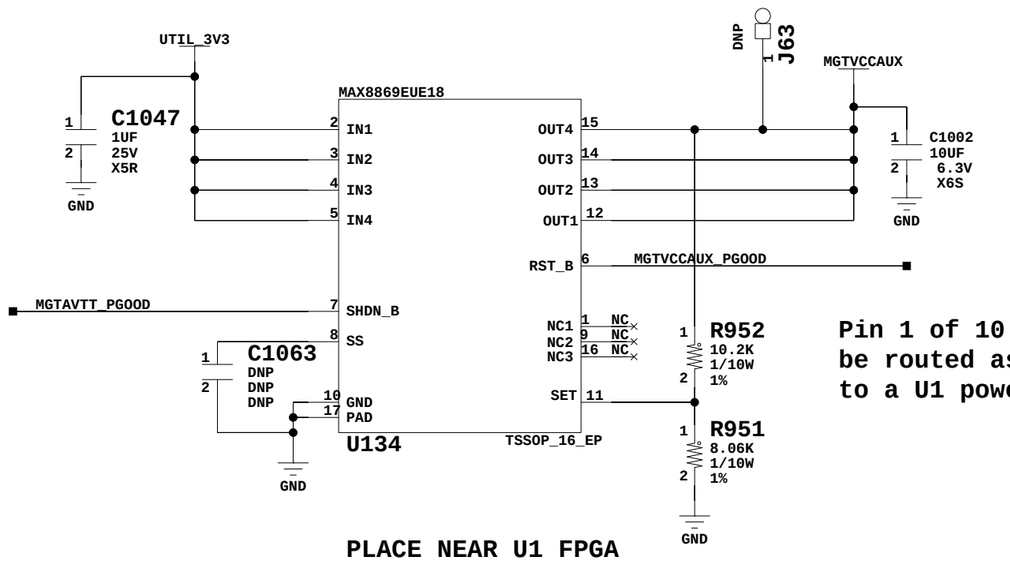
NOTES

1. Capacitors should be placed as close as possible to Pin12 and 14

MGTAVTT 5A Regulator

XILINX

TITLE: MGTAVTT 5A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 59 OF 66	DRAWN BY: BF



Pin 1 of 10.2K resistor must be routed as a sense line directly to a U1 power pin

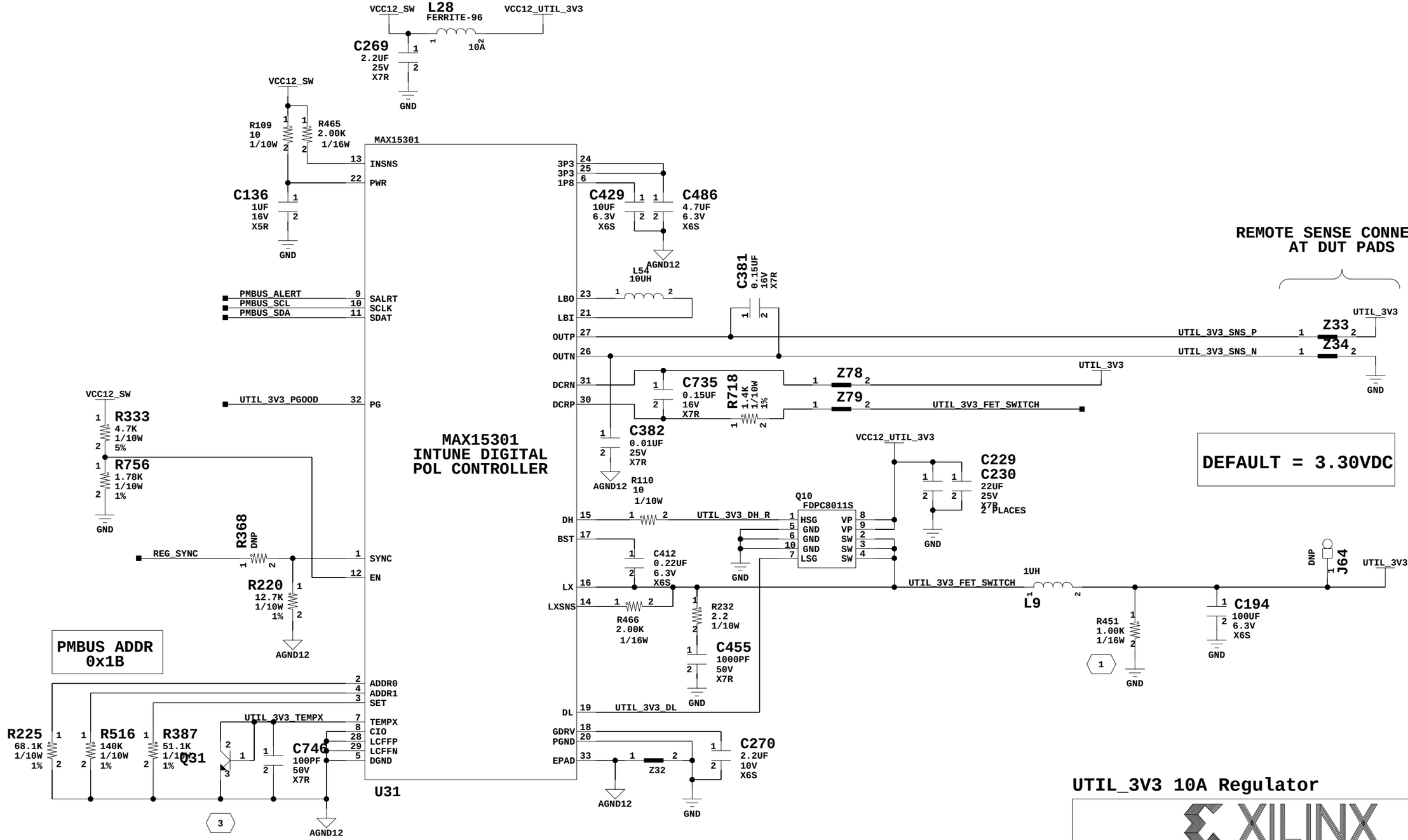
PLACE NEAR U1 FPGA

DEFAULT = 1.80VDC

MGTVCCAUX 1A Regulator

XILINX

TITLE: MGTVCCAUX 1A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 60 OF 66	DRAWN BY: BF



3 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

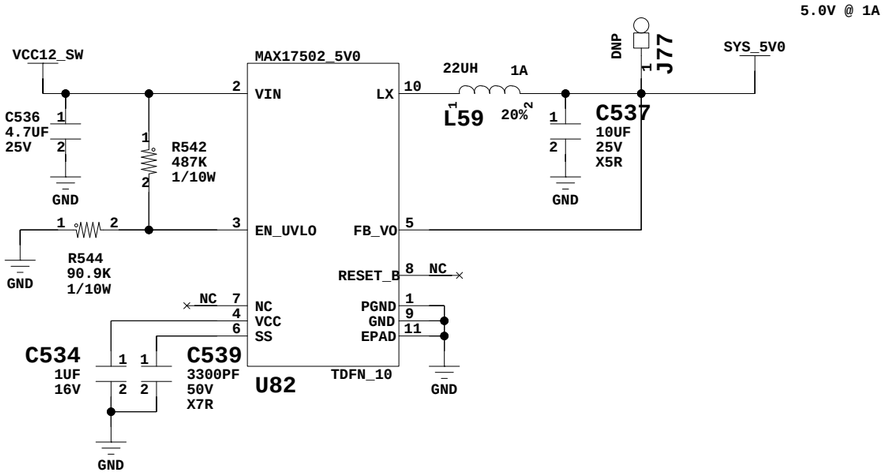
2 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

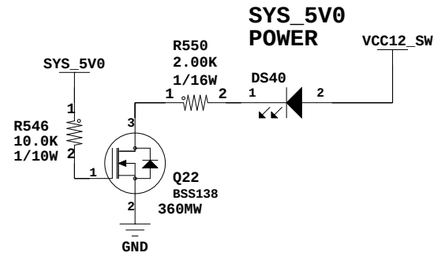
1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

UTIL_3V3 10A Regulator

XILINX

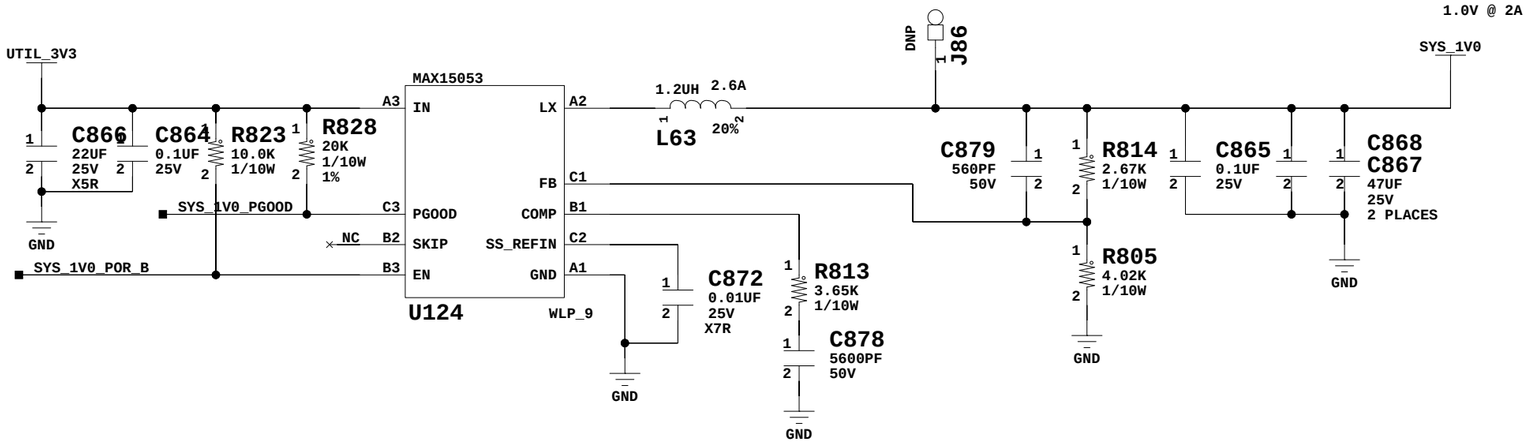
TITLE: UTIL_3V3 10A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 61 OF 66	DRAWN BY: BF

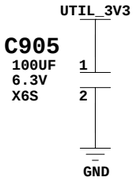




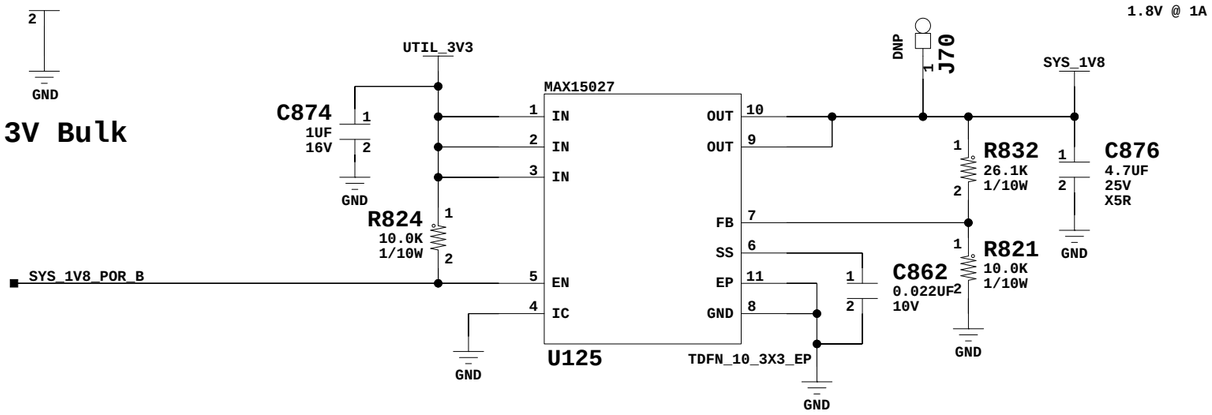
SYS_5V0 Regulator

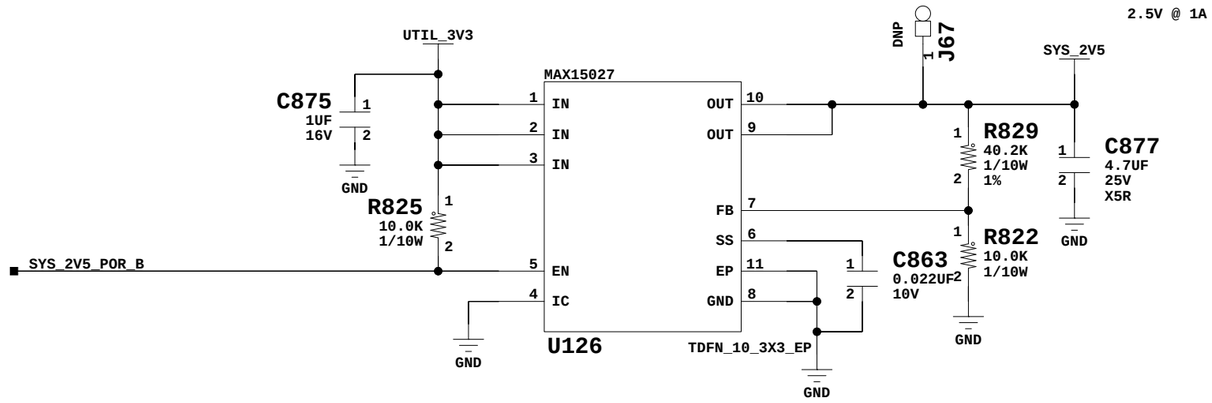
TITLE: SYS_5V0 Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 62 OF 66	DRAWN BY: BF

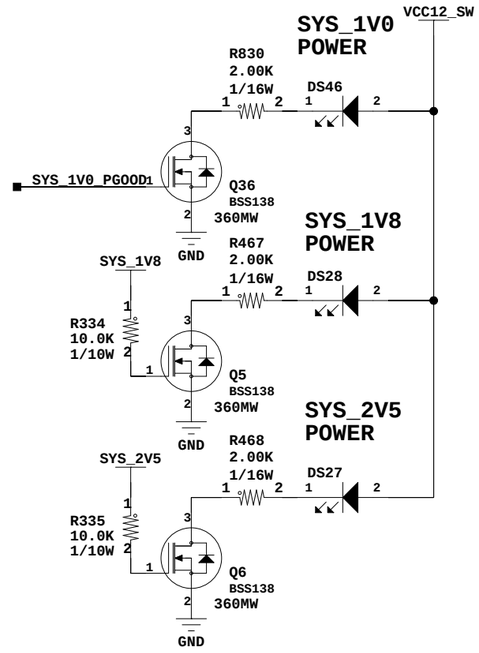




3.3V Bulk



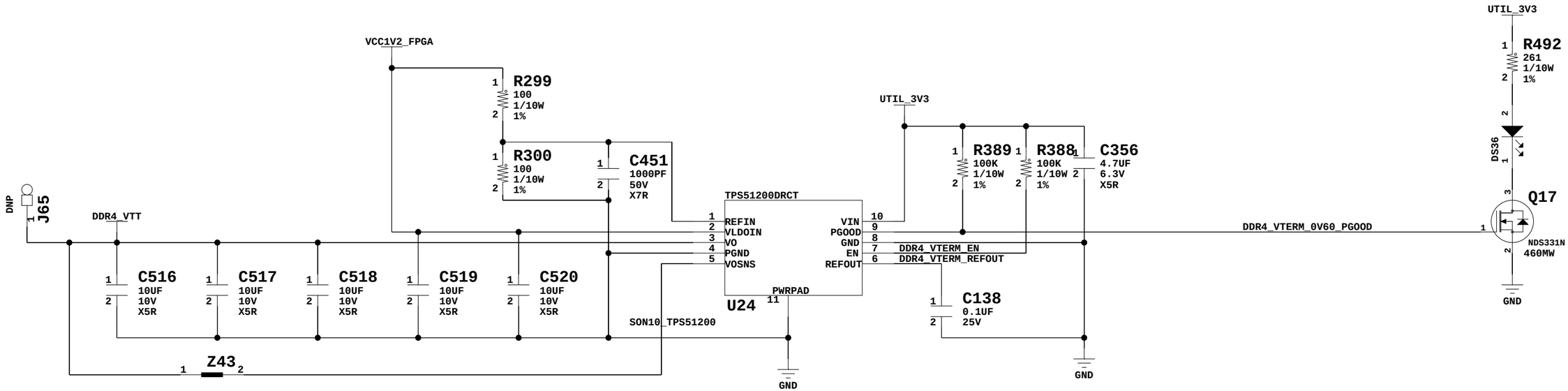




SYS_2V5 SYS_1V8 SYS_1V0 Regulators

XILINX

TITLE: SYS_2V5 SYS_1V8 SYS_1V0 Regulators SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 63 OF 66	DRAWN BY: BF



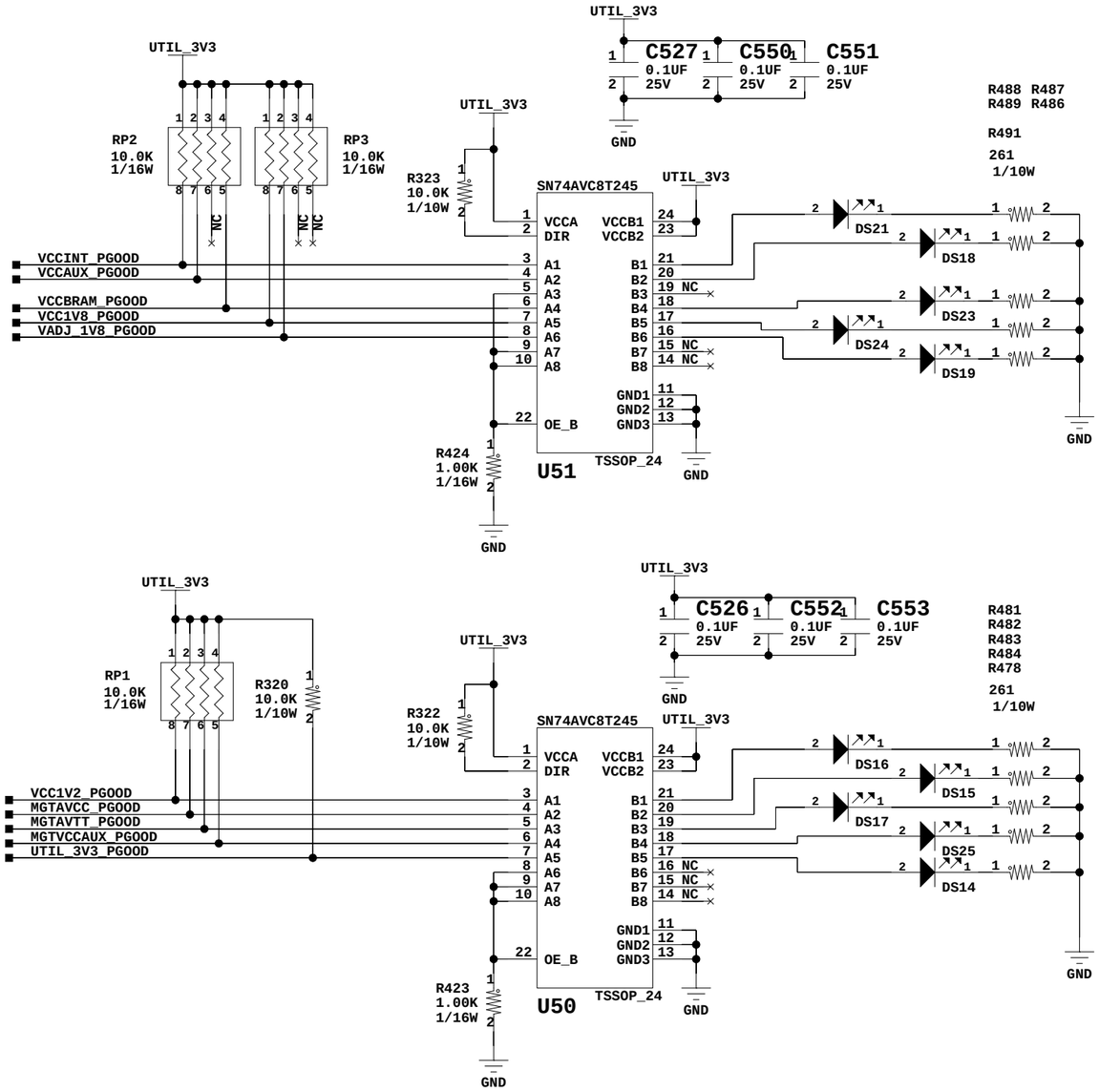
Place sense near DDR4 components

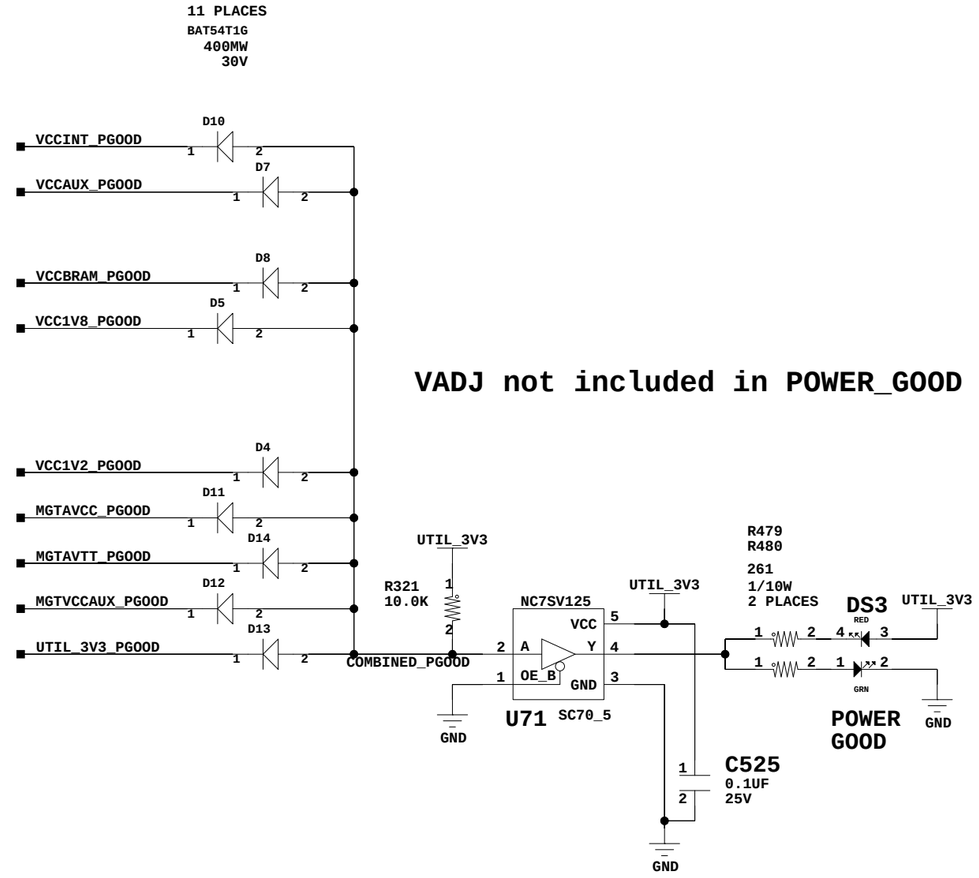
DDR4 Termination Supply

XILINX

TITLE: DDR4 Termination Supply SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 64 OF 66	DRAWN BY: BF

DS19 must be labeled VADJ Power Good





VADJ not included in POWER_GOOD logic

Place LEDs near top right corner of board

Power Status LEDs

XILINX

TITLE: Power Status LEDs SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 65 OF 66	DRAWN BY: BF

HS1
12V Fan / Heatsink
12VDC

MSTK1 0250446
PCIE
POWER
PCIE_POWER_STICKER

CBL1
110V Prong IEC320-C13
PC_POWER_CABLE
Power Cord

PB1
12v Power Brick
PWR_BRICK_12V

CBL2
USB A USB Mini-B
USB Mini-B Cable
USB_MINIB_CABLE

CBL3
USB A USB Mini-B
USB Micro-B Cable
USB_MICRO_CABLE

CBL4
4-Pin ATX Power 6-Pin Molex Mini-fit Jr.
PCIe Adapter Cable
PCIE_ADAPTER_CABLE

PL1
KCU105_PCIE_PLATE

NOTE: These two standoffs are shorter and must be connected to MH4 and MH5 to level the board properly

MS01 MW1 MRB1 MS1 MS2 MH_125_250 MH1 GND
STANDOFF_0P375 WASHER_FLAT_4 RUBBER_BUMPER MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25" MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

NOTE: No standoff foot on MH2

MS3 MH_125_250 MH2 GND
MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

MS02 MW2 MRB2 MS4 MS5 MH_125_250 MH3 GND
STANDOFF_0P375 WASHER_FLAT_4 RUBBER_BUMPER MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25" MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

MS03 MW3 MRB3 MS6 MS7 MH_125_250 MH4 GND
STANDOFF_0P250 WASHER_FLAT_4 RUBBER_BUMPER MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 3/16" MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 3/16"

MS04 MW4 MRB4 MS8 MS9 MH_125_250 MH5 GND
STANDOFF_0P250 WASHER_FLAT_4 RUBBER_BUMPER MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25" MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 3/16"

MS05 MW5 MRB5 MS10 MS11 MH_125_250 MH6 GND
STANDOFF_0P375 WASHER_FLAT_4 RUBBER_BUMPER MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25" MACHINE_SCREW_4-40 #4-40 MACHINE SCREW 0.25"

MJB1 MJB2 MJB3 MJB4 MJB5 MJB6 MJB7 MJB8
JUMPER_BLOCK_2-PIN

MJB9 MJB10 MJB11 MJB12 MJB13 MJB14
JUMPER_BLOCK_2-PIN

Mechanical Components

XILINX

TITLE: Mechanical Components SCHEM, ROHS COMPLIANT HW-U1-KCU105_REV1_1	ASSY P/N: 0431811 PCB P/N: 1280723 SCH P/N: 0381556 TEST P/N: TSS0165
DATE: 05/20/2015:19:32	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 66 OF 66	DRAWN BY: BF