Lab 2: Cadence Tutorial on Layout and DRC/LVS/PEX

Kit Documentation

The IBM design kits include many reference documents available in PDF format. You can access the most relevant of these from the cadence (virtuoso) CIW window. Select IBM_PDK > Document > Design Manual. Under 'Technology' select cmrf8sf and click ok. A PDF document should open called the Design Rule Manual (DRM). If this does not work, the DRM can be accessed directly by typing the following in a terminal window, where % represents the terminal window prompt (i.e. type the text *after* the %).

% acroread ~/eecs413/../../../IBM_PDK/cmrf8sf/V1.8.0.3DM/doc/cmrf8sf.design_manual.pdf

This document contains all of the electrical properties of the devices in the process. It also contains layout design rules and other information about the process. You can find a cross section of the process on page 28.

Introduction

This tutorial describes how to generate a layout view in the Cadence Virtuoso Layout Editor, how to perform layout verification in Calibre, and how to re-simulate your design with extracted parasitics in Spectre. In the first section, you will generate a layout for a simple CMOS inverter. In the second, you will create a buffer using the inverter cell you have created.

When doing layout, a techfile must be attached to the library. This defines layers, parameterized cells (pcells) and other layout-related technology information. This should have been set in Lab 1, but we will double check the techfile. To do this, start virtuoso in your cadence directory.

% cd ~/eecs413/
% module load /afs/umich.edu/class/coe/modules/eecs413/f15
% virtuoso &

Open the Library Manager from the CIW by browsing to

Tools > Library Manager

Right click on the *tutorial* library that was created in tutorial session 1 and choose *Properties*. The techLibname field should read cmrf8sf. If it does not, enter *cmrf8sf* in the textbox for techLibname and click on OK. You have now attached the techfile. In the list of cells, click on *cmos_inverter* (or the name you chose for your inverter in Lab 1), then choose File > New > Cell View.

Select Type field as *layout*, which is the layout editor, as the Tool. The View Name should automatically change to *layout* if you click in a different field. Click Ok and a Virtuoso Layout window will now open. You might see an error window about undefined packets – this should be ok. Click 'Yes'.

Before entering any layout, set the grid by browsing to Options > Display (or press the shortcut key 'e') and changing the X and Y Snap Spacings to 0.02 and click on Ok. Toggle Gravity OFF by typing the "g" key. Look at the CIW (main Cadence window) print-out to check the status of Gravity. With Gravity on, the cursor will snap to objects, making it difficult to perform portions of the layout entry.

Layout: Creating Devices

Begin by adding an instance of an nfet transistor from the cmrf8sf library. This is done by choosing

Create > Instance (or press the shortcut key 'i')

in the layout window. Browse the cmrf8sf library and select nfet cell, with the layout view. The Create Instance window will now show parameters specific to this cell. In order to set the dimensions of this nfet to match the cmos_inverter schematic created in the first tutorial, change the width to 500nm and the length to 120nm in the parameter field. Place an instance of this cell by moving the cursor over the layout window and clicking LMB. Now, browse for the pfet cell in the same way. Change the width to 2µm and the length to 120nm. Scroll down in the 'Add Instance' window and enable 'Add NW contact?'. This places a bulk connection automatically. Add the instance of this pfet to the layout. If you have already placed the device, you can access these properties by selecting the transistor, pressing 'q' and clicking on the 'parameter' radio button at the top.

Other than width and length, you don't need to consider the other parameters in the Create Instance pop-up for this lab. You may find occasional use for the *number of fingers* parameter. This is useful in generating layout for wide transistors by instantiating multiple devices (for eventual parallel connection) whose individual widths add to the total intended width.

To see the complete layouts for the instantiated devices, press Shift-f. This changes 'Display Levels-Stop' in 'Display Options' (shortcut key 'e') to 32. If you later wish to view only the top-level layout data, press Ctrl-f.

Layers

At this point you can see a variety of shapes on different layers that form the nfet and pfet cells. You will use some of these layers when connecting terminals of the devices and adding pins. The complete set of layers available to you is shown in the LSW window which automatically appears when opening a layout view. The primary layers you'll be using are described in Table 1:

Table 1: Mask Layers (as seen in LSW)	**Layer Name**	**Color**	**Primary Function**
M1	Metal 1	Blue	first level of metal used for device interconnection
PC	Poly	bright red	forms transistor gate when crossing diffusion; short interconnect
RX	Diffusion	Green	defines active areas for transistor formation as well as substrate and well contacts *RX by itself defines N^+ region* *RX enclosed by BP defines P^+ region*
CA	Contact	yellow (densely dotted, always square), intersects M1	defines oxide cut for M1 connections to RX or PC
NW	N-Well	yellow (less densely dotted)	pfet devices will reside in n-well
BP	P+ implant	dark red/brown	defines p+ regions for pfets and substrate contacts
V1	Via	yellow (similar to CA, duller)	defines oxide cut for M2 connections to M1
M2	Metal 2	Purple	second level of metal used for further connections

The IBM 0.13µm kit supports up to 8 levels of metal for interconnect, each with a respective via to the layer below. The process has different versions which use anywhere as few as 5 of the 8 available metal layers. This information is not relevant right now. When designing circuits that will be fabricated, knowing the exact process flow is important.

Design Rules

There are various inter/intralayer rules to follow when performing layout to ensure reliable fabrication of the circuit. A list of these design rules can be found in Section 3 of the Design Rule Manual (DRM) that you browsed to above.

There are many rules for this technology but only some are relevant to your designs. You will probably spend more time to complete your first few layouts, since you are still learning the most common rules. Each layer will have minimum width and spacing associated with it. Vias and contacts each have fixed

dimensions. There are also spacing rules between shapes on different layers (e.g. diffusion to n-well edge, metal overlap of contact, etc.).

Layout: Interconnect and Pins

There are many ways to go about placing the nfet and pfet and wiring the terminals together to form the inverter layout. One way to do this is shown in Figure 1. Vdd runs horizontally on top in M1. Gnd is on the bottom, running horizontally in M1. Vin comes in from the left and vout comes out from the right, both in M1. Use this example for your layout. Don't be concerned about matching the dimensions. You can move the devices instances (or any other object you create) by first selecting the device with the LMB, then clicking on the Move icon (or shortcut 'm'). You will be prompted for a reference point for the move. Click the LMB on the layout window then move the cursor. You will see a ghost image of the object being moved. Click LMB once again to complete the move. You can set the edit snap mode by typing the 'e' key in the layout window. anyAngle and orthogonal are commonly used settings in Display Options dialog box. Orthogonal is recommended for most editing.

Other selected-object edit operations of interest include copy, delete, property modification and rotate. Copy, delete and property modification all have associated icons. A common use of property modification would be to change the width or length parameter of a device that has already been instantiated. For rotate, select the instance then:

Edit > Rotate (or type the 'Shift-o' key).

There are three ways to enter layout shapes: rectangle, polygon or path. Each has an associated icon. Experiment with each by first selecting the active layer in the LSW window. Do this by clicking with the LMB on the layer you wish to enter. For most layers, you'll see multiple layer subtypes in the LSW. Use the **drw** (drawing) subtype for drawing all of the shapes in your layout. Use the label (**lbl**) subtype to designate pins. *Whenever you have an active command (e.g. Move, Copy, Path, Rectangle), hit F3 to activate the options window for the command.*

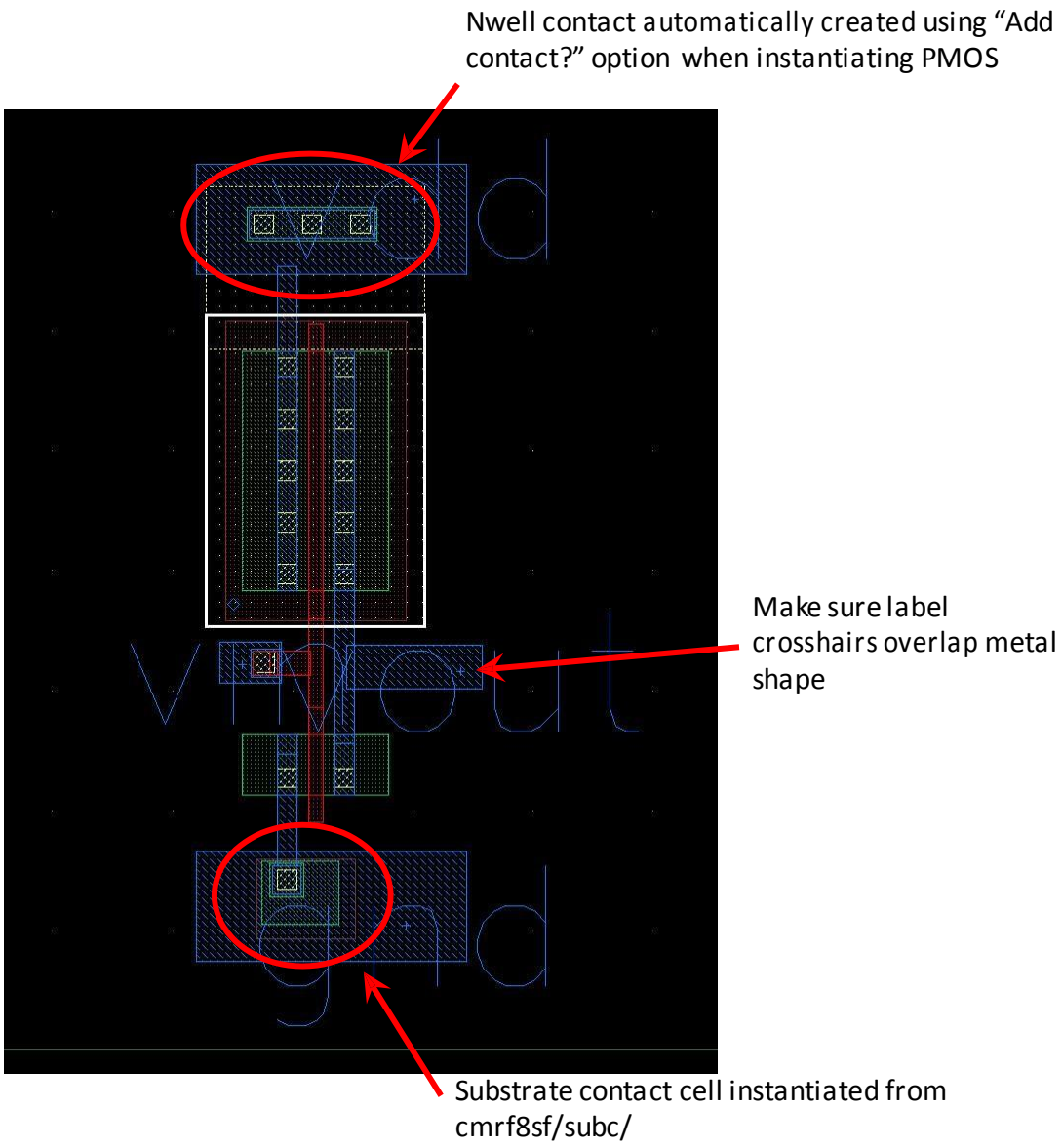


Figure 1. Example Inverter Layout

Using the LSW, you can turn viewing and/or selection on or off for any layer. To toggle viewing for a specific layer (other than the active layer), click with the MMB on the layer. To toggle selection, click with the RMB. You can also toggle viewing and selection for all layers with the AV/NV/AS/NS buttons near the top of the LSW. Type Ctrl-r in the layout window to redraw the window with the new settings.

The ruler can be used to measure distances in the layout window. This is especially useful when considering design rules. You can activate the ruler by clicking on its icon or pressing the 'k' key. Then LMB click on the start and end points. Clear rulers with Window > Clear All Rulers or type 'Shift'+'k'.

Using the above techniques, move the nfet and pfet to approximate the placement in Figure 1. *Make sure*

*to **read past this section** for complete instructions on how to complete your layout.* Draw a PC rectangle (shortcut 'r') to connect the gates and draw M1 rectangles or paths for vdd, gnd and out connections for the devices sources and drains. The nwell contact should be connected to vdd as well. Unlike nwell contacts, substrate contacts are created separate from the device instantiation. To create a substrate (p+) contact, you need to instantiate the subc cell from the cmrf8sf library. The default size is large, so you should edit the properties to make it something reasonable (and the numbers must be matched in the schematic). The subc cell has all the layers that an n+ contact has plus BP to make the diffusion P+. You will need to add the subc cell into your schematic as well. The purpose of this cell is to model resistance between the bulk connection of your NMOS devices and the cell ground. Place the cell as shown in figure 2, and edit the properties to match what you placed in the layout.

The input in Figure 1 is in M1. You can create a contact from M1 to PC by choosing:

Create > Via

Set the Via Definition to be VPC_M1 (poly to metal1) and place the contact such that it touches the PC shape. Next, draw the horizontal M1 for vin.

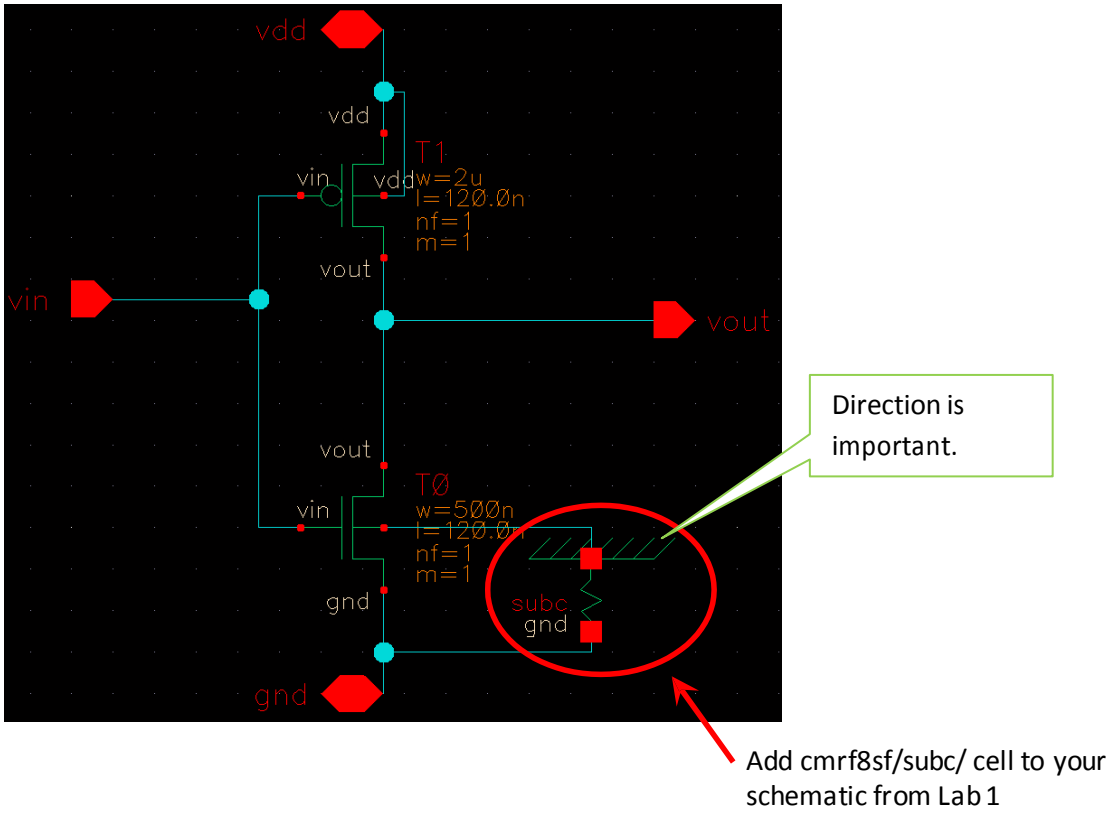


Figure 2. Sample schematic with subc cell placed

The final step is to add pins to the layout. Pins will be used as initial correspondence points in the layout

vs. schematic check. You can see the pins in Figure 1. They are the small M1 squares you see on vdd, gnd, vin and vout. Follow these instructions carefully to ensure that the pins extract correctly later during LVS.

1. Select the appropriate layer in the LSW. For example, if you want to place a pin on a piece of M1 you would select the M1 – label (lbl) layer in the LSW. For M2 you would select M2 – label (lbl), etc.
2. Create the pin with Create > Pin (or shortcut Ctrl+'p').
3. Select 'Display Terminal Name', and click on the "display pin name options..." button. In the new window select 'pin layer' and click OK.
4. Make sure that I/O Type matches the I/O type in schematic (i.e. input, output, inout).
5. Type the name of the pin in the 'Terminal Names' field.
6. Switch the active window to your layout by either clicking on the window title bar or Alt-tab. Single click where you want the upper left corner of the pin to be (must be inside the metal drawing layer in the layout), then single click where you want the lower right corner of the pin to be (must be inside the metal drawing layer), and then single click inside of the rectangle to place the pin name. If you cannot see the pin name turn on pin name display in Display Options ("e" key) in order to see displayable pin names.
7. Repeat the steps above to create pins for vin, vout, gnd, and vdd.

Design Rule Check (DRC)

To check if your layout violates any of the design rules, run Calibre DRC by selecting:

Calibre > Run DRC

Calibre will ask for a runset file to load. Browse to the file

/afs/umich.edu/class/eecs413/f15/student/uniqname/cadence/IBM13.drc

and click OK. The first time you might get a warning about a directory not existing. Click yes to create this directory. The Calibre DRC interface will now open. You will see a few tabs on the left hand side that will lead you to different configuration sections. As you become more familiar with DRC/LVS you will be able to make more use of the capabilities of the design tools. Click 'Run DRC' to run the check. A new window labeled DRC RVE will pop-up with a list of violations. The list will contain different rules (i.e. RULE_XX) and when you click on each rule you will see a list of coordinates for where the rule is violated. An example window is show in figure 3. You will also see a brief verbal description of the rule. More detailed descriptions, often with picture representations of the rule, can be found in the design rule manual (DRM). If you double click on an instance of rule violation, a marker will show up in the layout. This marker is often useful for spacing rule violations. Correcting DRC errors is often an iterative process. Sometimes fixing errors can create new ones. After fixing errors, rerun DRC to

confirm the errors have been resolved. When you rerun DRC, you may be asked about overwriting a file – this is ok. A passing DRC window will look like figure 4, except there will be lots of green checks. Once you've corrected all violations, move on to the next section to run layout vs. schematic (LVS).

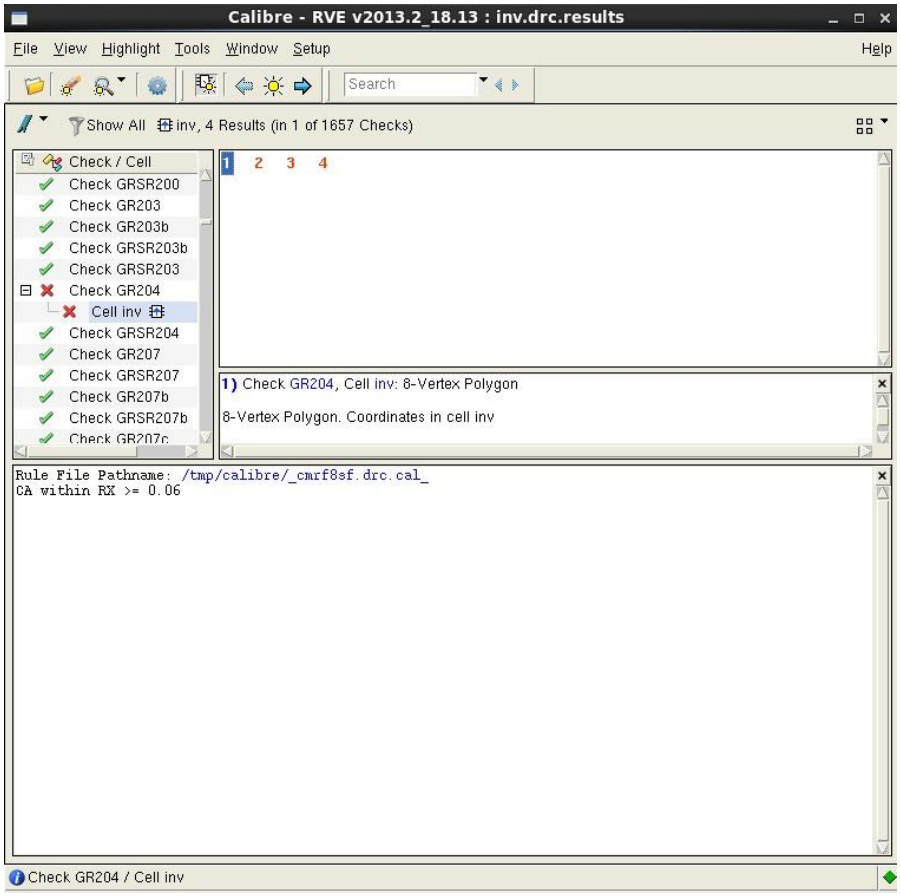


Figure 3. Example Calibre DRC RVE Window

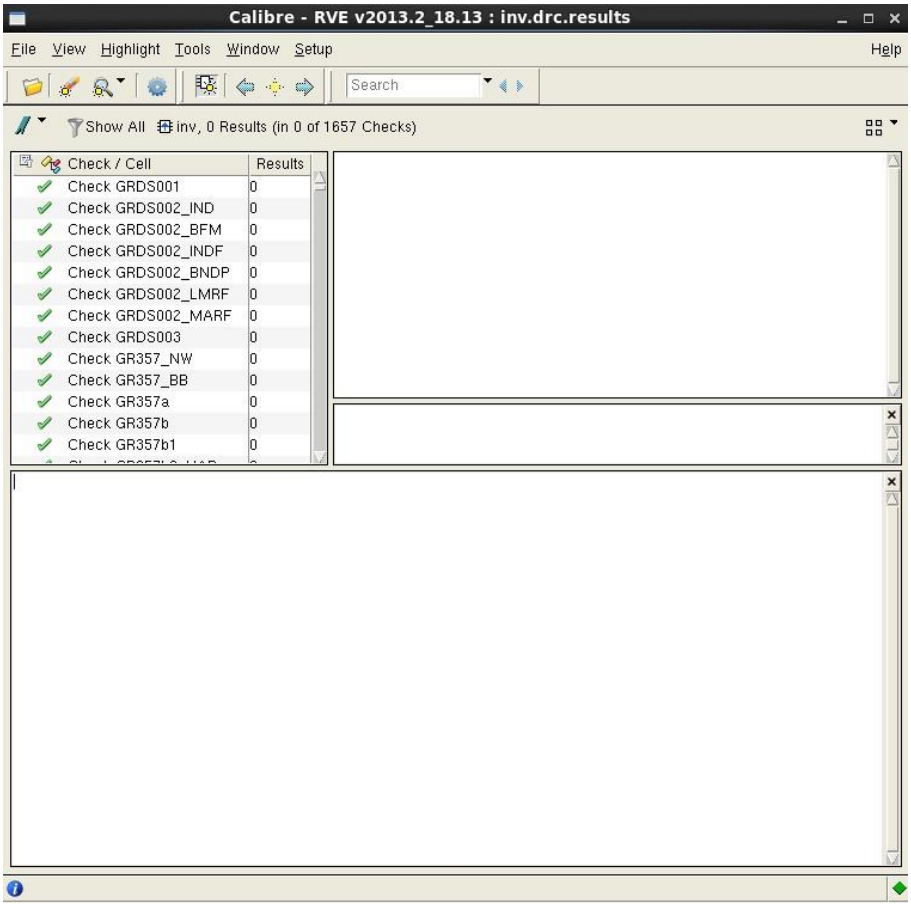


Figure 4. Example Calibre DRC RVE Window

LVS

Your layout can be DRC clean, but will not perform as expected if it does not match the schematic. For example, if you forgot to connect the pfet gate to the nfet gate, your inverter will not work, even if it passed DRC. Once you've saved your schematic, run LVS by selecting:

Calibre > LVS

Similar to when opening DRC, a configuration window will open. A window asking for a runset file will then open. Browse to the file

/afs/umich.edu/class/eecs413/f15/student/uniqname/cadence/IBM13.lvs

and click OK. The first time you might get a warning about a directory not existing. Click yes to create this directory. The Calibre LVS interface will now open. Click on Run LVS. The LVS RVE window will popup showing you mismatches between the schematic and layout (if any). A successful LVS output is shown in figure 5. If you encounter any problems in LVS, you can see a LVS output depicted in figure 6. LVS will check that all devices are connected in the same manner and that they have the same width and length parameters. Top-level pins or terminals are checked as well. LVS problems can

be difficult to debug. You may find it helpful to view the netlists that are being compared. They can be found in the LVS RVE on the left side under “Source Netlist” (schematic) and “Layout Netlist” (layout extracted netlist). When rerunning LVS you may get two windows about overwriting schematic and layout netlists – click OK.

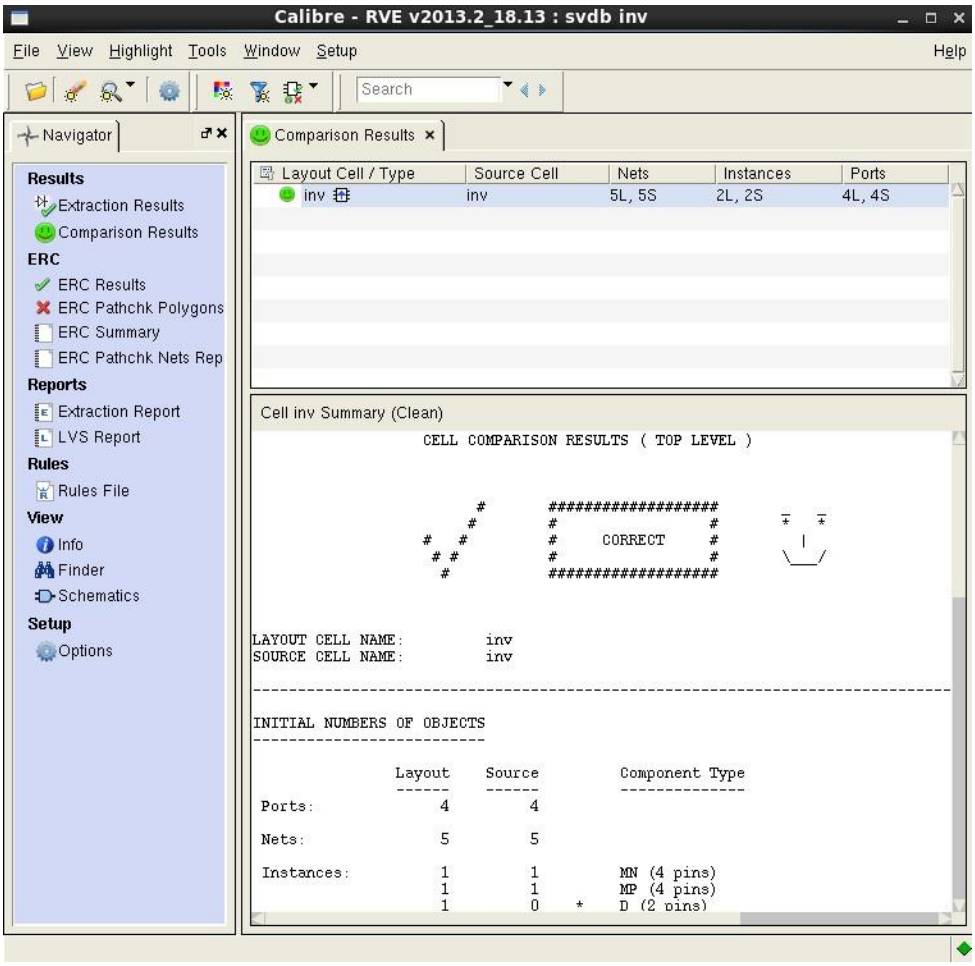


Figure 5. Example Calibre Correct LVS RVE Window

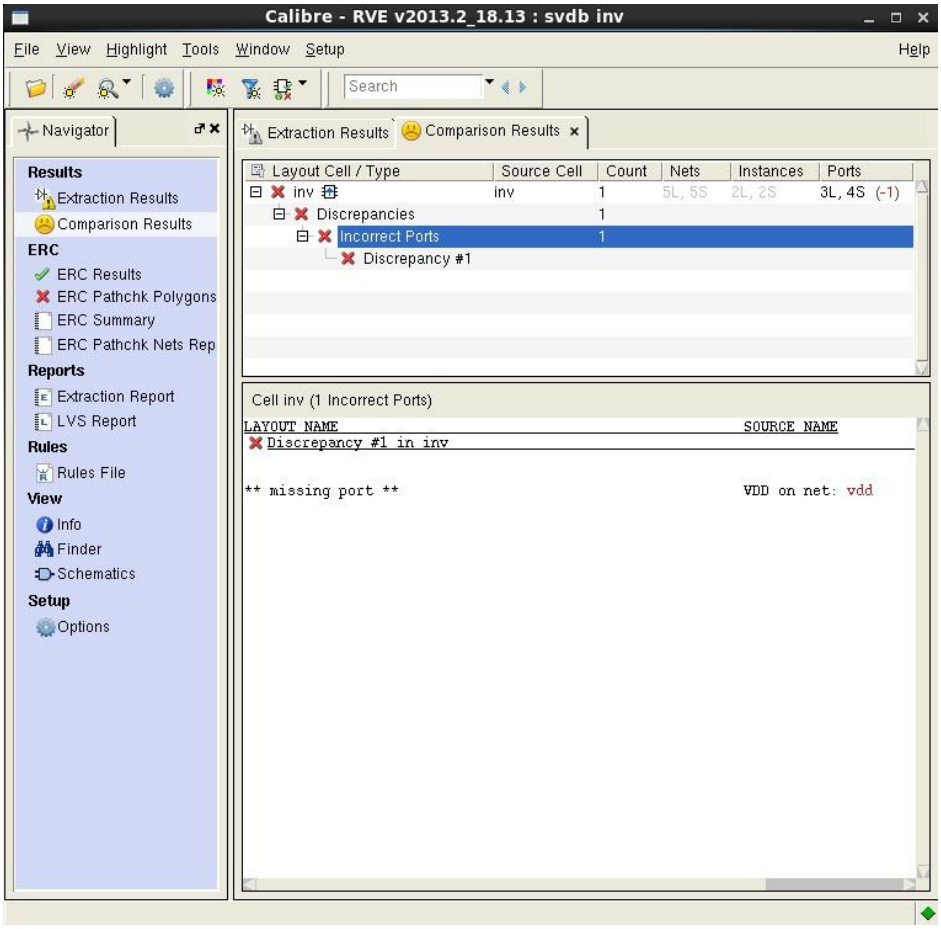


Figure 6. Example Calibre Incorrect LVS RVE Window

PEX

This section describes how to extract a netlist from your layout that includes parasitic resistances and capacitances. You will then be able to re-simulate your design with extracted parasitics in Spectre. PEX requires a clean LVS so that extracted parasitics can be correlated to nets on the schematic. Initiate the PEX interface by clicking on:

Calibre > Run PEX

A window asking to load a runset file will now appear. Browse to the file

/afs/umich.edu/class/eecs413/f15/student/uniqname/cadence/IBM13.pex

You will notice that the interface is similar to the DRC and LVS views. All the settings should be correct. Check Input tab on the left, and in Layout tab click 'Export from layout viewer' and in Netlist tab click 'Export from schematic viewer' (Figure 10 (b)&(c)). In addition, in the Outputs tab on the left to make sure that 'Format' is set to CALIBREVIEW (Figure 10 (d)). Also, at the top of this

window you will see options for Extraction Type. Typically you will use Transistor Level and not extract inductance. However it is common to use different forms of RC extraction depending on the type of simulation you will be running. Suppose there are 2 nodes, A and B. Figure 7 shows what R's and C's the different options will extract (R, C, and Cc).

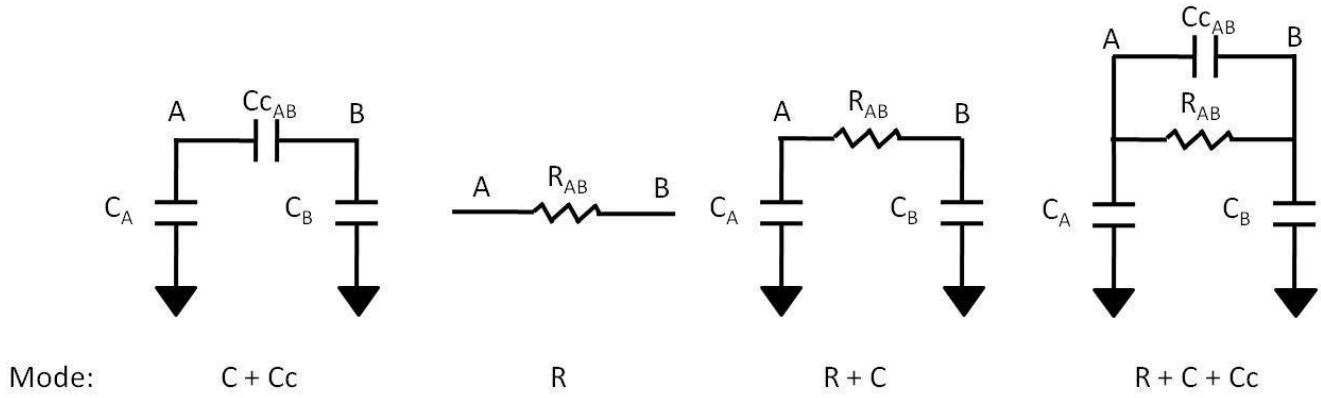


Figure 7. Different Types of RC Extraction

Essentially 'R' means that resistances between all nodes are extracted. 'C' means that a lumped parasitic capacitance is extracted to ground. This means that all parasitic capacitances on that node are summed together and connected to ground. This approach helps simplify the extracted netlist and is useful when you have a lot of DC bias lines (i.e. AC ground) around a node and you are interested in the effect of that capacitance. 'Cc' is the most complex type of capacitance to extract and a coupling capacitor is extracted for every pair of nodes. There are many more options you may explore in PEX including only extracting parasitics for a few nodes instead of every node and changing the lumped reference node (i.e. instead of ground you can have C_A and C_B connect to some other node).

For this tutorial we use the default options. Then, check the PEX options tab on the left and select include tab, then browse the rule file

/afs/umich.edu/class/eecs413/f15/IBM_PDK/cmrf8sf/V1.8.0.3DM/Calibre/xRC/cmrf8sf_8LM_323_detailed.xrc.cal

Make sure you have checked 'Include Rule Files After Main PEX Rules File' (Figure 10(e)).

You may now click on 'Run PEX' to begin the extraction process. The operation may take a few minutes, and after it is completed you should see a Calibre view setup window. Ensure that the options are set as in figure 8 below.

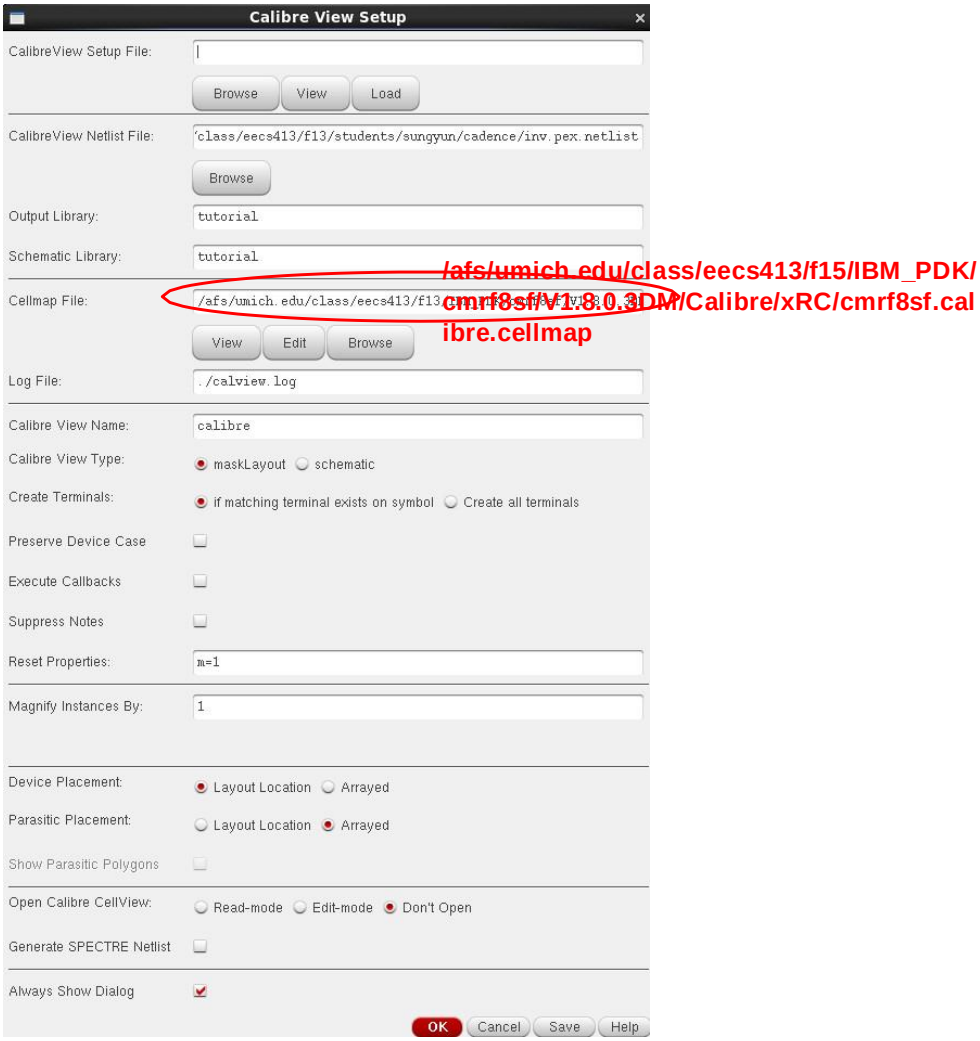


Figure 8. Calibre View Setup options

The extracted schematic now opens. You will notice that it isn't a pretty schematic to look at and it might be difficult to see how everything is connected. Generally, the original circuit components and pins will be at the top of the schematic and the parasitic components will be near the bottom. An example is in figure 9. Figure 10 shows the summary of PEX settings.

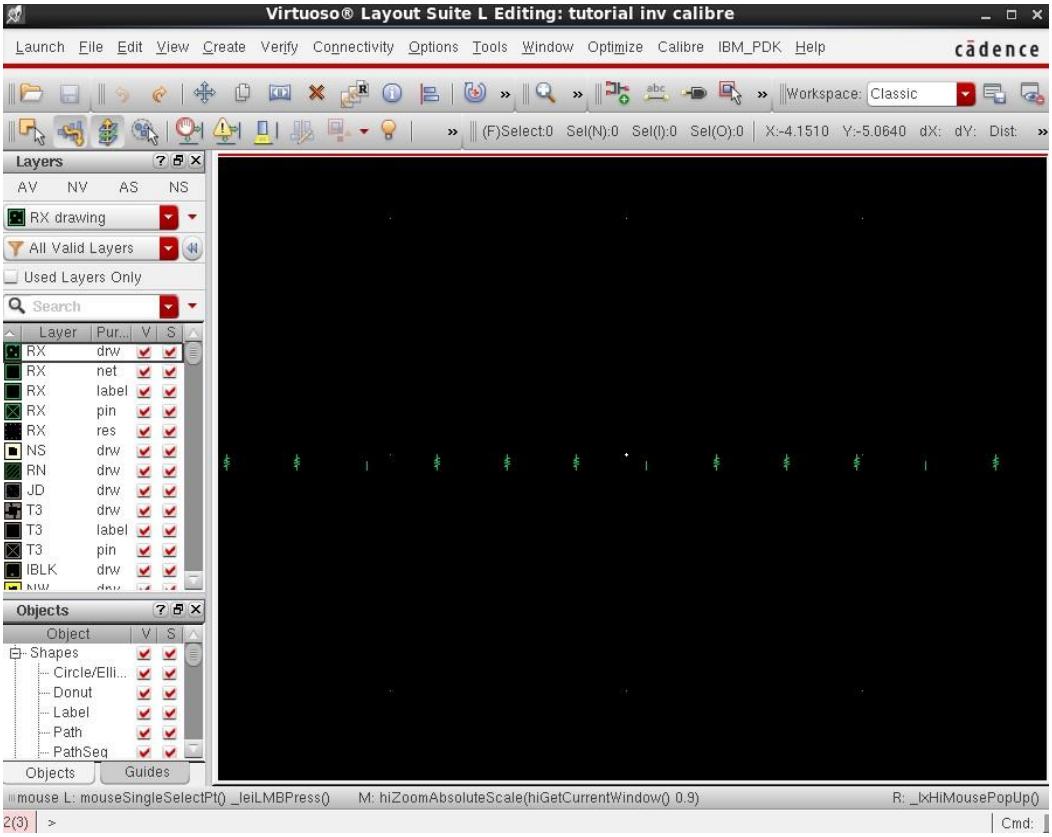
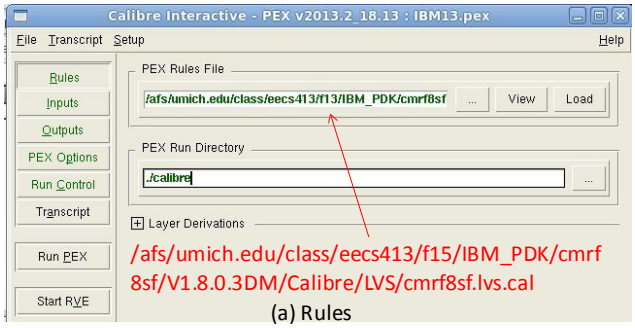
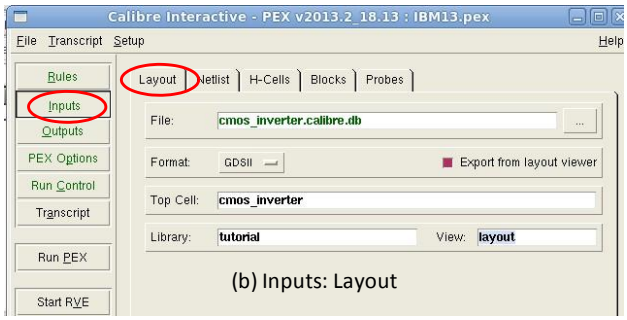


Figure 9. Example generated calibre view extracted schematic

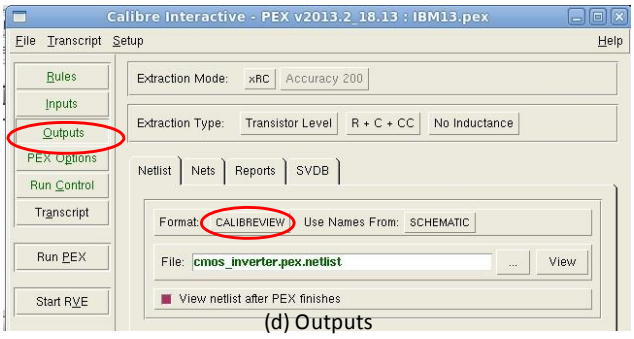


(a) Rules

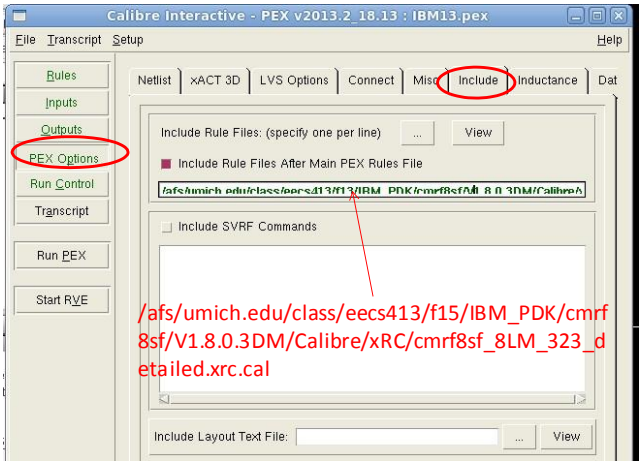


(b) Inputs: Layout

(c) Inputs: Netlist



(d) Outputs



(e) PEX Options

Figure 10. PEX settings summary

Simulating the extracted netlist

Open your inverter testbench, might be called ‘test_inverter’ from previous tutorial. (i.e. the schematic view with an instantiation of the cell cmos_inverter). Open ADE L and load your previous state. If you do not have a previous state, setup a DC sweep of vin from 0 to 1.2V. Remember to add the correct spectre model files to Setup > Model Libraries.

To ensure that the extracted netlist will be simulated you need to change the “Switch List.” The switch list is an ordered list of cellviews that is used to determine what view (i.e. schematic, calibre, or any other views you may have created) is netlisted. To edit the switch list, from the ADE window select

Setup > Environment

The first line is the switch view list. Add 'calibre' (without the quotes) as the first item in the list (Figure 11). Click OK. If you would like to double check which view is going to be used in simulation, you may click on the symbol in question and push 'e' (the shortcut key for descend). A window opens (note that sometimes in Linux this window opens behind the active schematic window) showing the available views to descend into, the default view is the view that will be used to generate the simulation netlist. Alternatively you can click

Simulation > Netlist > Create

and visually check the textual netlist to ensure that the correct view is used. Now run the simulation by clicking 'Netlist and Run'. After the simulation completes you can plot the outputs and compare them to the results of the schematic simulation.

If there are significant discrepancies, it is often useful to look at the textual netlist and check sensitive nodes for large parasitic capacitances or resistances.

You now have all the tools to design, simulate, and verify various circuits in IBM 0.13µm technology. In the future, whether designing in school or in industry, you will probably use the same Cadence and Calibre tools even when designing with other, non-IBM design kits.

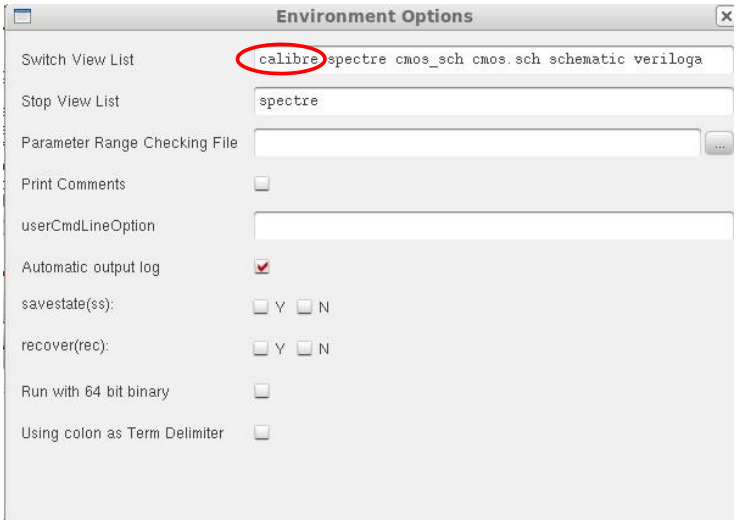


Figure 11. ADE L: Environment Optioins