

Ramp Generators and Integrators

INTRODUCTION

A simple ramp generator circuit can be constructed using a capacitor charged via a resistance, in conjunction with a discharge transistor. To improve the ramp output linearity, a transistor *constant current circuit* can be employed. When the discharge is replaced by a *unijunction* transistor, the circuit becomes a *relaxation oscillator*. The *bootstrap ramp generator*, which produces a closely linear ramp, can be constructed using a transistor or an IC operational amplifier. An IC operational amplifier can also be employed in a *Miller integrator*.

7-1 CR RAMP GENERATOR

The simplest ramp generator circuit is a capacitor charged via a series resistance. A transistor must be connected in parallel with the capacitor to provide a discharge path, as shown in the circuit of Figure 7-1(a). Capaci-

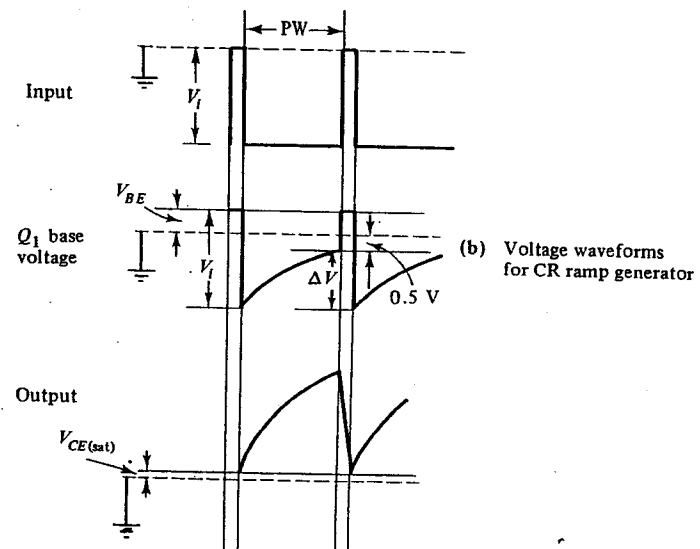
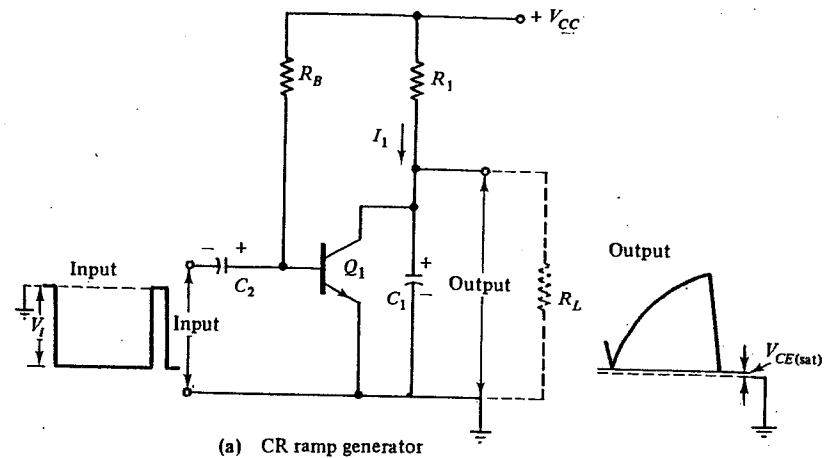


FIGURE 7-1. CR ramp generator circuit and voltage waveforms.

tor C_1 is charged from V_{CC} via R_1 . Q_1 is biased *on* via R_B so the capacitor is normally in a discharged state. When a negative-going input pulse is coupled by C_2 to Q_1 base, the transistor switches *off*. Then, C_1 begins to charge; this provides an approximate ramp output until the input pulse ends [see Figure 7-1(b)]. At this point, Q_1 switches *on* again, and rapidly discharges the capacitor.

The output from a simple CR circuit is exponential rather than linear. For voltages very much less than the supply voltage, however, the output is approximately linear. When the transistor is *on*, the capacitor is discharged to $V_{CE(sat)}$. Hence, $V_{CE(sat)}$ is the starting level of the output ramp. Output amplitude control can be provided by making the charging resistance (R_1) adjustable.

Capacitor C_2 , which couples the input pulse to the transistor base, should be selected as small as possible, both for minimum cost and smallest possible physical size. The minimum suitable size can be determined by allowing the base voltage of Q_1 to rise during the input pulse time, as shown in Figure 7-1(b). The base voltage starts approximately at 0.7 V when Q_1 is *on*. Then, V_{B2} is pulled negative by the input pulse, but starts to rise again as C_2 is charged through R_B . To ensure that Q_1 is still *off* at the end of the pulse time, V_{B2} should not rise above -0.5 V. This approach to coupling capacitor selection is outlined in Sec. 5-2.

EXAMPLE 7-1

Design a simple CR ramp generator to give an output that peaks at 5 V. The supply voltage is 15 V, and the load to be connected at the output is 100 k Ω . The ramp is to be triggered by a negative-going pulse with an amplitude of 3 V, PW = 1 ms, and the time interval between pulses is 0.1 ms. Take the transistor $h_{FE(min)}$ as 50.

solution

This circuit is shown in Figure 7-1(a). The maximum output current is

$$\begin{aligned} I_{L(max)} &= \frac{V_P}{R_L} \\ &= \frac{5 \text{ V}}{100 \text{ k}\Omega} = 50 \mu\text{A} \end{aligned}$$

Select the minimum capacitor charging current $I_1 \gg I_{L(max)}$. At peak output

Sec. 7-1 CR RAMP GENERATOR

voltage, let

$$\begin{aligned} I_1 &= 100 \times I_{L(max)} \\ &= 100 \times 50 \mu\text{A} = 5 \text{ mA} \\ R_1 &= \frac{V_{CC} - V_P}{I_1} \\ &= \frac{15 \text{ V} - 5 \text{ V}}{5 \text{ mA}} = 2 \text{ k}\Omega \quad (\text{use } 2.2 \text{ k}\Omega \text{ standard value}) \end{aligned}$$

The voltages for capacitor C_1 are

$$\begin{aligned} \text{Initial voltage} &= E_o \approx 0 \\ \text{Final voltage} &= e_c = 5 \text{ V} \\ \text{Charging voltage} &= E = V_{CC} = 15 \text{ V} \\ e_c &= E - (E - E_o)e^{-t/CR} \quad [\text{Equation (2-2)}] \\ C_1 &= \frac{t}{R \ln \frac{E - E_o}{E - e_c}} \\ &= \frac{1 \text{ ms}}{2.2 \text{ k}\Omega \ln \frac{15 \text{ V} - 0}{15 \text{ V} - 5 \text{ V}}} \\ &\approx 1 \mu\text{F} \end{aligned}$$

The discharge time for C_1 is 0.1 ms, which is one-tenth of the charging time. For Q_1 to discharge C_1 in the specified time,

$$\begin{aligned} I_C &\approx 10 \times (C_1 \text{ charging current}) \\ &= 10 I_1 = 50 \text{ mA} \\ I_B &= \frac{I_C}{h_{FE(min)}} \\ &= \frac{50 \text{ mA}}{50} = 1 \text{ mA} \\ R_B &= \frac{V_{CC} - V_{BE}}{I_B} \\ &= \frac{15 \text{ V} - 0.7 \text{ V}}{1 \text{ mA}} \\ &= 14.3 \text{ k}\Omega \quad (\text{use } 12 \text{ k}\Omega \text{ standard value}) \end{aligned}$$

For Q_1 to remain biased *off* at the end of the input pulse, let $V_B = -0.5$ V.

$$\begin{aligned}\therefore \Delta V &= V_i - V_{BE} - V_B \quad [\text{See Figure 7-1(b)}] \\ &= 3 \text{ V} - 0.7 \text{ V} - 0.5 \text{ V} = 1.8 \text{ V}\end{aligned}$$

The charging current for C_2 is equal to the current through R_B when Q_1 is *off*:

$$\begin{aligned}I &\approx \frac{V_{CC} - V_i}{R_B} = \frac{15 \text{ V} - (-3 \text{ V})}{12 \text{ k}\Omega} \\ &= 1.5 \text{ mA}\end{aligned}$$

From Equation (2-7):

$$\begin{aligned}C_2 &= \frac{It}{\Delta V} = \frac{1.5 \text{ mA} \times 1 \text{ ms}}{1.8 \text{ V}} \\ &= 0.83 \mu\text{F} \quad (\text{use } 1 \mu\text{F standard value})\end{aligned}$$

7-2 CONSTANT CURRENT RAMP GENERATORS

7-2.1 Bipolar Transistor Constant Current Circuits

The major disadvantage of the single CR ramp generator is its nonlinearity. To produce a linear ramp, the capacitor charging current must be held constant. This can be achieved by replacing the charging resistance with a *constant current circuit*.

A basic transistor constant current circuit is shown in Figure 7-2(a). The potential divider (R_1 and R_2) provides a fixed voltage V_1 at the base of *npn* transistor Q_2 . The voltage across the emitter resistor R_3 remains constant at $(V_1 - V_{BE})$. Thus, the emitter current is also constant: $I_E = (V_1 - V_{BE})/R_3$. Since $I_C \approx I_E$, the collector current remains constant. Figure 7-2(b) shows an arrangement that allows the level of constant current to be adjusted. R_4 provides adjustment of V_B . Since $V_3 = (V_B - V_{BE})$, V_3 also is adjustable by R_4 , and I_E can be set to any desired level over a range dependent upon R_4 .

Figure 7-3(a) shows a ramp generator that employs the constant current circuit. Note that because I_C of Q_2 is a constant charging current

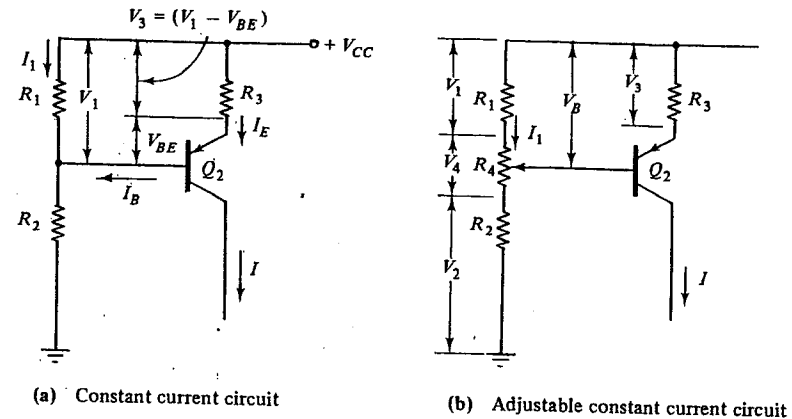


FIGURE 7-2. Transistor fixed and adjustable constant current circuits.

for C_1 ; the capacitor voltage V_O grows linearly. The simpler capacitor-charging equation, Equation (2-7), may now be used for C_1 calculations. The circuit of Figure 7-3(a) functions like the simple CR ramp generator, with R_1 replaced by the constant current circuit.

The output voltage from the constant current ramp generator remains linear only if a sufficient voltage is maintained across Q_2 for it to operate in the active region of its characteristics. If Q_2 reaches saturation, the output stops at a constant level. Therefore, V_{CE2} should not fall below about 3 V. Because of this and the constant voltage V_3 across resistor R_3 , the maximum ramp output voltage obtainable from the circuit of Figure 7-3 is approximately $V_O = V_{CC} - V_3 - 3$ V.

In the circuit of Figure 7-3(b) the input pulse is directly connected to the base of transistor Q_1 . When the input is at ground level, Q_1 is *off* and capacitor C_1 charges via Q_2 . When a positive input is applied, Q_1 is switched *on* and C_1 is rapidly discharged. Q_1 remains *on* during the positive input pulse; thus C_1 is held in a discharged condition, and the ramp generator output voltage remains at the $V_{CE(sat)}$ of Q_1 .

EXAMPLE 7-2

Using a constant current circuit, modify the ramp generator designed in Example 7-1 to produce a linear ramp output.

solution

Refer to the circuit of Figure 7-3(a).

$$V_{O(\max)} = 5 \text{ V}$$

$$V_3 + V_{CE2} = V_{CC} - 5 \text{ V} = 10 \text{ V}$$

Let

$$V_{CE2} = 3 \text{ V, minimum}$$

then

$$V_3 = 10 \text{ V} - 3 \text{ V} = 7 \text{ V}$$

To maintain a constant level of I_E (and I_C), the voltage across R_3 should be several times larger than the base emitter voltage V_{BE} . This ensures that changes in V_{BE} do not significantly affect I_E .

$$C_1 = \frac{It}{\Delta V} \quad \therefore \quad I = \frac{C_1 \Delta V}{t}$$

For $C_1 = 1 \mu\text{F}$, $V = 5 \text{ V}$, and $t = 1 \text{ ms}$,

$$I = \frac{1 \mu\text{F} \times 5 \text{ V}}{1 \text{ ms}} = 5 \text{ mA}$$

$$R_3 \approx \frac{7 \text{ V}}{5 \text{ mA}} = 1.4 \text{ k}\Omega \quad (\text{use } 1.2 \text{ k}\Omega \text{ standard value})$$

For $I_E = 5 \text{ mA}$,

$$V_3 = 5 \text{ mA} \times 1.2 \text{ k}\Omega$$

$$= 6 \text{ V}$$

$$V_1 = V_3 + V_{BE2} = 6 \text{ V} + 0.7 \text{ V}$$

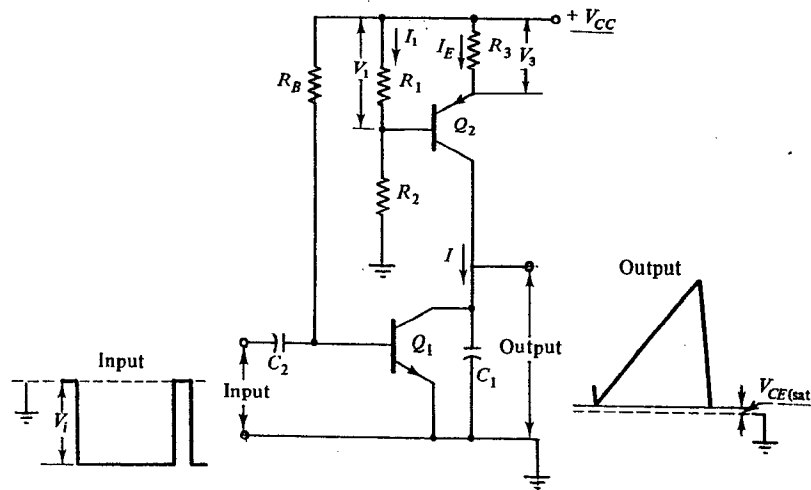
$$= 6.7 \text{ V}$$

V_1 must be a stable bias voltage unaffected by I_{B2} . Make $I_1 \approx I_E = 5 \text{ mA}$.

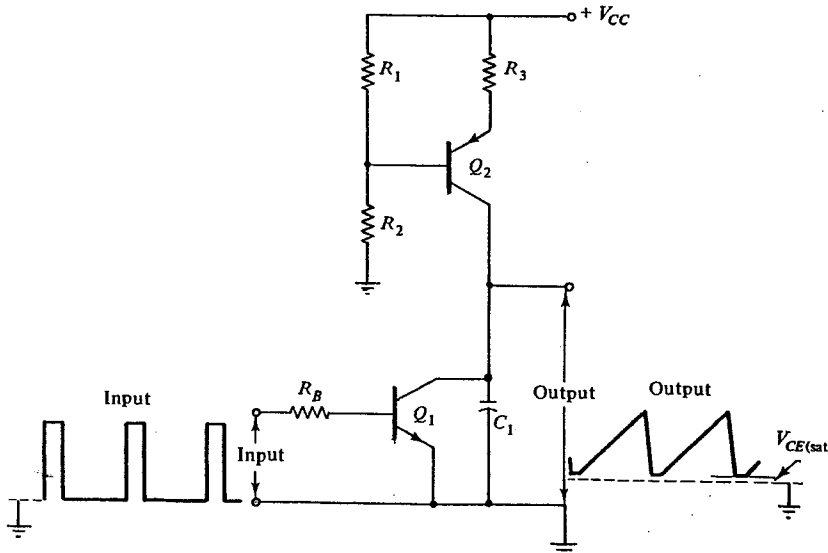
$$R_1 = \frac{V_1}{I_1}$$

$$= \frac{6.7 \text{ V}}{5 \text{ mA}}$$

$$= 1.34 \text{ k}\Omega \quad (\text{use } 1.2 \text{ k}\Omega \text{ standard value})$$



(a) Constant current ramp generator with capacitor-coupled input



(b) Constant current ramp generator with direct-coupled input

FIGURE 7-3. Constant current ramp generators.

Then I_1 becomes

$$I_1 = \frac{6.7 \text{ V}}{1.2 \text{ k}\Omega} = 5.58 \text{ mA}$$

$$V_2 = V_{CC} - V_1 = 15 \text{ V} - 6.7 \text{ V} = 8.3 \text{ V}$$

$$R_2 \approx \frac{V_2}{I_1} = \frac{8.3 \text{ V}}{5.58 \text{ mA}} \\ = 1.49 \text{ k}\Omega \quad (\text{use } 1.5 \text{ k}\Omega \text{ standard value})$$

EXAMPLE 7-3

Redesign the circuit of Example 7-2 to make the ramp amplitude adjustable from 3 V to 5 V.

solution

The circuit modification is shown in Figure 7-2(b). The charging current, with $\Delta V = 3 \text{ V}$, is

$$I = \frac{C_1 \Delta V}{t} \\ = \frac{1 \mu\text{F} \times 3 \text{ V}}{1 \text{ ms}} = 3 \text{ mA}$$

For $\Delta V = 5 \text{ V}$,

$$I = \frac{1 \mu\text{F} \times 5 \text{ V}}{1 \text{ ms}} = 5 \text{ mA}$$

For $I = 3 \text{ mA}$, $I_E \approx 3 \text{ mA}$ and

$$V_3 = I_E \times R_3 = 3 \text{ mA} \times 1.2 \text{ k}\Omega \\ = 3.6 \text{ V} \\ V_B = V_1 = V_3 + V_{BE} = 3.6 \text{ V} + 0.7 \text{ V} \\ = 4.3 \text{ V}$$

(At this point, the moving contact on the potentiometer is at the upper end.)

For $R_1 = 1.2 \text{ k}\Omega$,

$$I_1 = \frac{4.3 \text{ V}}{1.2 \text{ k}\Omega} \approx 3.6 \text{ mA}$$

For $I = 5 \text{ mA}$,

$$V_3 = 5 \text{ mA} \times 1.2 \text{ k}\Omega \\ = 6 \text{ V}$$

and

$$V_B = 6.7 \text{ V}$$

(At this point the potentiometer moving contact is at the lower end.)

$$V_B = V_1 + V_4 \\ V_4 = 6.7 \text{ V} - 3.6 \text{ V} = 3.1 \text{ V}$$

and

$$R_4 = \frac{V_4}{I_1} = \frac{3.1 \text{ V}}{3.6 \text{ mA}} \\ = 0.86 \text{ k}\Omega \quad (\text{use a } 1 \text{ k}\Omega \text{ standard potentiometer value})$$

Then V_4 becomes

$$V_4 = I_1 R_4 = 3.6 \text{ mA} \times 1 \text{ k}\Omega = 3.6 \text{ V}$$

and

$$V_2 = V_{CC} - V_1 - V_4 \\ = 15 \text{ V} - 4.3 \text{ V} - 3.6 \text{ V} \\ = 7.1 \text{ V}$$

$$R_2 = \frac{V_2}{I_1} \\ = \frac{7.1 \text{ V}}{3.6 \text{ mA}} \\ = 1.97 \text{ k}\Omega \quad (\text{use } 2.2 \text{ k}\Omega \text{ standard value})$$

7-2.2 FET Constant Current Circuits

A field effect transistor with a single source resistance can function as a constant current circuit. A *p*-channel FET is shown in Figure 7-4(a) with a resistor connected between the source terminal and V_{CC} . With the gate terminal also connected to V_{CC} , the gate-source voltage is the voltage drop across R_S , which is $I_S R_S$ or $I_D R_S$. Referring to the FET transconductance characteristics in Figure 7-4(b), the desired drain/source current (I_S) can be selected and the corresponding gate-source voltage (V_{RS}) determined as illustrated. Then,

$$R_S = \frac{V_{RS}}{I_S} \quad (7-1)$$

This approach is satisfactory only when the transconductance characteristic for the particular FET has been plotted. For any given FET type, there are two possible extreme characteristics as shown in Figure 7-4(c). These occur because of the spread in values of *drain-source saturation current* [$I_{DSS(max)}$ and $I_{DSS(min)}$], and *pinch-off voltage* [$V_{P(max)}$ and $V_{P(min)}$]. In this case it is necessary to draw a *bias line* for each possible value of source resistance. This is done simply by using Equation (7-1) to determine two convenient corresponding values of I_D and V_{GS} :

When $V_{GS}=0$,

$$I_D = V_{RS}/R_S = 0$$

Plot point *A* on Figure 7-4(c) at $V_{GS}=0$ and $I_D=0$.

When $V_{RS}=6\text{ V}$ and $R_S=3.3\text{ k}\Omega$,

$$I_D = 6\text{ V}/3.3\text{ k}\Omega = 1.8\text{ mA}$$

Plot point *B* on Figure 7-4(c) at $V_{GS}=6\text{ V}$ and $I_D=1.8\text{ mA}$.

Draw the bias line through points *A* and *B*. The maximum and minimum source current levels that can flow are now shown at the intersections of the bias lines and the characteristics. When it is desired to set I_S to a precise level R_S must be made adjustable.

One important caution that must be observed when using a FET constant current circuit is that the drain-source voltage V_{DS} must not be allowed to fall below the maximum value of pinch-off voltage $V_{P(max)}$. Just as a bipolar transistor cannot be expected to function linearly if its collector-base voltage approaches the saturation level, so too a FET will not function correctly in a linear circuit if its drain-source voltage falls below the pinch-off level.

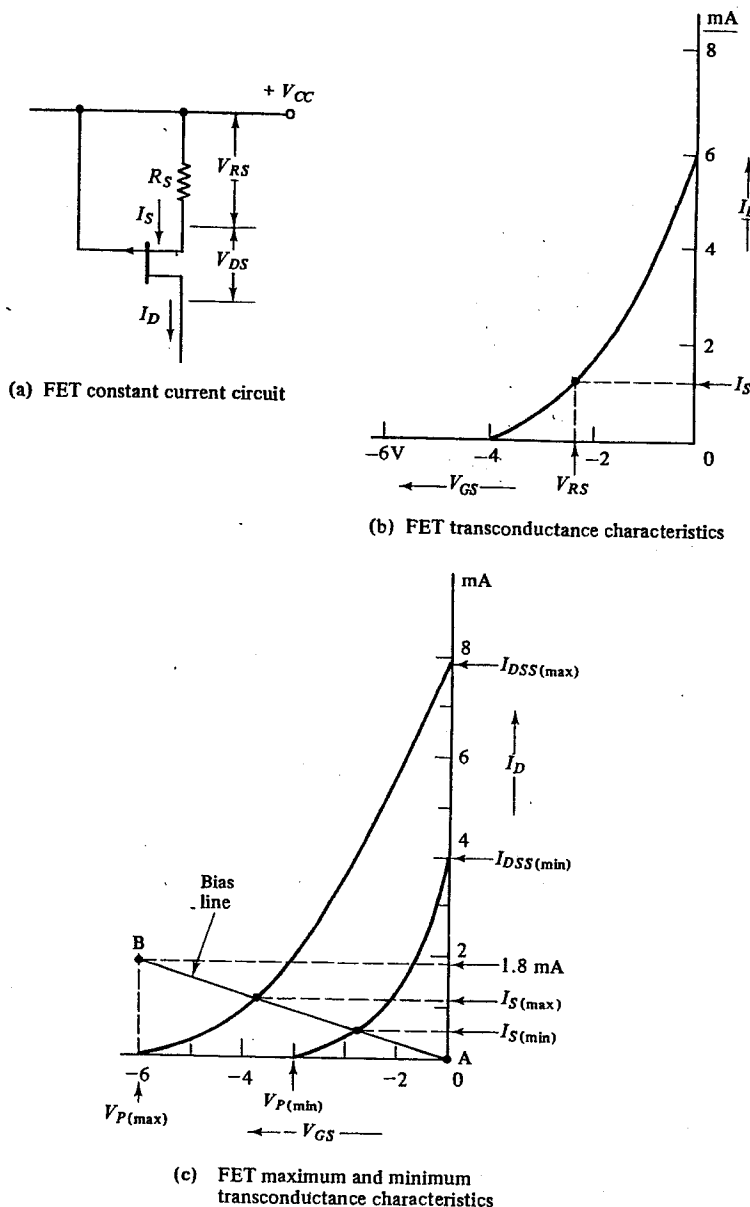


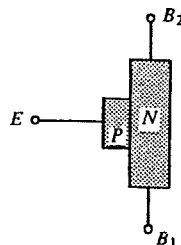
FIGURE 7-4. FET constant current circuit and transconductance characteristics.

A *constant current diode* (or *field effect diode*) is essentially a FET and a resistor connected as illustrated in Figure 7-4(a), and contained in a single package. These devices can be purchased with various constant current levels.

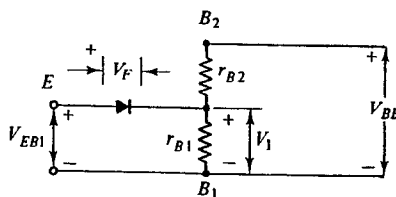
7-3 UJT RELAXATION OSCILLATORS

7-3.1 The Unijunction Transistor

The basic construction of a unijunction transistor (UJT) and its equivalent circuit are shown in Figure 7-5. The device can be thought of as a bar of lightly doped *n*-type silicon with a small piece of heavily doped *p*-type joined to one side [see Figure 7-5(a)]. The *p*-type is named the *emitter*, while the two end terminals of the bar are designated bases 1 and 2 (B_1 and B_2), as shown. In the equivalent circuit of Figure 7-5(b), the silicon bar is represented as two resistors, r_{B1} and r_{B2} while the *pn* junction formed by the emitter and the bar is represented by a diode.



(a) Basic construction



(b) Equivalent circuit

FIGURE 7-5. Basic construction and equivalent circuit of unijunction transistor.

The ratio, $r_{B1}/(r_{B1}+r_{B2})$ is termed the *intrinsic standoff ratio* of the UJT, and is designated η . Thus the voltage across r_{B1} is given by

$$V_1 = V_{BB} \frac{r_{B1}}{r_{B1} + r_{B2}}$$

or

$$V_1 = V_{BB} \eta \quad (7-2)$$

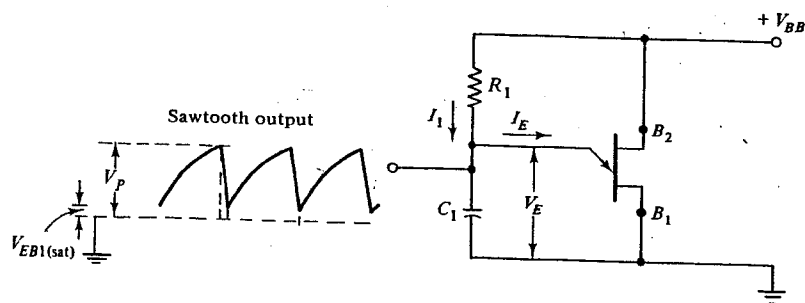
The *pn* junction becomes forward-biased at a peak voltage, $V_P = V_{EB1} = V_1 + V_F$. When this peak is reached, the flow of charge carriers through r_{B1} causes its resistance to fall. Thus, a capacitor connected across *E* and B_1 is rapidly discharged. The flow of current into the emitter terminal continues until V_E falls to the *emitter saturation voltage* $V_{EB1(sat)}$, at which time the device switches off.

Two more important parameters for the UJT are *peak point current* I_P and the *valley point current* I_V . The peak point current is the minimum emitter current that must flow for the UJT to switch on or fire. This current occurs when V_E is at the *firing voltage*, that is, at peak point V_P . The valley point current is the emitter current that flows when V_E is at the emitter saturation voltage, $V_{EB1(sat)}$.

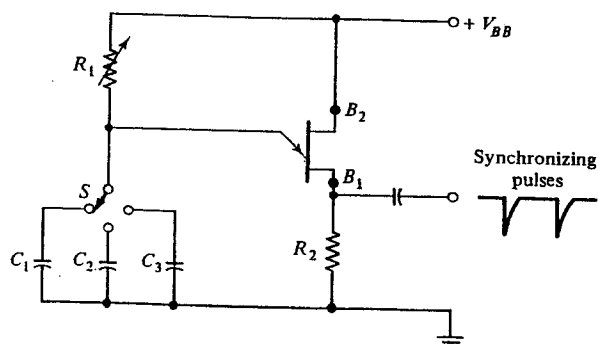
7-3.2 UJT Relaxation Oscillator

A unijunction transistor can be used in conjunction with a capacitor and a charging circuit, to construct an oscillator with an approximate ramp-type output. Figure 7-6(a) shows the simplest form of such a circuit, which is called a *UJT relaxation oscillator*. The UJT remains off until its emitter voltage V_{EB1} approaches the firing voltage V_P for the particular device. At this point, the UJT switches on and a large emitter current I_E flows. This causes capacitor C_1 to discharge rapidly. When the capacitor voltage falls to the emitter saturation level, the UJT switches off, allowing C_1 to begin to charge again.

The frequency of a relaxation oscillator can be made variable by switched selection of capacitors and/or by adjustment of the charging resistance [see Figure 7-6(b)]. The resistance R_2 , in series with UJT terminal B_1 , allows synchronizing input pulses to be applied. When an input pulse pulls B_1 negative, V_{EB1} is increased to the level at which the UJT fires. Once the UJT fires it will not switch off again until the capacitor is discharged.



(a) UJT relaxation oscillator



(b) Variable frequency UJT relaxation oscillator

FIGURE 7-6. Basic UJT relaxation oscillator and variable frequency circuit.

In the design of a UJT relaxation oscillator, the charging resistance R_1 must be selected between certain upper and lower limits. Resistance R_1 must not be so large that the emitter current is less than the peak point current when V_{EB1} is at the firing voltage; otherwise, the device may not switch on. If R_1 is very small, then when V_{EB1} is at the emitter saturation level, a current greater than the valley point current might flow into the

emitter terminal. In this case, the UJT may not switch off. Thus, for correct UJT operation, R_1 must be selected between two limits that allow the emitter current to be a minimum of I_P and a maximum of I_V .

The UJT oscillator circuits shown in Figures 7-6(a) and (b) will produce exponential output waveforms because the capacitors are charged by resistances. Constant current circuits could be used here to generate linear ramp output waveforms.

EXAMPLE 7-4

The circuit of Figure 7-6(a) is to use a 2N3980 UJT. The supply voltage V_{BB} is 20 V, and output frequency is to be 5 kHz. Design a suitable circuit, and calculate the output amplitude.

solution

Capacitor C_1 charges from $V_{EB1(sat)}$ to the firing voltage, $V_P = V_F + \eta V_{BB}$. The data sheet for the 2N3980 (Appendix 1-12) gives the following specifications:

$$V_{EB1(sat)} = 3 \text{ V maximum}, \quad I_P = 2 \mu\text{A}, \quad I_V = 1 \text{ mA}$$

and

$$\eta = 0.68 \text{ to } 0.82$$

$$\approx 0.75 \text{ average}$$

$$V_P = 0.7 + (0.75 \times 20 \text{ V}) \\ = 15.7 \text{ V}$$

Therefore, for the capacitor,

$$E = \text{Supply voltage} = V_{BB} = 20 \text{ V}$$

$$E_o = \text{Initial charge} = V_{EB1(sat)} = 3 \text{ V}$$

$$e_c = \text{Final charge} = V_P = 15.7 \text{ V}$$

Now, to select R_1 :

$$R_{1(\max)} = \frac{V_{BB} - V_P}{I_P} \\ = \frac{20 \text{ V} - 15.7 \text{ V}}{2 \mu\text{A}} \approx 2.15 \text{ M}\Omega$$

$$R_{I(\min)} = \frac{V_{BB} - V_{EBI(sat)}}{I_V}$$

$$= \frac{20 \text{ V} - 3 \text{ V}}{1 \text{ mA}} \approx 17 \text{ k}\Omega$$

So R_I must be in the range $17 \text{ k}\Omega$ to $2.15 \text{ M}\Omega$. If R_I is very large, C_I must be a very small capacitor. Let R_I have a value of $22 \text{ k}\Omega$; then from Equation (2-2)

$$C_I = \frac{t}{R_I \ln \left(\frac{E - E_o}{E - e_c} \right)}$$

$$t = \frac{1}{\text{Output frequency}} = \frac{1}{5 \text{ kHz}} = 200 \mu\text{s}$$

then

$$C_I = \frac{200 \mu\text{s}}{22 \text{ k}\Omega \ln \left(\frac{20 \text{ V} - 3 \text{ V}}{20 \text{ V} - 15.7 \text{ V}} \right)}$$

$$= 6600 \text{ pF} \quad \left[\text{use } 6800 \text{ pF standard capacitor} \right]$$

(see Appendix 2-2)]

$$\text{Output amplitude} = V_P - V_{EBI(sat)}$$

$$= 15.7 \text{ V} - 3 \text{ V}$$

$$= 12.7 \text{ V}$$

7-4 FOUR-LAYER DIODE RELAXATION OSCILLATOR

A very simple relaxation oscillator can be constructed using a *four-layer diode* or *Shockley diode*.

The theory of operation of the four-layer diode is illustrated in Figure 7-7. The device consists of four semiconductor layers p_1 , n_1 , p_2 , and n_2 , with a connecting terminal to p_1 identified as the *anode* and that to n_2 as

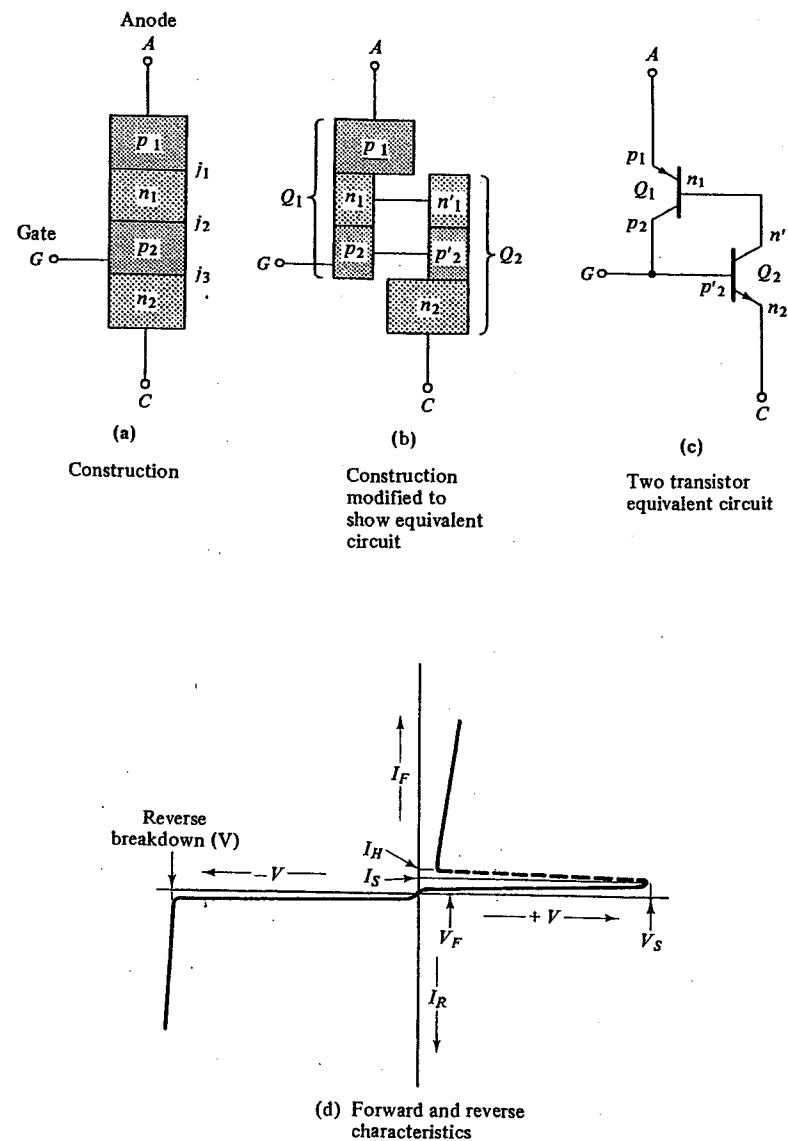


FIGURE 7-7. Four-layer diode: construction, equivalent circuit, and characteristics.

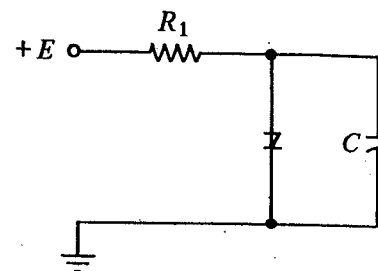
the cathode [Figure 7-7(a)]. To help understand the operation of the device, Figure 7-7(b) shows layers n_1 and p_2 split into sections n_1 , n'_1 , p_2 and p'_2 . Since these sections are connected together, there is no real change. However, p_1 , n_1 , and p_2 can now be thought of as a pnp transistor, and n'_1 , p'_2 and n_2 can be considered an npn transistor. This gives the two-transistor equivalent circuit in Figure 7-7(c). Now return to Figure 7-7(a) and note that when the anode is biased positively with respect to the cathode (forward bias), junctions j_1 and j_3 are forward-biased while junction j_2 is reverse-biased. Thus, at small forward bias voltages only a very low leakage current flows. When the forward bias is increased to the breakdown voltage of junction j_2 , a large forward current flows.

Going back to Figure 7-7(c), it is seen that when a substantial current flows into the emitter of transistor Q_1 , an equally large collector current flows from the collector of Q_1 into the base of Q_2 . Similarly, Q_2 has substantial emitter and collector currents, and the collector current of Q_2 provides base current for Q_1 . The result is that both transistors are switched on into saturation, and the total anode-to-cathode voltage V_{AK} is around 0.9 V.

The device forward characteristics shown in Figure 7-7(d) can now be understood. When $+V$ is small only a low level leakage current flows. When the breakdown or switching voltage V_s is reached, j_2 breaks down, the two transistors switch on into saturation, and the device voltage rapidly falls to a low level V_F . Any further increase in forward current now causes only a slight increase in V_F . The device reverse characteristics are similar to those of a reverse-biased diode, except that two junctions j_1 and j_3 must break down before the four-layer diode goes into reverse breakdown.

The circuit of a four-layer diode relaxation oscillator is shown in Figure 7-8. Note the device circuit symbol. Capacitor C_1 is charged via resistor R_1 until the diode switching voltage is reached. Then D_1 rapidly switches to the low level on voltage V_F , discharging C_1 in the process. D_1 continues conducting until its current falls below the minimum level that can maintain conduction. This level is known as the holding current I_H [see Figure 7-7(d)]. Once D_1 ceases to conduct, current flows into the capacitor again (via R_1), charging it up to V_s . The cycle is repetitive, generating an output waveform as illustrated.

In designing a relaxation oscillator using a four-layer diode the considerations are similar to those that apply for the UJT. Resistor R_1 must not be so large that the current flowing through it is less than the diode switching current I_S . Neither can it be so small that its current is greater than the diode holding current I_H . Thus R_1 is selected between these limitations, and C_1 is determined exactly as in the case of the UJT relaxation oscillator.



Relaxation oscillator using four-layer diode.

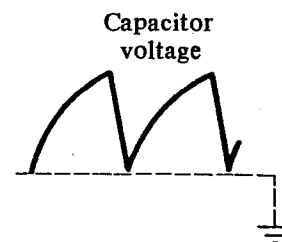
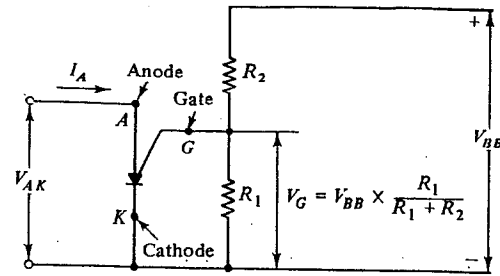


FIGURE 7-8. Relaxation oscillator using four-layer diode.

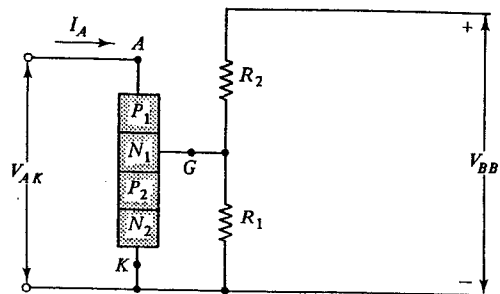
7-5 PROGRAMMABLE UJT RELAXATION OSCILLATORS

The *programmable unijunction transistor* (PUT) is a four-layer device used in a particular way to simulate a UJT. The interbase resistances r_{B1} and r_{B2} and the intrinsic standoff ratio η may be programmed to any desired values by selecting two resistors. This means that the device firing voltage V_P can also be programmed.

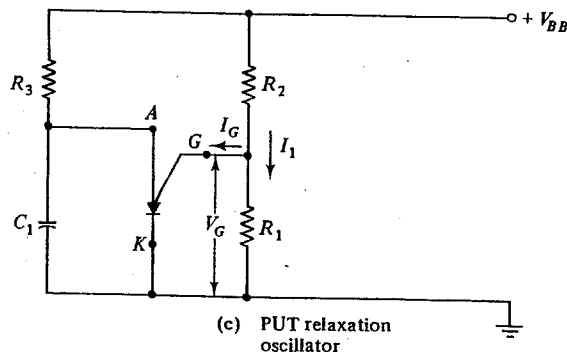
Consider Figures 7-9(a) and (b). The *gate* of the $pnpn$ device is connected to the junction of resistors R_1 and R_2 . The gate voltage is



(a) Programmable UJT circuit



(b) Four layer construction of programmable UJT



(c) PUT relaxation oscillator

FIGURE 7-9. Programmable UJT, four-layer construction, and PUT relaxation oscillator circuit.

$V_G = V_{BB} R_1 / (R_1 + R_2)$. The device will trigger on when the input voltage V_{AK} makes the anode (layer P_1) positive with respect to the gate (layer N_1). [This forward-biases the base-emitter junction of Q_1 in Figure 7-7(c).] When this occurs, the anode-to-cathode voltage rapidly drops to a low level, and the device conducts heavily from anode to cathode. This situation continues until the current becomes too low to sustain conduction. With the anode used as an emitter terminal, and with R_1 and R_2 substituted for r_{B1} and r_{B2} , the circuit action simulates a UJT. Figure 7-9(c) shows the PUT employed in a relaxation oscillator.

A data sheet for 2N6027 and 2N6028 PUT devices is included in Appendix 1-13. For the 2N6027, the value of I_P is given as $1.25 \mu A$ typical, and I_V as $18 \mu A$ typical. The offset voltage, which is equivalent to $V_{EB1(sat)}$, is typically $0.7 V$.

EXAMPLE 7-5

Design a relaxation oscillator using a 2N6027 PUT. The supply voltage is $15 V$, and the output is to be $5 V$ peak at $1 kHz$.

solution

The circuit is as shown in Figure 7-9(c).

$$V_P = V_G + (p_1 n_1 \text{ junction voltage drop})$$

$$5 V = V_G + 0.7 V$$

$$V_G = 5 V - 0.7 V = 4.3 V$$

To provide a stable gate bias voltage the current through the potential divider (R_1 and R_2) must be much larger than the gate current at switch-on:

$$I_1 \gg I_G$$

Since $I_G \approx 5 \mu A$ (typical), let

$$I_1 = 100 \times I_G$$

$$= 100 \times 5 \mu A = 0.5 \text{ mA}$$

$$R_1 = \frac{V_G}{I_1} = \frac{4.3 V}{0.5 \text{ mA}}$$

$$= 8.6 \text{ k}\Omega \quad (\text{use } 8.2 \text{ k}\Omega \text{ standard})$$

Now, I_1 becomes

$$I_1 = \frac{4.3 \text{ V}}{8.2 \text{ k}\Omega} = 524 \mu\text{A}$$

$$V_{R2} = V_{BB} - V_G$$

$$= 15 \text{ V} - 4.3 \text{ V} = 10.7 \text{ V}$$

$$R_2 = \frac{V_{R2}}{I_1} = \frac{10.7 \text{ V}}{524 \mu\text{A}}$$

$$= 20.4 \text{ k}\Omega \quad (\text{use } 18 \text{ k}\Omega \text{ standard})$$

Now V_G becomes

$$V_G = \frac{15 \text{ V} \times 8.2 \text{ k}\Omega}{18 \text{ k}\Omega + 8.2 \text{ k}\Omega}$$

$$= 4.69 \text{ V} \quad (\text{i.e., instead of } 4.3 \text{ V})$$

and

$$V_P = V_G + 0.7 \text{ V}$$

$$= 4.69 \text{ V} + 0.7 \text{ V} = 5.39 \text{ V}$$

The valley voltage V_V is 0.7 V.

For the capacitor C_1 :

$$E = \text{Supply voltage} = V_{BB} = 15 \text{ V}$$

$$E_O = \text{Initial charge} = V_V = 0.7 \text{ V}$$

$$e_c = \text{Final charge} = V_P = 5.39 \text{ V}$$

For selection of R_3 :

$$R_{3(\max)} = \frac{V_{BB} - V_P}{I_P}$$

$$= \frac{15 \text{ V} - 5.39 \text{ V}}{1.25 \mu\text{A}} = 7.7 \text{ M}\Omega$$

$$R_{3(\min)} = \frac{V_{BB} - V_V}{I_V}$$

$$= \frac{15 \text{ V} - 0.7 \text{ V}}{18 \mu\text{A}} = 790 \text{ k}\Omega$$

Thus, R_3 must be in the range from 790 k Ω to 7.7 M Ω . Let $R_3 = 1 \text{ M}\Omega$.

$$t = \frac{1}{\text{Output frequency}} = \frac{1}{1 \text{ kHz}} = 1 \text{ ms}$$

and from Equation (2-2)

$$C_1 = \frac{t}{R_3 \ln \left(\frac{E - E_O}{E - e_c} \right)}$$

$$= \frac{1 \text{ ms}}{1 \text{ M}\Omega \ln \left(\frac{15 \text{ V} - 0.7 \text{ V}}{15 \text{ V} - 5.39 \text{ V}} \right)}$$

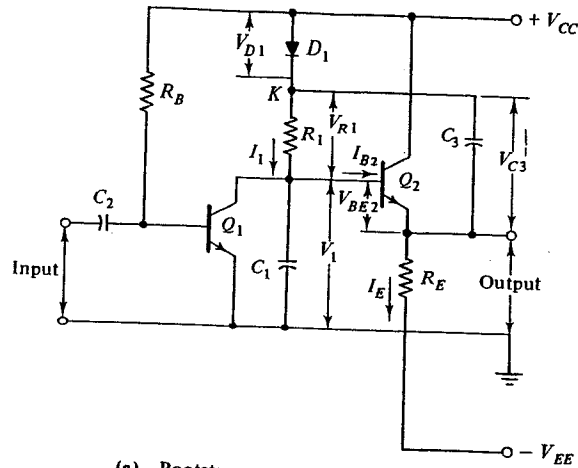
$$= 0.0025 \mu\text{F} \quad (\text{standard value})$$

7-6 TRANSISTOR BOOTSTRAP RAMP GENERATOR

The circuit of a transistor *bootstrap ramp generator* is shown in Figure 7-10(a). The ramp is generated across capacitor C_1 , which is charged via resistance R_1 . The discharge transistor Q_1 holds the capacitor voltage V_1 down to $V_{CE(\text{sat})}$ until a negative input pulse is applied. Transistor Q_2 is an emitter follower that provides a low-output impedance. The emitter resistor R_E is connected to a negative supply level, rather than to ground. This is to ensure that Q_2 remains conducting when its base voltage V_1 is close to ground. Capacitor C_3 , known as the *bootstrapping capacitor*, has a much larger capacitance than C_1 . The function of C_3 , as will be shown, is to maintain a constant voltage across R_1 and thus maintain the charging current constant.

To understand the operation of the bootstrap ramp generator, first consider the dc voltage levels before an input signal is applied. Transistor Q_1 is *on*, and its voltage is $V_{CE(\text{sat})}$, which is typically 0.2 V. Thus $V_1 = 0.2 \text{ V}$. This level is indicated as point *A* on the graph of voltage V_1 in Figure 7-10(b). The emitter of Q_2 is now at $(V_1 - V_{BE2})$, which is also the output voltage V_O (point *B* on the V_O graph). At this time, the voltage at the cathode of diode D_1 is $V_K = V_{CC} - V_{D1}$, where V_{D1} is the diode forward voltage drop. The voltage, $V_{CC} - V_{D1}$ is shown at point *C* on the graph of V_K [Figure 7-10(b)]. The voltage across capacitor C_3 is the difference between V_K and V_O .

When Q_1 is switched *off* by an input pulse, C_1 starts to charge via R_1 . Voltage V_1 now increases, and the emitter voltage V_O of Q_2 (the emitter follower) also increases. Thus, as V_1 grows V_O also grows, remaining only V_{BE} below V_1 [see Figure 7-10(b)]. As V_O increases, the lower terminal of



(a) Bootstrap ramp generator

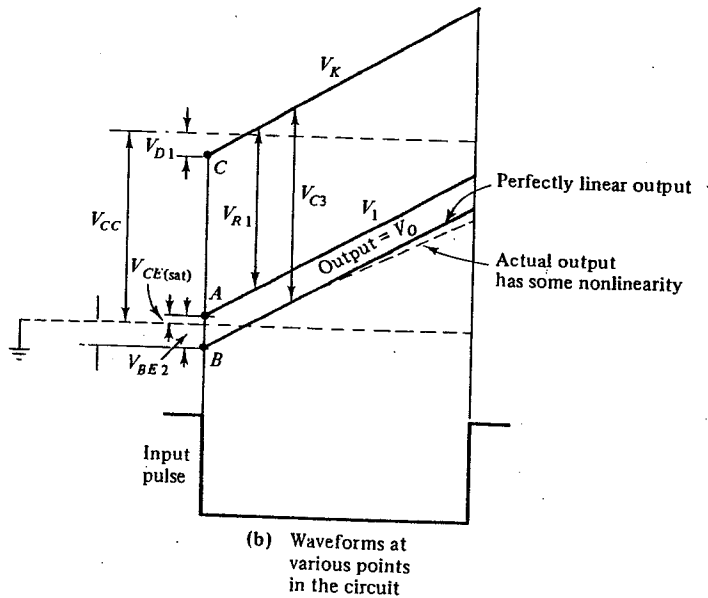


FIGURE 7-10. Transistor bootstrap ramp generator and circuit waveforms.

C_3 is pulled up. Because C_3 is a large capacitor it retains its charge, and as V_O increases the voltage at the upper terminal of C_3 also increases. Thus, V_K increases as V_O increases, and V_K remains V_{C3} volts above V_O . In fact, V_K goes above the level of V_{CC} , and D_1 is reverse-biased. The constant voltage across C_3 maintains the voltage V_{R1} constant across R_1 . Therefore, the charging current through R_1 is held constant, and the capacitor charges linearly, giving a linear output ramp.

During the ramp time D_1 is reverse-biased as already explained, and the charging current through R_1 is provided by capacitor C_3 . If C_3 is very large and I_1 is small, then C_3 will discharge by only a very small amount. When the input pulse is removed and C_1 is discharged rapidly by Q_1 , V_O drops to its initial level. Also, V_K drops, allowing D_1 to become forward-biased. At this time a current pulse through D_1 replaces the small charge lost from C_3 . The circuit is then ready to generate another output ramp.

In addition to producing a very linear output ramp, another advantage of the bootstrap generator is that the amplitude of the ramp can approach the level of the supply voltage. Note that the output ramp amplitude may be made adjustable over a fixed time period by making R_1 adjustable.

The broken line on the graph of output voltage [Figure 7-10(b)] shows that the output, instead of being perfectly linear, may be slightly nonlinear. If the difference between the actual output and the ideal output is 1% of the output peak voltage, then the ramp can be said to have 1% nonlinearity. Some nonlinearity results from the slight discharge of C_3 that occurs during the ramp time. Another source of nonlinearity is the base current I_{B2} . As the capacitor voltage grows, I_{B2} increases. Since I_{B2} is part of I_1 , the capacitor charging current decreases slightly as I_{B2} increases. Thus, the charging current does not remain perfectly constant, and the ramp is not perfectly linear. The design of a bootstrap ramp generator begins with a specification of ramp linearity. This dictates the charging current and the capacitance of C_3 . The percentage of nonlinearity usually is allocated in equal parts to ΔI_{B2} and ΔV_{C3} .

EXAMPLE 7-6

Design a transistor bootstrap ramp generator to provide an output amplitude of 8 V over a time period of 1 ms. The ramp is to be triggered by a negative-going pulse with an amplitude of 3 V, a pulse width of 1 ms, and a time interval between pulses of 1 ms. The load resistor to be supplied has a value of 1 k Ω and the ramp is to be linear within 2%. The supply voltage is to be ± 15 V. Take $h_{FE(\min)} = 100$.

solution

The circuit is shown in Figure 7-10(a).

$$R_E = R_L = 1 \text{ k}\Omega$$

When $V_O = 0$,

$$I_E \approx \frac{V_{EE}}{R_E}$$

$$\frac{15 \text{ V}}{1 \text{ k}\Omega} = 15 \text{ mA}$$

When $V_O = V_P$,

$$I_E \approx \frac{V_{EE} + V_P}{R_E}$$

$$= \frac{15 \text{ V} + 8 \text{ V}}{1 \text{ k}\Omega} = 23 \text{ mA}$$

$$I_{B2} \approx \frac{I_{E2}}{h_{FE}}$$

At $V_O = 0$,

$$I_{B2} = \frac{15 \text{ mA}}{100} = 0.15 \text{ mA}$$

At $V_O = V_P$,

$$I_{B2} = \frac{23 \text{ mA}}{100} = 0.23 \text{ mA}$$

$$\Delta I_{B2} = 0.23 \text{ mA} - 0.15 \text{ mA} = 80 \mu\text{A}$$

Allow 1% nonlinearity due to ΔI_{B2} , (that is, ΔI_{B2} represents a loss of charging current to C_1):

$$I_1 = 100 \times \Delta I_{B2}$$

$$= 100 \times 80 \mu\text{A}$$

$$= 8 \text{ mA}$$

$$C_1 = \frac{I_1 t}{\Delta V} = \frac{I_1 \times (\text{Ramp time})}{V_P}$$

$$= \frac{8 \text{ mA} \times 1 \text{ ms}}{8 \text{ V}}$$

Sec. 7-7 IC BOOTSTRAP RAMP GENERATOR

$$= 1 \mu\text{F} \quad (\text{standard capacitor value})$$

$$V_{R1} = V_{CC} - V_{D1} - V_{CE(\text{sat})}$$

$$= 15 \text{ V} - 0.7 \text{ V} - 0.2 \text{ V}$$

$$= 14.1 \text{ V}$$

$$R_1 = \frac{V_{R1}}{I_1} = \frac{14.1 \text{ V}}{8 \text{ mA}}$$

$$= 1.76 \text{ k}\Omega \quad (\text{use } 1.8 \text{ k}\Omega \text{ standard value})$$

For 1% nonlinearity due to C_3 discharge,

$$\Delta V_{C3} = 1\% \text{ of initial } V_{C3} \text{ level}$$

$$V_{C3} \approx V_{CC} = 15 \text{ V}$$

$$\Delta V_{C3} = \frac{15 \text{ V}}{100} = 0.15 \text{ V}$$

and C_3 discharge current is equal to $I_1 = 8 \text{ mA}$.

$$C_3 = \frac{I_1 t}{\Delta V_{C3}} = \frac{8 \text{ mA} \times 1 \text{ ms}}{0.15 \text{ V}}$$

$$= 53 \mu\text{F} \quad (\text{use } 56 \mu\text{F standard capacitance value})$$

R_B and C_2 are calculated in the same way as for Example 7-1.

Note that the recharge path for C_3 is via D_1 and R_E in the circuit of Figure 7-10(a). Using Equation (2-2) and the component values from Example 7-6, it is found that the time required to recharge C_3 by ΔV_{C3} of 0.15 V is approximately 0.6 ms. This means that the time interval between ramp outputs (and between input pulses) should be not less than 0.6 ms. Where Q_2 is replaced by a *complementary emitter follower* or *voltage follower* (see Sec. 7-7), the recharge time for C_3 is usually small enough to be ignored.

7-7 IC BOOTSTRAP RAMP GENERATOR

An IC operational amplifier (see Sec. 5-4) connected as a *voltage follower* forms part of the bootstrap ramp generator in Figure 7-11. When an operational amplifier is used as a voltage follower, the inverting input

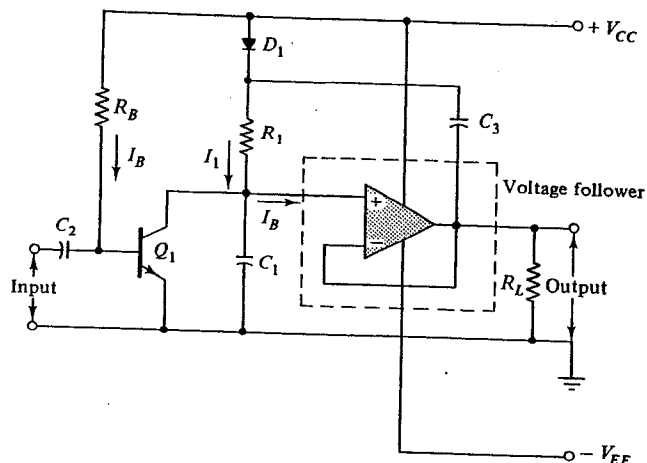


FIGURE 7-11. Bootstrap ramp generator using an IC operational amplifier.

terminal is connected directly to the output. The input signal is applied at the noninverting input.

The operation of the voltage follower can best be understood if it is assumed that both input terminals are initially at ground level. The output is also at ground level at this time. *Note that the output from an operational amplifier is the amplified voltage difference between the two input terminals.* Now, suppose an input of 1 V is applied at the noninverting terminal. Since the amplifier has a very large gain, the output tends to move positively towards the saturation level. However, as the output increases positively, the voltage at the inverting terminal also increases positively. When the inverting terminal voltage equals the noninverting terminal voltage (*i.e.*, 1 V), there is no longer any voltage difference between the two input terminals. Consequently, there is no longer an input signal, and the output voltage ceases to increase. Thus, the output voltage *follows* the input very closely.

Actually, there is a small voltage difference between the input terminals of a voltage follower. This difference is equal to the output voltage divided by the amplifier gain. For a 741 with an output of 10 V, the input difference would be typically:

$$\frac{10 \text{ V}}{200,000} = 50 \mu\text{V}$$

This means that the output voltage is only 50 μV behind the input voltage. This is a big improvement on the transistor emitter follower, where V_o is typically 0.7 V behind V_i .

It is seen that the voltage follower is an amplifier with a gain of 1, and that the output closely follows the input. The voltage follower also has the high input impedance and low output impedance characteristic of the IC operational amplifier.

The circuit of the IC operational amplifier bootstrap generator is almost exactly like that of the transistor bootstrap circuit. The voltage follower takes the place of the emitter follower. Note that although a $\pm V$ supply is still required, the load resistance R_L now can be grounded. Also note that the output ramp starts at $V_{CE(\text{sat})}$ instead of at $V_{CE(\text{sat})} - V_{BE}$. The low input current to the operational amplifier has an almost negligible effect on the charging current to C_1 in the IC bootstrap circuit of Figure 7-11. In fact, the reverse leakage current of D_1 (when it is reverse-biased) is much more significant than the input bias current of the amplifier. Using a 1N914 diode (Appendix 1), I_R is typically 3 μA . For the 741, the maximum input bias current is 500 nA. (Note that for the transistor bootstrap circuit, I_R of D_1 is very much smaller than I_B of transistor Q_2 .) The leakage current of D_1 can be the starting point for the IC bootstrap circuit design. This results in a lower charging current to C_1 and in smaller values of C_1 , C_2 , and C_3 .

If D_1 leakage current is extremely small, the above approach may result in a very small charging current and consequently in a very small capacitance value for C_1 . The typical input capacitance for an oscilloscope is 30 pF. So C_1 should not be made small enough that the circuit performance is affected when an oscilloscope is connected to any part of it. As a minimum, C_1 should be selected approximately 1000 times greater than the typical 30 pF C_{in} of an oscilloscope. This will also ensure that C_1 is not affected by the *stray capacitance* of wiring, etc.

EXAMPLE 7-7.

Design a bootstrap ramp generator using a 741 operational amplifier. The specifications for the circuit are the same as those for the circuit of Example 7-6, with the exception that the time interval between input pulses is 0.1 ms.

solution

The circuit is shown in Figure 7-11.

$$R_L = 1 \text{ k}\Omega$$

$$I_R = 3 \mu\text{A} \quad (\text{when } D_1 \text{ is reverse-biased})$$

Allow 1% nonlinearity due to I_R :

$$\begin{aligned} I_1 &= 100 \times I_R \\ &= 100 \times 3 \mu\text{A} = 300 \mu\text{A} \\ C_1 &= \frac{I_1 t}{\Delta V} = \frac{I_1 \times (\text{Ramp time})}{V_P} \\ &= \frac{300 \mu\text{A} \times 1 \text{ ms}}{8 \text{ V}} \\ &= 0.0375 \mu\text{F} \quad (\text{use } 0.039 \mu\text{F standard value}) \end{aligned}$$

$$\begin{aligned} V_{R1} &= V_{CC} - V_{D1} - V_{CE(\text{sat})} \\ &= 15 \text{ V} - 0.7 \text{ V} - 0.2 \text{ V} \\ &= 14.1 \text{ V} \end{aligned}$$

$$\begin{aligned} R_1 &= \frac{V_{R1}}{I_1} = \frac{14.1 \text{ V}}{300 \mu\text{A}} \\ &= 47 \text{ k}\Omega \quad (\text{standard value}) \end{aligned}$$

For 1% nonlinearity due to C_3 discharge:

$$\Delta V_{C3} = 1\% \text{ of initial } V_{C3}$$

$$V_{C3} \approx V_{CC} = 15 \text{ V}$$

$$\Delta V_{C3} = \frac{15 \text{ V}}{100} = 0.15 \text{ V}$$

C_3 discharge current $= I_1 = 300 \mu\text{A}$

$$C_3 = \frac{I_1 t}{\Delta V_{C3}} = \frac{300 \mu\text{A} \times 1 \text{ ms}}{0.15 \text{ V}} = 2 \mu\text{F} \quad (\text{standard value})$$

Compare this to $C_3 = 56 \mu\text{F}$ for the transistor circuit of Example 7-6. The discharge time of C_1 is equal to one-tenth of the charge time. Therefore, the discharge current of C_1 is ten times greater than the charge current.

Minimum I_C of $Q_1 = 10 \times I_1$

$$= 10 \times 300 \mu\text{A} = 3 \text{ mA}$$

$$I_B = \frac{I_C}{h_{FE}} = \frac{3 \text{ mA}}{100}$$

$$= 30 \mu\text{A}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{15 \text{ V} - 0.7 \text{ V}}{30 \mu\text{A}}$$

$$= 477 \text{ k}\Omega \quad (\text{use } 470 \text{ k}\Omega \text{ standard value})$$

During the input pulse, $\Delta V_{C2} = 1.8 \text{ V}$ (see Example 7-1) and the charging current of C_2 can be expressed by

$$\begin{aligned} I &= \frac{V_{CC} - V_1}{R_B} = \frac{15 \text{ V} - (-3 \text{ V})}{470 \text{ k}\Omega} \\ &= 38 \mu\text{A} \end{aligned}$$

Thus,

$$\begin{aligned} C_2 &= \frac{It}{\Delta V} = \frac{38 \mu\text{A} \times 1 \text{ ms}}{1.8 \text{ V}} \\ &= 0.02 \mu\text{F} \quad (\text{standard value}) \end{aligned}$$

7-8 FREE-RUNNING RAMP GENERATOR

A bootstrap ramp generator may be made free-running by employing a Schmitt circuit to detect the output peak level and generate a capacitor discharge pulse. In the circuit shown in Figure 7-12(a) *pnp* transistor Q_1 discharges C_1 when the Schmitt circuit output is negative. Diode D_2 protects the base-emitter junction of Q_1 against excessive reverse bias when the Schmitt output is positive.

Consider the circuit waveforms shown in Figure 7-12(b). During the time that the Schmitt circuit output is positive, Q_1 remains off and C_1 charges; this provides a positive-going ramp output. When the ramp amplitude arrives at the UTP of the Schmitt circuit, the Schmitt output becomes negative. This causes I_{B1} to flow, biasing Q_1 on and discharging C_1 . As the voltage of capacitor C_1 falls, the ramp output also falls rapidly, and this continues until the Schmitt LTP is reached. The presence of D_2 makes the Schmitt circuit have an LTP close to ground (see Sec. 6-7.2). Therefore, when the ramp output falls to ground level, the Schmitt output goes positive again, switching Q_1 off and allowing ramp generation to commence again.

The free-running ramp generator can be synchronized with another waveform by means of negative pulses coupled via capacitor C_3 . The presence of the negative pulse lowers the UTP of the Schmitt circuit, so that the Schmitt output becomes negative, causing the ramp to go to zero when the synchronizing pulse is applied.

Potentiometer R_7 [Figure 7-12(c)] allows the charging current to C_1 to be adjusted, thus controlling the ramp length and the output frequency. In Figure 7-12(d) R_6 affords adjustment of the Schmitt UTP. This provides control of the ramp amplitude.

EXAMPLE 7-8

Design a free-running ramp generator with an output frequency of 1 kHz and an output amplitude in the range 0 V to 8 V. Use 741 operational amplifiers and a supply voltage of ± 15 V.

solution

Schmitt circuit. For an output of 0 V to 8 V, the Schmitt circuit must have an LTP of 0 V and a UTP of 8 V. Design the Schmitt circuit as explained in Section 6-7.

Bootstrap circuit. The bootstrap output should go from 0 V to 8 V over a time period of $1/1$ kHz. (i.e., 1 ms). Design the circuit as in Example 7-7, substituting a *pn*p transistor for Q_1 .

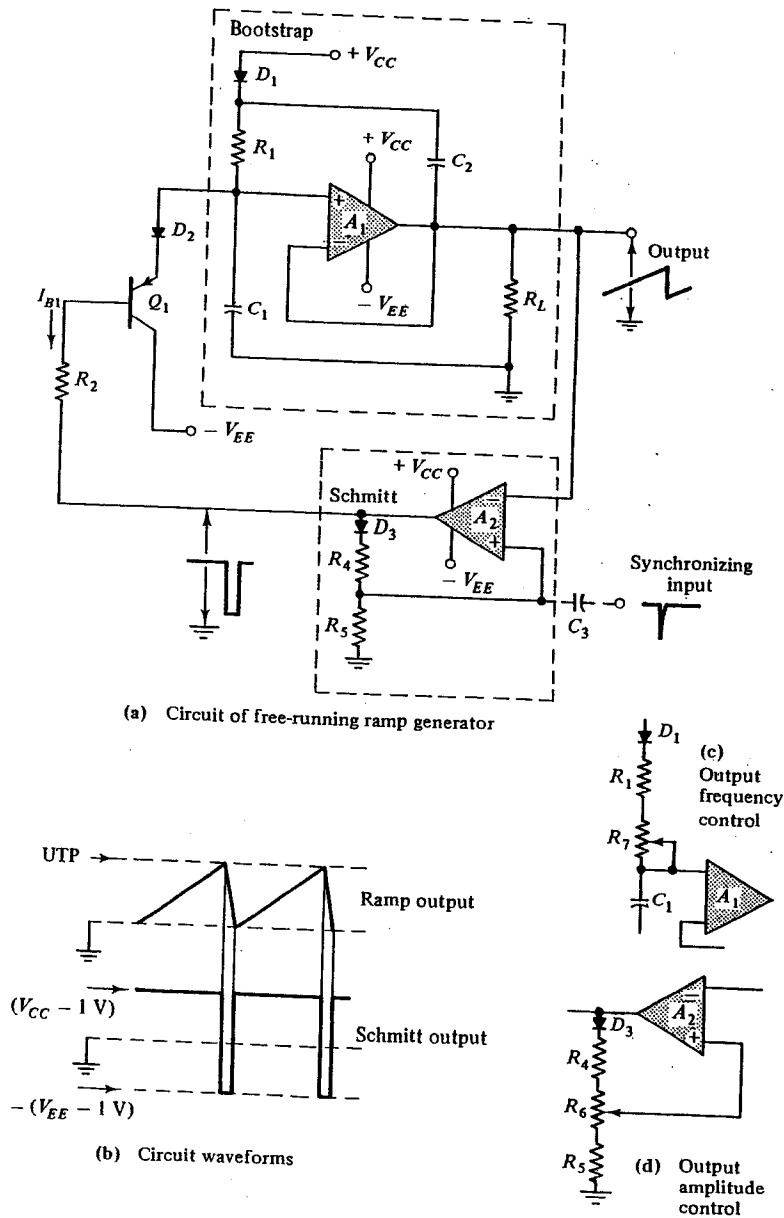


FIGURE 7-12. Free-running ramp generator circuit, circuit waveforms, and controls.

7-9 MILLER INTEGRATOR CIRCUIT

7-9.1 Miller Effect

Consider the circuit of Figure 7-13 in which an operational amplifier is connected as an *inverting amplifier*. Let the amplifier voltage gain be $-A_v$. Then,

$$V_O = -A_v V_i$$

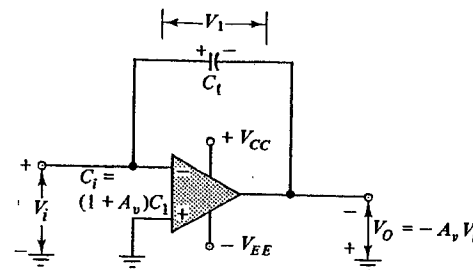


FIGURE 7-13. Miller effect or amplification of capacitance by inverting amplifier.

Note that because of the amplifier phase shift, the voltage at the left-hand terminal of C_1 increases by V_i , while that at the right-hand terminal of the capacitor decreases by $A_v V_i$ when V_i is positive. This results in a total capacitor voltage change of

$$\begin{aligned}\Delta V_1 &= V_i + A_v V_i \\ &= V_i(1 + A_v)\end{aligned}$$

Using the equation $Q = C \times \Delta V$, the charge supplied to the capacitor is

$$\begin{aligned}Q &= C_1 \times \Delta V_1 \\ &= C_1 \times V_i(1 + A_v)\end{aligned}$$

or

$$Q = (1 + A_v)C_1 \times V_i$$

Thus it appears that the input has supplied a charge to a capacitor with a value of $(1 + A_v)C_1$, instead of C_1 alone. Capacitance C_1 is said to have been *amplified* by a factor of $(1 + A_v)$. This is known as the *Miller effect*.

7-9.2 Miller Integrator

The *Miller integrator* utilizes the Miller effect to generate a linear ramp. In the circuit of Figure 7-14(a), a square wave input supplies charging current, alternatively positive and negative, to C_1 . The noninverting input terminal is grounded by a resistance R_2 equal to the resistance R_1 at the inverting input terminal. This is to ensure that the small bias currents cause equal voltage drops at each input terminal. Recall that, because of the very large gain of the operational amplifier, the voltage difference between the two input terminals is never greater than about $50 \mu\text{V}$. Thus, it can be said that the inverting input terminal is always very close to ground level. The inverting input terminal of an inverting amplifier is frequently termed a *virtual ground*, or *virtual earth*. Thus, the input voltage appears across R_1 , and the input current is simply V_i/R_1 , which remains constant.

If the input current I_1 is much greater than the input bias current of the amplifier, then I_1 will not flow into the amplifier. Instead, effectively all of I_1 flows through capacitor C_1 . For a positive input voltage, I_1 flows into C_1 , charging it positively on the left-hand side and negatively on the right-hand side [Figure 7-14(b)]. In this case the output voltage becomes negative, because the positive terminal, that is, the left-hand terminal, of the capacitor is held at the virtual ground level of the inverting input. A

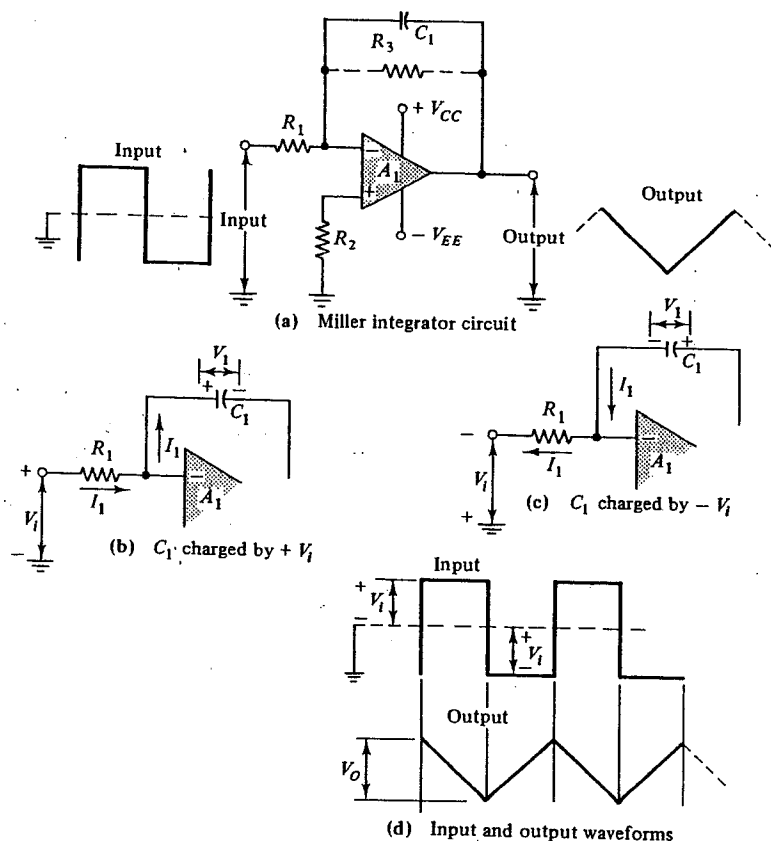


FIGURE 7-14. Miller integrator circuit, C_1 charging action, and waveforms.

negative input voltage produces a flow of current out of C_1 [Figure 7-14(c)]. Thus the capacitor is charged negatively on the left-hand side and positively on the right-hand side. Now the output becomes positive, because the negative terminal of the capacitor is held at virtual ground.

Since I_1 is a constant (+ or -) quantity, and since effectively all of I_1 flows through the capacitor, C_1 is charged linearly. Thus the output voltage changes linearly, providing either a positive or negative ramp. When the input voltage is positive, the output is a negative-going ramp. When the input is negative, a positive-going output ramp is generated. Therefore, when the input is a square wave, the output waveform is triangular. This is illustrated in Figure 7-14(d).

Consider the Miller circuit of Figure 7-14(a). If the input is supposed to be zero but is, say, $20\ \mu\text{V}$ away from ground level, then the output voltage could be $(A_v \times 20\ \mu\text{V}) = \pm(200,000 \times 20\ \mu\text{V}) = \pm 4\ \text{V}$. In this case the output is said to have *drifted* from its zero level. Even when the input terminal is maintained exactly at ground level, there could be a slight difference in the voltage at the amplifier inputs, due to small differences in the resistances of R_1 and R_2 , for example. Thus, because of the very high gain of the operational amplifier, its output voltage is very likely to drift from the zero level. The output voltage drift produces a charge on capacitor C_1 ; this charge gives the output an *offset* so that it is not symmetrical above and below ground (see Figure 7-15).

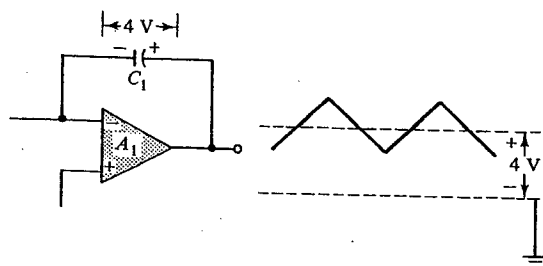


FIGURE 7-15. Effect of charge on C_1 due to output drift.

To minimize the output voltage drift, a large resistance [R_3 in Figure 7-14(a)] is connected between the output and the inverting input terminals. The effect of this resistance is to *cut down* the dc gain of the amplifier. When $R_3/R_1 = 10$, for example, the output drift will be only 10 times the input voltage difference. A ratio of 10:1 is typical for R_3/R_1 .

The presence of R_3 has the disadvantage that it affects the performance of the integrator at low frequencies. If the input frequency is so low that the capacitance impedance is very much larger than R_3 , then the capacitor has a negligible effect and the circuit will not function as an integrator. Therefore, C_1 should be selected so that

$$X_{C1} \ll R_3$$

As a lower limit, $X_{C1} = R_3/10$, so

$$\frac{1}{2\pi f C_1} = \frac{R_3}{10}$$

The lowest operating frequency of the integrator is

$$f = \frac{10}{2\pi C_1 R_3} \quad (7-3)$$

The design of a Miller integrator circuit begins with selection of the input current I_1 very much larger than the amplifier bias current. Then, R_1 is calculated as V_i/I_1 . From $C = It/V$, C_1 is determined using the desired output voltage, the time period, and the input current.

EXAMPLE 7-9

Design a Miller integrator circuit to produce a triangular waveform output with a peak-to-peak amplitude of 4 V. The input is a $\pm 10\ \text{V}$ square wave with a frequency of 250 Hz. Use a 741 operational amplifier with a supply of $\pm 15\ \text{V}$. Calculate the lowest operating frequency for the integrator.

solution

The circuit is shown in Figure 7-14(a). The 741 data sheet in Appendix 1-11 gives the input bias current as

$$I_B = 500\ \text{nA, maximum} \quad I_1 \gg I_B$$

Let

$$\begin{aligned} I_1 &= 1\ \text{mA} \\ R_1 &= \frac{V_i}{I_1} = \frac{10\ \text{V}}{1\ \text{mA}} \\ &= 10\ \text{k}\Omega \end{aligned}$$

Let

$$\begin{aligned} R_3 &= 10 R_1 = 100\ \text{k}\Omega \\ R_2 &= R_3 \parallel R_1 \approx 10\ \text{k}\Omega \end{aligned}$$

The ramp length is equal to one-half of the time period of the input, which is $1/(2f)$, or

$$t = \frac{1}{2 \times 250\ \text{Hz}} = 2\ \text{ms}$$

The ramp amplitude is equal to the peak-to-peak voltage output, which is 4 V.

$$C_1 = \frac{It}{\Delta V} = \frac{1 \text{ mA} \times 2 \text{ ms}}{4 \text{ V}} = 0.5 \mu\text{F}$$

Thus from Equation (7-3) the lowest operating frequency is

$$f = \frac{10}{2\pi \times 0.5 \mu\text{F} \times 100 \text{ k}\Omega} \\ = 32 \text{ Hz}$$

The circuit in Figure 7-16 shows a Miller integrator operating as a ramp generator. The negative-going pulse generates the positive ramp by producing current I_1 in the direction shown. At this time n -channel FET (Q_1) is biased *off* by the negative input pulse. When the input goes to ground level, I_1 goes to zero and Q_1 is switched *on*. Q_1 discharges C_1 and keeps it discharged until the input becomes negative again. If C_1 is to be discharged in one-tenth of the charge time, then Q_1 must be able to pass a

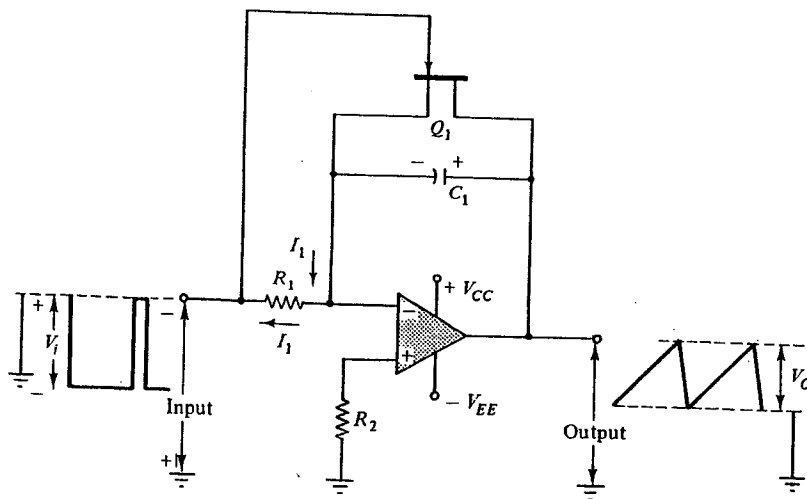


FIGURE 7-16. Miller integrator circuit as ramp generator.

current ten times greater than the charge current I_1 . To ensure that Q_1 is biased *off* when the input pulse is present, the input pulse must have a negative amplitude greater than the FET pinchoff voltage. Because the capacitor is completely discharged by the action of the FET, there is no need to include resistor R_3 [Figure 7-14(a)] in this circuit.

7-10 TRIANGULAR WAVEFORM GENERATOR

A free-running triangular waveform generator can be constructed, using the output of the Miller circuit in Figure 7-14(a) to generate its own square wave input. Consider the circuit in Figure 7-17(a). The Miller integrator circuit used is exactly as discussed in the last section. The output of the Miller circuit is fed directly to a noninverting Schmitt trigger circuit. The Schmitt is designed to have a positive UTP and a negative LTP (see Sec. 6-7.3), and its output is applied as an input to the Miller circuit.

Operation of the circuit is easily understood by considering the waveforms in Figure 7-17(b). At time t_1 the integrator output has reached the UTP (a positive voltage) and the noninverting Schmitt circuit output is positive at approximately $-(V_{EE} - 1 \text{ V})$. The positive voltage from the Schmitt causes current I_1 to flow into the Miller circuit, charging C_1 positive on the left-hand side. As C_1 charges in this direction, the integrator output is a negative-going ramp. The integrator continues to produce a negative-going ramp while its input is a positive voltage. At time t_2 , the integrator output arrives at the LTP (negative voltage). The Schmitt trigger circuit output now becomes negative and reverses the direction of I_1 . Thus the integrator output becomes a positive-going ramp. This positive-going ramp generation continues until the integrator output arrives at the UTP of the Schmitt circuit once again. Synchronizing pulses may be applied via C_2 to lower the trigger point of the Schmitt circuit, causing it to trigger before the ramp arrives at its normal peak level.

The circuit described above generates a triangular waveform with a constant peak-to-peak output amplitude and a constant frequency. The modifications shown in Figures 7-17(c) and (d) allow both frequency and amplitude adjustment. R_5 adjusts the UTP and LTP of the Schmitt circuit, and thus controls the peak-to-peak output amplitudes. R_6 affords adjustment of the input current to the integrator, and therefore controls the rate of charge of C_1 . This means that the ramp time period is controlled by adjusting R_6 .

In the design of a triangular waveform generator, each section must be treated separately.

EXAMPLE 7-10

Design a free-running triangular waveform generator to have a peak-to-peak output of 4 V at a frequency of 250 Hz. Use 741 operational amplifiers and a supply voltage of ± 15 V.

solution

Schmitt circuit. For 4 V, p-to-p, the Schmitt circuit $UTP = 2$ V and $LTP = -2$ V. A Schmitt circuit can be designed as in Example 6-6 to give these desired trigger points.

Miller integrator circuit. The input to the Miller circuit is the Schmitt output, that is, $\approx \pm 14$ V.

$$\text{Ramp amplitude} = 4 \text{ V}$$

$$\text{Ramp time period} = \frac{1}{2f} = \frac{1}{2 \times 250 \text{ Hz}} = 2 \text{ ms}$$

Design the Miller circuit as in Example 7-9.

When amplitude and frequency controls are employed with the circuit of Figure 7-17, a disadvantage is that the amplitude control affects the frequency. The frequency control Figure 7-17(d) sets the capacitor charging current through R_1 and R_6 at a constant level. Variation of the UTP and LTP of the Schmitt circuit has no effect on the rate of charge. Consequently, when the output amplitude is adjusted, for example from ± 2 V to ± 4 V, the time required for the capacitor to charge from -4 V to $+4$ V is twice that to charge from -2 V to $+2$ V. This means that the output frequency has been halved. The problem is solved by replacing the noninverting Schmitt with an inverting Schmitt trigger circuit and an inverting amplifier, as illustrated in Figure 7-18.

The amplifier has a gain of 1 when $R_7 = R_8$, and with the amplifier input terminal connected to moving contact of R_5 , the capacitor charging current is always proportional to the Schmitt trigger voltage. Thus, if the output voltage is doubled, the capacitor charging current is doubled, and the frequency is unaffected. In designing this circuit, the current through R_3 , R_4 and R_5 must be made much larger than that through R_7 and R_8 .

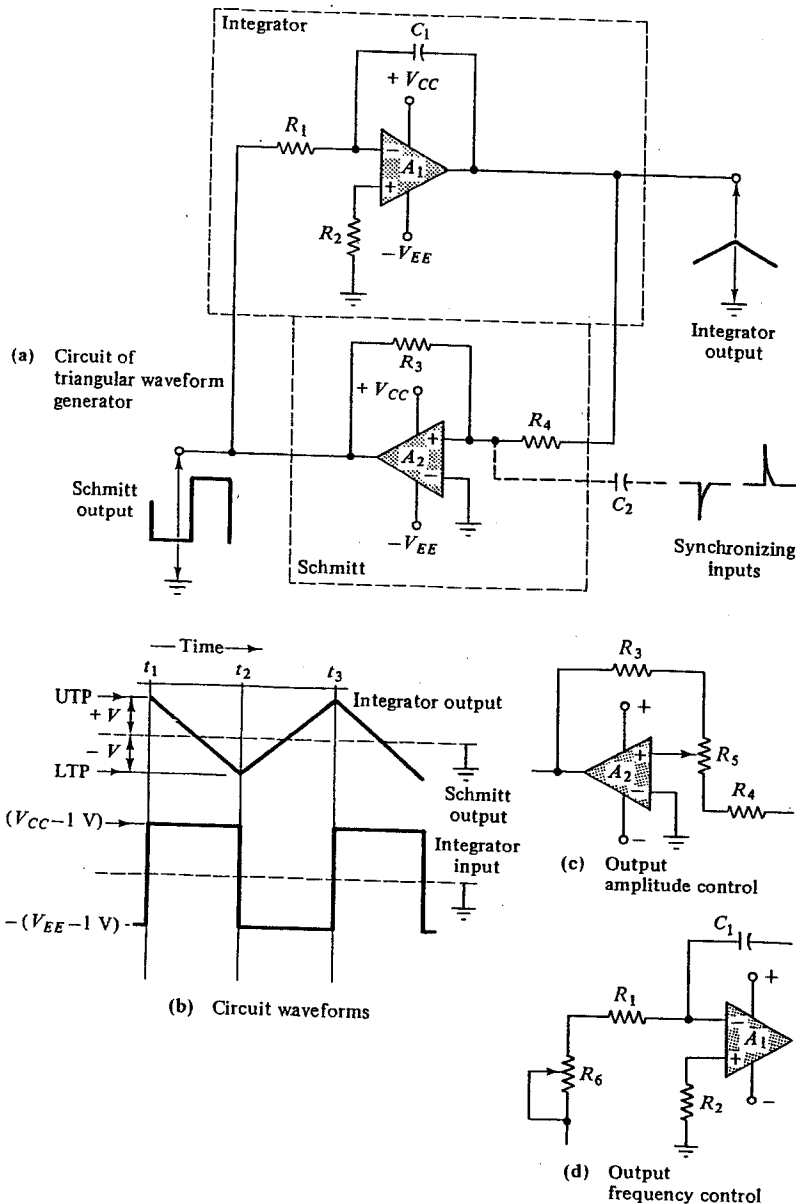


FIGURE 7-17. Triangular waveform generator circuit, circuit waveforms, and controls.

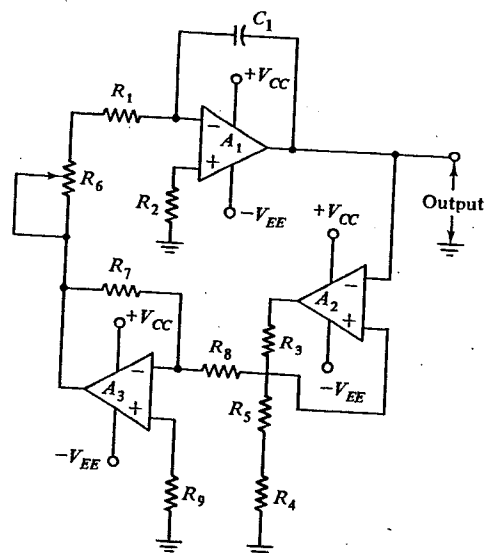


FIGURE 7-18. Triangular waveform generator with independent frequency and amplitude controls.

7-11 CRT TIME BASE

The need to synchronize a ramp generator is best understood by considering the time base for a cathode-ray oscilloscope. While the signal to be displayed provides vertical deflection of the electron beam, a ramp generator provides horizontal deflection. To obtain a correctly displayed signal, the electron beam must start at the left-hand side of the tube at the same instant that the input signal is going positive. Thus, the ramp must commence at this instant.

Figure 7-19 illustrates the process of obtaining synchronism of the ramp and the input signal. The signal normally is applied to a *vertical amplifier*, which controls the voltage on the vertical deflecting plates. This amplifier produces two equal output voltages, which are opposite in polarity, to the deflecting plates. One output is also fed to a Schmitt trigger which simply converts it to a square wave. The square wave is then *differentiated* to obtain a spike waveform, and the negative spikes are clipped off. This results in a series of positive spikes, each of which occurs exactly at the instant that the signal is entering its positive half-cycle.

REVIEW QUESTIONS AND PROBLEMS

20

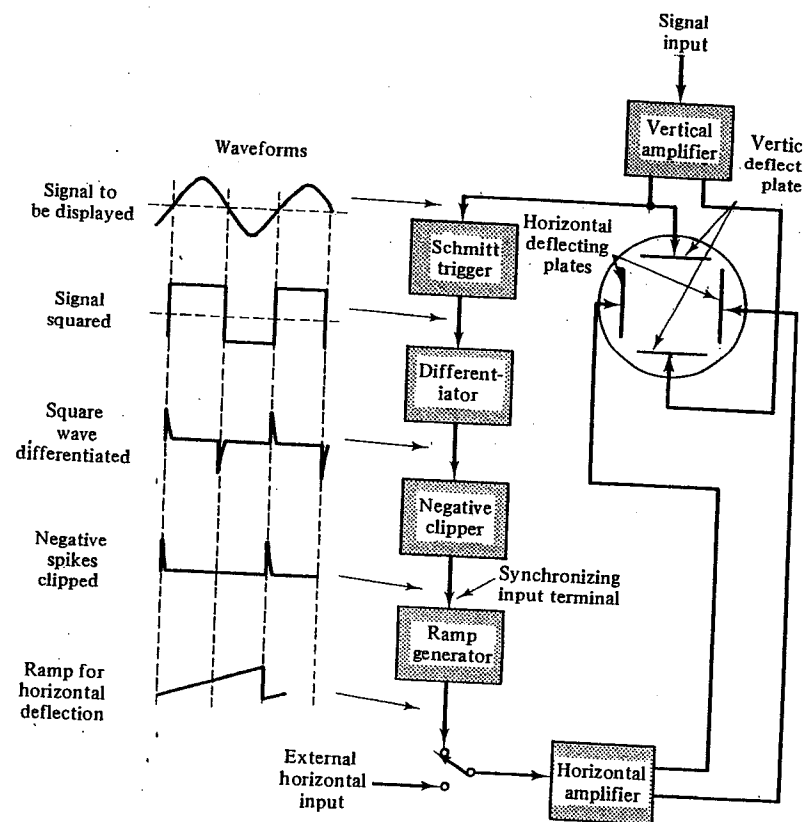


FIGURE 7-19. Automatic time base for cathode ray tube.

These spikes are fed to the ramp generator synchronizing input terminal causing the ramp to return instantaneously to its starting level.

REVIEW QUESTIONS AND PROBLEMS

- 7-1 Sketch the circuit of a simple CR ramp generator. Briefly explain its operation and its limitations. Also sketch the typical input and output waveforms.
- 7-2 Design a CR ramp generator to give an output of 3 V peak. The supply voltage is 20 V, and the load to be connected at the output is