TEXAS INSTRUMENTS
TX7316
SLOS950B – MAY 2019 – REVISED JULY 2019

TX7316 Three-Level, 16-Channel or Five-Level, 8-Channel Transmitter With 2.4-A Pulser, T/R Switch, and Integrated Transmit Beamformer

1 Features

- Transmitter supports:
  - 16-channel 3-level or 8-channel 5-level pulser and active transmit/receive (T/R) switch
  - Very low power on-chip beamforming mode (5-level mode):
    - In receive-only mode: 17 mW
    - In transmit-receive mode: 598 mW
    - In CW mode (0.6-A mode): 1.97 W
    - In global power-down mode: 4.3 mW
- 3-level, 5-level pulser:
  - Maximum output voltage: ±100 V
  - Minimum output voltage: ±1 V
  - Maximum output current: 2.4 A to 0.6 A
  - Maximum clamp current: 1 A to 0.25 A (in 3-level mode)
  - Maximum clamp current: 2 A to 0.5 A (in 5-level mode)
  - Second harmonic of –45 dBc at 5 MHz
  - CW mode jitter: 100 fs measured from 100 Hz to 20 kHz
  - CW mode close-in phase noise: –154 dBc/Hz at 1 kHz offset for 5 MHz signal
  - Supports 4.8-A mode in 5-level mode
  - –3-dB Bandwidth with 1-kΩ || 240-pF load
    - 20 MHz (For ±100-V supply in 2.4-A mode)
    - 36 MHz (For ±100-V supply in 4.8-A mode)
    - 25 MHz (For ±70-V supply in 2.4-A mode)
- Active transmit/receive (T/R) switch with:
  - ON/OFF control signal
  - Turnon resistance of 12 Ω
  - Bandwidth: 50 MHz
  - HD2: -50 dBc
  - Turnon time: 0.5 µs
  - Turnoff time: 1.75 µs
  - Transient glitch: 50 mV_{PP}
- Off-chip beam former with:
  - Jitter cleaning using synchronization feature
  - Maximum synchronization clock frequency: 200 MHz
- On-chip beam former with:
  - Delay resolution: one beamformer clock period, minimum 5 ns
  - Maximum delay: 2^{13} beamformer clock period
  - Maximum beamformer clock speed: 200 MHz
  - On-chip RAM to store
    - 16 Delay profiles
    - 48/28 pattern-profiles for 3- or 5-level mode
- High-speed (100 MHz maximum) 1.8-V and 2.5-V CMOS serial programming interface
- Automatic thermal shutdown
- No specific power sequencing requirement in 3-level mode
- Small package: NFBGA-216 (15 mm × 10 mm) with 0.8-mm pitch

2 Applications

- Ultrasound imaging system
- Piezoelectric driver
- In-probe ultrasound imaging

3 Description

The TX7316 is a highly integrated, high-performance transmitter solution for ultrasound imaging system. The device has total 16 pulser circuits (PULS), 16 transmit/receive (T/R) switches, and supports both on-chip and off-chip beamformer (TxBF). The device also integrates on-chip floating power supplies that reduce the number of required high voltage power supplies.

Device Information(1)

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TX7316	NFBGA (216)	15.0 mm × 10.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

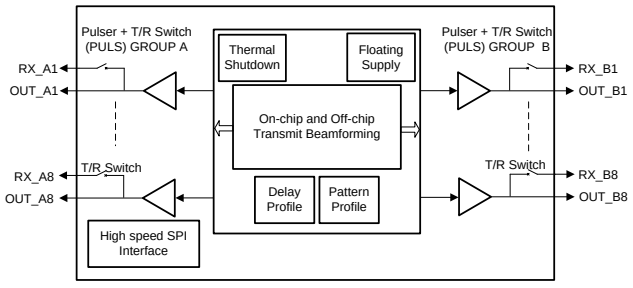


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description (continued) ... 4
6 Pin Configuration and Functions ... 5
7 Specifications ... 10
7.1 Absolute Maximum Ratings ... 10
7.2 ESD Ratings ... 10
7.3 Recommended Operating Conditions ... 10
7.4 Thermal Information ... 11
7.5 Electrical Characteristics ... 12
7.6 Digital Characteristics ... 15
7.7 Timing Requirements ... 16
7.8 Typical Characteristics ... 18
8 Detailed Description ... 23
8.1 Overview ... 23
8.2 Functional Block Diagram ... 24
8.3 Feature Description ... 24
8.4 Device Functional Modes ... 61
8.5 Programming ... 63
8.6 Register Maps ... 67
9 Application and Implementation ... 107
9.1 Application Information ... 107
9.2 Typical Applications ... 112
9.3 Application Curves ... 117
9.4 Do's and Don'ts ... 120
9.5 Initialization Set Up ... 120
10 Power Supply Recommendations ... 122
10.1 3-level mode ... 122
10.2 5-Level Mode ... 122
11 Layout ... 123
11.1 Layout Guidelines ... 123
11.2 Layout Examples ... 124
12 Device and Documentation Support ... 127
12.1 Trademarks ... 127
12.2 Electrostatic Discharge Caution ... 127
12.3 Glossary ... 127
13 Mechanical, Packaging, and Orderable Information ... 127
13.1 Package Option Addendum ... 131

4 Revision History

Changes from Revision A (May 2019) to Revision B **Page**

- Changed *Feature*: In CW mode: 2.98 W To: In CW mode (0.6-A mode): 1.97 W ... 1
- Changed *Feature*: Second harmonic of –40 dBc at 5 MHz To: Second harmonic of –45 dBc at 5 MHz ... 1
- Added *Feature*: 36 MHz (For ±100-V supply in 4.8-A mode) ... 1
- Changed *Feature*: Turnoff time: 1.6 µs To: Turnoff time: 1.75 µs. ... 1
- Added sentence to the description of *BIAS_2P5, FLOATM_HV_A1, FLOATM_HV_A2, FLOATM_HV_B1, FLOATM_HV_B2, FLOATP_HV_A1, FLOATP_HV_A2, FLOATP_HV_B1,* and *FLOATP_HV_B2* pins. ... 6
- Changed the nominal value of *default power mode* of f_{SYNC} from *5 kHz* to *10 kHz* in *Recommended Operating Conditions* table. ... 11
- Changed the nominal value of $HD2_{PUL}$ from *40 dBc* to *45 dBc* in *Electrical Characteristics* table. ... 13
- Changed the test conditions of CT_{TR} in *Electrical Characteristics* table. ... 13
- Added 0.6-A mode and the relevant values to all parameters within *POWER DISSIPATION IN 5-LEVEL, CW-MODE* in *Electrical Characteristics* table. ... 14
- Changed the third table note in *Electrical Characteristics* table. ... 14
- Added t_{GBL_DYN} parameter in *Electrical Characteristics* table. ... 14
- Changed *FFT of Pulse Inversion* figure. ... 18
- Changed the *PRF* value from *5 kHz* to *10 kHz* across the document. ... 30
- Changed *Pulser Control Signal Logic for Group A Pulser* table. ... 40
- Changed *Pulser Control Signal Logic for Group B Pulser* table. ... 40
- Added Note. ... 41
- Changed *Pulser Control Signal Logic* table. ... 41
- Added Note. ... 42
- Changed from *BF_PROF_G2* to *BF_PROF_SEL_G2* in *Delay Profile* section. ... 54
- Changed *Pattern Profile Mapping* figure. ... 55
- Deleted the last sentence of the second list item in *T/R Switch Control in On-Chip Beam-Forming Mode* section. ... 57

Revision History (continued)

- Changed the description in *Full Timing Diagram For On-chip Beamforming Mode* section. ... 59
- Changed *4A Mode* section To: *4.8-A Mode* section. ... 61
- Changed bits *4A_CNTRL_1* and *4A_CNTRL_2* to bits *4A_MODE_CNTRL_1* and *4A_MODE_CNTRL _2* in *4.8-A Mode* section. ... 61
- Changed from *PDN_PUL_An_Bn* to *PDN_PUL_An* in *Pulser Power Down* section. ... 61
- Changed the description in *Thermal Shutdown* section. ... 62
- Changed from *before* to *for* in *Powering Up the Device from Global Power Down Mode* section. ... 62
- Changed from *Yes* to *No* for *Channel Power Down* in *Register Maps Range* table. ... 67
- Changed *Register 0Bh Field Descriptions*. ... 72
- Changed *Register 14h Field Descriptions*. ... 74
- Changed the value of Field from *PAT_SEL_A3* to *PAT_SEL_A2* for *registers 13-8* in *Register 1Fh Field Descriptions*. ... 82
- Changed *Register 21h to 9Fh (offset = 21h to 9Fh) [reset = 21h to 9Fh]* section. ... 91
- Changed *Register 21h to 5Fh (offset = 21h to 5Fh) [reset = 21h to 5Fh]* section. ... 93
- Changed the name of the figure from *Elastography Data* to *Repeatability Data* ... 109
- Changed the name of the figure from *FFT of Different Points on Elastogrpahy Output* to *FFT of Different Points on Repeatability Waveform* ... 110
- Added *Power Supply Design* section. ... 110
- Changed the number of channels from *32* to *16* in *CW Mode* section. ... 111
- Changed from: 4x1uF cap pf 100V rating To: 4x1µF cap of 100V rating pin AVDDM_HVA_A in the *Schematic Checklist* table. ... 117
- Changed |*ABDDP/M_HV_A*| from |*AVDDP/M_HV_A*| in *Application Curves* section. ... 117
- Changed |*ABDDP/M_HV_B*| from |*AVDDP/M_HV_B*| in *Application Curves* section. ... 118
- Changed *Package Outline* details. ... 128

Changes from Original (May 2019) to Revision A **Page**

- Changed the document status From: *Advanced Information* To: *Production* data ... 1
- Changed from Pulsar to Pulser across the document. ... 1
- Changed the values of *CW* and *global power-down* modes ... 1
- Changed the supply voltage value in *–3-dB Bandwidth with 1-kΩ || 240-pF load* feature. ... 1
- Changed *Pulser Output Waveform* figure. ... 17
- Added *Typical Characteristics* section and details about the figures in *Application Curves* section. ... 18
- Changed *Note*. ... 59
- Added *4A Mode* section. ... 61

5 Description (continued)

The TX7316 (referred to as device in this data sheet) has a pulser circuit that generates three-level high voltage pulses (up to ±100 V) that can be used to excite multiple channels of an ultrasound transducer. The device supports total 8 outputs for 5-level mode and 16 outputs for 3-level mode. The maximum output current is configurable from 2.4 A to 0.6 A.

A T/R switch under OFF state protects the receiver circuit by providing high isolation between the high-voltage transmitter and the low-voltage receiver when the pulser is generating high-voltage pulses. When the transducer is receiving echo signals, the T/R switch turns ON and connects the transducer to the receiver. The ON/OFF operation of the T/R switch is either controlled by an external pin or controlled by on-chip beamforming engine in the device. The T/R switch offers 12-Ω impedance in the ON state.

Ultrasound transmission relies on the excitation of multiple transducer elements with the delay profile of the excitation across the different elements defining the direction of the transmission. Such an operation is referred to as transmit beamforming. The TX7316 supports staggered pulsing of the different channels, allowing for transmit beamforming. The device supports both off-chip and on-chip beamforming operation.

In the off-chip beamformer mode, the output transition of each pulser and TR switch ON/OFF operation is controlled by external control pins. To eliminate the effect of jitter from the external control signals, the device supports a synchronization feature. When the synchronization feature is enabled, the external control signals are latched using a low-jitter beamformer clock signal.

In the on-chip beamformer mode, the delay profile for the pulsing of the different channels is stored within the device. The device supports a transmit beamformer delay resolution of one beamformer clock period and a maximum delay of 2^{13} beamformer clock periods. An internal pattern generator generates the output pulse patterns based on pattern profiles stored in a profile RAM. Up to 16 beamforming profiles and 48/28 pattern profiles for 3/5-level mode can be stored in the profile RAM. On-chip beamforming mode reduces the number of control signals that must be routed from the FPGA to the device.

TX7316 is available in a 15-mm × 10-mm 216-pin NFBGA package (ZCX package) and is specified for operation from 0°C to 70°C.

6 Pin Configuration and Functions

ZCX Package
260-Pin NFBGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12
A	RX_B8	AVSS	AVSS	AVSS	AVSS	IN_A7_1	FLOATM_HV_B2	AVDDP_5	FLOATP_HV_B2	OUT_A8	OUT_B8	OUT_B8
B	RX_B7	AVSS	AVSS	AVSS	AVSS	IN_A7_0	AVDDM_HV_B	AVDDM_5	AVDDP_HV_B	OUT_A8	OUT_B7	OUT_B7
C	RX_B6	AVSS	AVSS	AVSS	AVSS	IN_A6_1	AVDDM_HV_B	AVSS	AVDDP_HV_B	AVSS	OUT_A7	OUT_A7
D	RX_B5	AVSS	AVSS	AVSS	AVSS	IN_A6_0	IN_B6_1	IN_B6_0	IN_B8_0	AVSS	OUT_B6	OUT_B6
E	RX_A8	AVSS	AVSS	AVSS	AVSS	IN_A5_1	IN_A8_1	IN_B5_1	IN_B8_1	AVSS	OUT_A6	OUT_A6
F	RX_A7	AVSS	STDBY	AVSS	AVSS	IN_A5_0	IN_A8_0	IN_B5_0	IN_B7_1	AVDDM_HV_A	AVDDM_HV_A	FLOATM_HV_A2
G	RX_A6	AVSS	BIAS_2P5	AVSS	AVSS	TR_EN4	TR_EN3	LVL_3Z_5	IN_B7_0	AVSS	OUT_B5	OUT_B5
H	RX_A5	AVSS	BIAS_2P5	AVSS	AVSS	AVSS	DSEL_0	DSEL_1	AVSS	AVSS	OUT_A5	OUT_A5
J	BF_CLKP	TR_BF_SYNCP	AVDDP_5	AVSS	SEN_GRP1	SDATA_GRP2	AVDDM_5	AVDDM_5	AVSS	AVDDP_HV_A	AVDDP_HV_A	FLOATP_HV_A2
K	BF_CLKM	TR_BF_SYNCM	AVDDP_5	SEN_GRP2	SCLK	SDOUT	SDATA_GRP1	AVDDP_5	AVSS	AVDDP_HV_B	AVDDP_HV_B	FLOATP_HV_B1
L	RX_B4	AVSS	AVDD_IO	AVSS	AVSS	SHUTZ	RESET	AVDDP_5	AVSS	AVSS	OUT_B4	OUT_B4
M	RX_B3	AVSS	CW_EN	AVSS	AVSS	TR_EN2	TR_EN1	RESYNC	IN_B4_1	AVSS	OUT_A4	OUT_A4
N	RX_B2	AVSS	AVSS	AVSS	AVSS	IN_A3_1	IN_B2_1	IN_B2_0	IN_B4_0	AVDDM_HV_B	AVDDM_HV_B	FLOATM_HV_B1
P	RX_B1	AVSS	AVSS	AVSS	AVSS	IN_A3_0	IN_A4_1	IN_B1_1	IN_B3_1	AVSS	OUT_B3	OUT_B3
R	RX_A4	AVSS	AVSS	AVSS	AVSS	IN_A2_1	IN_A4_0	IN_B1_0	IN_B3_0	AVSS	OUT_A3	OUT_A3
T	RX_A3	AVSS	AVSS	AVSS	AVSS	IN_A2_0	AVDDM_HV_A	AVSS	AVDDP_HV_A	AVSS	OUT_B2	OUT_B2
U	RX_A2	AVSS	AVSS	AVSS	AVSS	IN_A1_1	AVDDM_HV_A	AVDDM_5	AVDDP_HV_A	OUT_B1	OUT_A2	OUT_A2
V	RX_A1	AVSS	AVSS	AVSS	AVSS	IN_A1_0	FLOATM_HV_A1	AVDDP_5	FLOATP_HV_A1	OUT_B1	OUT_A1	OUT_A1

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDDM_5	B8, J7, J8, U8	P	Low voltage negative supply pin, -5V
AVDDM_HV_A	F10, F11, T7, U7	P	High voltage negative supply pin for group A pulser, for example -100V
AVDDM_HV_B	B7, C7, N10, N11	P	High voltage negative supply pin for group B pulser, for example -100V
AVDDP_5	A8, J3, K8, K3, L8, V8	P	Low voltage positive supply pin, 5V
AVDDP_HV_A	J10, J11, T9, U9	P	High voltage positive supply pin for group A pulser, for example 100V
AVDDP_HV_B	B9, C9, K10, K11	P	High voltage positive supply pin for group B pulser, for example 100V
AVDD_IO	L3,	P	Digital IO supply pin, 2.5V or 1.8 V

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
AVSS	A2, A3, A4, A5, B2, B3, B4, B5, C2, C3, C4, C5, C8, C10, D2, D3, D4, D5, D10, E2, E3, E4, E5, E10, F2, F4, F5, G2, G4, G5, G10, H2, H4, H5, H6, H9, H10, J4, J9, K9, L2, L4, L5, L9, L10, M2, M4, M5, M10, N2, N3, N4, N5, P2, P3, P4, P5, P10, R2, R3, R4, R5, R10, T2, T3, T4, T5, T8, T10, U2, U3, U4, U5, V2, V3, V4, V5	—	Ground pin
BF_CLKM	K1	I	Differential clock input for the beam former clock, (negative) with internal 5-kΩ common mode force resistor. A single-ended clock is also supported. Connect BF_CLKM to AVDDP_5 when using a single-ended clock.
BF_CLKP	J1	I	Differential clock input for the beam former clock, (positive) with internal 5-kΩ common mode force resistor. A single-ended clock is also supported. Connect clock to BF_CLKP pin when using a single-ended clock. In single-ended mode BF_CLKP pin has an internal 10-kΩ resistor to AVDDP_5.
BIAS_2P5	G3, H3	O	Bypass to ground with 0.1-µF capacitor. The capacitor should have a voltage rating greater than 6 V. **Must short pin G3 and H3**.
CW_EN	M3	I	CW mode enable pin; active high. This pin has an internal 50-kΩ pulldown resistor to ground.(1)
DSEL_0	H7	I	Pulser's output stage current drive selection pin. This pin has an internal 50-kΩ pulldown resistor to ground.(1)
DSEL_1	H8	I	Pulser's output stage current drive selection pin. This pin has an internal 50-kΩ pulldown resistor to ground.(1)
FLOATM_HV_A1	V7	O	Bypass to supply AVDDM_HV_A with 2 × 0.27-µF capacitor. The capacitor should have a voltage rating greater than 6 V.
FLOATM_HV_A2	F12	O	Bypass to supply AVDDM_HV_A with 2 × 0.27-µF capacitor. The capacitor should have a voltage rating greater than 6 V.
FLOATM_HV_B1	N12	O	Bypass to supply AVDDM_HV_B with 2 × 0.27-µF capacitor. The capacitor should have a voltage rating greater than 6 V.
FLOATM_HV_B2	A7	O	Bypass to supply AVDDM_HV_B with 2 × 0.27-µF capacitor. The capacitor should have a voltage rating greater than 6 V.
FLOATP_HV_A1	V9	O	Bypass to supply AVDDP_HV_A with 2 × 0.27-µF capacitor. The capacitor should have a voltage rating greater than 6 V.
FLOATP_HV_A2	J12	O	Bypass to supply AVDDP_HV_A with 2 × 0.27-µF capacitor. The capacitor should have a voltage rating greater than 6 V.
FLOATP_HV_B1	K12	O	Bypass to supply AVDDP_HV_B with 2 × 0.27-µF capacitor. The capacitor should have a voltage rating greater than 6 V.
FLOATP_HV_B2	A9	O	Bypass to supply AVDDP_HV_B with 2 × 0.27-µF capacitor. The capacitor should have a voltage rating greater than 6 V.

(1) 2.5 V or 1.8 V logic is supported depending upon voltage set at AVDD_IO pin.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
IN_A1_0	V6	I	Output level control pin for channel 1, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A1_1	U6	I	Output level control pin for channel 1, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A2_0	T6	I	Output level control pin for channel 2, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A2_1	R6	I	Output level control pin for channel 2, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A3_0	P6	I	Output level control pin for channel 3, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A3_1	N6	I	Output level control pin for channel 3, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A4_0	R7	I	Output level control pin for channel 4, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A4_1	P7	I	Output level control pin for channel 4, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A5_0	F6	I	Output level control pin for channel 5, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A5_1	E6	I	Output level control pin for channel 5, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A6_0	D6	I	Output level control pin for channel 6, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A6_1	C6	I	Output level control pin for channel 6, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A7_0	B6	I	Output level control pin for channel 7, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A7_1	A6	I	Output level control pin for channel 7, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A8_0	F7	I	Output level control pin for channel 8, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_A8_1	E7	I	Output level control pin for channel 8, group A pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B1_0	R8	I	Output level control pin for channel 1, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B1_1	P8	I	Output level control pin for channel 1, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B2_0	N8	I	Output level control pin for channel 2, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B2_1	N7	I	Output level control pin for channel 2, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B3_0	R9	I	Output level control pin for channel 3, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B3_1	P9	I	Output level control pin for channel 3, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B4_0	N9	I	Output level control pin for channel 4, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B4_1	M9	I	Output level control pin for channel 4, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B5_0	F8	I	Output level control pin for channel 5, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B5_1	E8	I	Output level control pin for channel 5, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B6_0	D8	I	Output level control pin for channel 6, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)

(2) In on-chip beam forming mode, connect to AVSS.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
IN_B6_1	D7	I	Output level control pin for channel 6, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B7_0	G9	I	Output level control pin for channel 7, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B7_1	F9	I	Output level control pin for channel 7, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B8_0	D9	I	Output level control pin for channel 8, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
IN_B8_1	E9	I	Output level control pin for channel 8, group B pulser; active only in off-chip beam forming mode. This pin has an internal 50-kΩ pulldown resistor to ground.(1) (2)
LVL_3Z_5	G8	I	Pulser level mode control pin. Connect to ground for 3-level mode, connect to AVDDP_5 for 5-level mode. This pin has an internal 50-kΩ pulldown resistor to ground. Only 5V logic is supported.
OUT_A1	V11, V12	O	Group A, channel 1 pulser output.
OUT_A2	U11, U12	O	Group A, channel 2 pulser output.
OUT_A3	R11, R12	O	Group A, channel 3 pulser output.
OUT_A4	M11, M12	O	Group A, channel 4 pulser output.
OUT_A5	H11, H12	O	Group A, channel 5 pulser output.
OUT_A6	E11, E12	O	Group A, channel 6 pulser output.
OUT_A7	C11, C12	O	Group A, channel 7 pulser output.
OUT_A8	A10, B10	O	Group A, channel 8 pulser output.
OUT_B1	U10, V10	O	Group B, channel 1 pulser output.
OUT_B2	T11, T12	O	Group B, channel 2 pulser output.
OUT_B3	P11, P12	O	Group B, channel 3 pulser output.
OUT_B4	L11, L12	O	Group B, channel 4 pulser output.
OUT_B5	G11, G12	O	Group B, channel 5 pulser output.
OUT_B6	D11, D12	O	Group B, channel 6 pulser output.
OUT_B7	B11, B12	O	Group B, channel 7 pulser output.
OUT_B8	A11, A12	O	Group B, channel 8 pulser output.
RESET	L7	I	Hardware reset pin with an internal 50-kΩ pulldown resistor to ground; active high.(1)
RESYNC	M8	I	Active high re-synchronization enable control pin – enables latching of the external control signals using a low-jitter beamformer clock in the Off-chip beamformer mode. This pin has an internal 50-kΩ pulldown resistor to ground. Always connect RESYNC pin to '1' when device is configured in on-chip beam-forming mode. (1)
RX_A1	V1	O	Group A, channel 1 T/R switch low voltage side output, connect to input of receiver
RX_A2	U1	O	Group A, channel 2 T/R switch low voltage side output, connect to input of receiver
RX_A3	T1	O	Group A, channel 3 T/R switch low voltage side output, connect to input of receiver
RX_A4	R1	O	Group A, channel 4 T/R switch low voltage side output, connect to input of receiver
RX_A5	H1	O	Group A, channel 5 T/R switch low voltage side output, connect to input of receiver
RX_A6	G1	O	Group A, channel 6 T/R switch low voltage side output, connect to input of receiver
RX_A7	F1	O	Group A, channel 7 T/R switch low voltage side output, connect to input of receiver
RX_A8	E1	O	Group A, channel 8 T/R switch low voltage side output, connect to input of receiver
RX_B1	P1	O	Group B, channel 1 T/R switch low voltage side output, connect to input of receiver
RX_B2	N1	O	Group B, channel 2 T/R switch low voltage side output, connect to input of receiver
RX_B3	M1	O	Group B, channel 3 T/R switch low voltage side output, connect to input of receiver
RX_B4	L1	O	Group B, channel 4 T/R switch low voltage side output, connect to input of receiver
RX_B5	D1	O	Group B, channel 5 T/R switch low voltage side output, connect to input of receiver
RX_B6	C1	O	Group B, channel 6 T/R switch low voltage side output, connect to input of receiver
RX_B7	B1	O	Group B, channel 7 T/R switch low voltage side output, connect to input of receiver

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RX_B8	A1	O	Group B, channel 8 T/R switch low voltage side output, connect to input of receiver
SCLK	K5	I	High-speed SPI interface clock pin. This pin has an internal 50-kΩ pulldown resistor to ground.(1)
SDATA _GRP1	K7	I	High-speed SPI interface data pin for group1 channel. This pin has an internal 100-kΩ pulldown resistor to ground.(1)
SDATA_GRP2	J6	I	High-speed SPI interface data pin for group2 channel. This pin has an internal 100-kΩ pulldown resistor to ground.(1)
SDOUT	K6	O	High-speed SPI interface data out pin. This pin is in high impedance state by default. (1)
SEN_GRP1	J5	I	High-speed SPI interface enable pin for group1 channel. This pin has an internal 100-kΩ pulup resistor to AVDD_IO.(1)
SEN_GRP2	K4	I	High-speed SPI interface enable pin for group2 channel. This pin has an internal 100-kΩ pullup resistor to AVDD_IO.(1)
SHUTZ	L6	O	This pin functions as thermal shutdown flag open drain, active low output. When this pin is set to low, it indicates that channels of group 1 or group 2 or both the groups of the device is in power down mode because of high temperature. On SHUTZ pin connect an external 2-kΩ resistor to AVDD_IO supply. There is an internal 50-kΩ pullup resistor on this pin to AVDD_IO. (1)
STDBY	F3	I	Standby pin; active high . This pin has an internal 50-kΩ pulldown resistor to ground.
TR_BF_SYNCM	K2	I	Differential input (negative) for the synchronization of the on-chip beamformer operation. A single-ended input is also supported. Connect TR_BF_SYNCM to AVDDP_5 when using a single-ended input. In off-chip beamforming mode connect this pin to ground.
TR_BF_SYNCP	J2	I	Differential input (positive) for the synchronization of the on-chip beamformer operation. A single-ended input is also supported. Connect input to TR_BF_SYNCP pin when using a single-ended input mode. In single-ended mode TR_BF_SYNCP pin has an internal 10-kΩ resistor to AVDDP_5. In off-chip beamforming mode connect this pin to ground.
TR_EN1	M7	I	T/R switch enable control pin for T/R switch of channel A1 to channel A4; active high. This pin has an internal 100-kΩ pullup resistor to AVDD_IO.(1)
TR_EN2	M6	I	T/R switch enable control pin for T/R switch of channel B1 to channel B4; active high. This pin has an internal 100-kΩ pullup resistor to AVDD_IO.(1)
TR_EN3	G7	I	T/R switch enable control pin for T/R switch of channel A5 to channel A8; active high. This pin has an internal 100-kΩ pullup resistor to AVDD_IO.(1)
TR_EN4	G6	I	T/R switch enable control pin for T/R switch of channel B5 to channel B8; active high. This pin has an internal 100-kΩ pullup resistor to AVDD_IO.(1)

Table 1. Pin Name to Signal Name Map

SIGNAL NUMBER	PIN NAME	SIGNAL NAME
1	BF_CLKP–BF_CLKM	BF_CLK
2	TR_BF_SYNCP-TR_BF_SYNCM	TR_BF_SYNC
3	OUT_A1, OUT_A2, OUT_A3, OUT_A4 OUT_A5, OUT_A6, OUT_A7, OUT_A8	Group A Pulser
4	OUT_B1, OUT_B2, OUT_B3, OUT_B4 OUT_B5, OUT_B6, OUT_B7, OUT_B8	Group B Pulser
5	OUT_A1, OUT_A2, OUT_A3, OUT_A4, OUT_B1, OUT_B2, OUT_B3, OUT_B4, RX_A1, RX_A2, RX_A3, RX_A4, RX_B1, RX_B2, RX_B3, RX_B4	Group 1 channels
6	OUT_A5, OUT_A6, OUT_A7, OUT_A8, OUT_B5, OUT_B6, OUT_B7, OUT_B8, RX_A5, RX_A6, RX_A7, RX_A8, RX_B5, RX_B6, RX_B7, RX_B8	Group 2 channels
7	FLOATP_HV_A1, FLOATP_HV_B1, FLOATM_HV_A1, FLOATM_HV_B1	Group 1 LDOs
8	FLOATP_HV_A2, FLOATP_HV_B2, FLOATM_HV_A2, FLOATM_HV_B2	Group 2 LDOs

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	AVDD_IO	-0.3	5.5	V
	AVDDM_5	-5.5	0.3	V
	AVDDP_5	-0.3	5.5	V
	AVDDM_HV_A, AVDDM_HV_B	-105	0.3	V
	AVDDP_HV_A, AVDDP_HV_B	-0.3	105	V
Voltage at digital inputs		-0.3	5.5	V
Storage temperature, T_{stg}	Maximum junction temperature (T_J), any condition		105	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
SUPPLIES						
V_{IO}	AVDD_IO	For 1.8V I/O logic	1.7	1.8	1.9	V
		For 2.5V I/O logic	2.4	2.5	2.6	
V_{M_5}	AVDDM_5		-5.25	-5	-4.75	V
V_{P_5}	AVDDP_5		4.75	5	5.25	V
V_{MHV_A}	AVDDM_HV_A		-100		-1.5	V
V_{MHV_B}	AVDDM_HV_B, when AVDDM_HV_A is -100V		-100		-1.5	V
V_{PHV_A}	AVDDP_HV_A		1.5		100	V
V_{PHV_B}	AVDDP_HV_B, when AVDDP_HV_B is 100V		1.5		100	V
TEMPERATURE						
T_A	Ambient temperature		0		70	°C
BIAS VOLTAGES (1)						
	Common-mode voltage	BF_CLKM, BF_CLKP		2.5		V
	Bias Voltage	BIAS_2P5		2.5		V
	Floating Supplies	V_{MHV_A} - (FLOATM_HV_A1, FLOATM_HV_A2)		-5		V
		V_{MHV_B} - (FLOATM_HV_B1, FLOATM_HV_B2)		-5		V
		V_{PHV_A} - (FLOATP_HV_A1, FLOATP_HV_A2)		5		V
		V_{PHV_B} - (FLOATP_HV_B1, FLOATP_HV_B2)		5		V
BF_CLK INPUT						
f_{BF_CLK}	Minimum BF_CLK frequency			10		MHz
	Maximum BF_CLK frequency	In single ended mode		100		MHz
		In differential-mode, except on-chip CW mode		200		MHz
		In differential-mode, on-chip CW mode		160		MHz

(1) Internally set by the device.

Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{DE_BF}	Differential clock amplitude	Sine-wave, ac-coupled	0.7			V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
V_{SE_BF}	Single-ended clock amplitude with BF_CLKM connected to AVDDP_5	LVCMOS on BF_CLKP with AVDD_IO = 1.8		1.8		V
		LVCMOS on BF_CLKP with AVDD_IO = 2.5		2.5		V
D_{BF}	Minimum BF_CLK duty cycle			45		%
	Maximum BF_CLK duty cycle			55		%
TR_BF_SYNC INPUT						
f_{SYNC}	Maximum TR_BF_SYNC frequency	For default power mode		10		kHz
		For dynamic power mode		60		kHz
V_{CM_SYNC}	Input common mode		1.125		1.375	V
V_{DE_SYNC}	Differential amplitude	LVPECL, dc-coupled		1.6		V_{PP}
		LVDS, dc-coupled		0.7		V_{PP}
V_{SE_SYNC}	Single-ended amplitude with TR_BF_SYNCM connected to AVDDP_5	LVCMOS on TR_BF_SYNCP AVDD_IO = 1.8V		1.8		V
		LVCMOS on TR_BF_SYNCP AVDD_IO = 2.5V		2.5		V
w_{SYNC}	Minimum TR_BF_SYNC pulse width			10		BF_CLK clock cycles
	Maximum TR_BF_SYNC pulse width			20		BF_CLK clock cycles

7.4 Thermal Information

THERMAL METRIC[1]			TX7316 ZXC 216	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		20.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		4.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	Board temp taken at short side of the package	7.4	°C/W
		Board temp taken at long side of the package	5.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter		0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	Board temp taken at short side of the package	6.8	°C/W
		Board temp taken at long side of the package	5.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report..

7.5 Electrical Characteristics

Typical values are at 25°C. **Device supplies:** AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = -5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V, and AVDDM_HV_B = –50 V. **Device input:** BF_CLK = 200MHz, TR_BF_SYNC = 5kHz applied with differential mode, pins RESYNC and LVL_3Z are set to logic level '1'. **Load:** Connected to the pulser output is 1KΩ||240pF, and to T/R switch low voltage output is 50Ω||20pF. If not specified then given parameter is applicable for on-chip, off-chip beam forming mode, 3-level, 5-level mode, and default, dynamic power mode. All control signals are kept to logic level '0', unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PULSER							
R_H	Output transistor ON resistance (1)				15		Ω
R_G	Clamp transistor ON resistance (1)	3-Level Mode			12		Ω
		5-Level Mode			6		Ω
R_{DAMP}	Damp transistor ON resistance (1)	3-Level Mode			500		Ω
		5-Level Mode			250		Ω
R_{DIS}	Discharge resistance	3-Level Mode			11.2		kΩ
		5-Level Mode			5.6		kΩ
C_{PAR}	Pulser Output Parasitic Capacitance	3-Level Mode	When TR switch is OFF		34		pF
			When TR switch is ON		82		pF
		5-Level Mode	When TR switch is OFF		70		pF
			When TR switch is ON		120		pF
V_{DIODE}	Knee voltage of diode used in pulser (1)	For 1mA current			0.75		V
I_{OSAT}	Output transistor saturation current	DSEL_0, DSEL_1 = "00"			2.4		A
		DSEL_0, DSEL_1 = "01"			1.8		A
		DSEL_0, DSEL_1 = "10"			1.2		A
		DSEL_0, DSEL_1 = "11"			0.6		A
I_{CSAT}	Clamp transistor saturation current	3-Level Mode	DSEL_0, DSEL_1 = "00"		1		A
			DSEL_0, DSEL_1 = "01"		0.75		A
			DSEL_0, DSEL_1 = "10"		0.5		A
			DSEL_0, DSEL_1 = "11"		0.25		A
		5-Level Mode	DSEL_0, DSEL_1 = "00"		2		A
			DSEL_0, DSEL_1 = "01"		1.5		A
			DSEL_0, DSEL_1 = "10"		1		A
			DSEL_0, DSEL_1 = "11"		0.5		A
$t_{R\_GP\_A}$	Pulser output rise time, ground to positive high (A-group)	See Figure 2			11		ns
$t_{R\_MP\_A}$	Pulser output rise time, minus high to positive high (A-group)	See Figure 2			25		ns
$t_{R\_MG\_A}$	Pulser output rise time, minus high to ground (A-group)	See Figure 2			11		ns
$t_{F\_PG\_A}$	Pulser output fall time, positive high to ground (A-group)	See Figure 2			11		ns
$t_{F\_PM\_A}$	Pulser output fall time, positive high to minus high (A-group)	See Figure 2			25		ns
$t_{F\_GM\_A}$	Pulser output fall time, ground to minus high (A-group)	See Figure 2			11		ns
$t_{R\_GP\_B}$	Pulser output rise time, ground to positive high (B-group)	See Figure 2			6		ns
$t_{R\_MP\_B}$	Pulser output rise time, minus high to positive high (B-group)	See Figure 2			14		ns
$t_{R\_MG\_B}$	Pulser output rise time, minus high to ground (B-group)	See Figure 2			6		ns
$t_{F\_PG\_B}$	Pulser output fall time, positive high to ground (B-group)	See Figure 2			7		ns
$t_{F\_PM\_B}$	Pulser output fall time, positive high to minus high (B-group)	See Figure 2			17		ns

(1) Refer Figure 45.

Electrical Characteristics (continued)

Typical values are at 25°C. **Device supplies:** AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = -5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V, and AVDDM_HV_B = –50 V. **Device input:** BF_CLK = 200MHz, TR_BF_SYNC = 5kHz applied with differential mode, pins RESYNC and LVL_3Z are set to logic level '1'. **Load:** Connected to the pulser output is 1KΩ||240pF, and to T/R switch low voltage output is 50Ω||20pF. If not specified then given parameter is applicable for on-chip, off-chip beam forming mode, 3-level, 5-level mode, and default, dynamic power mode. All control signals are kept to logic level '0', unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{F\_GM\_B}$	Pulser output fall time, ground to minus high (B-group)	See Figure 2		8.5		ns
BW	Maximum Pulser BW Frequency at which output peak to peak amplitude reduces by 3dB	+/-100V supply, 2.4A mode		20		MHz
		+/-100V supply, 4.8A mode		36		MHz
		+/-70V supply, 2.4A mode		25		
F_{CW}	Maximum CW signal frequency	For AVDDP_HV and |AVDDM_HV_A/B| >3V		8		MHz
		For AVDDP_HV and |AVDDM_HV_A/B| < 3V		5		
$HD2_{PUL}$	Second harmonic distortion	At 5MHz, 5 cycles		45		dBc
CT_{PUL}	Cross talk	With only single channel pulser excited with signal frequency = 5MHz		60		dBc
t_J	Output jitter	In CW mode, signal frequency 5 MHz, measured from 100 Hz to 20 kHz		100		fs
T/R SWITCH						
R_{ON}	On DC resistance	See Figure 46		12		Ω
R_{OFF}	Impedance at DC and at 1MHz	See Figure 46		1		MΩ
R_{SHORT}	Off short resistance	See Figure 46		15		Ω
C_{PDIS}	TR switch disabled parasitic capacitance	Measure on the RX_n node		20		pF
T_{TON}	Turn -on time			0.5		us
T_{TOFF}	Turn -off time			1.75		us
V_{GON}	Turn -on, -off glitch voltage			50		mV_{PP}
BW_{TR}	Bandwidth	Measured by feeding the signal at the pulser output with 50Ω source impedance and measuring the voltage at RX_n node		50		MHz
$HD2_{TR}$	Second harmonic distortion	At 5 MHz, Signal is applied with source impedance of 50 ohms at TXout_n node and amplitude of 1Vpp is ensured at RX_n node		50		dBc
CT_{TR}	Cross talk with only single channel T/R switch is excited with signal frequency = 5MHz	Measured on channels within the group		52		dBc
		Measured on all other channels		70		dBc
THERMAL SHUTDOWN						
T_{SHUT}	Shutdown Temperature			110		°C
POWER SUPPLY REJECTION						
$PSRR_{PHV}$	AVDDP_HV_A or AVDDP_HV_B power supply rejection at 100kHz	When T/R switch is On		90		dBc
$PSRR_{MA}$	AVDDM_HV_A power supply rejection at 100kHz	When T/R switch is On		70		dBc
$PSRR_{MB}$	AVDDM_HV_B power supply rejection at 100kHz	When T/R switch is On		90		dBc
$PSRR_{P5}$	AVDDP_5 PSRR at 100kHz	When T/R switch is On		65		dBc
$PSRR_{LV}$	AVDDM_5 PSRR or AVDD_IO at 100kHz	When T/R switch is On		90		dBc
POWER DISSIPATION IN 5-LEVEL, TRANSMIT RECEIVE MODE(2)						
I_{PH_A}	AVDDP_HV_A supply current			3.2		mA
I_{PH_B}	AVDDP_HV_B supply current	Default power mode		135		uA
		Dynamic power mode		75		uA
I_{MH_A}	AVDDM_HV_A supply current			2.2		mA

(2) Different supply voltages used to measure power are: AVDDP_5 = 5 V, AVDDM_5 = –5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50V, AVDDM_HV_A = –100 V and AVDDM_HV_B = –50V. If not mentioned, the listed parameter in the table is applicable to the modes off-chip beamforming, on-chip beamforming, default power mode and dynamic power mode. To measure power device is configured to generate patterns shown in Figure 1 on all the channels with 0 transmit delay beam forming.

Electrical Characteristics (continued)

Typical values are at 25°C. **Device supplies:** AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = -5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V, and AVDDM_HV_B = –50 V. **Device input:** BF_CLK = 200MHz, TR_BF_SYNC = 5kHz applied with differential mode, pins RESYNC and LVL_3Z are set to logic level '1'. **Load:** Connected to the pulser output is 1KΩ||240pF, and to T/R switch low voltage output is 50Ω||20pF. If not specified then given parameter is applicable for on-chip, off-chip beam forming mode, 3-level, 5-level mode, and default, dynamic power mode. All control signals are kept to logic level '0', unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MH_B}	AVDDM_HV_B supply current	Default power mode		135		uA
		Dynamic power mode		40		uA
I_{ML_TR}	AVDDM_5 supply current			3		mA
I_{PL_TR}	AVDDP_5 supply current	In off-chip beam forming mode, default power mode		6		mA
		In on-chip beam forming mode, default power mode		20		mA
		In on-chip and off-chip beam forming mode, dynamic power mode		8		mA
I_{IO_B}	AVDD_IO supply current			0.1		mA
P_{D_TR}	Total power dissipation	In off chip beam forming mode, default power mode		596		mW
		In off chip beam forming mode, dynamic power mode		588		mW
		In on chip beam forming mode, default power mode		666		mW
		In on chip beam forming mode, dynamic power mode		598		mW
POWER DISSIPATION IN 5-LEVEL, CW-MODE(3)						
I_{PHA_CW}	AVDDP_HV_A supply current			140		uA
I_{PHB_CW}	AVDDP_HV_B supply current	With drive strength of 2.4 A		216		mA
		With drive strength of 0.6 A		140		mA
I_{MHA_CW}	AVDDM_HV_A supply current			150		uA
I_{MHB_CW}	AVDDM_HV_B supply current	With drive strength of 2.4 A		191		mA
		With drive strength of 0.6 A		133		mA
I_{ML_CW}	AVDDM_5 supply current	With drive strength of 2.4 A		78		mA
		With drive strength of 0.6 A		37		mA
I_{PL_CW}	AVDDP_5 supply current in	In off-chip beam forming mode, with drive strength of 2.4 A		62		mA
		In on-chip beam forming mode, with drive strength of 2.4 A		106		mA
		In off-chip beam forming mode, with drive strength of 0.6 A		37		mA
		In on-chip beam forming mode, with drive strength of 0.6 A		82		mA
I_{IO_CW}	AVDD_IO supply current			0.1		mA
P_{D_CW}	Total power dissipation	In off-chip beam forming mode, with drive strength of 2.4 A		2.75		W
		In on-chip beam forming mode, with drive strength of 2.4 A		2.98		W
		In off-chip beam forming mode, with drive strength of 0.6 A		1.74		W
		In on-chip beam forming mode, with drive strength of 0.6 A		1.97		W
POWER DISSIPATION IN OTHER MODES						
P_{SB}	Total power dissipation in standby mode			23		mW
P_{D_R}	Total power dissipation in receive only mode	Default power mode		50		mW
		Transmit-less power mode		15		mW
P_{GBL_PDN}	Total power dissipation in Global Power Down mode			4.3		mW
t_{WUP_GBL}	Wake-up time	Global Power Down mode		2		ms
t_{GBL_DYN}	Wake-up time	Global Power Down mode and LDO in dynamic mode		200		us

(3) For CW-mode, value of all the supplies used to measure power are AVDDP_5 = +5V, AVDDM_5 = -5V, AVDDP_HV_A = +100V, AVDDP_HV_B = +5V, AVDDM_HV_A = -100V and AVDDM_HV_B = -5V.
All B-group pulsers (8 channels) generate CW waveform of +5V -> -5V -> +5V at a frequency of 5 MHz. The BF_CLK frequency used is 80 MHz.

7.6 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. Typical values are at T_A = 25°C, minimum and maximum values are across the full temperature range. Supplies: AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5 V = –5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V and AVDDM_HV_B = –50 V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
DIGITAL INPUTS (CW_EN, DSEL_0, DSEL_1, IN_A*, IN_B*, RESET, RESYNC, SCLK, SDATA_GRP1, SDATA_GRP2, SEN_GRP1, SEN_GRP2, STDBY, TR_EN*)(1)						
V_{IH1}	High-level input voltage	For AVDD_IO = 1.8V	1.35			V
		For AVDD_IO = 2.5V	1.875			V
V_{IL1}	Low-level input voltage	For AVDD_IO = 1.8V			0.45	V
		For AVDD_IO = 2.5V			0.625	V
I_{IH1}	High-level input current			100		µA
I_{IL1}	Low-level input current			100		µA
C_{i1}	Input capacitance			6		pF
DIGITAL INPUTS (LVL_3Z_5)(1)						
V_{IH2}	High-level input voltage		3.75			V
V_{IL2}	Low-level input voltage				1.25	V
I_{IH2}	High-level input current			100		µA
I_{IL2}	Low-level input current			100		µA
C_{i2}	Input capacitance			6		pF
DIGITAL OUTPUTS (SDOUT, SHUTZ)(1)						
V_{OH}	High-level output voltage	For AVDD_IO = 1.8V	1.44	1.8		V
		For AVDD_IO = 2.5V	2	2.5		V
V_{OL}	Low-level output voltage			0	0.2	V
z_o	Output impedance for SDOUT			250		Ω
z_o	Output impedance for SHUTZ	When high		50		kΩ
		When low		100		Ω

(1) All digital specifications are characterized across operating temperature range but are not tested at production.

7.7 Timing Requirements(1)

Typical values are at T_A = 25°C, AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = –5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V and AVDDM_HV_B = –50 V (unless otherwise noted); minimum and maximum values are across the full temperature range

		MIN	TYP	MAX	UNIT
SERIAL INTERFACE TIMING					
t_{SCLK}(2)	SCLK period in write mode	10			ns
t_{SCLK_H}(2)	SCLK high time in write mode	4			ns
t_{SCLK_L}(2)	SCLK low time in write mode	4			ns
t_{DSU}(2)	Data setup time in write mode	3			ns
t_{DH}(2)	Data hold time in write mode	3			ns
t_{SEN_SU}(2)	SEN falling edge to SCLK rising edge in write mode	4.5			ns
t_{SEN_HO}(2)	Time between last SCLK rising edge to SEN rising edge in write mode	1			ns
t_{SCLK_RD}(3)	SCLK period in read mode	50			ns
$t_{SCLK\_H\_RD}$(3)	SCLK high time in read mode	20			ns
$t_{SCLK\_L\_RD}$(3)	SCLK low time in read mode	20			ns
t_{DSU_RD}(3)	Data setup time in read mode	5			ns
t_{DH_RD}(3)	Data hold time in read mode	5			ns
$t_{SEN\_SU\_RD}$(3)	SEN falling edge to SCLK rising edge in read mode	5			ns
$t_{SEN\_HO\_RD}$(3)	Time between last SCLK rising edge to SEN rising edge in read mode	5			ns
t_{OUT_DV}(3)	SDOUT delay in read mode	4	6	10	ns
TIMING REQUIREMENT FOR ON-CHIP BEAM FORMING MODE					
t_{WUP}(4)	Minimum time to apply TR_EN* signal before applying TR_BF_SYNC signal	8			µs
W_{SYNC}(4)	Sync pulse width	10		20	BF_CLK clock cycles
t_{SU_SYNC}(4)	Setup time related to TR_BF_SYNC (Differential) relative to the rising edge of the BF_CLK (Differential) clock	2.14			ns
	Setup time related to TR_BF_SYNC (Single-ended) relative to the rising edge of the BF_CLK (Single-ended) clock	1.27			ns
t_{H_SYNC}(4)	Hold time related to TR_BF_SYNC (Differential) relative to the rising edge of the BF_CLK (Differential) clock	1.16			ns
	Hold time related to TR_BF_SYNC (Single-ended) relative to the rising edge of the BF_CLK (Single-ended) clock	1.57			ns
t_{PROP_INT}	From a 50% transition point of BF_CLK rising edge on which TR_BF_SYNC is latched to 1-V deviation at output; see Figure 50		15		ns
TIMING REQUIREMENT FOR OFF-CHIP BEAM FORMING					
t_{SU_IN}(5)	Setup time related to IN_* relative to the rising edge of the BF_CLK (Differential) clock for RESYNC = 1	1.78			ns
	Setup time related to IN_* relative to the rising edge of the BF_CLK (Single-ended) clock for RESYNC = 1	2.15			ns
t_{H_IN}(5)	Hold time related to IN_* relative to the rising edge of the BF_CLK (Differential) clock for RESYNC = 1	2.03			ns
	Hold time related to IN_* relative to the rising edge of the BF_CLK (Single-ended) clock for RESYNC = 1	3.85			ns
t_{PROP}	Propagation delay with RESYNC = 0, from a 50% transition point of IN_* control signal to 1-V deviation at output; see Figure 44		15		ns
t_{PROP_SYNC}	Propagation delay with RESYNC = 1, from 50% transition point of BF_CLK rising edge to 1-V deviation at output; see Figure 44		16		ns
t_{WUP_OFF}	Minimum time to apply TR_EN* signal before transmitting in dynamic power mode		10		µs

(1) All timing specifications are characterized but are not tested at production.
(2) See Figure 63 for more details.
(3) See Figure 66 for more details.
(4) See Figure 47 and Figure 48 for more details.
(5) See Figure 43 for more details.

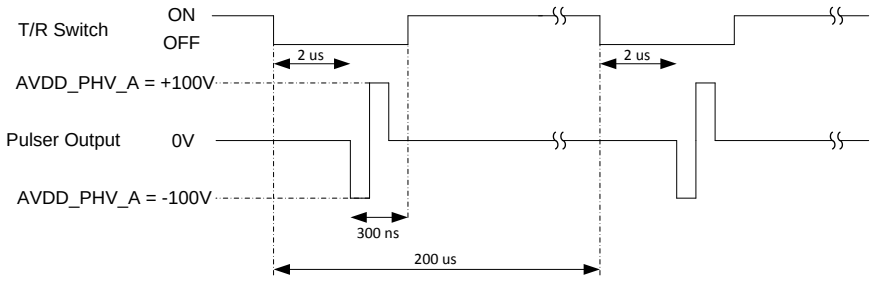


Figure 1. Transmit Receive Mode Output Pattern

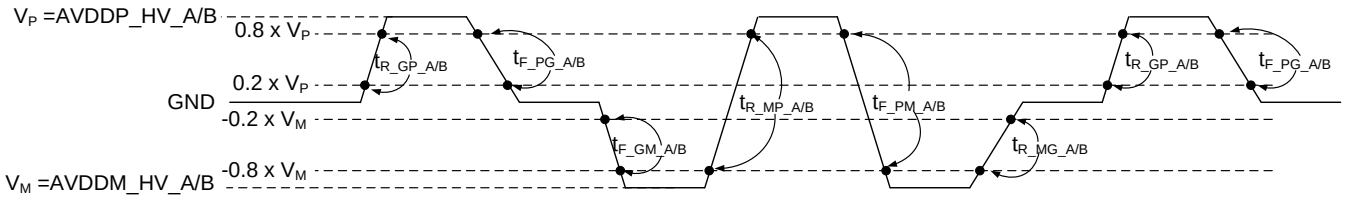


Figure 2. Pulser Output Waveform

7.8 Typical Characteristics

Typical values are at 25°C. **Device Supplies**: AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = –5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V, and AVDDM_HV_B = –50 V. **Device Input**: BF_CLK = 200 MHz, TR_BF_SYNC = 5 kHz applied with differential mode, pins RESYNC and LVL_3Z are set to logic level '1'. **Load**: Connected to the pulser output is 1 KΩ||240 pF, and to T/R switch low voltage output is 50 Ω||20 pF. If not specified then given parameter is applicable for on-chip, off-chip beam forming mode, 3-level, 5-level mode, and default, dynamic power mode. All control signals are kept to logic level '0', unless otherwise specified. See Application Curves for more details of each plot.

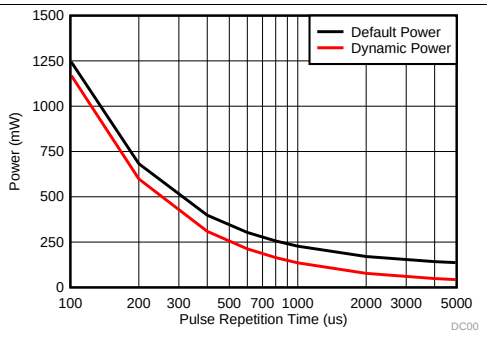


Figure 3. Power vs Pulse Repetition time (PRT) for Output Waveform shown in Figure 2

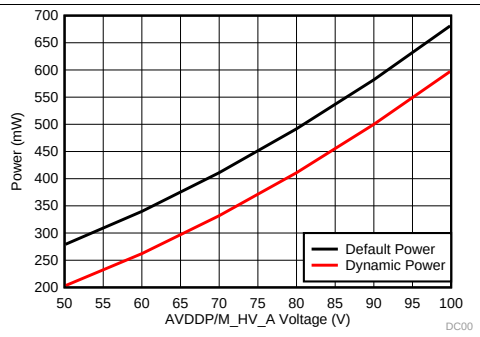


Figure 4. Power vs High Voltage Supply for Output Waveform shown in Figure 2

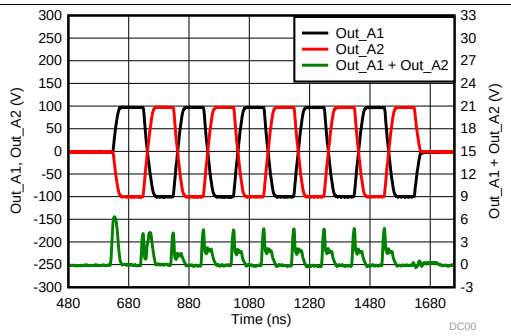


Figure 5. Pulser Inversion

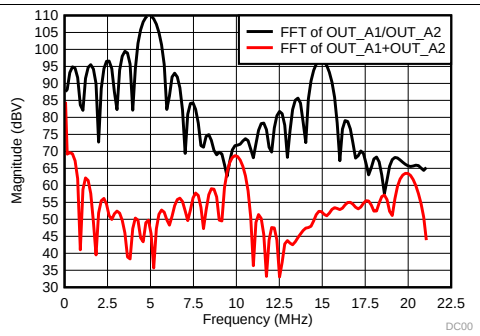


Figure 6. FFT of Pulse Inversion

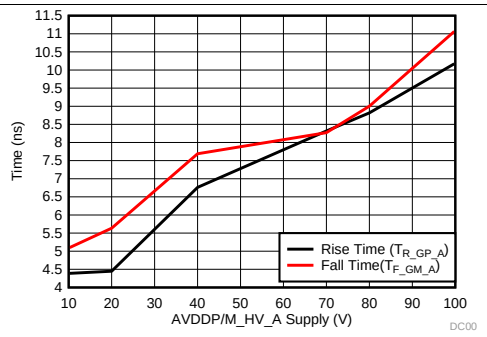


Figure 7. Pulser Output Rise Time ($t_{R\_GP\_A}$) and Fall Time ($t_{F\_GM\_A}$) vs AVDDP/M_HV_A supplies (For AVDDP/M_HV_B = 10 V)

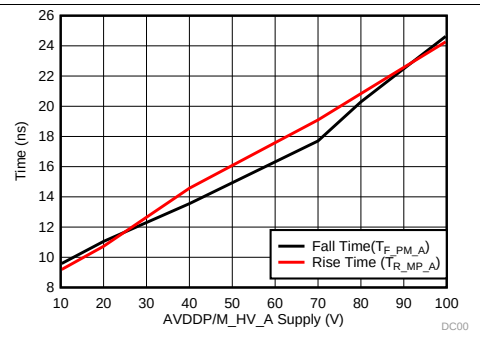


Figure 8. Pulser Output Rise Time ($t_{R\_MP\_A}$) and Fall Time ($t_{F\_PM\_A}$) vs AVDDP/M_HV_A supplies (For AVDDP/M_HV_B = 10 V)

Typical Characteristics (continued)

Typical values are at 25°C. **Device Supplies**: AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = –5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V, and AVDDM_HV_B = –50 V. **Device Input**: BF_CLK = 200 MHz, TR_BF_SYNC = 5 kHz applied with differential mode, pins RESYNC and LVL_3Z are set to logic level '1'. **Load**: Connected to the pulser output is 1 KΩ||240 pF, and to T/R switch low voltage output is 50 Ω||20 pF. If not specified then given parameter is applicable for on-chip, off-chip beam forming mode, 3-level, 5-level mode, and default, dynamic power mode. All control signals are kept to logic level '0', unless otherwise specified. See Application Curves for more details of each plot.

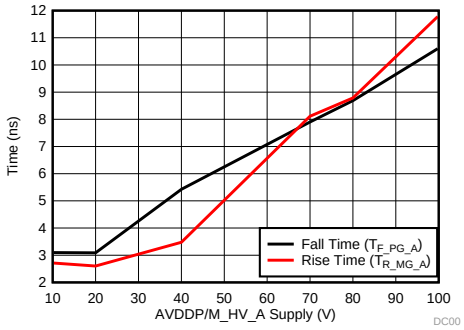


Figure 9. Pulser Output Rise Time ($t_{R\_MG\_A}$) and Fall Time ($t_{F\_PG\_A}$) vs AVDDP/M_HV_A supplies (For AVDDP/M_HV_B = 10 V)

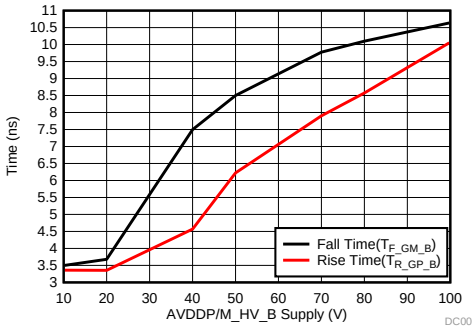


Figure 10. Pulser Output Rise Time ($t_{R\_GP\_B}$) and Fall Time ($t_{F\_GM\_B}$) vs AVDDP/M_HV_B supplies (For AVDDP/M_HV_A = 100 V)

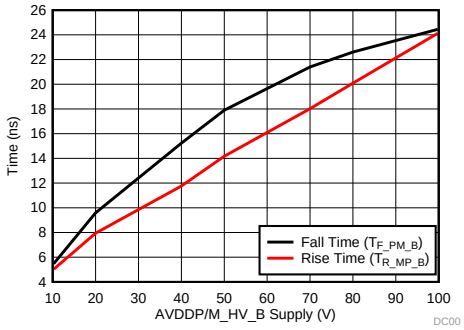


Figure 11. Pulser Output Rise Time ($t_{R\_MP\_B}$) and Fall Time ($t_{F\_PM\_B}$) vs AVDDP/M_HV_B supplies (For AVDDP/M_HV_A = 100 V)

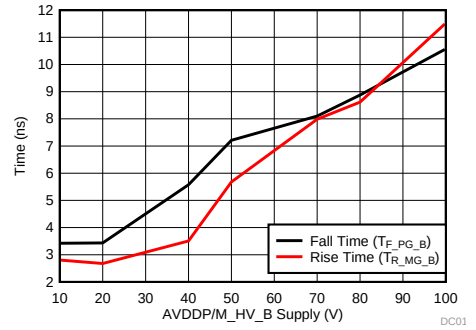


Figure 12. Pulser Output Rise Time ($t_{R\_MG\_B}$) and Fall Time ($t_{F\_PG\_B}$) vs AVDDP/M_HV_B supplies (For AVDDP/M_HV_A = 100 V)

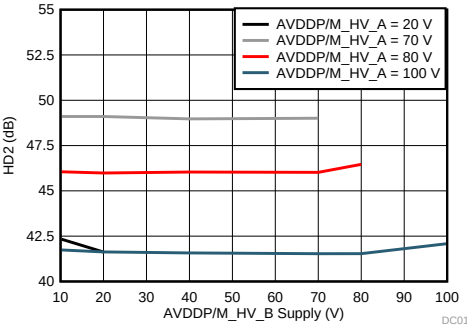


Figure 13. A Group Pulser HD2 vs AVDDP/M_HV_B Supply Voltage

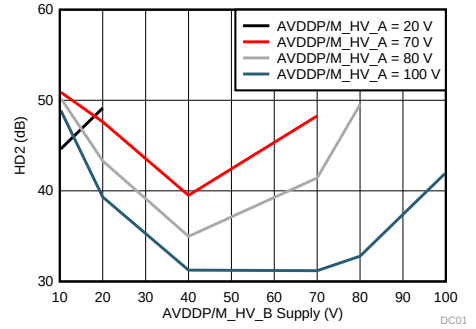


Figure 14. B Group Pulser HD2 vs AVDDP/M_HV_B Supply Voltage

Typical Characteristics (continued)

Typical values are at 25°C. **Device Supplies**: AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = –5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V, and AVDDM_HV_B = –50 V. **Device Input**: BF_CLK = 200 MHz, TR_BF_SYNC = 5 kHz applied with differential mode, pins RESYNC and LVL_3Z are set to logic level '1'. **Load**: Connected to the pulser output is 1 KΩ||240 pF, and to T/R switch low voltage output is 50 Ω||20 pF. If not specified then given parameter is applicable for on-chip, off-chip beam forming mode, 3-level, 5-level mode, and default, dynamic power mode. All control signals are kept to logic level '0', unless otherwise specified. See Application Curves for more details of each plot.

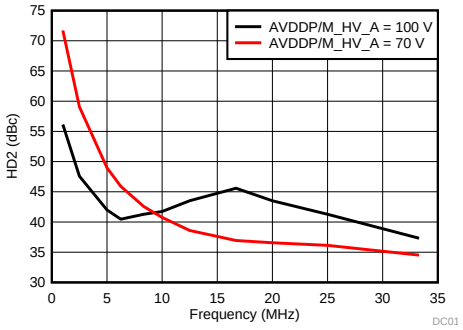


Figure 15. Pulser HD2 vs Frequency

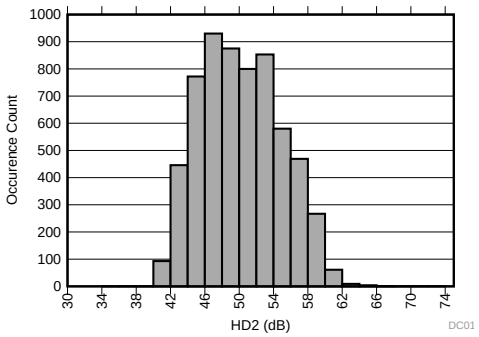


Figure 16. Pulser HD2 Histogram Across Channels and Devices

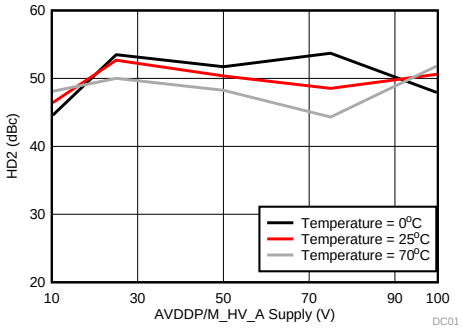


Figure 17. Pulser HD2 vs Supply and Temperature

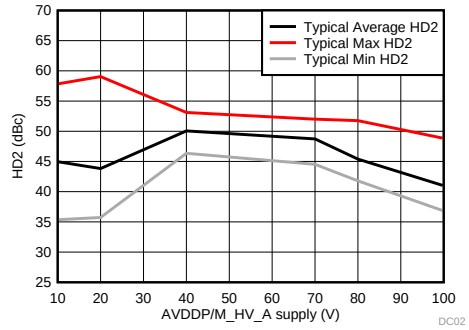


Figure 18. Pulser HD2 vs HV supply

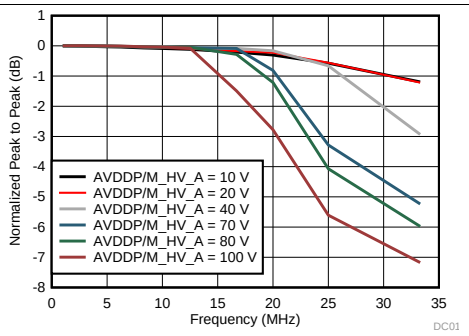


Figure 19. Pulser Bandwidth

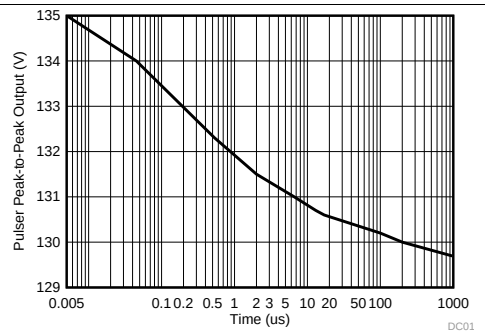


Figure 20. Pulser Output Peak-to-peak Voltage vs Time in Elastography Mode for AVDDP/M_HV_A supply voltage of 70 V

Typical Characteristics (continued)

Typical values are at 25°C. **Device Supplies**: AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = –5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V, and AVDDM_HV_B = –50 V. **Device Input**: BF_CLK = 200 MHz, TR_BF_SYNC = 5 kHz applied with differential mode, pins RESYNC and LVL_3Z are set to logic level '1'. **Load**: Connected to the pulser output is 1 KΩ||240 pF, and to T/R switch low voltage output is 50 Ω||20 pF. If not specified then given parameter is applicable for on-chip, off-chip beam forming mode, 3-level, 5-level mode, and default, dynamic power mode. All control signals are kept to logic level '0', unless otherwise specified. See Application Curves for more details of each plot.

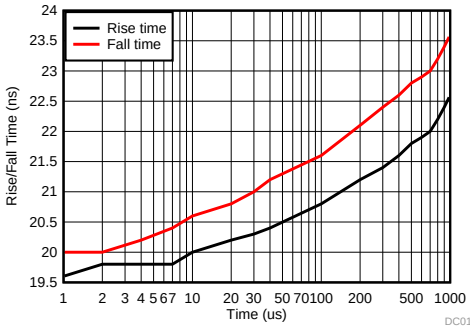


Figure 21. Pulser Output Rise and Fall Time vs Time in Elastography Mode for AVDDP/M_HV_A supply voltage of 70 V

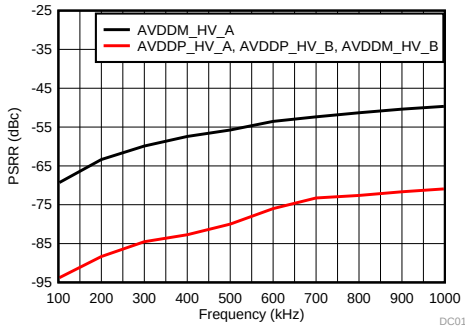


Figure 22. High Voltage Supplies PSRR vs Supply Tone Frequency

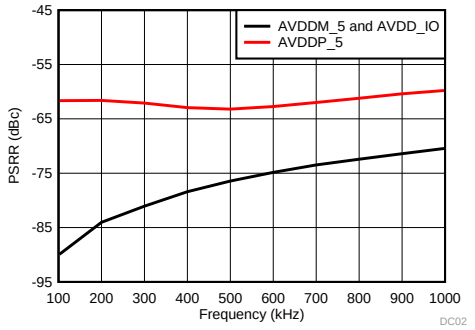


Figure 23. Low Voltage Supplies PSRR vs Supply Tone Frequency

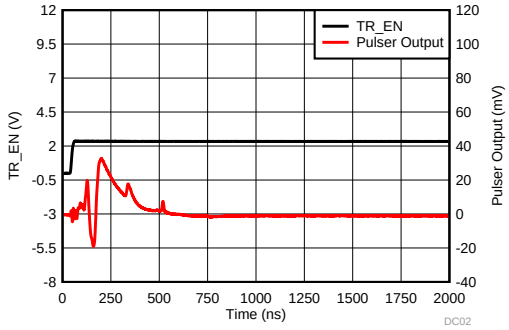


Figure 24. T/R Switch Turn ON Glitch

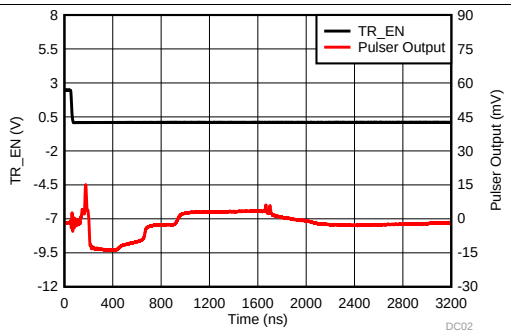


Figure 25. T/R Switch Turn OFF Glitch

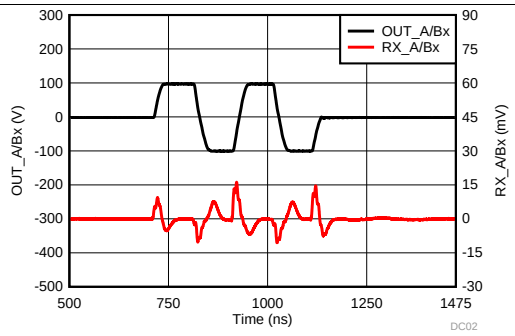


Figure 26. T/R Switch Isolation

Typical Characteristics (continued)

Typical values are at 25°C. **Device Supplies**: AVDD_IO = 2.5 V, AVDDP_5 = 5 V, AVDDM_5V = –5 V, AVDDP_HV_A = 100 V, AVDDP_HV_B = 50 V, AVDDM_HV_A = –100 V, and AVDDM_HV_B = –50 V. **Device Input**: BF_CLK = 200 MHz, TR_BF_SYNC = 5 kHz applied with differential mode, pins RESYNC and LVL_3Z are set to logic level '1'. **Load**: Connected to the pulser output is 1 KΩ||240 pF, and to T/R switch low voltage output is 50 Ω||20 pF. If not specified then given parameter is applicable for on-chip, off-chip beam forming mode, 3-level, 5-level mode, and default, dynamic power mode. All control signals are kept to logic level '0', unless otherwise specified. See Application Curves for more details of each plot.

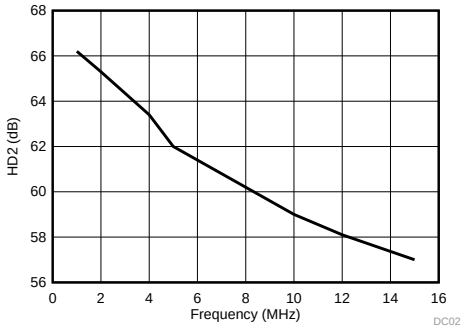


Figure 27. T/R Switch HD2 vs Frequency

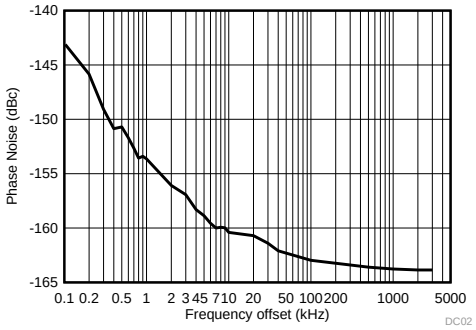


Figure 28. Pulser CW Phase Noise

8 Detailed Description

8.1 Overview

The device is a highly integrated, high performance transmitter solution for ultrasound imaging system. The device is a multi-chip module comprising two dies: Die 1 and Die 2. Each die has 2 sets of 4 channels, Set A and Set B. Die 1 has channels A1, B1, A2, B2, A3, B3, A4, B4 (referred to as Group 1) and Die 2 has channels A5, B5, A6, B6, A7, B7, A8, B8 (referred to as Group 2). The channel numbers prefixed by 'A' have output pulsing circuits that pulse to high and low levels controlled by AVDDP_HV_A and AVDDM_HV_A respectively. The channel numbers prefixed by 'B' have output pulsing circuits that pulse to high and low levels controlled by AVDDP_HV_B and AVDDM_HV_B respectively. Each channel of the device consist of a pulser to generate high voltage pulses and a transmit/receive (T/R) switch.

When the device is operated in the 3-level mode, the 'A' and 'B' supplies are kept the same, for example ±100V. This results in a total of 3 levels of pulsing: –100 V, 0V and +100 V. Each of the 16 channels (8 channels in each die) pulses to the same high and low level and 16 outputs are supported. The outputs pins are labelled OUT_xy where x is 'A' or 'B' and y is 1..8.

When the device is operated in the 5-level mode, the 'A' and 'B' supplies are kept unequal. For example, the 'A' supply set may be set to ±100 V and the 'B' supply set may be set to ±50 V. The 'A' and 'B' pulser circuits of the same channel number (for eg. A1 and B1) are made active and tri-state in a mutually exclusive manner, and their outputs are multiplexed to a common output. Such an operation results in a 5-level output voltage: –100 V, –50 V, 0 V, +50 V and +100 V. Because two pulsing channels are combined together to construct one output, the 5-level mode supports a total of only 8 channels. In the 5-level mode, the output pins OUT_Ay (y is 1..8) need to be shorted externally to the output pins OUT_By, resulting in a single output set OUT_y.

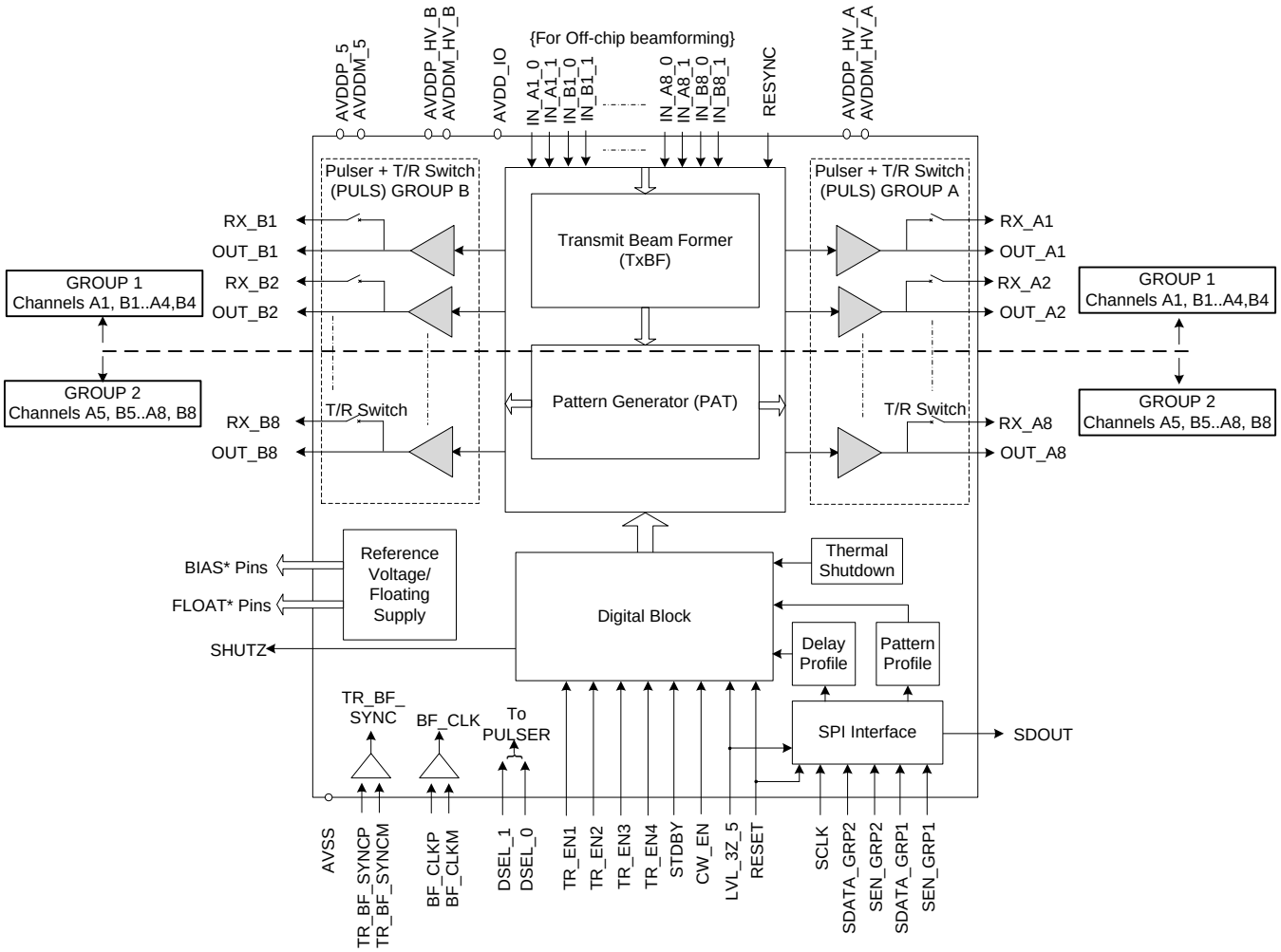
The high voltage pulser outputs (OUT_xy) are meant to drive the ultrasound transducer in the transmission phase. However, the transducer must interface with a sensitive receiver, which cannot withstand the high-voltage excitation. A high level of isolation is required between the pulser output in the transmission phase and the receiver input. The device integrates a T/R switch that can be used to provide such isolation. By connecting the receiver inputs (from a receiver chip) to the RX_xy (x is A,B and y is 1..8) pins, the T/R switch gets inserted between the high-voltage pulser in its transmission phase and the receiver, automatically providing the required isolation.

The device supports two beamformer modes: on-chip beamforming and off-chip beamforming. In the off-chip beamforming mode, the instantaneous pulsing transitions of each of the 16 channels are controlled by two control pins. For example, the pulsing operation of channel A1 is controlled by control signals on pins IN_A1_1 and IN_A1_0. These signals are meant to be driven from the FPGA and may have high jitter. To prevent the jitter on these control signals from affecting the beamforming operation, these control signals can all be optionally set to be re-latched within the device by a common beamformer clock input on the BF_CLKP/BF_CLKM pins.

In the on-chip beamforming mode, the pulsing transitions of the 16 channels are controlled by delay and pattern profiles stored in a profile RAM inside the device. The delay profiles store the relative pulsing delays for the different channels and the pattern profiles define the shape/ pattern of the pulses in each channel. An internal pattern generator runs on the clock provided on the BF_CLKP/BF_CLKM pins. The operation of all the channels can be synchronized using a signal on the TR_BF_SYNCP/ TR_BF_SYNCM pins.

The full functional diagram of the device is shown in Functional Block Diagram.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 BF_CLK Clock and TR_BF_SYNC Input

BF_CLK clock and TR_BF_SYNC input signals are used by the device to perform multiple operation like on-chip beamforming, re-synchronization, etc. This BF_CLK clock and TR_BF_SYNC signal can be driven differentially (sine wave, LVPECL, or LVDS) or single-ended (LVCMOS). Owing to the timing relationship that must be satisfied between BF_CLK and TR_BF_SYNC, TI strongly recommends using the same electrical interface standard (for example, LVDS, LVCMOS, etc.) for both. The device automatically senses and reconfigures its input buffers on these pins based on whether the input is single-ended or differential. For example, when BF_CLKM / TR_BF_SYNCM pin is connected to AVDDP_5, the device automatically switches to a single-ended input buffer configuration for these pins.

NOTE

Both the inputs BF_CLK and TR_BF_SYNC must be configured in the same mode that is both must be in differential input mode or single ended mode.

Feature Description (continued)

8.3.1.1 Differential Input Mode

The equivalent circuit of BF_CLK and TR_BF_SYNC input buffer in differential mode is shown in Figure 29. To apply differential clock (sine wave, LVPECL, or LVDS) to the device AC couple the input of the device with the required termination as close to the device as possible; see Figure 29. The BF_CLK input is meant to be a high-speed free-running clock and can be AC coupled to the clock input pin(s). The TR_BF_SYNC input however is not a free-running clock and would require to be DC coupled to the device.

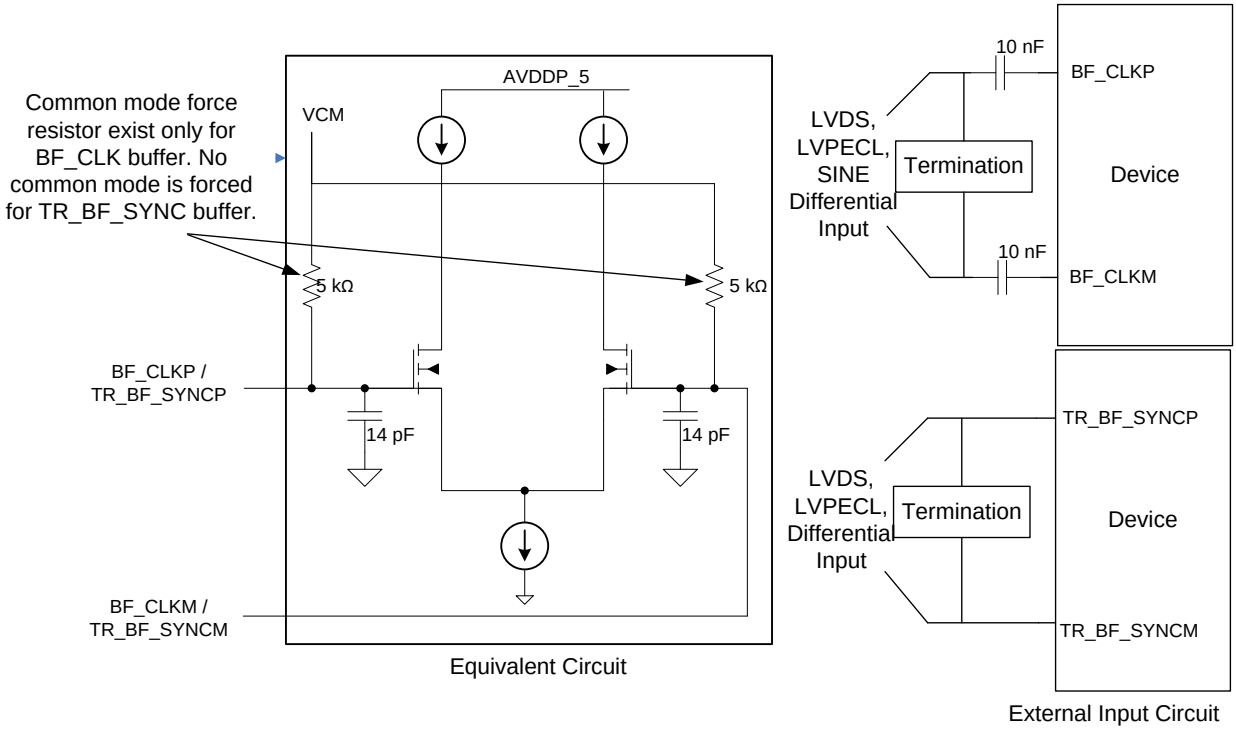


Figure 29. Internal Clock Buffer for Differential Clock Mode

8.3.1.2 Single Ended Input Mode

If the preferred clocking scheme for the device is single-ended, connect the single-ended input to BF_CLKP/TR_BF_SYNCP and connect the BF_CLKM/TR_BF_SYNCM pin to AVDDP_5 as shown in Figure 30. In this case, the auto-detect feature within the device shuts down the internal differential clock buffer and the device automatically goes into a single-ended clock mode. Figure 30 also shows an equivalent input circuit of the device in the single-ended mode. Connect the single-ended clock source directly (Without the AC coupling capacitor) to the BF_CLKP/TR_BF_SYNCP pin. Low-jitter, square signals (LVCMOS levels) are recommended to drive the device input.

Feature Description (continued)

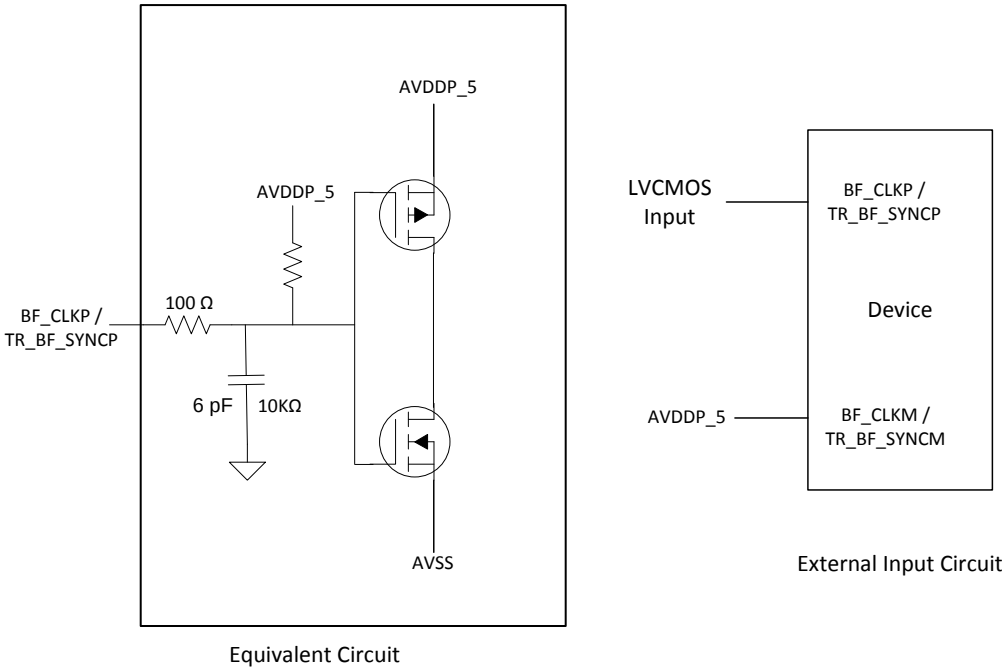


Figure 30. Single-Ended Clock Driving Circuit

8.3.2 Device Operating Modes

The device support two modes of beam forming operation: Off-chip beam forming mode and On-chip beam forming mode. The device also supports two modes of output levels: 3-level mode and 5-level mode. A brief description of all these modes is given in following sections.

8.3.2.1 Beam-Forming Mode

Table 2 list down the hardware difference between off-chip and on-chip beam forming mode.

Table 2. Hardware Configuration for Off-chip and On-chip Beam-forming Mode

PINS	OFF-CHIP BEAMFORMING MODE	ON-CHIP BEAMFORMING MODE
IN_* Control Signals	Apply control signals from the FPGA	Connect to ground
TR_BF_SYNC	Connect to ground	Apply TR_BF_SYNC signal
Timing constraints	Meet timing constraints between BF_CLK and IN_* control signals so that the control signals can be latched and resynchronized by the device on BF_CLK	Meet timing constraints between TR_BF_SYNC and BF_CLK
RESYNC pin	Connect to '0' or '1' as per the requirement	Always connect to '1'
TR_EN* pins	Controls the T/R switch	Connect to FPGA. Apply a pulse to power up the BF_CLK clock, TR_BF_SYNC buffer and floating LDOs in dynamic power mode.

1. Off-chip beam forming mode: A simplified block diagram of the device in off-chip beamforming is shown in Figure 31. In off-chip beamforming mode, the instantaneous pulser output of each channel is controlled by the control signals applied at input pins (IN_A*, IN_B*) of the device. A transmit beam forming block passes on all the control signals to a pattern generator block directly or by latching it on BF_CLK clock based on whether the re-synchronization feature is enabled or disabled. The Pattern generator block decodes the control signals and generates instantaneous control of the required voltage levels for the pulser block in both the 3-level and 5-level modes. Based on the output of the pattern generator block, the Pulser generates the high voltage output pulses.

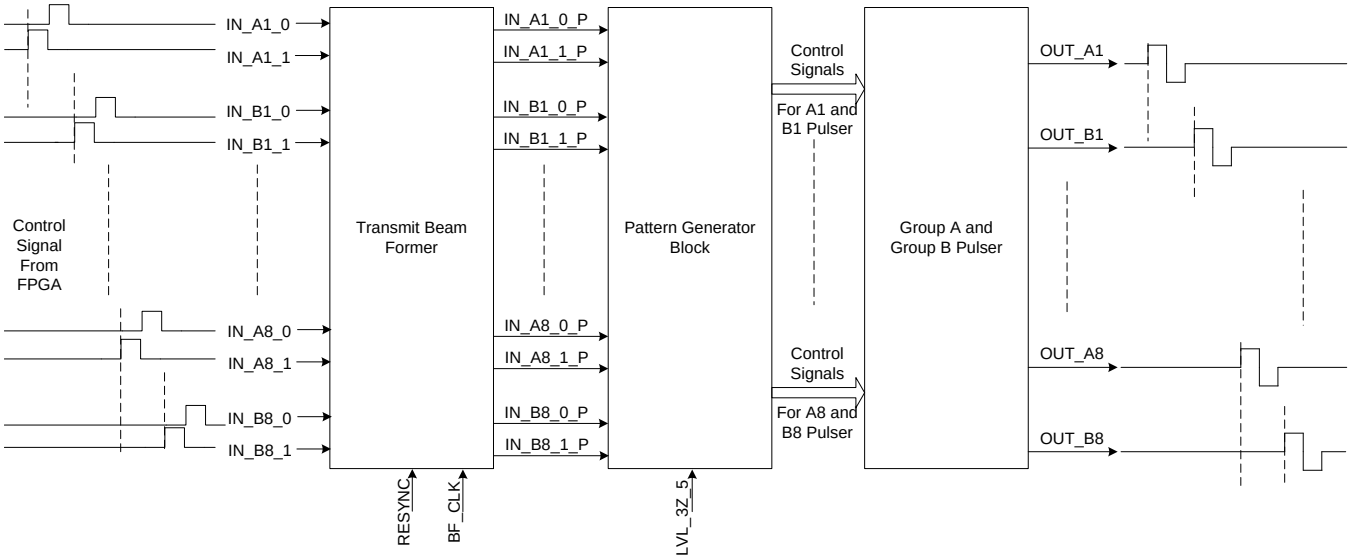


Figure 31. Off-chip Beam Forming Mode

2. On-chip beamforming mode: Figure 32 shows a simplified block diagram of the device in on-chip beam forming mode. In the on-chip beamforming mode, all the control signals for the pulse transitions are generated within the device. Following steps explain the sequence of operation in on-chip beamforming mode:
    1. An input pulse is applied at TR_EN1/3 pins. This input pulse wakes up the BF_CLK and the TR_BF_SYNC buffer of the device. When the system hardware does not have the capability to generate the signal on TR_EN* pins, the BF_CLK clock and the TR_BF_SYNC buffer can be made permanently ON by writing register bits DIS_DYN_CNTRL_1 and DIS_DYN_CNTRL_2 to ‘1’. Keeping these buffers permanently ON leads to extra power from the device.
    2. An input pulse is applied at TR_BF_SYNC pin. On receiving this pulse signal the transmit beamformer block of the device starts generating the clocks (CLK_A1, CLK_B1…CLK_A8, CLK_B8) for pattern-generator block after counting certain number of BF_CLK period as per the content of delay profile.
    3. After the pattern-generator block receives the clock, it starts generating control signal for the pulser as per the values programmed in the pattern profile.
    4. The pulser then generates the high voltage output pulse signal as per the control signals generated by the pattern-generator block.

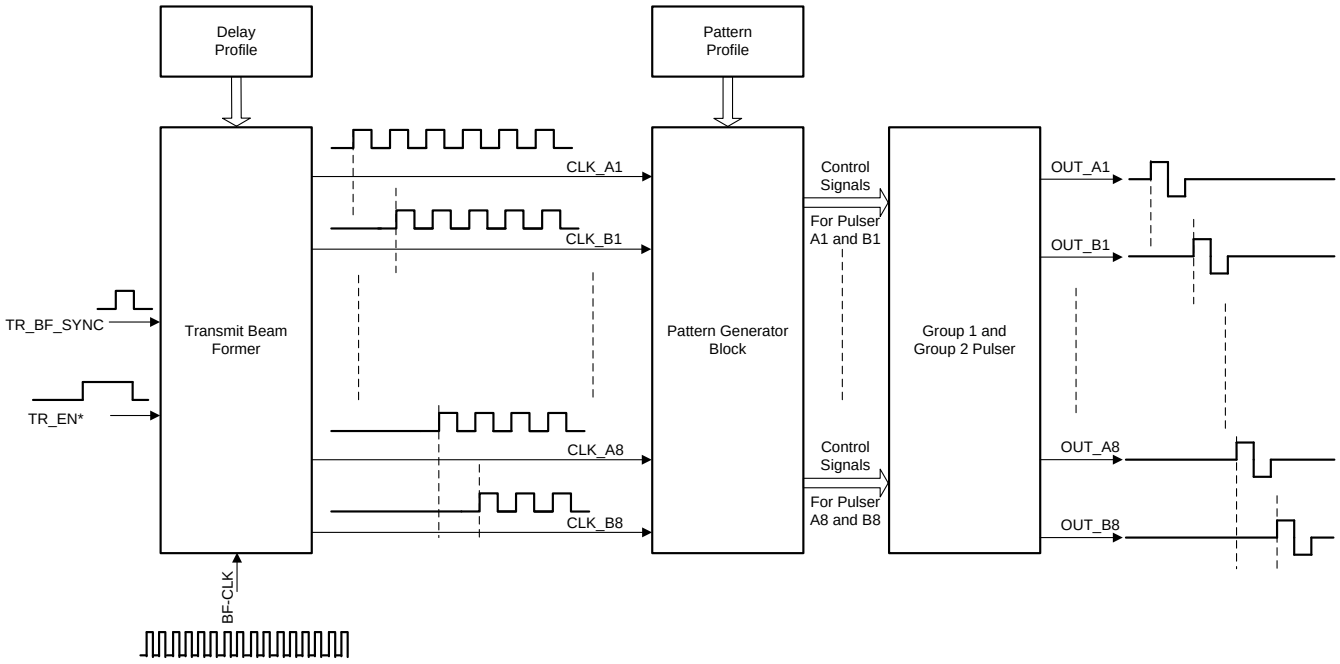


Figure 32. On-chip Beamforming Mode

8.3.2.2 Output Level Modes

The device has total 16 pulsers divided in two groups referred as group A and group B with 8 pulsers in each group. Group A pulsers operate on AVDDP_HV_A and AVDDM_HV_A high voltage supplies and group B operates on AVDDP_HV_B and AVDDM_HV_B high voltage supplies. These 16 pulsers can be configured to generate either 16 sets of 3-level or 8 sets of 5-level output waveforms. Table 3 list down the hardware configuration differences between 3-level and 5-level mode.

1. 3-Level Mode: Each pulser can generates 3-level of high voltage pulses i.e. output can make transition to AVDDP_HV_A/B, AVDDM_HV_A/B supplies, or to ground; see Figure 33.
2. 5-Level Mode: Two pulsers (one from Group A and the other from Group B) combine to generates a 5-levels output waveform. To achieve this, the same numbered channel outputs of group A and group B have to be shorted. In the 5-level mode, the output can make transition to AVDDP_HV_A, AVDDP_HV_B, AVDDM_HV_A, AVDDM_HV_B supplies, and to ground; see Figure 33.

Table 3. Hardware Configuration for 3-Level and 5-Level Mode

Device pin	3-Level Mode	5-Level Mode
LVL_3Z_5 pin	Connect to logic level '0'	Connect to logic level '1'
Supplies	Short supplies AVDDP_HV_A to AVDDP_HV_B and AVDDM_HV_A to AVDDM_HV_B.	Apply all the supplies AVDDP_HV_A, AVDDM_HV_A, AVDDP_HV_B, and AVDDM_HV_B separately. Maintain below voltage condition for high voltage supplies: **AVDDP_HV_A > AVDDP_HV_B, |AVDDM_HV_A| > |AVDDM_HV_B|**
Power sequencing	No power sequencing constraint	During power up/down sequencing, make sure that AVDDP_HV_A > AVDDP_HV_B and AVDDM_HV_A > AVDDM_HV_B
Pulser Output	All the 16 output pins OUT_An (1) and OUT_Bn output 3-level output pulses..	Short group A output to group B output. i.e. short OUT _A1 to OUT_B1, OUT_A2 to OUT_B2 and so on. So the total number of output signals becomes half.
T/R Switch Output	All the 16 T/R switch output RX_An(1) and RX_Bn are active.	Connect Rx_An (1) to receiver AFE. Keep Rx_Bn no connect.

(1) n is from 1 to 8.

Table 3. Hardware Configuration for 3-Level and 5-Level Mode (continued)

Device pin	3-Level Mode	5-Level Mode
T/R Switch control signal in off-chip beamforming mode	Keep TR_EN1 to TR_EN4 pins separate to control TR switch of group of four channels respectively.	Short TR_EN1 to TR_EN2 and TR_EN3 pin to TR_EN4 pin.

NOTE

In 3-level mode, the output signal is allowed to make a transition from any of the (3 defined) output levels to any other output level. However in the 5-level mode transitions between (AVDDP_HV_A to AVDDP_HV_B) or from (AVDDM_HV_A to AVDDM_HV_B) are not allowed. If the device is programmed to make these transitions, then device output goes to high impedance state and output voltage discharges with load time constant.

Typical output waveforms for 3-level and 5-level modes is shown in Figure 33

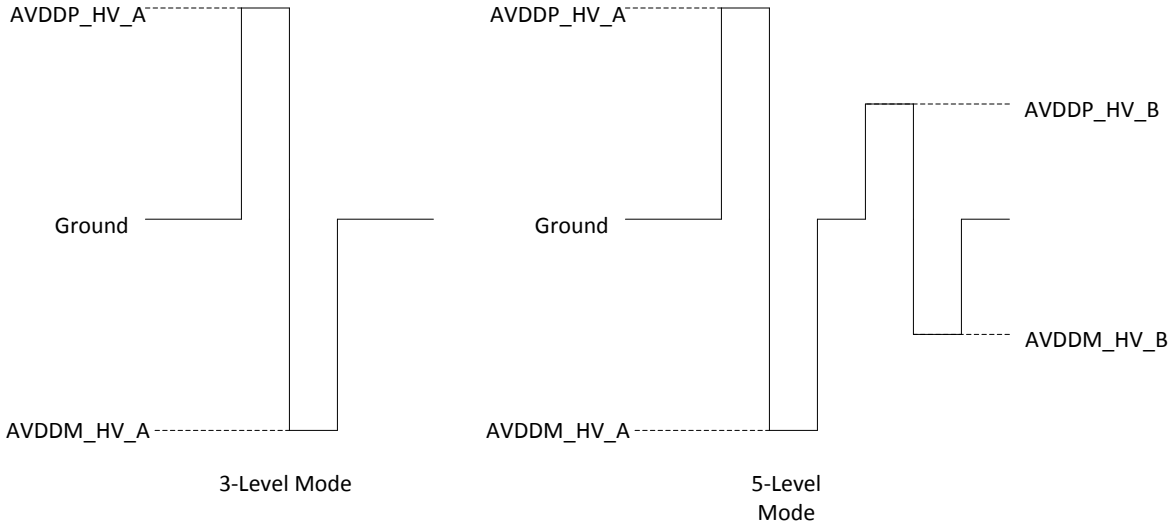


Figure 33. Typical 3-level and 5-level output waveform

The Table 4 list down the different features supported in 3-level and 5-level modes.

Table 4. Supported Modes for 3-Level and 5-Level Mode. See On-Chip Beam-Forming Mode

OUTPUT LEVEL MODE	# OF CHANNELS	# OF DELAY PROFILE	# OF PATTERN PROFILE	# OF TRANSITIONS PER PATTERN PROFILE
3-Level	16	16	48	16
5-Level	8	16	28	32

8.3.2.3 Floating LDO Power Modes

Floating LDO power modes: The significant part of device power is consumed by floating LDOs integrated in the device. The device has total eight floating LDOs, four are positive LDOs (FLOATP_HV_A1/2, FLOATP_HV_B1/2) generating V_{PHV_A} – 5, V_{PHV_B} – 5 volt supplies and other four are negative LDOs (FLOATM_HV_A1/2, FLOATM_HV_B1/2) generating V_{MHV_A} + 5, V_{MHV_B} + 5 volt supplies. All of these floating LDOs support different power modes as listed in Table 5. Device configures floating LDOs automatically in different power modes based on power mode of the device.

Table 5. Floating LDO Power Modes

FLOATING LDO POWER MODE	BIASING CURRENT	CURRENT THROUGH AVDD_PHV_A AND AVDD_PHV_B SUPPLIES	CURRENT THROUGH AVDD_MHV_A AND AVDD_MHV_B SUPPLY	TOTAL LDO POWER FOR ±100 V
Default power mode	Each LDO is biased with approximately 60-µA current.	60 µA × 2 = 120 µA	60 µA × 2 = 120 µA	48 mW
Power-down mode	LDO is completely powered down, and output of LDO discharges slowly.	0	0	0
High power mode	Each LDO is biased with approximately 330-µA current.	330 µA × 2 = 660 µA	330 µA × 2 = 660 µA	264 mW
Low power mode	Each LDO is biased with approximately10-µA current.	10 µA × 2 = 20 µA	10 µA × 2 = 20 uA	8 mW

8.3.2.4 Device Power Modes

The device supports different power modes through which user can optimize the system performance and operating complexity per requirements. Across power modes the BF_CLK, TR_BF_SYNC buffers and floating LDOs are biased in different modes. Supported power modes are:

1. Default power mode
2. Dynamic power mode
3. Transmitless power mode
4. Continuous wave mode
5. Standby mode
6. Global power-down mode

The 16 channels of the device are divided in two groups. Channel numbers A1, B1 to A4, B4 form group 1 channels, and channel A5, B5 to A8, B8 form group 2 channels. Floating supply LDOs FLOATP_HV_A1/B1 and FLOATM_HV_A1/B1 are referred as group 1 LDOs and FLOATP_HV_A2/B2 and FLOATM_HV_A2/B2 are referred as group 2 LDOs. These group terminologies are used while explaining the power modes. More details about different power modes listed in on-chip and off-chip beamforming modes are given as below.

8.3.2.4.1 Power Modes in Off-chip Beamforming Mode

In off-chip beamforming across all the different power modes, the BF_CLK buffer is powered down during receive mode, that is, whenever TR switch of all the channels is ON. The BF_CLK buffer is powered up during transmit mode, that is, whenever the TR switch of all the channels is OFF if RESYNC pin is set to ‘1’. If RESYNC pin is set to ‘0’ then BF_CLK buffer is always OFF.

8.3.2.4.1.1 Default Power Mode

After reset, device is configured by default in off-chip beamforming and default power mode. In this mode floating LDOs are configured in default power mode during both receive and transmit durations. Refer to Figure 34 and Table 6 for more details. Default power mode gives higher power compared to dynamic power mode because floating LDOs are always ON and it is easy to use. Not powering down the floating LDOs during receive mode removes the requirement of refreshing the floating node voltage periodically, which is required in dynamic power mode. In default power mode the maximum number of cycles in the output waveform is limited to 4 and maximum PRF supported is 10 kHz. Using more than 4 cycles in the output waveform or PRF higher than 10 kHz leads to performance degradation. When the device is transmitting more than 4 cycles, configure the LDO in high power mode by setting register bits LDO_MODE_G1, LDO_MODE_G2 to ‘1111’.

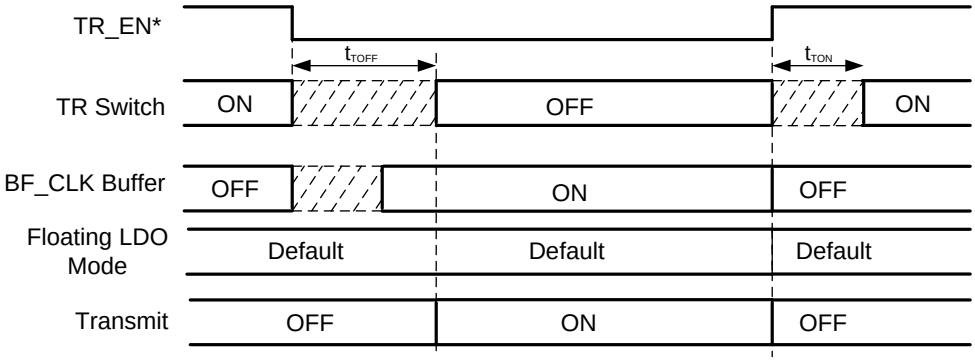


Figure 34. Default Power Mode in Off-chip Beamforming mode

8.3.2.4.1.2 Dynamic Power Mode

To get the lowest power and best performance from the device in transmit and receive mode (mainly in B-mode), TI recommends using dynamic power mode. To enable this mode set register bit EN_DYN_LDO to '1'. Refer to Figure 35 and Table 6 for more details. In dynamic power mode:

- Group 1 floating LDOs are configured in high power mode when either of TR_EN1 or TR_EN2 signal goes low (when TR switch is OFF) and in power-down mode when both TR_EN1 and TR_EN2 signal goes high (when TR switch is ON).
- Group 2 floating LDOs are configured in high power mode when either of TR_EN3 or TR_EN4 signal goes low (when TR switch is OFF) and in power-down mode when both TR_EN3 and TR_EN4 signal goes high (when TR switch is ON).
- Powering down LDOs in receive mode leads to the discharge of external capacitor connected between FLOAT* nodes and high voltage supplies. To avoid this discharge of the external capacitor, periodically power up the floating LDOs by keeping the TR_EN* signal low for minimum duration of 10 µs at rate of 200 Hz. Floating LDOs takes t_{WUP} time to wake up, and therefore only start the transmit after floating LDOs are powered up.

Dynamic power mode enables the device to consume lowest power in receive mode since LDOs does not consume any power. This mode is also considered as fast power-up mode with power-up time equals to t_{WUP} after applying the TR_EN* signal.

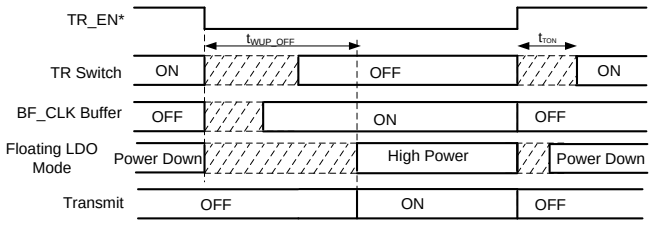


Figure 35. Dynamic Power Mode in Off-chip Beamforming mode

8.3.2.4.1.3 Transmit-Less Power Mode

To draw the lowest power from the device when device is not transmitting high voltage pulses, TI recommends using transmit-less power mode. Configure both group 1 and group 2 independently in transmit-less mode. To enable this mode first set register bit “EN_DYN_LDO” to ‘1’. To configure group 1 channels in transmit-less mode enable register bit PDN_CLK_SYNC_1 to ‘1’. To configure group 2 channels in transmit-less mode enable register bit PDN_CLK_SYNC_2 to ‘1’. The register bits PDN_CLK_SYNC* power down the clock buffer of corresponding groups. Transmit-less power mode is similar to dynamic power mode except the clock buffer is permanently powered down to save the power from digital clock switching. Refer to Figure 36 and Table 6 for more details. In transmit-less power mode:

- Group 1 floating LDOs get configured in high power mode when either of TR_EN1 or TR_EN2 signal goes low (when TR switch is OFF) and in power-down mode when both TR_EN1 and TR_EN2 signal goes high (when TR switch is ON).
- Group 2 floating LDOs get configured in high power mode when either of TR_EN3 or TR_EN4 signal goes low (when TR switch is OFF) and in power-down mode when both TR_EN3 and TR_EN4 signal goes high (when TR switch is ON).
- Powering down LDOs in receive mode leads to the discharge of the external capacitor connected between FLOAT* nodes and high voltage supplies. To avoid discharging the external capacitor, power up the floating LDOs periodically by keeping TR_EN* signal low for minimum duration of 10 µs at a rate of 200 Hz. Avoid powering up the floating LDO at a higher rate as it leads to increase in power from the device.

Transmit-less power mode is useful when device is not transmitting and it is possible to apply TR_EN* signal at a 200-Hz rate. This mode consumes the lowest power in receive mode because LDOs do not consume any power. Switching from transmit less power to dynamic power down is very fast. Set the register bits PDN_CLK_SYNC_1 and PDN_CLK_SYNC_2 to ‘0’ then make the TR_EN* signals low to transmit the signal.

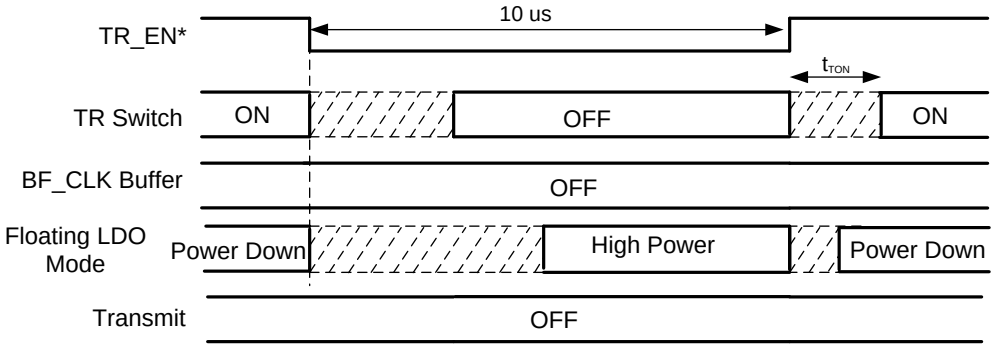


Figure 36. Transmit-Less Power Mode in Off-chip Beamforming mode

8.3.2.4.1.4 Continuous Wave (CW) Mode

For generating continuous signal on pulser output (required for CW imaging mode), TI recommends configuring the device in continuous-wave power mode. To configure the device in CW mode set pin CW_EN to 1. In this mode floating LDOs are configured in high power mode for both TR switch ON and OFF duration.

8.3.2.4.1.5 Standby Mode

Use standby power-down mode to draw lower power from the device when the device is not transmitting any signal. In this mode floating LDOs are configured in low power mode. The wake-up time from standby mode is given in *Electrical Characteristics*. The TR switch can be turned ON or OFF in this mode by applying TR_EN* signals.

8.3.2.4.1.6 Global Power-Down Mode

Use global power-down mode to get the lowest power from device when device is neither transmitting nor receiving any signal. In this mode floating LDOs and other internal biasing circuitry is switched off. The wake-up time from global power down mode is in range of ms (see *Electrical Characteristics*). To configure the device in global power down mode set register bit PDN_GBL to '1' and TX_BF_MODE bit to '0'.

In global power down mode:

- T/R switch gets configured in ON state.
- Keep TR_BF_SYC and TR_EN* control signals to logic '0'.

Table 6. Power Modes in Off-chip Beamforming Mode With Resync Set to ‘1’

POWER MODE	LDO POWER MODE		BF_CLK BUFFER		MAXIMUM PRF	MINIMUM LDO REFRESH RATE USING TR_EN* SIGNAL	MAXIMUM NUMBER OF CYCLES IN OUTPUT WAVEFORM
	DURING TRANSMIT	DURING RECEIVE	DURING TRANSMIT	DURING RECEIVE			
Default	Default	Default	ON	OFF	10 kHz	Not required	4
Dynamic	High power	Power down	ON	OFF	Not limited	200 Hz	Not limited
Transmit-less	High power	Power down	OFF	OFF	NA	200 Hz	NA
Continuous wave	High power	NA	ON	NA	Not limited	Not required	Not limited
Standby mode	Low power	Low power	OFF	OFF	NA	NA	NA
Global power down	Power down	Power down	OFF	OFF	NA	NA	NA

8.3.2.4.2 Power Modes in On-chip Beamforming Modes

Different power modes supported in on-chip beamforming mode are described in the following sections:

8.3.2.4.2.1 Default Power Mode

To configure the device in on-chip default power mode, apart from configuring the pattern and delay profile information, set the register bits DIS_DYN_CNTRL_1 and DIS_DYN_CNTRL_2 to ‘1’. In this mode floating LDOs are configured in default power mode during both receive and transmit durations and BF_CLK, TR_BF_SYNC buffers are always ON. See Figure 37 and Table 7 for more details. Default power mode gives higher power compared to dynamic power mode because floating LDOs are always ON, and it is easy to use. Not powering down the floating LDOs during receive mode removes the requirement of periodically refreshing the floating node voltage as required in dynamic power mode. In default power mode the maximum number of cycle in the output waveform is limited to 4, and maximum PRF supported is 10 kHz. Using more than 4 cycles in the output waveform or PRF higher than 10 kHz leads to performance degradation. When the device is transmitting more than 4 cycles, configure the LDO in high power mode by setting register bits LDO_MODE_G1, LDO_MODE_G2 to ‘1111’. Keep TR_EN* signals '0' throughout the device operation.

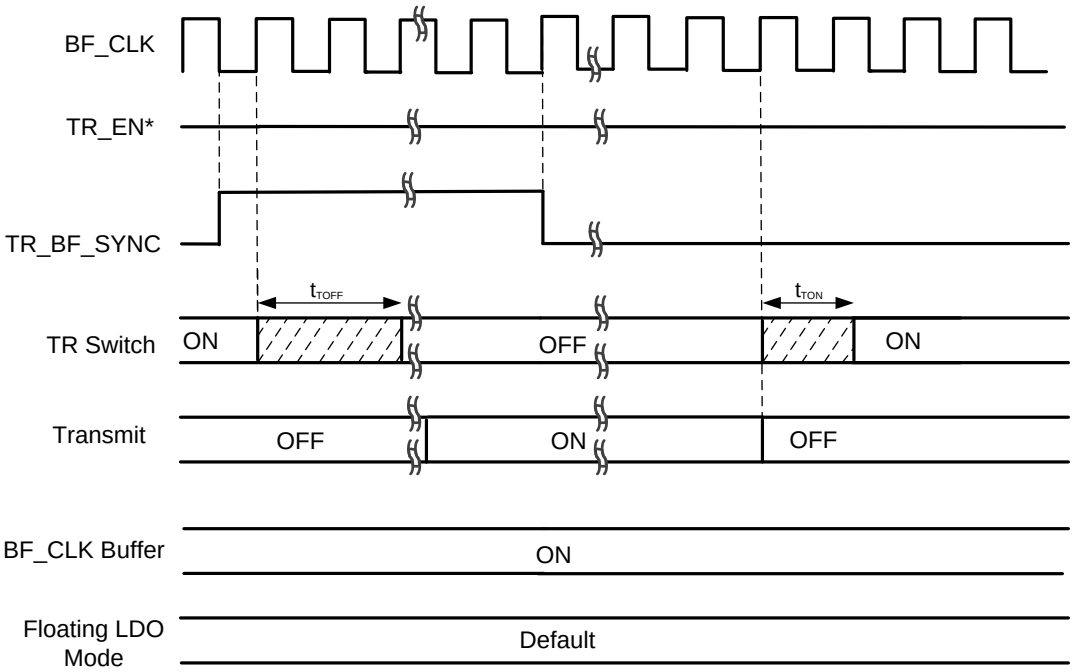


Figure 37. Default Power-Mode Timing in On-chip Beamforming

8.3.2.4.2.2 Dynamic Power Mode

For the lowest power and best performance from the device in transmit and receive mode (mainly in B-mode) TI recommends using dynamic power mode. To enable this mode set register bits DIS_DYN_CNTRL_1 and DIS_DYN_CNTRL_2 to '0' and "EN_DYN_LDO" to '1'. Refer to Figure 38 and Table 7 for more details. In dynamic power mode:

- The clock going to digital of group 1 channels shuts down once all the TR switches of group 1 channels turns ON. The clock for digital of group 1 channels turns ON when TR_EN1 signal goes high. TR_EN2 signal is not used.
- The clock going to digital of group 2 channels shuts down once all the TR switches of group 2 channels turns ON. The clock for digital of group 2 channels turns ON when TR_EN3 signal goes high. TR_EN4 signal is not used.
- Group 1 floating LDOs are configured in high power mode when TR_EN1 signal goes high and in power-down mode when TR switch of group 1 channels turns ON.
- Group 2 floating LDOs are configured in high power mode when TR_EN3 signal goes high and in power-down mode when TR switch of group 2 channels turns ON.
- Powering down LDOs in receive mode leads to the discharge of external capacitor connected between FLOAT* nodes and high voltage supplies. To avoid discharging the external capacitor, periodically power up the floating LDOs by keeping TR_EN* signal high for minimum duration of 10 us at rate of 200 Hz. Floating LDOs take t_{WUP} time to wake up, therefore only start the transmit after floating LDOs are powered up.

  Dynamic power mode enables the device to consume lowest power in receive mode because LDOs do not consume any power. Also consider this mode as fast power-up mode with power-up time equal to t_{WUP} after applying the TR_EN* signal.

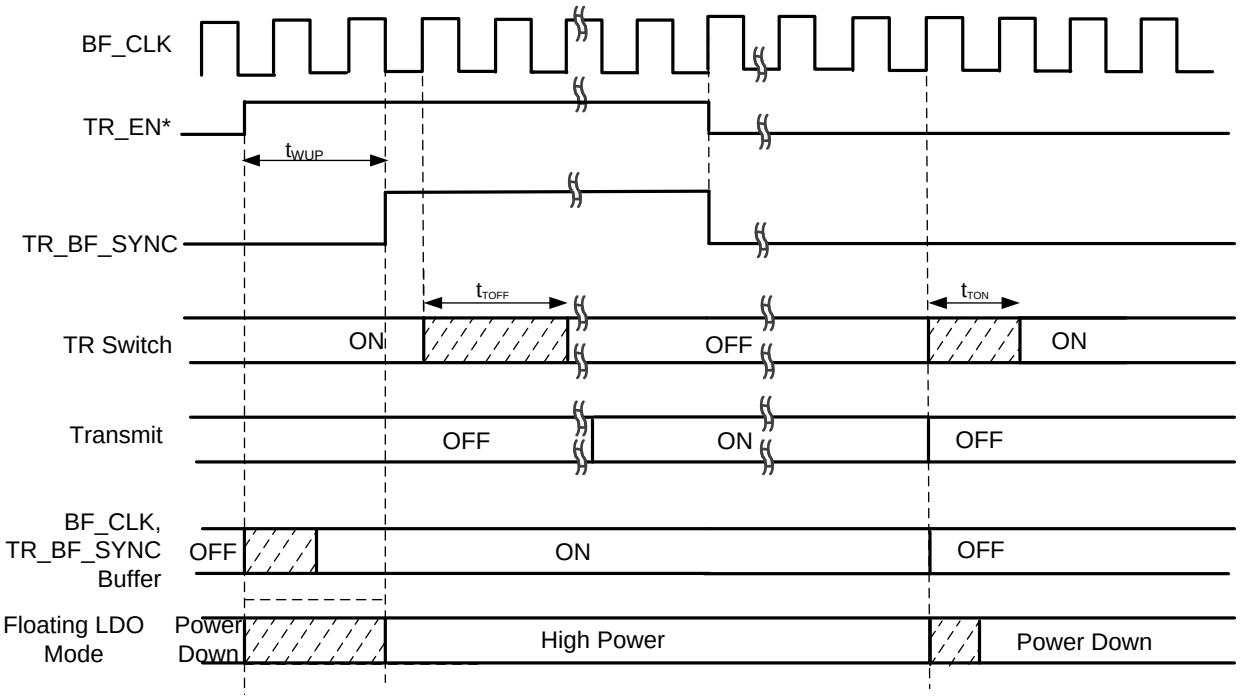


Figure 38. Dynamic Power Mode in On-chip Beamforming Mode

8.3.2.4.2.3 Transmit-Less Power Mode

To draw the lowest power from the device when device is not transmitting high voltage pulses, TI recommends using transmit-less power mode. Configure both group 1 and group 2 channels independently in transmit-less mode. To enable this mode set register bits DIS_DYN_CNTRL_1 and DIS_DYN_CNTRL_2 to '0' and "EN_DYN_LDO" to '1'. To configure group 1 channels in transmit-less mode enable register bit PDN_CLK_SYNC_1 to '1' and to configure group 2 channels in transmit less mode enable register bit PDN_CLK_SYNC_2 to '1'. The register bits PDN_CLK_SYNC* power down the clock buffer of corresponding groups. Transmit-less power mode is similar to dynamic power mode except the clock buffer is permanently powered down to save the power from digital clock switching. Refer to Figure 39 and table Table 7 for more details. In transmit-less power mode:

- Group 1 floating LDOs are configured in high power mode when the TR_EN1 signal goes high and in power-down mode when TR_EN1 signal goes low.
- Group 2 floating LDOs are configured in high power mode when the TR_EN3 signal goes high and in power-down mode when TR_EN3 signal goes low.
- Powering down LDOs in receive mode leads to the discharge of the external capacitor connected between FLOAT* nodes and high voltage supplies. To avoid discharging the external capacitor, power up the floating LDOs periodically by keeping TR_EN* signal high for minimum duration of 10 µs at rate of 200 Hz. Avoid powering up the floating LDO at a higher rate as it leads to increase in power from the device.

Transmit-less power mode is useful when device is not transmitting, and it is possible to apply TR_EN* signal at 200 Hz rate. This mode consume the lowest power in receive mode because LDOs do not consume any power. Switching from transmit-less power to dynamic power down is very fast. Set the register bits PDN_CLK_SYNC_1 and PDN_CLK_SYNC_2 to '0', make the TR_EN* signals high, and apply TR_BFSYNC signal.

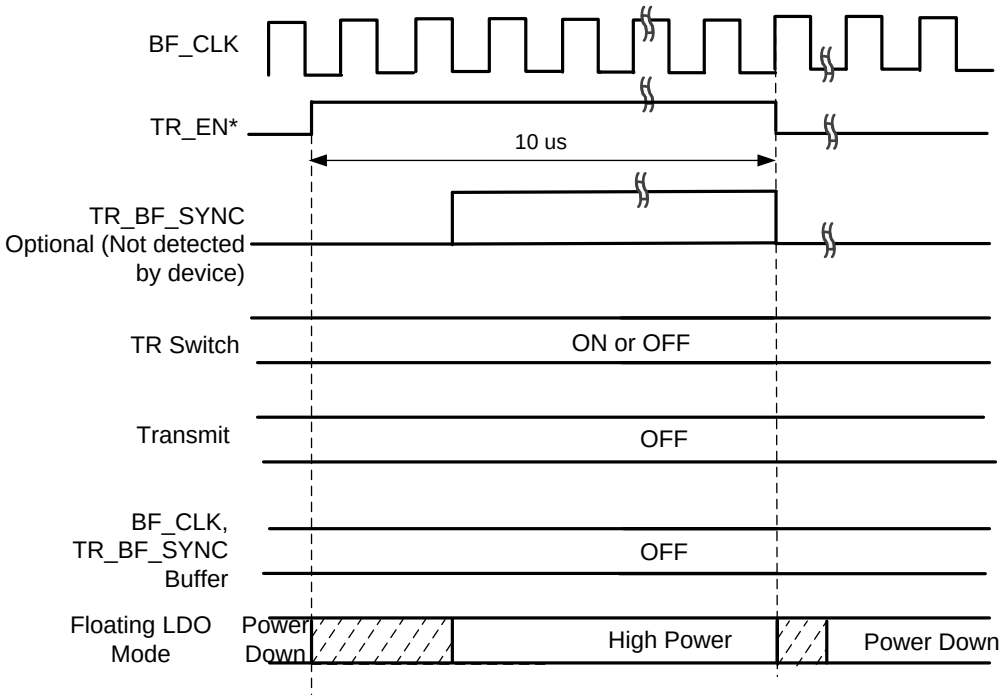


Figure 39. Transmit-less Power Mode in On-chip Beamforming mode

8.3.2.4.2.4 Continuous-Wave (CW) Mode

For generating a continuous signal on the pulser output (required for CW imaging mode), configure the device in CW power mode. The device is configured in CW power mode once CW mode of the device is enabled. Refer to Continuous Wave Mode (CW) for more details. In this mode floating LDOs are configured in high power mode permanently.

8.3.2.4.2.5 Standby Mode

Standby power-down mode is used to get lower power from device when device is not transmitting any signal. In this mode floating LDOs is configured in low power mode. The wake-up time from standby mode is given in Timing Requirements(1). When standby mode is enabled the clock to the device is immediately shut down. Thus, the device status is frozen, that is, if TR switch is ON it remains ON and if TR switch is OFF, it remains OFF until the device comes out of standby mode. If the device is transmitting pulses and standby mode is enabled, the pulser output goes to high impedance state.

8.3.2.4.2.6 Global Power-Down Mode

Use global power-down mode to get the lowest power from device when device is neither transmitting nor receiving any signal. In this mode floating LDOs and other internal biasing circuitry is switched off. The wake-up time from global power down mode is in range of ms (see *Electrical Characteristics*). To configure the device in global power down mode set register bit PDN_GBL to '1' and TX_BF_MODE bit to '0'.

In global power down mode:

- T/R switch gets configured in ON state.
- Keep TR_BF_SYC and TR_EN* control signals to logic '0'.

(1) All timing specifications are characterized but are not tested at production.

Table 7. Power Modes in On-chip Beamforming Mode

POWER MODE	LDO POWER MODE		BF_CLK BUFFER		MAXIMUM PRF	MINIMUM LDO REFRESH RATE USING TR_EN* SIGNAL	MAXIMUM NUMBER OF CYCLE IN OUTPUT WAVEFORM
	DURING TRANSMIT	DURING RECEIVE	DURING TRANSMIT	DURING RECEIVE			
Default	Default	Default	ON	ON	10 kHz	Not required	4
Dynamic	High power	Power down	ON	OFF	Not limited	200 Hz	Not limited
Transmit-less	High power	Power down	OFF	OFF	NA	200 Hz	NA
Continuous wave	High power	High power	ON	NA	Not limited	Not required	Not limited
Standby mode	Low power	Low power	OFF	OFF	NA	NA	NA
Global power down	Power down	Power down	OFF	OFF	NA	NA	NA

8.3.2.4.2.6.1 Guidelines for Selecting the Device Power Mode for Both Off-chip and On-chip Beamforming Mode

Hardware configuration: Consider an ultrasound system with multiple TX7316 ICs; see Figure 40. In such system it is recommended to keep TR_EN* signal separate across devices. It gives flexibility to control the power mode of individual IC independently to achieve lowest system level power.

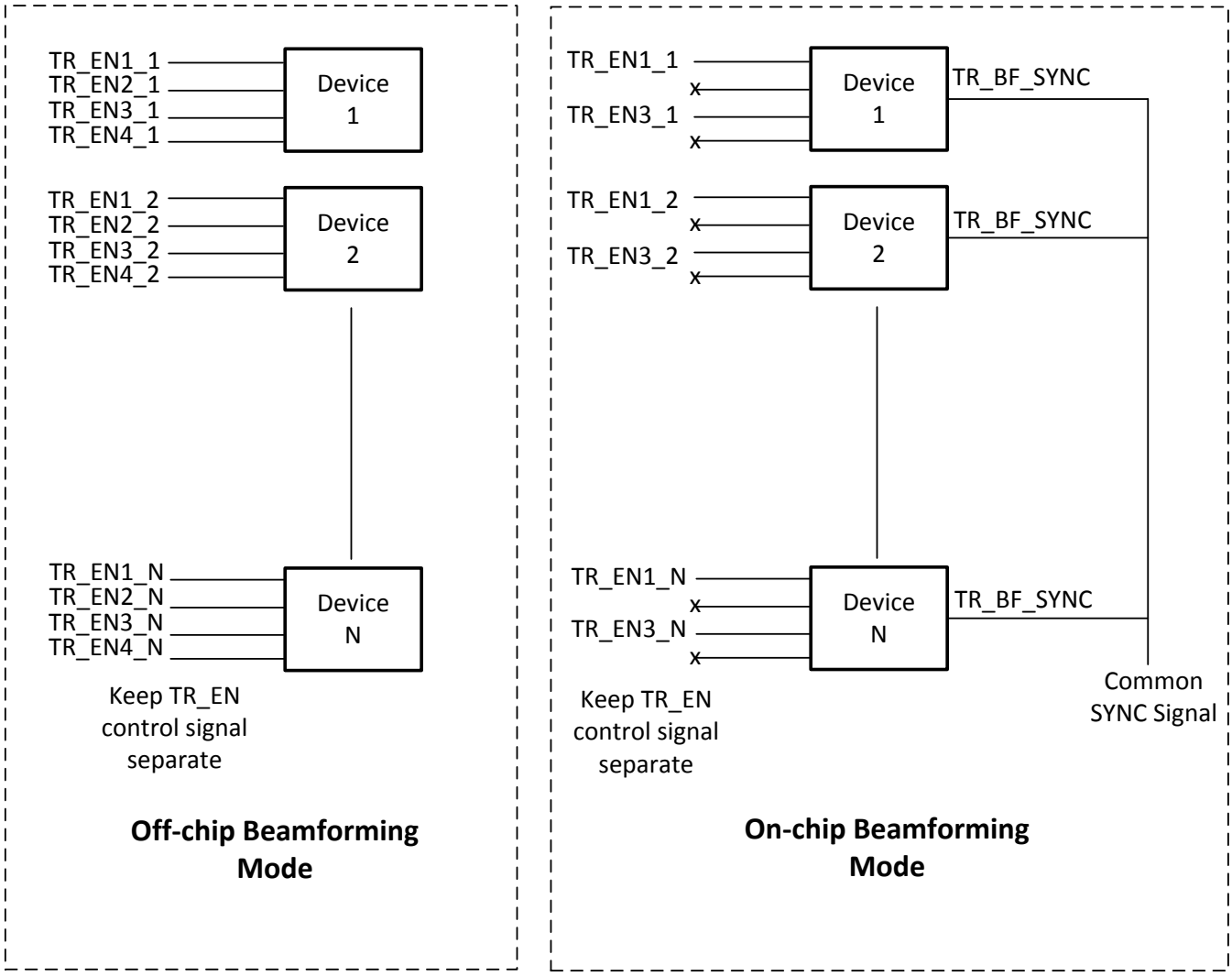


Figure 40. System Configuration Example

Configure the device as per suggestion below in the ultrasound systems:

1. *When device is both transmitting and receiving (transmit-receive mode):* This scenario occurs in B, PW mode of imaging. Configure the device either in default or dynamic power mode. Dynamic power mode gives lower power as compared to default mode however TR_EN* signals must be toggled at a minimum rate of 200 Hz in dynamic power mode. Dynamic power mode also allows exciting more than 4 cycles and PRF higher than 10 kHz in the output waveform without affecting the performance.
2. *When device is not transmitting but only receiving echo (T/R switch needs to be switched OFF during transmit phase and ON in receive phase):* This scenario occurs in B, PW mode of imaging. Configure the device either in default or dynamic power mode. To disable the transmit the pulser can be powered down. Dynamic power mode gives lower power as compared to default mode however TR_EN* signals must be toggled at a minimum rate of 200 Hz in dynamic power mode. Dynamic power mode also allows exciting more than 4 cycles and PRF higher than 10 kHz in the output waveform without affecting the performance.
3. *When device is continuously transmitting (minimum one channel is transmitting continuously)*: This scenario occurs in CW mode of imaging. In CW mode half of the channels in the system keep transmitting the waveform and other half keeps receiving echo from the body. For such a use case configure the device in CW power mode.
4. *When device is continuously receiving echoes (CW receive only mode — TR switch of all the channels are always ON):* This scenario occurs in CW mode of imaging. In CW mode half of the channels in the system

keep transmitting the waveform and other half keeps receiving echo from the body. In such scenario, configure the device in default power mode. Default power mode is higher as compared to other power modes but it is the quietest power mode because it doesn't involve toggling of TR_EN* signal, therefore does not affect the receiving echo signals.

5. *When device is not transmitting but only receiving echoes for short duration (B-mode receive only mode — If TR switch of all the channels shall be kept always ON):* This scenario occurs if TR switch of the device is used as multiplexer or limited numbers of channels in the system are transmitting but TR switch is turned ON for more number of channels to receive echo from the body. In such cases configure the device either in default or transmit-less power mode. Transmit-less power mode gives lower power compared to default mode; however, TR_EN* signals must be toggled at a minimum rate of 200 Hz in dynamic power mode. Toggle TR_EN* signal when echo is not being received by the device.
6. *When device is neither transmitting nor receiving (Idle mode) but requires quick wake-up time:* This scenario occurs when in the system there are 128 channels but only few of the channels are used for transmit and receive. During scanning of multiple lines different devices are used for transmit and receive, therefore requires quick wake-up time and consumes less power when not in use. In such scenario configure the device either in transmit-less power mode or default power or standby mode. Transmit-less power mode offers the lowest power and fast wake-up time.
7. *When device is neither transmitting nor receiving with large wake-up time:* This scenario occurs when system is not performing any imaging and must shut down to save power. In such scenario use the global power down mode.

8.3.3 Off-Chip Beam Forming Mode

On device power up and on applying reset, the device is by default configured in the off-chip beam forming mode. Functionality of TxBF, pattern generator and pulser block in off-chip beam forming mode is discussed in the following sections. The functionality described in following sections remain same whether CW_EN pin is set to '0' or '1'. However when device is expected to use in CW mode, it is required to set CW_EN pin to '1'.

8.3.3.1 Transmit Beam Former (TxBF)

Functional block diagram of TxBF is shown in Figure 41. The TxBF block processes and transfer all the input signals coming from the device pins to the pattern generator block. When the RESYNC pin is set to logic level '0', the TxBF block transfer all the input signals directly to pattern generator block and when RESYNC is set to logic level '1', the TxBF latches all the input signals using the BF_CLK clock before transferring the signals to the pattern generator block. Latching on BF_CLK clock signal helps in preventing the jitter on the external control signals from affecting the beamforming operation assuming BF_CLK applied to the device is a clean clock source.

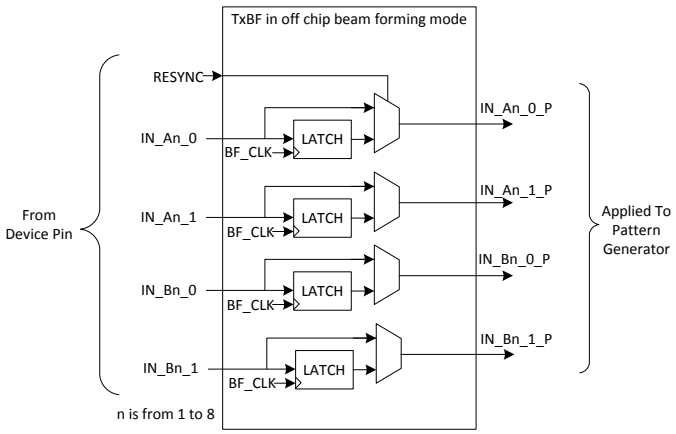


Figure 41. TxBF in off-chip transmit beam forming mode

8.3.3.2 Input Control Signal on Reset

Follow the below sequence for applying all the control signals IN_* to the device,

1. Apply reset to the device. During reset, all the pulser outputs get into high impedance state independent of signal applied on IN_* control signals.

2. After reset, first drive all the control signals IN_* to ‘0’.
3. After setting control signals to '0', apply control signals to the device as per the beamforming requirement.

8.3.3.3 Pattern Generator

The pattern generator block generates the control signals for the pulser based on the multiple input signals as shown in Figure 42. In following sections the pattern generator block operation is discussed for 3-level and 5-level modes.

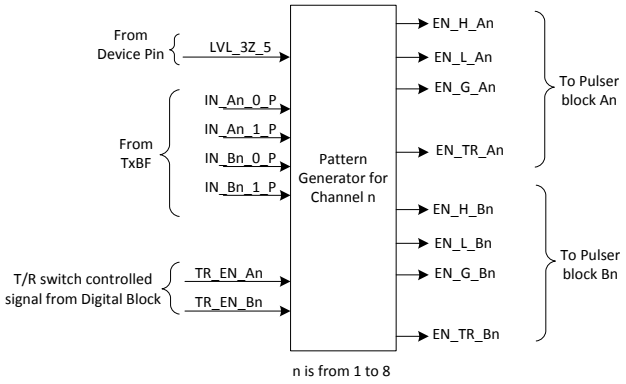


Figure 42. Pattern generator in off-chip transmit beam forming mode

8.3.3.3.1 3-Level Mode

When the device pin LVL_3Z_5 is set to logic level '0', the device operates in a 3-level mode. Table 8, and Table 9 list down the output signal level of the pattern generator block for the different combination of input signals.

Table 8. Pulser Control Signal Logic for Group A Pulser

PATTERN GENERATOR INPUT			PATTERN GENERATOR OUTPUT				DEVICE OUTPUT	
TR_EN_An	IN_An_1_P	IN_An_0_P	EN_H_An	EN_L_An	EN_G_An	EN_TR_An	Pulser output	T/R switch output
0	0	0	0	0	0	0	High impedance	Ground
0	0	1	0	1	0	0	AVDDM_HV_A	Ground
0	1	0	1	0	0	0	AVDDP_HV_A	Ground
0	1	1	0	0	1	0	Ground	Ground
1	0	0	0	0	0	1	High impedance	Connect to pulser output
1	0	1	0	0	0	1	High impedance	Connect to pulser output
1	1	0	0	0	0	1	High impedance	Connect to pulser output
1	1	1	0	0	1	1	Ground	Ground

Table 9. Pulser Control Signal Logic for Group B Pulser

PATTERN GENERATOR INPUT			PATTERN GENERATOR OUTPUT				DEVICE OUTPUT	
TR_EN_Bn	IN_Bn_1_P	IN_Bn_0_P	EN_H_Bn	EN_L_Bn	EN_G_Bn	EN_TR_Bn	Pulser output	T/R switch output
0	0	0	0	0	0	0	High impedance	Ground
0	0	1	0	1	0	0	AVDDM_HV_B	Ground
0	1	0	1	0	0	0	AVDDP_HV_B	Ground

Table 9. Pulser Control Signal Logic for Group B Pulser (continued)

PATTERN GENERATOR INPUT			PATTERN GENERATOR OUTPUT				DEVICE OUTPUT	
0	1	1	0	0	1	0	Ground	Ground
1	0	0	0	0	0	1	High impedance	Connect to pulser output
1	0	1	0	0	0	1	High impedance	Connect to pulser output
1	1	0	0	0	0	1	High impedance	Connect to pulser output
1	1	1	0	0	1	1	Ground	Ground

NOTE

When TR_EN_A/Bn signal is high, control signals IN_An/Bn_0 and IN_An/Bn_1 must not be kept to logic level '11'. Else, there will be high power consumption by the device.

8.3.3.4 5-Level Mode

When the device pin LVL_3Z_5 is set to logic level '1', the device operates in a 5-level mode. Table 10 list down the output signal level for the different combination of input signals. In 5-level mode, the signals are reconfigured as mentioned below:

- Input signal IN_Bn_1_P is not used by pattern generator block to decide output signals level.
- Output signal EN_TR_An = EN_TR_Bn.
- Output signals EN_G_An and EN_G_Bn are shorted.

Table 10. Pulser Control Signal Logic

PATTERN GENERATOR INPUT				PATTERN GENERATOR OUTPUT						DEVICE OUTPUT	
TR_EN_An/Bn	IN_Bn_0_P	IN_An_1_P	IN_An_0_P	EN_H_An	EN_L_An	EN_G_An = EN_G_Bn	EN_H_Bn	EN_L_Bn	EN_TR_An/Bn	Pulser output	T/R switch output
0	X	0	0	0	0	0	0	0	0	High impedance	Ground
0	0	0	1	0	1	0	0	0	0	AVDDM_HV_A	Ground
0	0	1	0	1	0	0	0	0	0	AVDDP_HV_A	Ground
0	X	1	1	0	0	1	0	0	0	Ground	Ground
0	1	0	1	0	0	0	0	1	0	AVDDM_HV_B	Ground
0	1	1	0	0	0	0	1	0	0	AVDDP_HV_B	Ground
1	X	0	0	0	0	0	0	0	1	High impedance	Connect to pulser output
1	X	0	1	0	0	0	0	0	1	High impedance	Connect to pulser output
1	X	1	0	0	0	0	0	0	1	High impedance	Connect to pulser output
1	X	1	1	0	0	1	0	0	0	Ground	Ground

NOTE

When TR_EN_A/Bn signal is high, control signals IN_An_0 and IN_An_1 must not be kept to logic level '11'. Else, there will be high power consumption by the device.

8.3.3.5 IN_* Control Signal Timing

In off-chip beam forming mode and with RESYNC = '1' , it is required to meet setup and hold timing constraints on the IN_* signals with respect to the BF_CLK clock signal; Refer to Figure 43. Parameter values are listed in the Timing Requirements(1) table.

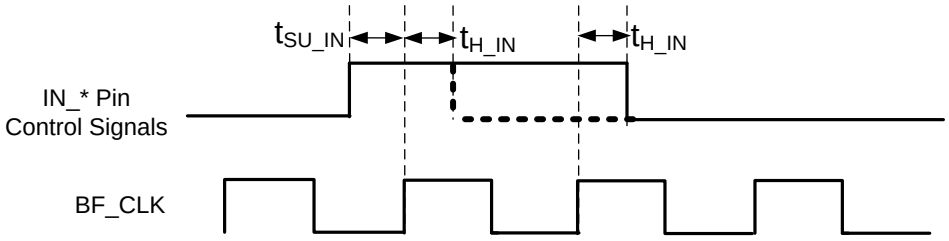


Figure 43. Setup and Hold Time Constraint for the IN_* Signal

8.3.3.6 IN_* to Pulser Output Propagation Delay

In the off-chip beam forming mode, the pulser output (OUT_*) changes after a fixed propagation delay from the change of input control signals (IN_*). For RESYNC pin set to '0', propagation delay is defined as the time difference between the instant when the input control signal crosses 50% threshold to the instant when the pulser output voltage changes by 1V. For RESYNC pin set to '1', propagation delay is defined as the time difference between the instant when the BF_CLK edge (that latches the IN_* signals) crosses 50% threshold to the instant when the pulser output voltage changes by 1V; see Figure 44. Parameter values are listed in the Timing Requirements(1) table.

(1) All timing specifications are characterized but are not tested at production.

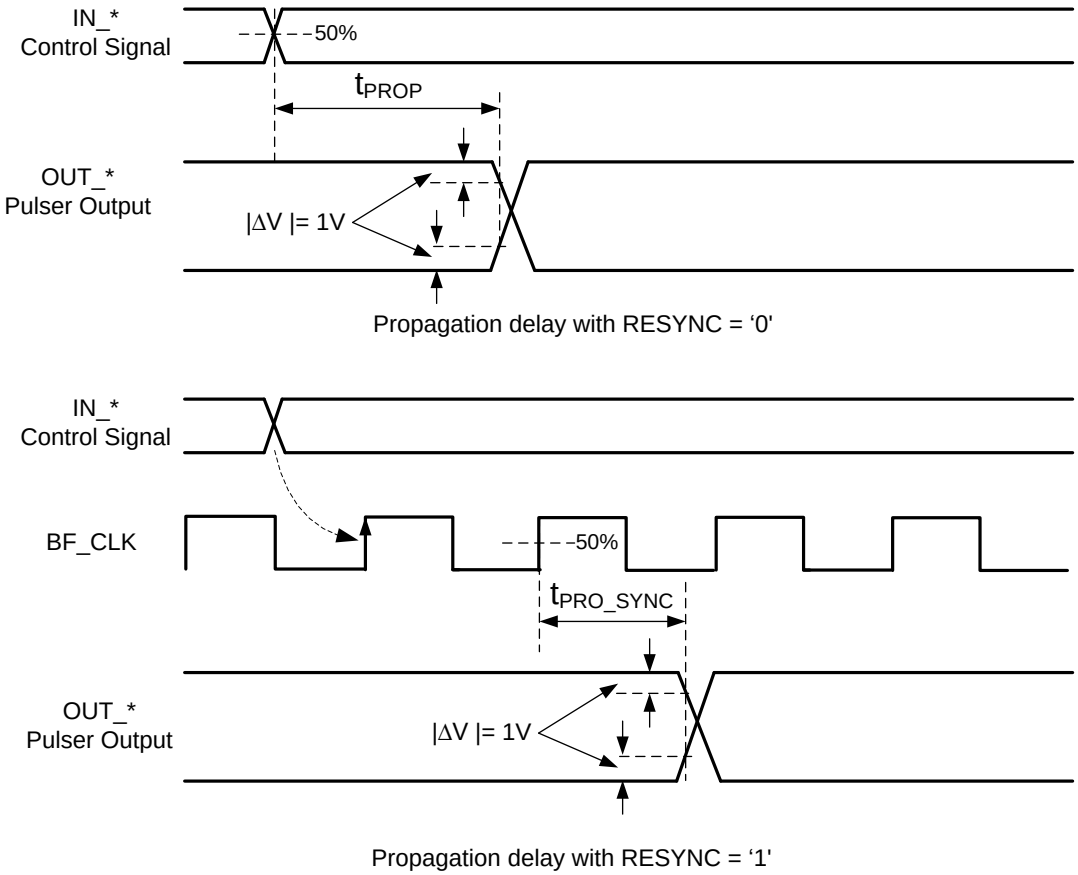


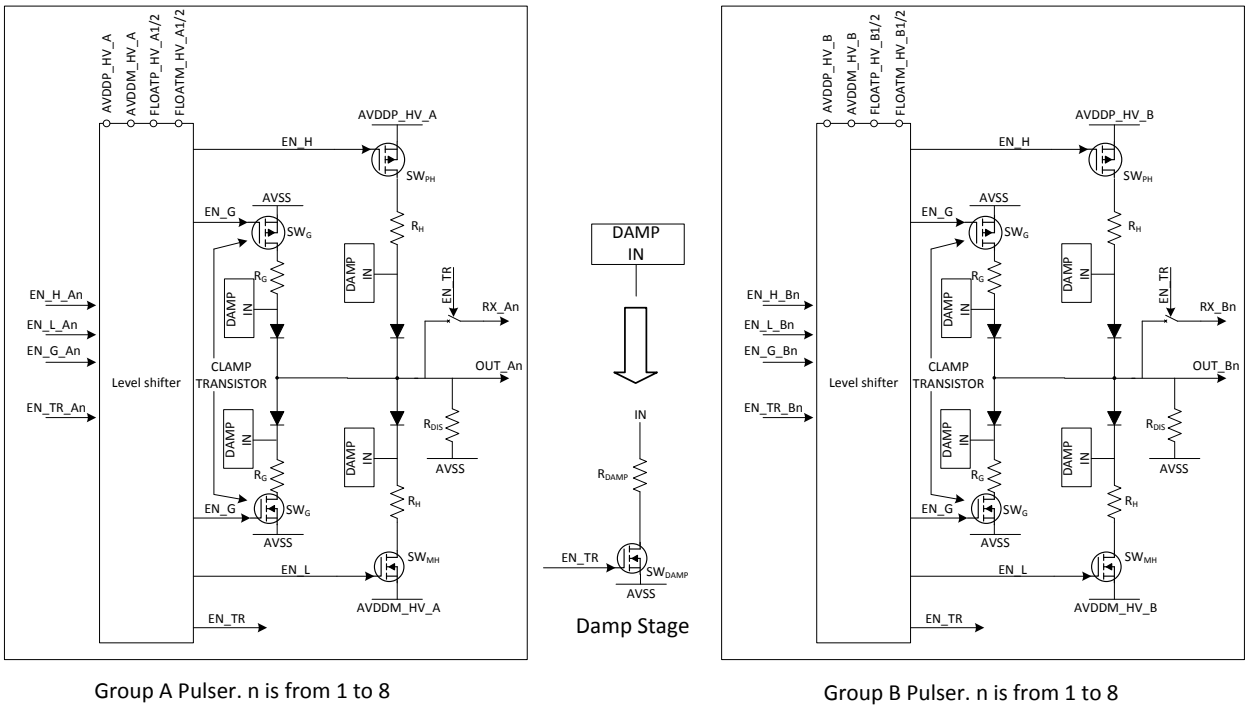
Figure 44. IN_* to Pulser Output Propagation Delay Diagram

8.3.3.7 Pulser

Functionality of the pulser block is independent of beam forming and output level mode. Figure 45 shows a combined block diagram of group A and group B pulser blocks. In the device there exist such 8 pulser blocks. The pulser get all the input signals from the pattern generator. Below list describes the pulser block diagram,

- Group A pulser operates on high voltage supplies AVDDP_HV_A and AVDDM_HV_A. Group B pulser operates on high voltage supplies AVDDP_HV_B and AVDDM_HV_B.
- Level shifter blocks shift the logic level from the low voltage signals coming from the pattern generator block to the high voltage domain.
- The pulser block consists of three types of transistors
  1. First one is output transistors SW_{PH} and SW_{MH} which connects the output to high voltage supplies.
  2. Second one is clamp transistor SW_G which connects the output to ground.
  3. And third one is damp transistor that connects the output to ground through damp resistor R_{DAMP}.
- In all the different arms of pulser block, there exist a diode to prevent the current flow in opposite direction.
- All the different transistors and T/R switches turns on when corresponding control signal goes to logic level '1'.
- At the OUT_A/Bn node a fix resistor R_{DIS} to AVSS is added to avoid the build of any unwanted DC voltage when pulser output is in high impedance state.
- A simplified schematic of the T/R switch is shown in Figure 46. T/R switch turns on when EN_TR is set to logic level '1', and turns off when EN_TR is set to logic level '0'. It consists of a series transistor which remain off when T/R switch is off and protects the low voltage Rx from high voltage pulses. This series transistor turns on when the T/R switch is on and connects the Rx input to the ultrasound transducer. On the low voltage Rx input side, there exists a transistor to AVSS which turns On when the T/R switch is Off. It helps in reducing a T/R switch leakage in transmission phase. T/R switch equivalent diagram in On and Off state is

also shown in Figure 46.



Group A Pulser. n is from 1 to 8

Group B Pulser. n is from 1 to 8

Figure 45. Group A and Group B Pulser Block Diagram

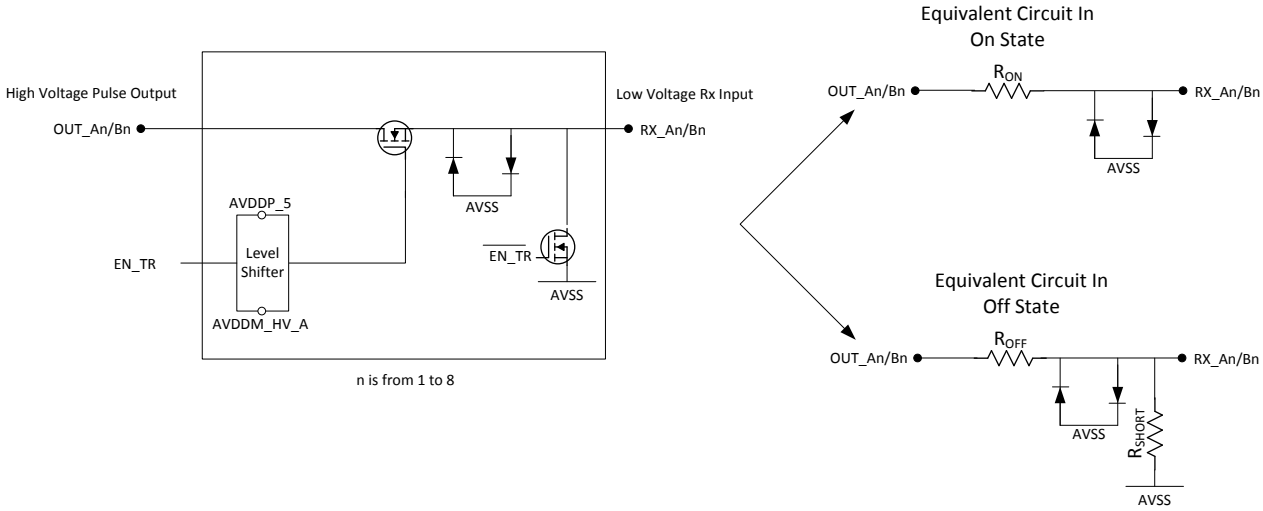


Figure 46. Simplified Schematic of T/R Switch

8.3.4 On-Chip Beam-Forming Mode

When the device is powered up and upon applying reset, by default, the device is configured in off-chip beamforming mode. To configure the device in on-chip beamforming mode, set the register bit TX_BF_MODE to '1'. In on-chip beamforming mode, connect all the IN_* input control pins to AVSS.

The on-chip beamforming mode greatly simplifies controlling the beamforming operation. Unlike the off-chip beamforming mode, it does not require additional input control signals to define the instantaneous pulse transitions. Instead, the delay and pattern (shape) of the pulse on each of the output channels are stored in delay and pattern profiles. There are many such profile sets that can be programmed at start through the SPI interface. Each transmit window is defined by a TR_BF_SYNC pulse, and the required profile to be used for a transmit window can be loaded through a single register control. Additionally, a new profile (for example, a delay profile required for a certain focusing depth) can also be programmed prior to the start of the transmit window. A pattern defined by the pattern profile can be set to be fired one-shot, or to be repeated a certain number of times. Also, in the CW mode (with CW_MODE_EN=1), the defined pattern can be made to repeat in a continuous manner until the next TR_BF_SYNC pulse. Additionally, an Elastography mode enables repetition of the pattern in a continuous manner for a specified period of time.

The on-chip beamformer mode also offers flexible dynamic control of the T/R switch turning on and off. For example, the turning on of the T/R switch (which signals the start of the receive phase) can be controlled based on a fixed delay either with respect to TR_BF_SYNC, or with respect to the end of the transmit window. In the event that the T/R switch is inadvertently timed to turn on while the transmit window is still active, the device automatically blanks out the pulsing operation and goes into high impedance output state before turning on the T/R switch.

Similar to the off-chip beamforming mode, the implementation of the on-chip beamforming mode also involves the TxBF and pattern generator blocks. The TxBF block loads the selected delay profile for all the channels and generates a delayed, divided version of the BF_CLK for each channel. The pattern generator block of each channel uses the output clock from the TxBF to generate a pattern based on the pattern profile for the channel.

The functionality of the TxBF and pattern generator block in on-chip beam forming mode is discussed in the following sections.

8.3.4.1 Trigger Signal in On-chip Beamforming

Applying the trigger signal to device is the first step to start the on-chip beamforming operation. There are two ways to apply the trigger signal, explained in the following:

1. Dynamic trigger mode: To achieve the low power from the device the floating LDOs, BF_CLK and the TR_BF_SYNC buffer in the device are powered down during the receive mode. In order to apply the trigger signal to the device, floating LDOs, BF_CLK and the TR_BF_SYNC buffer must be powered up. A signal applied on TR_EN* pins is used to power up these blocks. After this pulse on TR_BF_SYNC pin is used to trigger the device; see Figure 47.

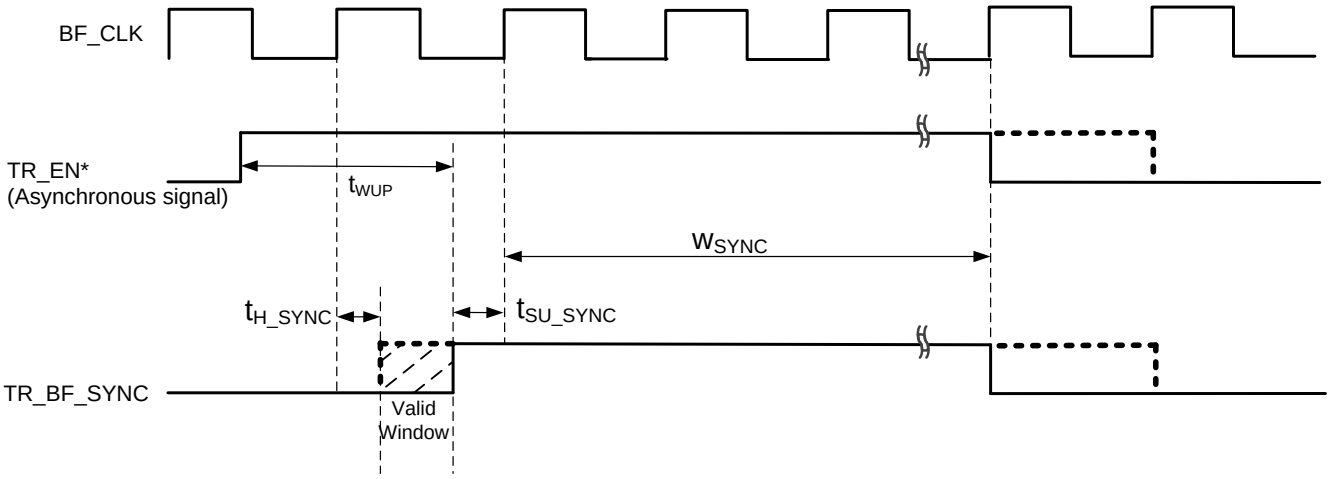


Figure 47. TR_BF_SYNC Timing requirement for Dynamic Trigger Mode

2. Static trigger mode: when the system hardware does not have capability to generate the signal on TR_EN* pins, the BF_CLK clock and the TR_BF_SYNC buffer can be made permanently ON by writing register bits DIS_DYN_CNTRL_1 and DIS_DYN_CNTRL_2 to '1'. Keeping these buffers permanently ON leads to extra power from the device. In this mode just applying a pulse on TR_BF_SYNC pin triggers the device; see Figure 48.

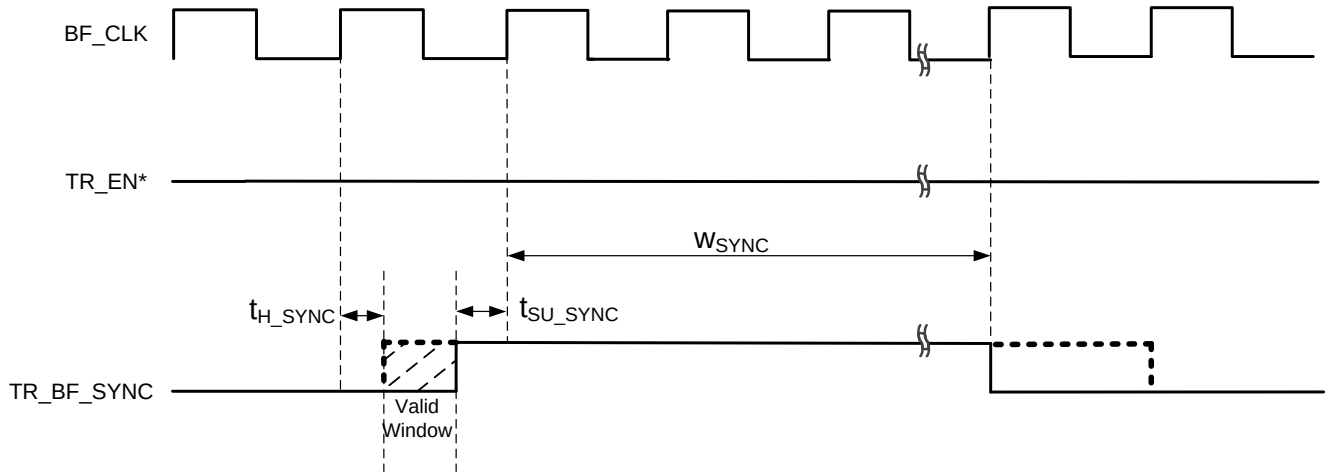


Figure 48. TR_BF_SYNC Timing Requirement for Static Trigger mode

NOTE

For simplicity in explanation, only TR_BF_SYNC pulse is shown as trigger signal in this document. It is assumed that TR_EN* signals is applied if device is configured in dynamic trigger mode.

8.3.4.1.1 TR_BF_SYNC Timing

In both dynamic and static trigger mode, proper functionality of the device TR_BF_SYNC signal requires meeting both setup and hold timing constraints with respect to the BF_CLK clock signal. Refer to Figure 47 and Figure 48 for static and dynamic trigger mode. *Electrical Characteristics* lists the parameter values.

8.3.4.2 Transmit Beamformer (TxBF)

The functional block diagram of TxBF block in on-chip beamforming mode is shown in Figure 49. TxBF block takes its input from the delay profiles, register settings and device pins. Based on these input signals, the TxBF block generates a clock signal for the pattern generator block. The TxBF block consist of total 16 counters and 16 clock dividers. These 16 counters and clock dividers are divided in two subgroups; group A and group B with each having 8 dividers and 8 counters.

The operation of delay generation as well as clock division is initiated by the TR_BF_SYNC pulse. The programmed delay is generated by a counter (individual for each channel), which also generates an enable for the clock divider block following it. The clock divider block generates a divided clock (with the division factor being programmable to the same value for all the channels). In this manner, a delay and divided clock is individually generated for each channel.

Note that on receiving the TR_BF_SYNC pulse, the T/R switch starts to turn off. However, the T/R switch takes about 2 µs to fully turn off. For this reason, a control is provided through the TX_START_DEL register control to delay the TxBF state machine relative to the TR_BF_SYNC pulse.

Figure 50 and the following steps describe the sequence of operations performed by the TxBF block:

- On reception of a TR_BF_SYNC, the outputs and values of all the counters are set to zero and each counter waits for an enable pulse. Similarly all the clock dividers get reset and disabled on the TR_BF_SYNC pulse and wait for the enable signal from the corresponding counter.
- The enable pulse for the counter is generated by delaying TR_BF_SYNC pulse by TX_DEL number of BF_CLK clock periods. This delay of TX_DEL number of BF_CLK clock periods is set by programming the TX_START_DEL register control. Table 11 list the value of TX_DEL based on the programmed TX_START_DEL for the 3-level and 5-level modes.
- On receiving the enable pulse, each counter {C_A1, C_B1}, .. to {C_A8, C_B8} starts counting and generates the enable signal for the clock divider (EN_DIV_An/Bn signals) after DEL_An/Bn number of BF_CLK clock cycles. The DEL_An/Bn control comes from the chosen delay profile. The device supports maximum delay

(DEL_An/Bn) value of 2^13 BF_CLK clock periods and minimum delay of 1 BF_CLK clock period.

- After receiving its enable signal, the clock divider generates output clock signals CLK_A1, CLK_B1,…to CLK_A8, CLK_B8 by dividing BF_CLK clock signal by factor 2^N. Here N represents decimal value of CLK_DIV register control with minimum and maximum value of 0 and 5 respectively. An internal propagation delay t_{PROP_INT} from BF_CLK to divided clock is also involved in the generation of the output clock. The parameter value of t_{PROG_INT} is listed in the table.
- In the 3-level pulser mode all the 16 counter and clock dividers are enabled. In the 5-level pulser mode, counter C_B1 to C_B8 and clock divider D_B1 to D_B8 gets disabled permanently.

NOTE

In both 3-level and 5-level mode it is required to configure TX_DEL to greater than 2 µs. Based on BF_CLK clock speed, a user need to program TX_START_DEL to get TX_DEL time duration greater than 2us. A duration of 2us is required to switch off the T/R switch.

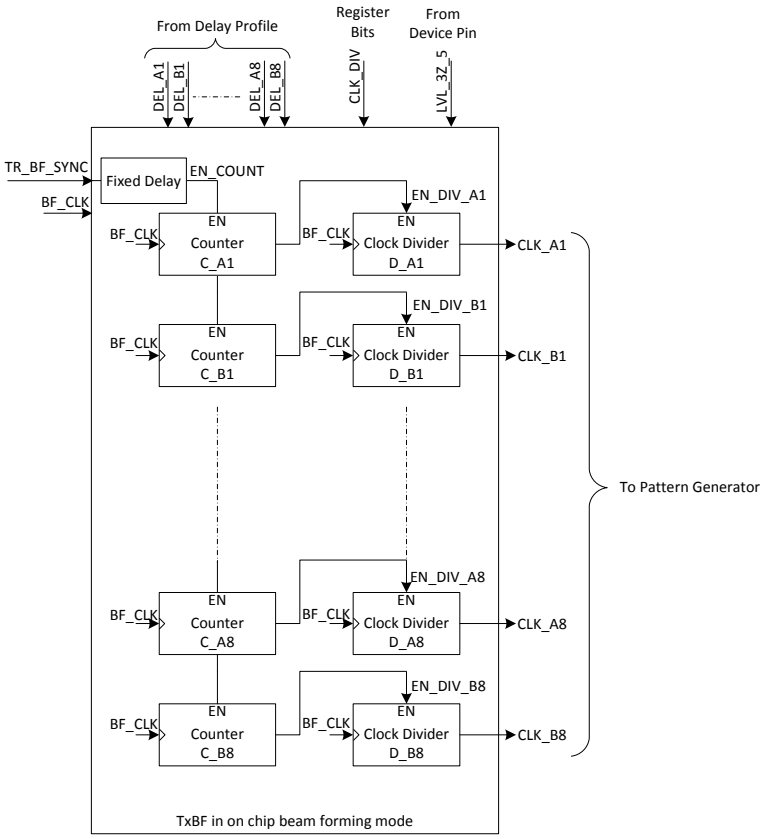


Figure 49. TxBF in On-chip Beamforming Mode

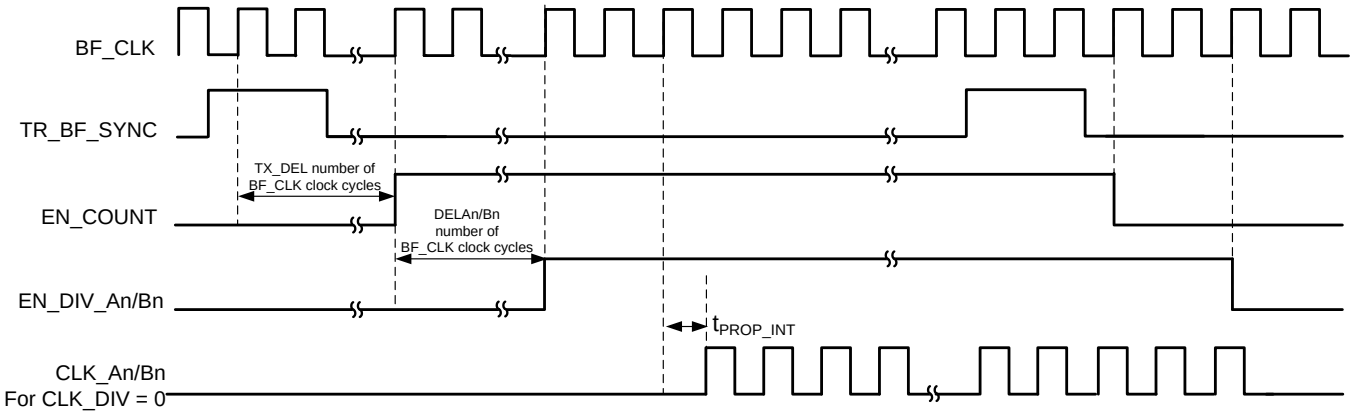


Figure 50. Timing Diagram of TxBF in On-chip Beam Forming Mode

Table 11. TxBF Timing Information in On Chip Beamforming Mod

PARAMETER	3-LEVEL	5-LEVEL
TX_DEL	8 * TX_START_DEL + 313	8 * TX_START_DEL + 297

8.3.4.3 Pattern Generator

A pattern generator in the device generates control signals for pulser based on the multiple input signals as shown in Figure 51. The pattern-generator block supports total three modes of operation as described in following sections.

8.3.4.3.1 B-Mode

In B-mode operation pattern generator generates a finite number of output pulses.

The pattern generator generates the controls for the switching operation in the pulser. Each transition is defined by two parameters in the patter profile: the level control (LVL_x) that defines the output level of the pulser and the period control (PER_x) that specifies the duration for which the level should be maintained. The state machine in the pattern generator keeps progressing in sequence across multiple such level/ period combinations until a level that specifies a termination of the pattern. Each such sequence represents one pulse pattern. The pulse pattern can be made to come just once (for each TR_BF_SYNC) or repeat a fixed number of times or repeat indefinitely.

The inputs to the pattern generator block in the on-chip beamforming mode are the following:

1. LVL_3Z_5: Specifies if the pulsing mode is 3-level or 5-level
2. TR_EN_An, TR_EN_Bn: The dynamic control for the T/R switch generated by the Digital block
3. CLK_An, CLK_Bn: The delayed, divided clock for the channel from the TxBF block
4. TR_BF_SYNC: The synchronization signal that starts a new transmission
5. The pattern information is contained in the parameters LVL_*, and PER_* from the chosen pattern profile, programmable register TAIL_COUNT and REPEAT_COUNT.

In the following sections the pattern generator block operation in on-chip beamforming mode is discussed for 3-level and 5-level pulser modes

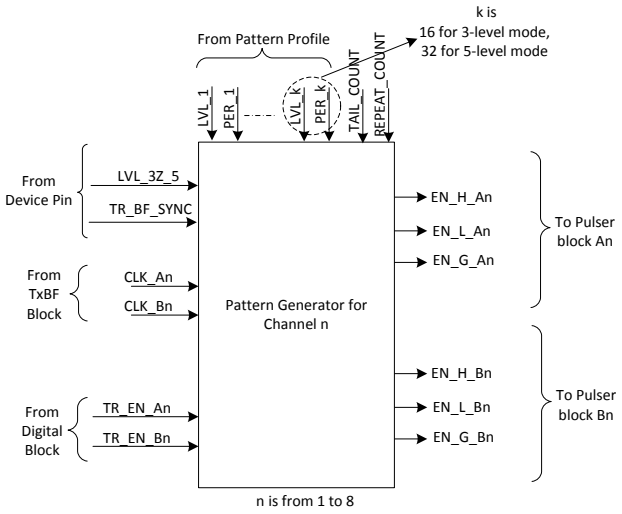


Figure 51. Pattern Generator in On-Chip beam Forming Mode

8.3.4.3.1.1 3-Level Mode

When the device is configured in 3-level mode, the pattern generator gets divided in two blocks; block A and block B with the same functionality. Block A operates on the CLK_An clock signal from the TxBF and generate signals for the group A pulser. Similarly block B operates on CLK_Bn clock signal from the TxBF and generates signals for the group B pulser. Below description explains the different steps followed by the group A block of the pattern generator. The same description also applies for the group B block of the pattern generator.

- The pattern generator block gets reset on receiving a pulse from the device pin TR_BF_SYNC. On getting reset all the output signals are set to ‘0’.
- The output signals of pattern generator block are gated with EN_TR_An signal. Whenever EN_TR_An signal goes to '1' then corresponding signals EN_H_An, EN_L_An, and EN_G_An goes to logic level '0'; see Table 12.
  1. Pattern generator block read the values of LVL_1 and PER_1 loaded from the pattern profile. LVL_1 decides the output level of the pulser as per Table 12. The output level which is determined by the LVL_1 parameter is held for (N+2) number of CLK_An clock cycles, where N represents value stored in the PER_1 parameter. N is programmable in the range of 0 to 30.
  2. In next step, the pattern generator reads the LVL_2 and PER_2 signals and generate the next set of pattern generator output.
  3. In a similar manner, the pattern generator keeps reading the subsequent sets of LVL_x and PER_x signals and keeps generating the corresponding output until after it has read and responded to the last signal i.e. LVL_16 and PER_16 or it reads any intermediate LVL_x equal to "111". In any of the cases, the pattern generator repeats step 1 to step 3 for M number of times and then goes to the tail state. Here M represents value programmed in register REPEAT_COUNT.
  4. Tail state: In the tail state, the output of pattern generator block remains fixed as EN_H_An = 0, En_L_An = 0, and EN_G_An = 1. This signal combination connects the pulser output to ground. The Pattern generator block remain in tail state for (P+1) number of CLK_An clock periods. Here P represents decimal value of signal TAIL_COUNT and can be programmed in range of 1 to 31. If the TAIL_COUNT is set to 0, there is no tail pattern.

5. After finishing up the tail pattern, the pattern generator disables all the output signal and the pulser output goes to “high impedance" state. The Pattern generator remain in this state till the next TR_BF_SYNC pulse is applied. Refer to Figure 52

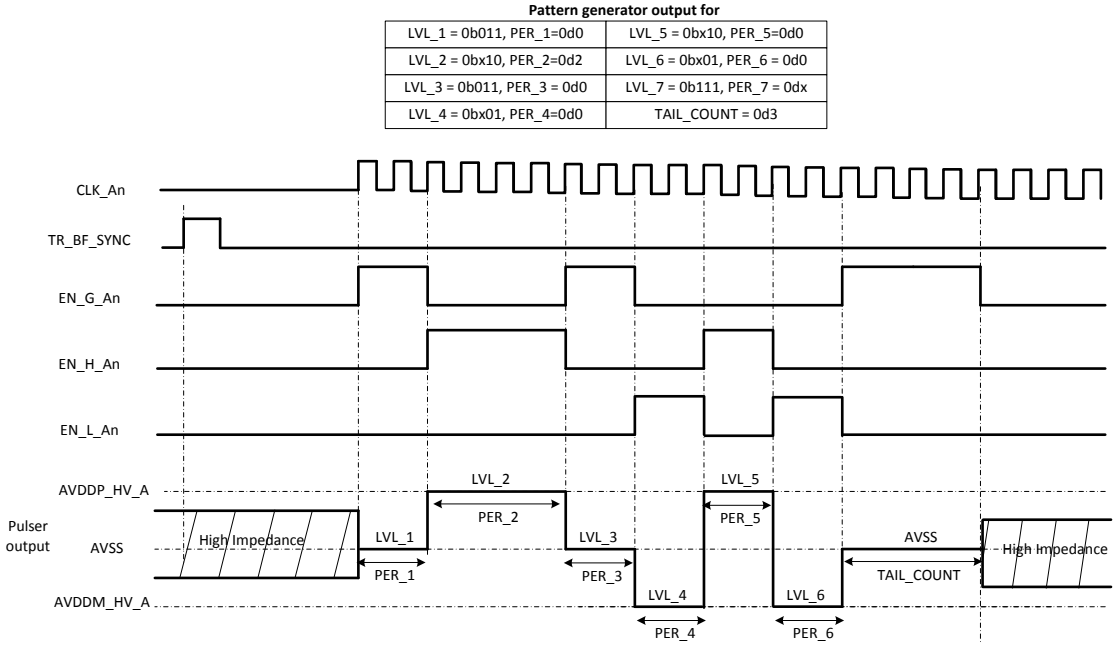


Figure 52. Pattern Generator Output for 3-Level Mode

Table 12. Pulser Control Signal Logic for Group A Pulser

PATTERN GENERATOR INPUT		PATTERN GENERATOR OUTPUT(1)			DEVICE OUTPUT	
EN_TR_An	LVL_x(1)	EN_H_An	EN_L_An	EN_G_An	Pulser output	T/R switch output
0	0bx00	0	0	0	High impedance	Ground
0	0bx01	0	1	0	AVDDM_HV_A	Ground
0	0bx10	1	0	0	AVDDP_HV_A	Ground
0	0b011	0	0	1	Ground	Ground
0	0b111	0	0	0	Represents end of pattern	Represents end of pattern
1	0bxxx	0	0	0	High impedance	Connect to pulser output

(1) x -> 1 to 16

Table 13. Pulser Control Signal Logic for Group B Pulser

PATTERN GENERATOR INPUT		PATTERN GENERATOR OUTPUT(1)			DEVICE OUTPUT	
EN_TR_Bn	LVL_x(1)	EN_H_Bn	EN_L_Bn	EN_G_Bn	Pulser output	T/R switch output
0	0bx00	0	0	0	High impedance	Ground
0	0bx01	0	1	0	AVDDM_HV_B	Ground
0	0bx10	1	0	0	AVDDP_HV_B	Ground

(1) x -> 1 to 16

Table 13. Pulser Control Signal Logic for Group B Pulser (continued)

PATTERN GENERATOR INPUT		PATTERN GENERATOR OUTPUT(1)			DEVICE OUTPUT	
0	0b011	0	0	1	Ground	Ground
0	0b111	0	0	0	Represents end of pattern	Represents end of pattern
1	0bxxx	0	0	0	High impedance	Connect to pulser output

8.3.4.3.1.2 5-Level Mode

When device is configured in 5-level mode, pattern generator operates only on CLK_An clock signal to generate signals for both group A and group B pulser. Below description explains the different steps followed by pattern generator.

- The pattern generator blocks get reset on receiving a pulse form the device pin TR_BF_SYNC. On getting reset all the output signals are set to ‘0’.
- The output signals of pattern generator block is gated with EN_TR_An signal. Whenever EN_TR_An signal goes to '1' then the corresponding EN_H_An/Bn, EN_L_An/Bn, and EN_G_An/Bn goes to logic level '0'; see Table 14.
  1. The Pattern generator block read the values of LVL_1 and PER_1 coming from pattern profile. LVL_1 decides the output level of the pulser as per Table 14. The output level which is determined by the LVL_1 parameter is held for (N+2) number of CLK_An clock cycles, where N represents value stored in the PER_1 parameter. N is programmable in the range of 0 to 30.
  2. In the next step, the pattern generator reads the LVL_2 and PER_2 signals and generate the next set of pattern generator output.
  3. In a similar manner, the pattern generator keeps reading the subsequent sets of LVL_x and PER_x signals and keeps generating the corresponding output until after it has read and responded to the last signal i.e. LVL_32 and PER_32 or it reads any intermediate LVL_x equal to "111". In any of the cases, the Pattern generator repeats step 1 to step 3 for M number of times and then goes to the tail state. Here M represents value programmed in register REPEAT_COUNT.
  4. Tail state: In the tail state, the output of pattern generator block remains fixed as EN_H_An/Bn = 0, and EN_G_An/Bn = 1. This signal combination connects the pulser output to ground. The Pattern generator block remain in tail state for (P+1) number of CLK_An clock periods. Here P represents decimal value of signal TAIL_COUNT and can be programmed in range of 1 to 31. If the TAIL_COUNT is set to 0, there is no tail pattern.
  5. After finishing up the tail pattern, the pattern generator disables all the output signals and the pulser output goes to “high impedance" state. The Pattern generator remain in this state till next TR_BF_SYNC pulse is applied. Refer toFigure 53

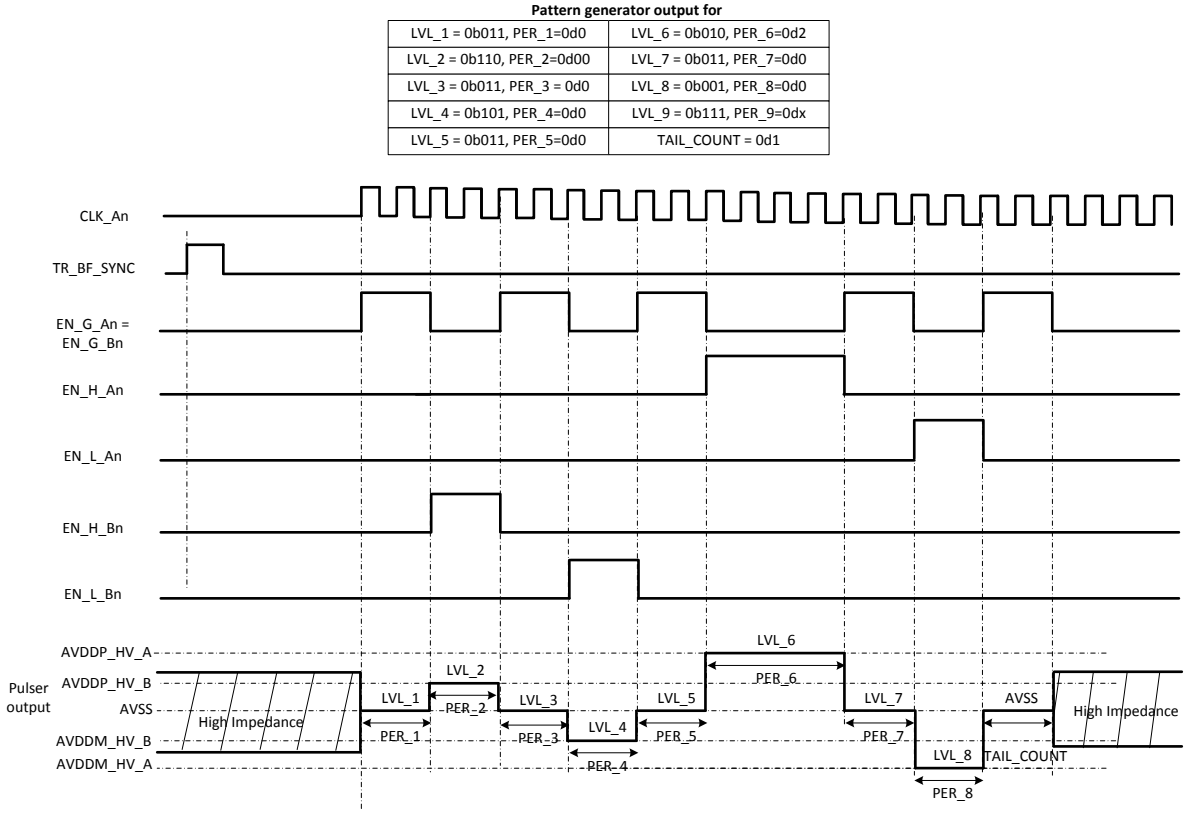


Figure 53. Pattern Generator Output for 5-Level Mode

Table 14. Pulser Control Signal Logic

PATTERN GENERATOR INPUT		PATTERN GENERATOR OUTPUT(1)					DEVICE OUTPUT	
EN_TR_An/Bn	LVL_x (1)	EN_H_An	EN_L_An	EN_G_An = EN_G_Bn	EN_H_Bn	EN_L_Bn	Pulser output	T/R switch output
0	0bx00	0	0	0	0	0	High impedance	Ground
0	0b001	0	1	0	0	0	AVDDM_HV_A	Ground
0	0b010	1	0	0	0	0	AVDDP_HV_A	Ground
0	0b011	0	0	1	0	0	Ground	Ground
0	0b101	0	0	0	0	1	AVDDM_HV_B	Ground
0	0b110	0	0	0	1	0	AVDDP_HV_B	Ground
0	0b111	0	0	0	0	0	Represents end of pattern	Represents end of pattern
1	0bxxx	0	0	0	0	0	High impedance	Connect to pulser output

(1) x -> 1 to 32

8.3.4.3.2 Continuous Wave Mode (CW)

In on-chip beamforming, CW mode the device generates a fix output waveform independent of the value programmed in the pattern profile. To enable the CW mode set CW_EN pin to '1'. For 3-level mode both A- and B-group pulser generates the CW waveform. For 5-level mode only B-side generates the CW waveform and A-side pulser remains in high impedance state.

By default the TR switch of all the channels turns ON when CW mode is enabled; that is, all the channels are configured in the receive mode. To configure the channel in transmit mode disable the TR switch of the corresponding channels by enabling the TR_SW_DIS_A/Bn (n is channel number) bit.

In CW mode, based on register CW_WAVE_MODE value, the device can generate total three types of waveform as show in Figure 54. The value of different parameters shown in Figure 54 is listed in Table 15.

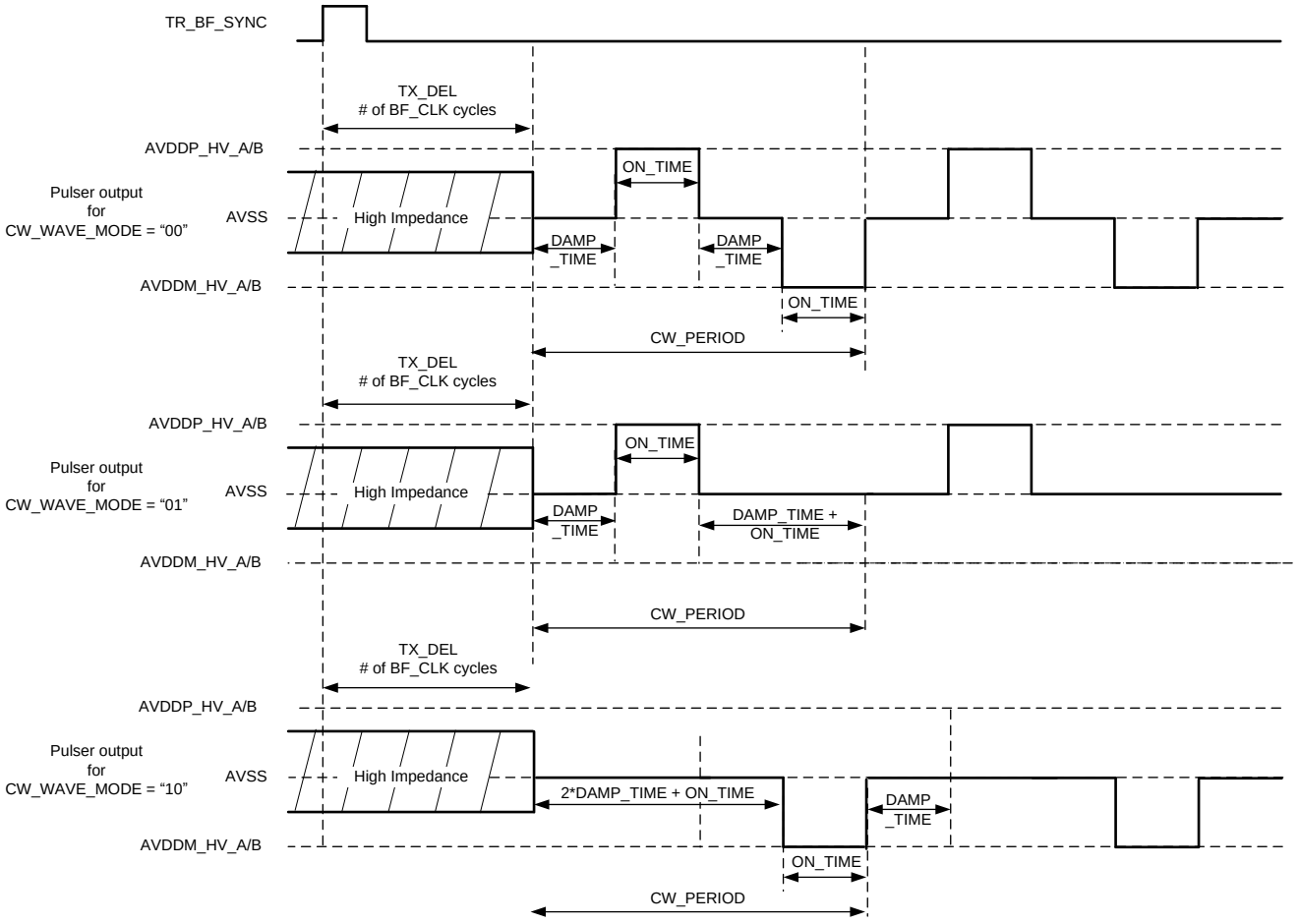


Figure 54. CW mode in On-chip beam forming

Table 15. CW Waveform Parameters

PARAMETER	VALUE IN NUMBER OF BF_CLK CLOCK CYCLES
TX_DEL	8 × TX_START_DEL + 313 for 3-level mode, 8 × TX_START_DEL + 297 for 5-level mode
ON_TIME	(8 - CW_DAMP_CNT) × $2^{(CLK\_DIV)}$ (1)
DAMP_TIME	CW_DAMP_CNT × $2^{(CLK\_DIV)}$
CW_PERIOD	16 × $2^{(CLK\_DIV)}$

(1) In CW mode CLK_DIV can be programmed from 0 to 3.

8.3.4.3.2.1 Beamforming in CW Mode

In CW mode the output waveform on different channels can be beamformed with minimum delay of DEL_An/Bn × $2^{(CLK\_DIV)}$ times BF_CLK cycles. DEL_An/Bn can be programmed from 0 to 15 only.

8.3.4.3.3 Elastography Mode

The device supports a special mode knows as elastography mode (applicable for both 3-level and 5-level mode) to enable elastography imaging in the ultrasound system. Elastography imaging in ultrasound system requires transmission of high voltage pulses for very long duration. To enable the elastography mode in on-chip beam forming mode set EN_ELASTIC_MODE to '1'. In default power mode the floating LDOs in the device also needs to be programmed in high power mode by setting register bit LDO_MODE_G1 and LDO_MODE_G2 to "1111". This mode generates the pulse wavefrom same way as described in B-Mode with only one difference. Instead of pattern going to tail state after step 3, patterns keep repeating step 1 to step 3 till (Q*16) BF_CLK clock periods after TR_BF_SYNC pulse is applied. Where Q (With minimum value = 0 and maximum value = 65535) represents a decimal value of the register ELASTIC_REPEAT. For example if BF_CLK speed is 100 MHz then high voltage pulses can be transmitted for maximum duration of 65535*16/100M = 10.48 ms using elastography mode..

In the elastography mode when the user transmit high voltage pulses (±100V) for long duration (>1ms) and high PRF of > 10 kHz it is possible that the device enters thermal shutdown state because of high power consumption.

8.3.4.4 Pulser

Functionality of the pulser block is independent of beam forming and output level mode. Refer to Pulser.

8.3.5 Digital Block

Following sections describe different operations performed by digital block.

8.3.5.1 Profile Selection

For on-chip beam-forming mode, the device supports multiple profiles to configure the delay of transmit beam-former block and the pattern of pattern generator block. In the following sections detail of profile selection is given.

NOTE

1. The content of both delay and pattern profile register maps are un-defined on power up and applying a reset. A user should configure it as per the requirement. Also applying reset to the device doesn't modify the content of delay and pattern profile.
2. After programming delay and pattern profile it is must to set a register bit LOAD_PROF to '1'. Register bit LOAD_PROF is a self-clearing bit.

8.3.5.1.1 Delay Profile

For both 3-level and 5-level mode of operations, a total of 16 delay profiles (Profile 1 to profile 16) can be programmed and stored within the device. Each delay profile contains delay information for each channel. A user can switch between delay profiles by choosing the new profile through the register control bits BF_PROF_SEL_G1 and BF_PROF_SEL_G2. Register bit BF_PROF_SEL_G1 controls profile for channel group 1 and BF_PROF_SEL_G2 controls profile for channel group 2. Programming a value of N (N can be any value from 0 to 15) in BF_PROF_SEL_G1/G2 register, enables the (N+1) delay profile; see Figure 55. Changing BF_PROF_SEL_G1/G2 doesn't change the profile instantaneously. The change in the profile is reflected in next profile read window as explained in Read and Write of Delay and Pattern Profile section.

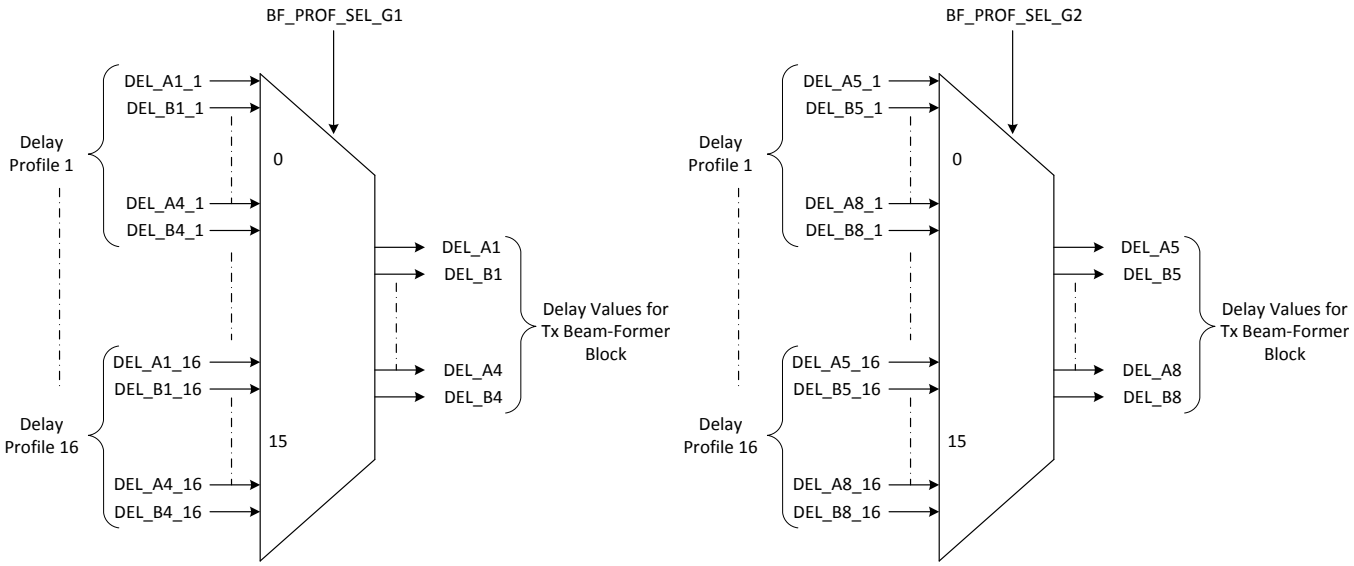


Figure 55. Delay Profile Mapping

8.3.5.1.2 Pattern Profile

Number of pattern profiles supported by the device depends upon level mode i.e. 3-level or 5-level mode. Each pattern profile contains pattern information used by a pattern generator block in the on-chip beamforming mode.

1. In 3-level mode, device supports total 48 pattern profiles with each profile consist of 16 transition (LVL_1, PER_1 to LVL_16, PER_16) information.
2. in 5-level mode, device supports total 28 pattern profiles with each profile consist of 32 transition (LVL_1, PER_1 to LVL_32, PER_32) information.

There is full flexibility to map any channel of the device to any profile using PAT_SEL_XY (X -> A/B for 3-level, X -> Only A for 5-level. Y -> 1 to 8 for both 3- and 5-level) register bits. Writing value of N (N can be any value from 0 to 47 for 3-level and 0 to 27 for 5-level) in PAT_SEL_XY register enables the (N+1) pattern profile see Figure 56. Changing PAT_SEL_XY doesn't change the profile instantaneously. The change in the profile is reflected in the next profile read window as explained in Read and Write of Delay and Pattern Profile section.

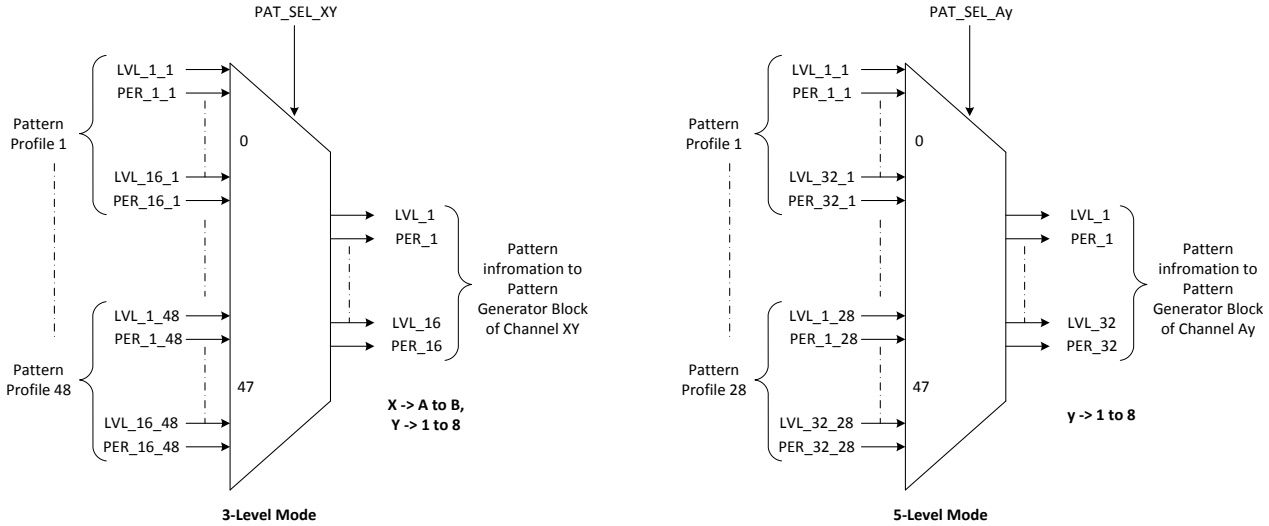


Figure 56. Pattern Profile Mapping

8.3.5.1.3 Read and Write of Delay and Pattern Profile

The read and the write window timing of profile is as shown in Figure 57. 'Write' refers to the SPI write to either modifying the delay or pattern profiles or changing the selection of the profile to be used for the next transmission window. 'Read' refers to the loading of the selected profile from the memory into the TxBF and pattern generator blocks. Parameters READ_DEL and READ_PROF are listed in Table 16. It is important to consider the following points related to write and read operation of profile.

- Write operation of profile is not allowed when device is in the middle of reading the profile content in the read window. Write operation must be carried out only in the write window indicated.
- Once profile content, BF_PROF_SEL, and PAT_SEL_X_Y is programmed, the effect of it is reflected only in the next read window. For example, in Figure 57 if BF_PROF_SEL is changed in write window 1 then the new delay profile is loaded only in read window 1 and used for the subsequent transmit cycle.

NOTE

TI recommends avoiding profile write operation while transmitting high voltage pulses.

After programming delay and pattern profile set register bit LOAD_PROF to '1'. Register bit LOAD_PROF is a self-clearing bit.

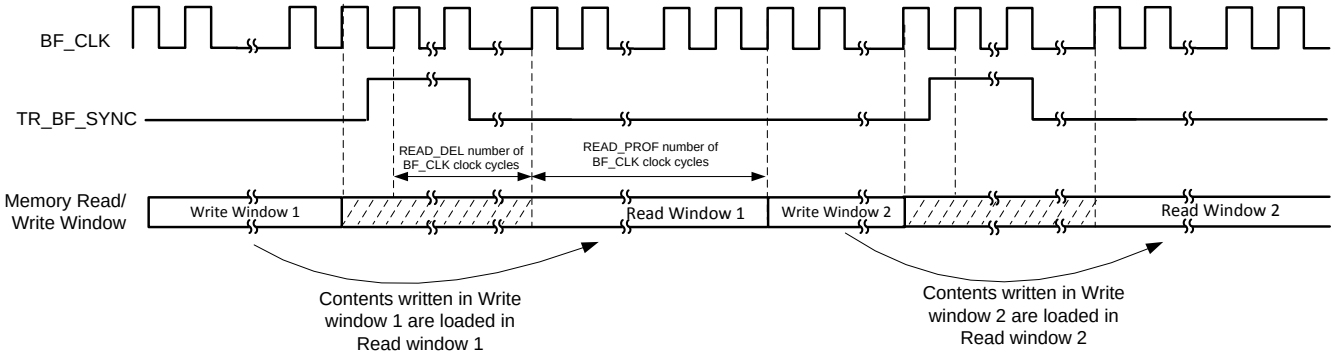


Figure 57. Read and Write Timing Window of Delay and Pattern Profile

Table 16. Read and Write Parameters Across Level Modes

Parameter	3-Level Mode	5-Level Mode
READ_DEL	(TX_START_DEL) * 8 + 5	(TX_START_DEL) * 8 + 5
READ_PROF	308	292

8.3.5.2 T/R Switch Control Signal

The turning ON and OFF of T/R switch is associated with the receive and transmit phases respectively. The T/R switch control signal is generated by digital block as described in the following sections. The Digital block generates 16 T/R switch control signals by using combination of device pin and register bits as shown in Figure 58. Table 17 list down the logic for channel A1 and similar logic applies to all the other channels. All the group B T/R switch get permanently disabled in 5-level mode.

8.3.5.2.1 T/R Switch Control Signal for Off-chip Beam-forming Mode

In the off-chip beamforming mode (TX_BF_MODE=0), the TR_EN* controls for the switches get generated directly from the TR_EN* pins. Each pin controls the T/R switches of 4 channels as shown in Figure 58. Additional register control (TR_SW_DIS*) can be used to disable the T/R switch control from the pins. Table 17 list down the control logic for channel A1. Similar logic applies to rest of the channels.

Table 17. T/R Switch Control Logic in Off-chip Beamforming Mode

REGISTER BIT TR_SW_DIS_A1 in 3-Level/5-Level	Pin TR_EN1	TR_EN_A1	T/R SWITCH OF CHANNEL A1
"00"/"0000"	0	0	OFF
"00"/"0000"	1	1	ON
"11"/"1111"	X	0	OFF

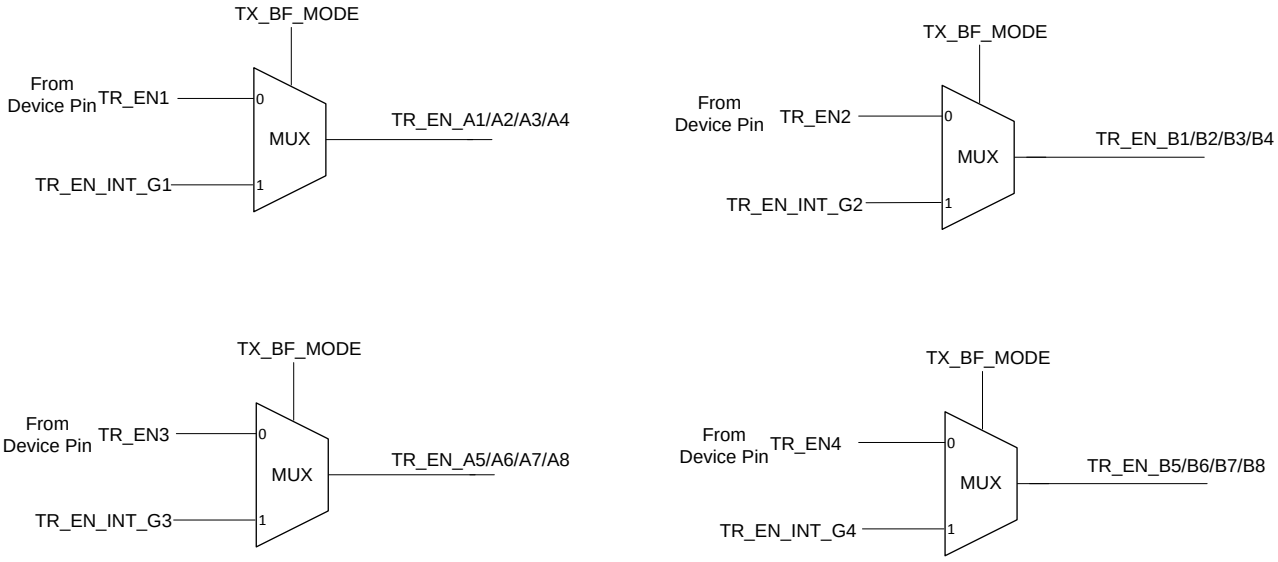


Figure 58. T/R Switch Control Logic

8.3.5.2.2 T/R Switch Control in On-Chip Beam-Forming Mode

In on-chip beamforming mode, control signals TR_EN_INT_G1 controls the T/R switches for channels A1 to A4, TR_EN_INT_G2 controls the T/R switches for channels B1 to B4, TR_EN_INT_G3 controls the T/R switches for channels A5 to A8, and TR_EN_INT_G4 controls the T/R switches for channels B5 to B8. These control signals are generated by the device per the following logic:

- T/R switch turn OFF operation: TR switch of all the channels starts to turn OFF as soon as TR_BF_SYNC pulse is applied. The device provides a flexibility to change the turn OFF start instant of TR switch across four group of channels. TR switch starts to turn OFF whenever signals TR_EN_INT_G1/G2/G3/G4 go low. These signals go to low after (8 × N + 5) number of BF_CLK clock cycles from the BF_CLK edge on which TR_BF_SYNC pulse is latched. Here N represents a decimal value programmed in register TR_SW_OFF_DEL_G1/G2/G3/G4; see Figure 59.
- To time the T/R switch turn ON controls with respect to the TR_BF_SYNC pulse (with device pin CW_EN = 0 and register bit TR_SW_DEL_MODE set to '0'): Signals TR_EN_INT_G1/G2/G3/G4 go high after 4 × N1 + 8 × N2 +309 (for 3-level mode) or 4 x N1 + 8 x N2 + 293 (for 5-level mode) number of BF_CLK clock cycles from TR_BF_SYNC signal. Here N1 and N2 represent a decimal value programmed in register TR_SW_DEL_G1/G2/G3/G4 and TX_START_DEL respectively.

NOTE

Value of register TR_SW_DEL_G1/G2 has to be greater than 73 for 3-level mode and 69 for 5-level mode. It is expected that user will turn On T/R switch when all the pulser of the device finishes transmission. Turning On T/R switch before that leads to abnormal response from the device.

- To time the T/R switch controls with respect to the end of the pulsed transmission: (with device pin CW_EN = 0 and register bit TR_SW_DEL_MODE set to '1'): signals TR_EN_INT_G1/G2/G3/G4 go high after (4 × N + 5 + 2^K) number of BF_CLK clock cycles from the instant when pulsers of corresponding channels complete the tail state. Here N represents a decimal value programmed in register TR_SW_DEL_G1/G2/G3/G4. The value

of K depends on CLK_DIV register value; see Table 18.

Table 18. K Value Across CLK_DIV Setting

CLK_DIV	K
0	1
1	1
2	2
3	3
4	4
5	5

- When device is in programmed in CW mode: Signals TR_EN_INT_G1/G2/G3/G4 are set to '1' always and enables the T/R switch of all the channels. To disable the T/R switch of any channel use the register bits TR_SW_DIS_xx.

NOTE

Whenever T/R switch of any channel is in On state, pulser of corresponding channel goes to high impedance state automatically.

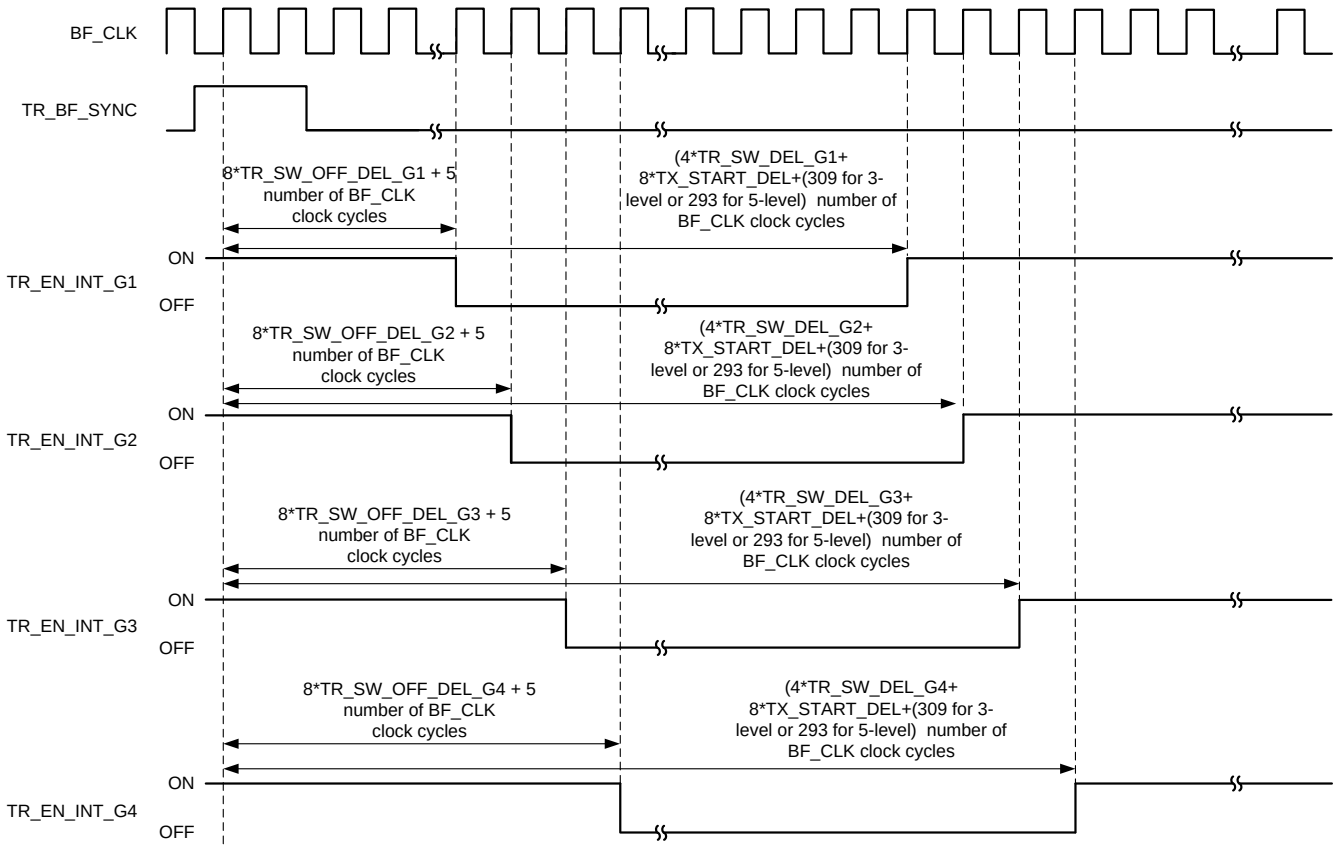


Figure 59. T/R Switch Control Signal for TR_SW_DEL_MODE = 0

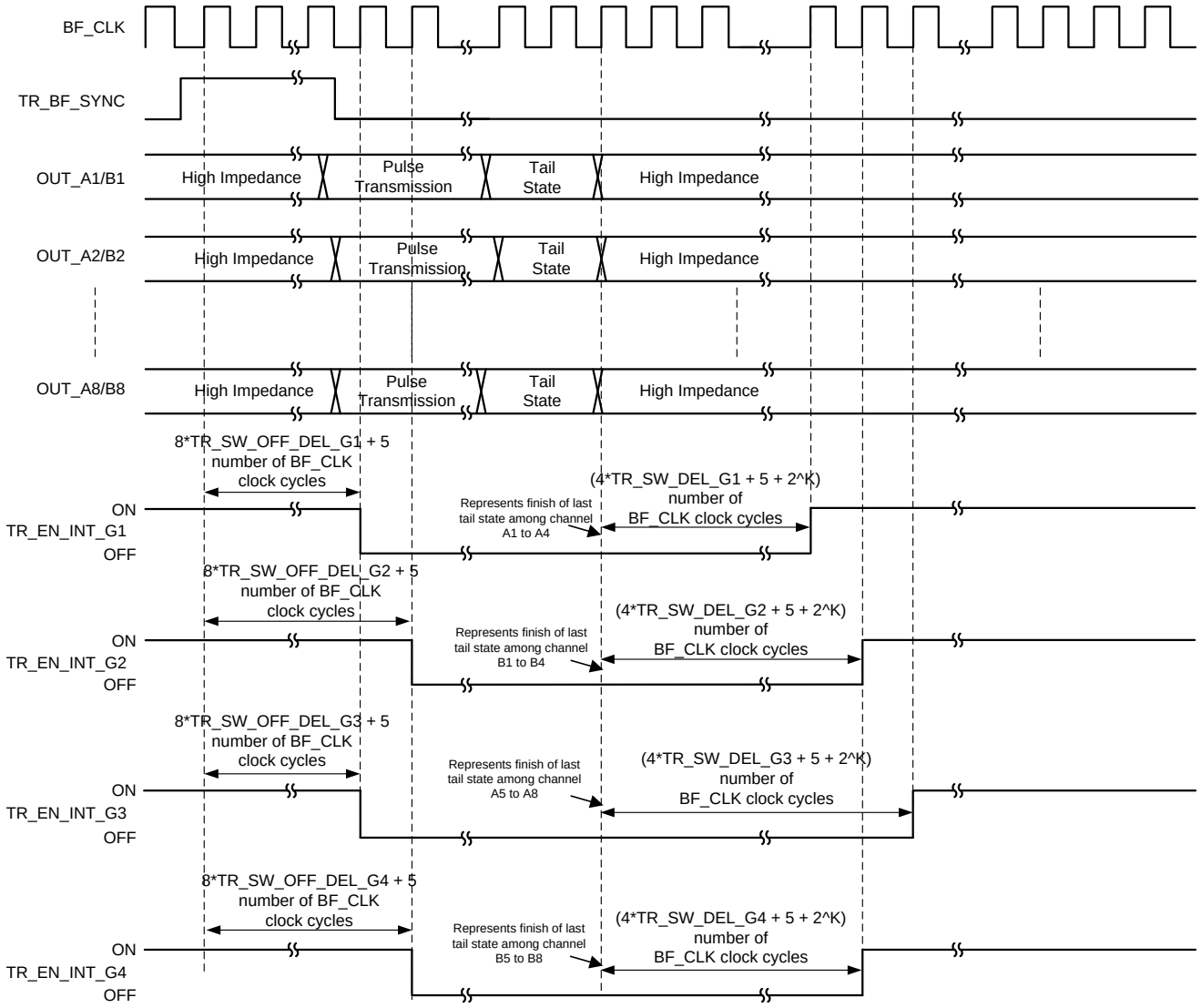


Figure 60. T/R Switch Control Signal for TR_SW_DEL_MODE = 1

8.3.5.2.2.1 Disabling T/R Switch

In both off-chip and on-chip beam forming modes, any of the 16 T/R switches can be disabled individually using the corresponding register bits TR_SW_DIS_An and TR_SW_DIS_Bn (n is from 1 to 8). Enabling any of this bit switches off the both the series and the shunt transistor of the T/R switch; see Figure 46.

NOTE

In 5-level mode, it is recommended to disable the TR switch of B group pulser by writing TR_SW_DIS_Bn to "11". This will reduce the parasitic capacitance on OUT_A/Bn.

To get TR switch on impedance of 6 ohms, RX_An and RX_Bn have to be shorted and TR_SW_DIS_A/Bn have to be "00". But this will increase the parasitic capacitance on OUT_A/Bn to 160 pF

8.3.6 Full Timing Diagram For On-chip Beamforming Mode

For quick reference different operations performed in the on-chip beamforming mode are summarized in Figure 61. Values of the different parameters shown in Figure 61 is listed in Table 19.

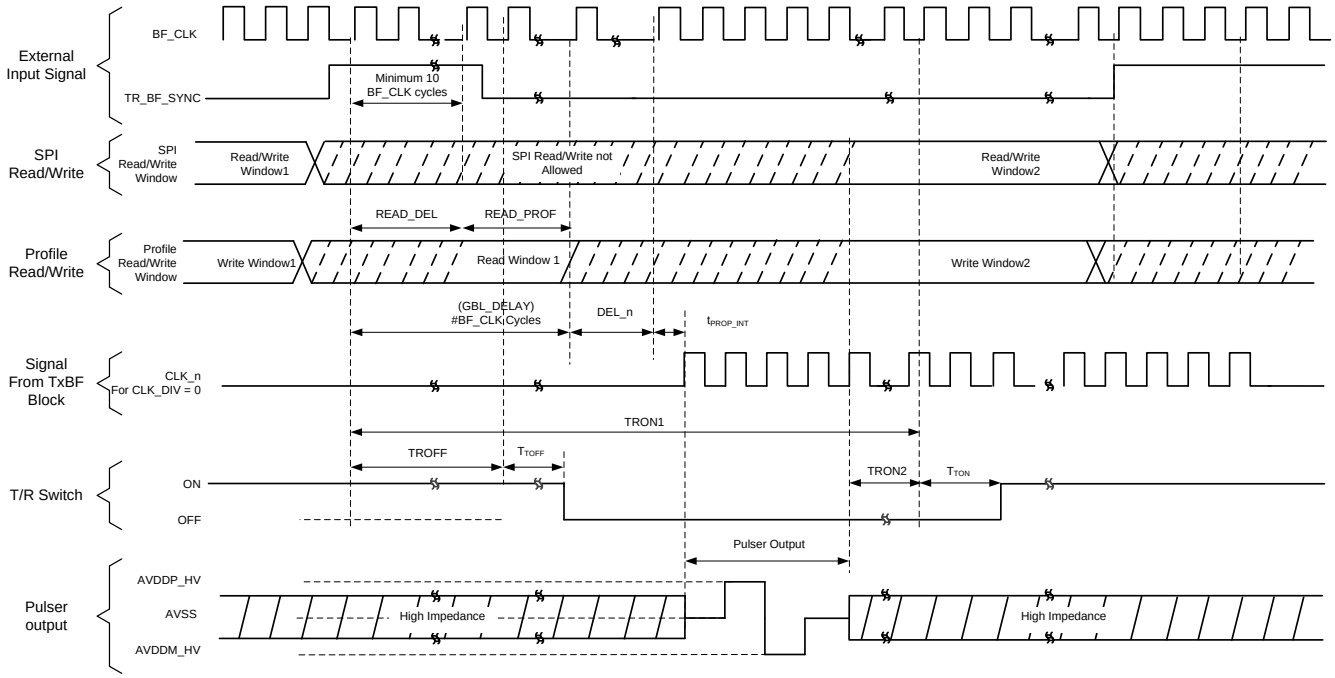


Figure 61. On-chip Beamforming Operation

Table 19. Parameters for On-chip Beamforming Mode

PARAMETER	INTERPRETATION	# of BF_CLK CLOCK CYCLES
READ_DEL	Represents a time from TR_BF_SYNC latch edge to start of delay and pattern profile loading	8 × TX_START_DEL + 5
READ_PROF	Represent time duration for which delay and pattern profiles are being loaded	308 for 3-level and 292 for 5-level mode
GBL_DELAY	Represent the global delay for all the channels from TR_BF_SYNC latch edge to start of pattern in pulser output	8*TX_START_DEL + 313 for 3-level and 8*TX_START_DEL + 297 for 5-level mode
DEL_n	Represents channel based delay. Used for transmit beamforming across channels	DEL_A1 for channel A1, DEL_B1 for channel B1, till DEL_A8 for channel A8 and DEL_B8 for channel B8
t_{PROP_INT}	Propagation delay from BF_CLK edge to the pulser output	Refer to *Characteristics*
TRON1	Represents start of T/R switch turn ON instant with respect to TR_BF_SYNC latch edge	Valid only with TR_SW_DEL_MODE = 0; TRON1 = 4 × TR_SW_DEL_G1 + 8 × TX_START_DEL + (309 in 3-level or 293 in 5-level) for channel A1 to A4 TRON1 = 4 × TR_SW_DEL_G2 + 8 × TX_START_DEL + (309 in 3-level or 293 in 5-level) for channel B1 to B4 TRON1 = 4 × TR_SW_DEL_G3 + 8 × TX_START_DEL + (309 in 3-level or 293 in 5-level) for channel A5 to A8 TRON1 = 4 × TR_SW_DEL_G4 + 8 × TX_START_DEL + (309 in 3-level or 293 in 5-level) for channel B5 to B8
TRON2	Represent start of T/R switch turn ON instant with respect to end of pulser output pattern	Valid only with TR_SW_DEL_MODE = 1; TRON2 = 4 × TR_SW_DEL_G1 + 5 + 2^K for channel A1 to A4 TRON2 = 4 × TR_SW_DEL_G2 + 5 + 2^K for channel B1 to B4 TRON2 = 4 × TR_SW_DEL_G3 + 5 + 2^K for channel A5 to A8 TRON2 = 4 × TR_SW_DEL_G4 + 5 + 2^K for channel B5 to B8 Value of K listed in Table 18
t_{TON}	Represent turn ON time duration of T/R switch	Refer to *Electrical Characteristics*

Table 19. Parameters for On-chip Beamforming Mode (continued)

PARAMETER	INTERPRETATION	# of BF_CLK CLOCK CYCLES
TROFF	Represents start of T/R switch turn OFF instant with respect to TR_BF_SYNC latch edge	TROFF = 8 × TR_SW_OFF_DEL_G1 + 5 for channel A1 to A4 TROFF = 8 × TR_SW_OFF_DEL_G2 + 5 for channel B1 to B4 TROFF = 8 × TR_SW_OFF_DEL_G3 + 5 for channel A5 to A8 TROFF = 8 × TR_SW_OFF_DEL_G4 + 5 for channel B5 to B8
t_{TOFF}	Represent turn OFF time duration of T/R switch	Refer to *Electrical Characteristics*
pulser output	Pulser output duration	Defined by values programmed pattern profile

8.4 Device Functional Modes

8.4.1 4.8-A Mode

The pulser of the device can be configured to give out 4.8-A current when device is used in 5-level mode. To get the 4.8-A output keep the voltage level of AVDDP/M_HV_A and AVDDP/M_HV_B supplies same. Set the register bits 4A_MODE_CNTRL_1 and 4A_MODE_CNTRL _2 to '1'. Writing these registers configures the device in 3-level mode even though pin LVL_3Z_5 is connected to logic level ‘1’. So configure the rest of the setting of device assuming it is in 3-level mode. So group A and group B pulser will get enabled together and gives out a maximum drive strength of 4.8 A at 100-V supply.

8.4.2 Pulser Power Down

In on-chip beam forming mode device support a feature to power down the individual pulser using a register bit. To power down any pulser in 3-level mode use register bit PDN_PUL_xy (x-> A or B, y-> 1 to 8) and in 5-level mode use register bit PDN_PUL_An (n -> 1 to 8). These bits are part of channel power down register map. On enabling pulser power down bit, the pulser output goes to high impedance state while T/R switch of corresponding channel remains active.

8.4.3 Invert Pattern

In on-chip beam forming mode, output signal level of pulser shall be inverted by just enabling a bit INV_PATTERN. Table 20 list down pulser output level with and without invert pattern mode. This bit ease the use of the device in harmonic imaging where inverted pulse is required.

Table 20. Invert Pattern

PULSER OUTPUT WITH INV_PATTERN = 0	PULSER OUTPUT WITH INV_PATTERN = 1
AVDDP_HV_A /B	AVDDM_HV_A /B
AVDDM_HV_A/B	AVDDP_HV_A/B
AVSS	AVSS
High Impedance	High Impedance

8.4.4 Pulser Current Programming

The peak switching current of the pulser output stage current driving capability can be programmed either using device pins DSEL_1 and DSEL_0 or by using register bits DSEL as per listed in Table 21

Table 21. Pulser's Output Stage Current Programming

DRV_MUX_SEL Register bit	DSEL_1, DSEL_0 Device Pin	DRV_SEL Register bit	Output Stage Current (A)
0	00	xx	2.4
0	01	xx	1.8
0	10	xx	1.2
0	11	xx	0.6

Table 21. Pulser's Output Stage Current Programming (continued)

DRV_MUX_SEL Register bit	DSEL_1, DSEL_0 Device Pin	DRV_SEL Register bit	Output Stage Current (A)
1	xx	00	2.4
1	xx	01	1.8
1	xx	10	1.2
1	xx	11	0.6

8.4.5 Thermal Shutdown

There are two temperature shutdown blocks in the device. One shutdown block protects the die-1 channels from temperature overstress, and one shutdown block protects the channels in die 2. Whenever internal temperature of any channel group exceeds the shutdown temperature (T_{SHUT}), the device automatically shuts down the corresponding channel group, and the voltage at SHUTZ pin goes to 0. The device comes out of temperature shutdown when reset is applied to the device and device temperature goes down below (T_{SHUT} – 10°C) temperature. Refer to *Electrical Characteristics* for T_{SHUT} parameter value.

Always connect an external 2-kΩ resistor (with a tolerance of 10%) to AVDD_IO supply on the SHUTZ pin of the device. If there are multiple device on the system board, the SHUTZ pin can be short of all the devices; see Figure 62

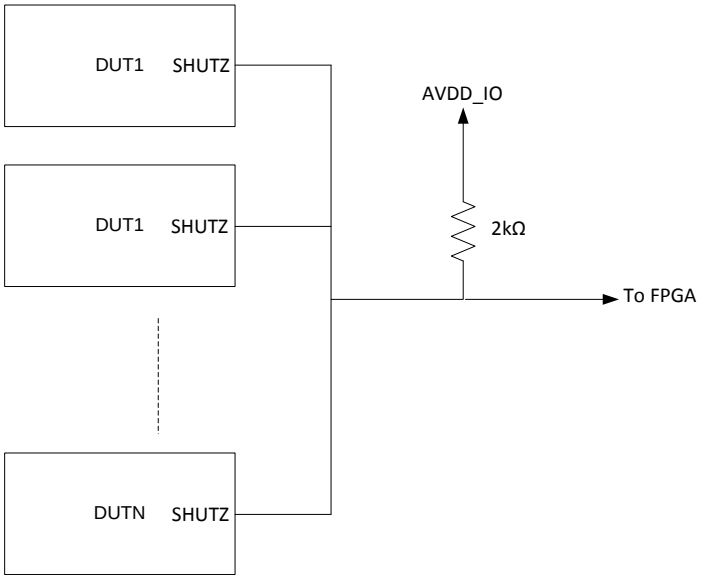


Figure 62. Thermal Shutdown Scheme for Multiple Devices on System Board

8.4.6 Powering Up the Device from Global Power Down Mode

Powering up the device from global power down state in default power mode is straight forward. Just disable the global power down mode and it takes t_{WUP_GBL} time to wake up the device. However in dynamic power mode, it requires extra steps to power up the device. In global power down mode the floating LDOs are powered down. When floating LDOs are in powered down state for long time (> 5 ms) the external capacitor connected at LDO output discharges. To charge the external cap in dynamic power mode, floating LDOs requires minimum of t_{GBL_DYN} time. So in dynamic power mode the LDO has to be enabled for t_{GBL_DYN} before firing the high voltage pulses. There are two approaches to power up the LDO for t_{GBL_DYN} time. One approach is keep the TR_ENx signal width to t_{GBL_DYN} after powering up the device and then apply TR_BF_SYNC signal. Second approach is keep TR_BF_SYNC signal low and apply the TR_ENx signal in burst such that the total accumulate high time of TR_ENx signal is equal to t_{GBL_DYN}. After that use the device in normal way as used in dynamic power mode.

8.4.7 Controlling Device Using Register Bits

To reduce the number of control lines coming from FPGA, different pins functionality of the device can be programmed using register bits. Table 22 lists the pins and alternate way to control the pin functionality using register bit. When pin is controlled through register bit then the status of pin is ignored by the device. TI recommends to not keep pins floating if controlled through register bit.

Table 22. Control Signals

PIN	TO ENABLE THE FUNCTIONALITY, SET THE REGISTERS BIT	TO DISABLE THE FUNCTIONALITY, SET THE REGISTERS BIT
CW_EN	CW_EN_MUX_SEL = 1 CW_EN_1 = 1 (To enable CW mode of die 1) CW_EN_2 = 1 (To enable CW mode of die 2)	CW_EN_MUX_SEL = 1 CW_EN_1 = 0 (To disable CW mode of die 1) CW_EN_2 = 0 (To disable CW mode of die 2)
DSEL_0/1	DRV_MUX_SEL = 1 Set the logic of DRV_SEL pin as required	
RESYNC	EN_RESYNC_MUX_SEL = 1 EN-RESYNC = 1	EN_RESYNC_MUX_SEL = 1 EN-RESYNC = 0
STDBY	STNDBY_G1 = 1 STNDBY_G2 = 1	STNDBY_G1 = 0 STNDBY_G2 = 0 and connect pin STDBY to ‘0’

8.5 Programming

8.5.1 Serial Programming Interface

The serial programming interface (SPI) block provides a high-speed read/write interface to program the device. This interface consists of 5 input pins named as SCLK, SDATA_GRP1, SDATA_GRP2, SEN_GRP1 and SEN_GRP2. The read out of the internal register is done through the output data pin SDOUT. The description of SPI write and read procedure is provided in *SPI Write Operation* and *Register Readout*.

Each of two dies (Die 1 and Die 2) has its own register map. Registers referencing Channels 1-4 (A1, B1,A2, B2, A3, B3, A4, B4) are associated with Die 1. Similarly, registers referencing Channels 5-8 (A5, B5, A6, B6, A7, B7, A8, B8) are associated with Die 2. While some registers are duplicated in both dies with the same address, some others (for example, the channel-specific registers) are present only in one or the other die. The description of the write and read operations in the following sections elaborate the suggested way to access the register maps in the two dies without having to keep track of which die is being written into or read from. The only exception to this is while writing to the delay profiles in the 6-wire mode – here, the availability of two sets of SPI interfaces is taken advantage of in enabling a faster update of the delay profiles of all the channels.

8.5.1.1 SPI Write Operation

Several different modes in the device can be programmed with the serial peripheral interface (SPI). This interface is formed by the SEN_GRP1, SEN_GRP2 (serial interface enable), SCLK (serial interface clock), SDATA_GRP1, and SDATA_GRP2 (serial interface data) pins. Serially incoming bits on pin SDATA_GRP1 are latched by the device on every SCLK rising edge when SEN_GRP1 is low. Similarly serially incoming bits on pin SDATA_GRP2 are latched by the device on every SCLK rising edge when SEN_GRP2 is low. SDATA_GRP1/SDATA_GRP2 serial data are loaded into the register for total 42 SCLK rising edge when SEN_GRP1/SEN_GRP2 is low. If the word length exceeds a multiple of 42 bits, the excess bits are ignored. Data can be loaded in multiples of 42-bit words within a single active SEN_GRP1/SEN_GRP2 pulse (an internal counter counts the number of 42 clock groups after the SEN_GRP1/SEN_GRP2 falling edge). Data are divided into two main portions: the register address (10 bits) and data (32 bits). Figure 63 shows the timing diagram for serial interface write operation.

NOTE

It is recommended to avoid SPI read and write operation while transmitting high voltage pulses.

Programming (continued)

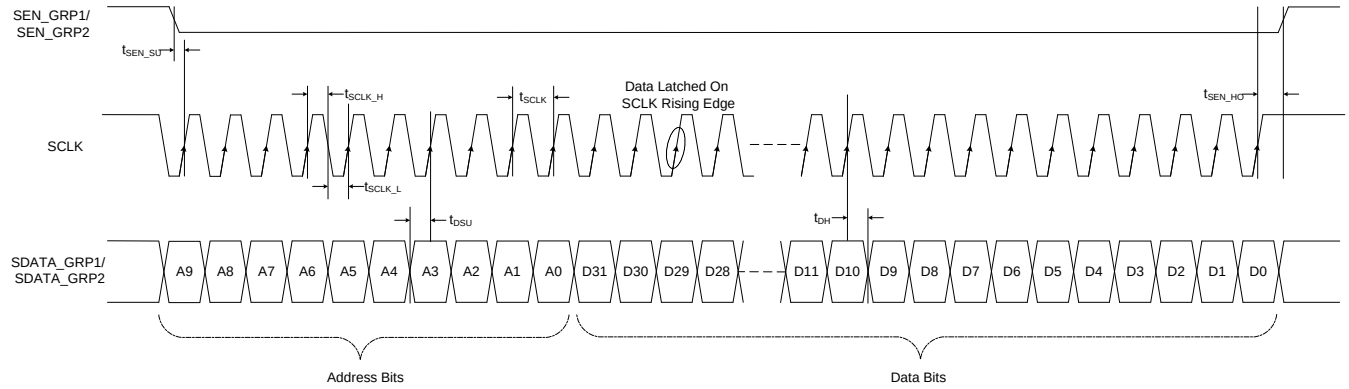


Figure 63. Serial Interface Timing

SPI write operation can be carried out using two possible ways as described below:

1. 4-Wire write mode: This mode writes to and reads from the device by communicating simultaneously between the two dies (Die 1 and Die 2). In this mode SDATA_GRP1, SDATA_GRP2 pins are shorted and similarly SEN_GRP1, SEN_GRP2 pins are shorted together. So from the FPGA side it requires only 4 signals (SEN, SCLK, SDATA and SDOUT) to perform SPI write and read operation; see Figure 64. All the register of the device can be programmed using these three FPGA lines.

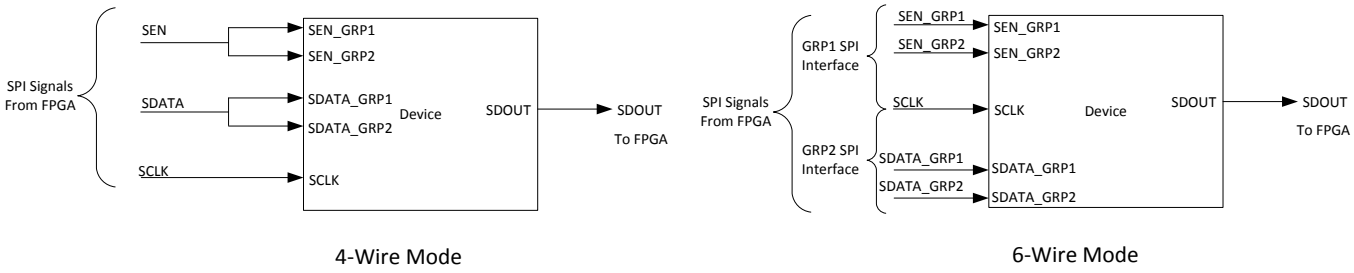


Figure 64. 4-Wire and 6-Wire Write Mode

2. 6-Wire write mode: This mode of operation requires total 6 signals (SEN_GRP1, SEN_GRP2, SDATA_GRP1, SDATA_GRP2, SCLK and SDOUT) to perform SPI write and read operations; see Figure 64. These six signals provide two SPI interfaces. Signals SEN_GRP1, SDATA_GRP1, SCLK and SDOUT forms the first SPI interface referred as GRP1 interface (communicating with Die 1) and signals SEN_GRP2, SDATA_GRP2, SCLK and SDOUT forms the second SPI interface referred as GRP2 interface (communicating with Die 2). The motivation for using a 6-wire write mode is that it allows altering the delay profile of the channels on-the-fly in a quicker manner. Having two SPI interfaces allows a user to configure the delay register maps of Die 1 and Die 2 in parallel with lesser programming time. Table 23 lists the registers which are configured using the two interfaces. Timing diagramFigure 63 is applicable for both the GRP1 and GRP2 interface.

Table 23. Register Programming for 5-Wire Mode

Register Map	Interface
Global Register Map, Channel PDN Register Map Pattern Select Register Map, Pattern Register Map	Register programming data has to be done on both the interfaces (GRP1 and GRP2)
Delay Register Map	Configure delay of group 1 channels (A1, B1,A2, B2, A3, B3, A4, B4) using GRP1 interface and group 2 channels (A5, B5, A6, B6, A7, B7, A8, B8) using GRP2 interface

8.5.1.2 Burst Write Mode

To reduce total device programming time, device support an extra write mode referred as burst write mode. To enable burst write mode set register bit BURST_WR_EN to '1'. When burst write mode is enabled it is required to send address of the register only once after SEN_GRP1/2 goes low and after that keep SEN_GRP1/2 continually low and send only data bits. Device automatically increments the address by one after receiving each set of 32 bits and write the next 32 register bit on incremented register address; see Figure 65.

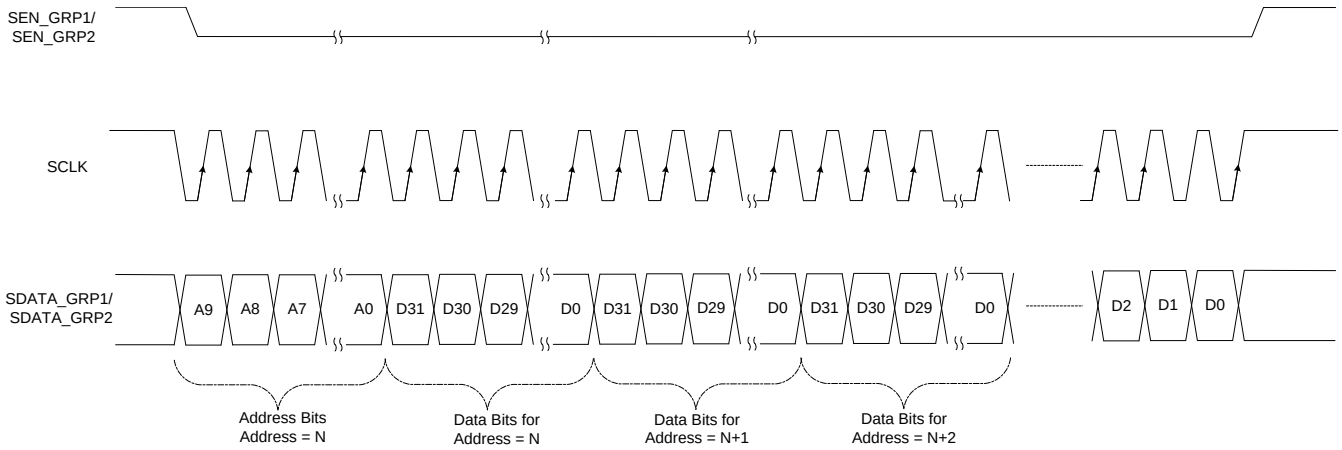


Figure 65. Burst Write Mode

8.5.1.3 Register Readout

The device includes an option where the contents of the internal registers can be read back. This read back feature can be useful as a diagnostic test to verify the serial interface communication between the external controller and the device. The SPI read operation involves reading a register that could be in both dies or in either one of them. As a result, the readout involves readout out twice – once from each die – and logically combining their outputs in the manner described below. SPI read operation shall be carried out using both the 4-Wire and 6-Wire modes as described below:

1. 4-Wire mode: All the registers of the device can be read out in readout mode except of register address 0, using FPGA lines SCLK, SDATA, SEN and SDOUT signals; see Figure 64. Register 0 always remains in write mode and can't be read back. Complete read out operation of any register address involves below steps:
   - Step 1: Set the READ_EN bits to "01" to read out from Die 1. Then, initiate a serial interface cycle specifying the address of the register (A[9:0]) whose content must be read. The data bits on SDATA lines are don’t care and ignored . The device outputs the 32 bits (DOUT1[31:0]) of the selected register on the SDOUT pin.
   - Step 2: Set the READ_EN bits to "10" to read out from Die 2. Then, initiate a serial interface cycle specifying the address of the register (A[9:0]) whose content must be read. The data bits on SDATA lines are don’t care and ignored . The device outputs the 32 bits (DOUT2[31:0]) of the selected register on the SDOUT pin.
   - Step 3: Final data of register address whose content is read in step 1 and 2 is given by OR of the data DOUT1[31:0] and DOUT2[31:0].
2. 6-Wire mode: All the registers of the device can be read out in readout mode except of register address 0, using GRP1 interface (Consist of SCLK, SDATA_GRP1, SEN_GRP1 and SDOUT) and GRP2 interface (Consist of SCLK, SDATA_GRP2, SEN_GRP2 and SDOUT) signals; see Figure 64. Register 0 always remain in write mode and can't be read back. Complete read out operation of any register address involves below steps:
   - Step 1: Set the READ_EN bits to "01". Then, initiate a serial interface cycle using GRP1 SPI interface specifying the address of the register (A[9:0]) whose content must be read. The data bits on SDATA_GRP1 lines are don’t care and ignored . The device outputs the 32 bits (DOUT1[31:0]) of the selected register on the SDOUT pin.
   - Step 2: Set the READ_EN bits to "10". Then, initiate a serial interface cycle using GRP2 SPI interface specifying the address of the register (A[9:0]) whose content must be read. The data bits on

SDATA_GRP2 lines are don't care and ignored . The device outputs the 32 bits (DOUT2[31:0]) of the selected register on the SDOUT pin.

– Step 3: Final data of register address whose content is read in step 1 and 2 is given by OR of the data DOUT1[31:0] and DOUT2[31:0].

The read operation timing diagram is shown in Figure 66(see the Serial Interface Timing Characteristics table). SDOUT has a delay of t_{OUT_DV} from the SCLK falling edge. To enable serial register writes, set the READ_EN bit back to "00". The device SDOUT buffer is 3-stated and is only enabled when the READ_EN bits are enabled. SDOUT pins from multiple devices can be tied together without any pullup resistors.

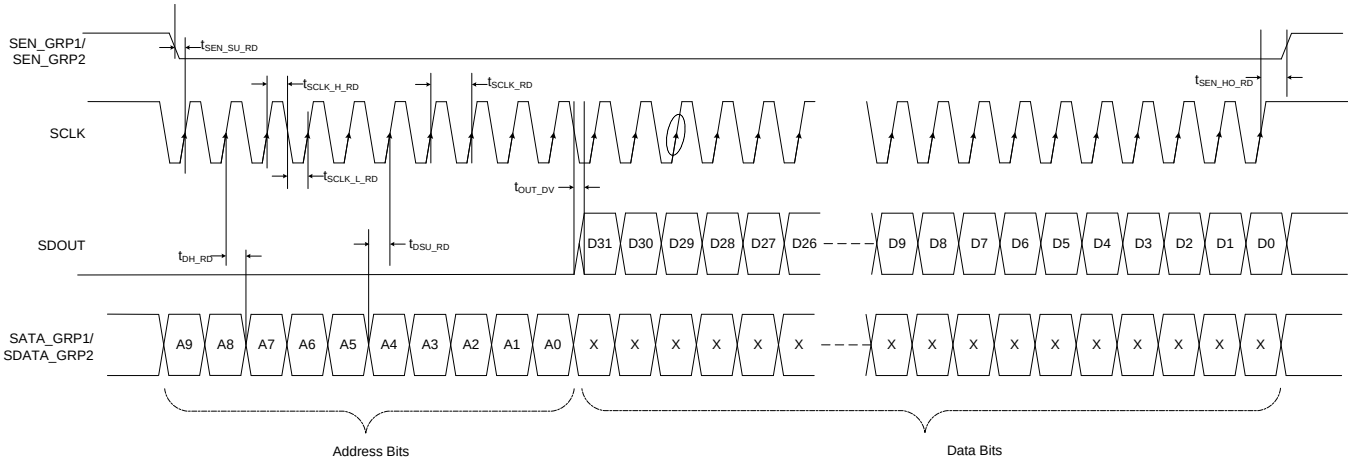


Figure 66. Serial Interface Register, Read Operation

8.5.1.3.1 Register Readout for Multiple Devices

Take special precaution while reading the register in ths system having multiple devices with SDOUT pin short together. It is required to enable the register read of one device at a time. The SDOUT buffer of the device remains enabled till the device is in the read mode gets tri-stated when register read mode is disabled. Thus, if register read of multiple devices is enabled simultaneously, the register read will not work as SDOUT buffer of multiple devices becomes active.

8.5.1.3.2 SPI Programming Window:

The SPI programming is not allowed untill all the channel pulser output goes to high Z state after applying the TR_BF_SYNC pulse; see Figure 67. Not complying to this requirement shall lead to the abnormal behavior from device.

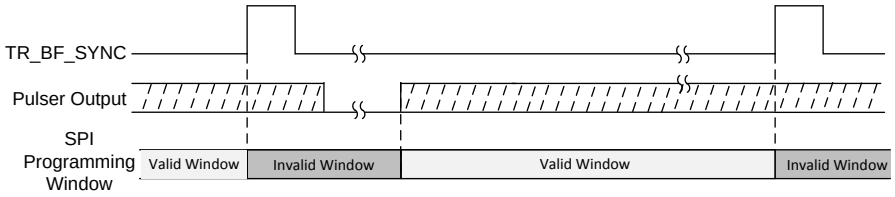


Figure 67. SPI Programming Valid Window

8.6 Register Maps

8.6.1 Register Map Description

Overall register map of the device is divided in multiple register maps as listed in Table 24

Table 24. Register Maps Range

Register Map	Does register map definition changes between 3-Level and 5-Level Mode?	What is the register value after power up and on applying reset?	Does applying reset change the register to default value?	Address Range (Decimal)	
				3-Level Mode	5-Level Mode
Global	No	Defined	Yes	0, 1, 6, 11, 12, 15, 20-25	0, 1, 6, 11, 12, 15, 20-25
Pattern Select	No	Defined	Yes	28-31	28-31
Channel Power Down	No	Defined	Yes	26, 27	26, 27
Delay Profile	Yes	Un-defined	No	32-159	32-95
Pattern Profile	Yes	Un-defined	No	160-351	96-319

8.6.2 Global Register Map

Table 25. Global Register Map

REGISTER ADDRESS		REGISTER DATA											
Hex	**Dec**	**D31:D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15:D12**
00	0	0											
00	0	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00	0	0			BURST_WR_EN	0				LOAD_PROF	READ_EN		RESET
01	1	**D31:D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15:D12**
01	1	0										STNDBY_G1	0
01	1	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
01	1	0										0	STNDBY_G2
06	6	**D31:D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15:D12**
06	6	0	0	0	0	0	0	0	0	0	0	0	0
06	6	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
06	6	0	0	0	0	0	0	0	DIS_DYN_CNTRL_2	0	0	0	0
0B	11	**D31:30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:18**	**D17**	**D16**	**D15:12**
0B	11	0	4A_MODE_CNTRL_1	0	0	0	LDO_MODE_G1				0	0	0	0
0B	11	**D13:D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0B	11	0	0	0	0	0	0	0	0	0	0	0	0
0C	12	**D31:D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15:D14**
0C	12	0	TR_SW_OFF_DEL_G2					0			TR_SW_OFF_DEL_G1			0
0C	12	**D13:D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0C	12	TR_SW_OFF_DEL_G4				0	0	TR_SW_OFF_DEL_G3					
0F	15	**D31:D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15:D12**
0F	15	0	0	0	0	0	0	0	0	0	0	0	0
0F	15	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0F	15	0	0	0	0	0	0	0	DIS_DYN_CNTRL_1	0	0	0	0
14	20	**D31:30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:18**	**D17**	**D16**	**D15:12**
14	20	0	4A_MODE_CNTRL_2	0	0	0	LDO_MODE_G2				0	0	0	0
14	20	**D13:D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Table 25. Global Register Map (continued)

REGISTER ADDRESS		REGISTER DATA											
14	20	0		0	0	0	0	0	0	0	0	0	0
15	21	**D31:D29**		**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15:D12**
15	21	0			TR_SW_DEL_G2									0
15	21	**D11**		**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
15	21	TR_SW_DEL_G4												
16	22	**D31:D29**		**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15:D12**
16	22	BF_PROF_SEL_G1			TR_SW_DEL_G1									BF_PROF_SEL_G2
16	22	**D11**		**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
16	22	TR_SW_DEL_G3												
17	23	**D31**	**D30**	**D29:D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15**
17	23	0	0	0	0	0	0	0	0	0	0	0	0	0
17	23	**D14:D11**		**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
17	23	0		PDN_CLK_SYNC_1	PDN_CLK_SYNC_2	0				DRV_MUX_SEL	DRV_SEL		EN_RESYNC_MUX_SEL	EN_RESYNC
18	24	**D31:D29**		**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15**
18	24	0				TX_START_DEL						CW_WAVE_MODE		CW_EN_MUX_SEL
18	24	**D14**	D13	**D12**	**D11:D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18	24	CW_EN_1	CW_EN_2	0	CW_DAMP_CNT			PAT_INV	CLK_DIV			0	TR_SW_DEL_MODE	TX_BF_MODE
19	25	**D31**	**D30**	**D29:D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21:D18**	**D17**	**D16**	**D15:D12**
19	25	PDN_GBL	EN_DYN_LDO	0	ELASTIC_REPEAT									
19	25	**D11**		**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
19	25	EN_ELASTIC		TAIL_COUNT					REPEAT_COUNT					0

8.6.2.1 Register 0h (offset = 0h) [reset = 0h]

Figure 68. Register 0h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BURST_WR_EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	LOAD_PROF	READ_EN		RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h		W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 26. Register 00 Field Descriptions

Bit	Field	Type	Reset	Description
31-9	0	W	0h	Must read or write 0
8-8	BURST_WR_EN	W	0h	0 = Normal operation 1 = Enables Burst mode for register write operation
7-4	0	W	0h	Must read or write 0
3	LOAD_PROF	W	0h	0 = Normal operation 1 = Load the profile data in memory This bit is self-clearing bit.
2-1	READ_EN	W	0h	00 = Normal operation 01 = Enable register read for die 1 10 = Enable register read for die 2 11 = Do not use
0-0	RESET	W	0h	0 = Normal operation 1 = Reset the device. It is self clearing bit

8.6.2.2 Register 1h (offset = 1h) [reset = 1h]

Figure 69. Register 1h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	STNDBY_G1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STNDBY_G2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 27. Register 1h Field Descriptions

Bit	Field	Type	Reset	Description
31-17	0	R/W	0h	Must write 0
16	STNDBY_G1	R/W	0h	0 = Normal operation 1 = Standby all the group 1 channels
15-1	0	R/W	0h	Must write 0
0	STNDBY_G2	R/W	0h	0 = Normal operation 1 = Standby all the group 2 channels

8.6.2.3 Register 6h (offset = 6h) [reset = 6h]

Figure 70. Register 6h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	DIS_DYN_CNTRL_2	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 28. Register 6h Field Descriptions

Bit	Field	Type	Reset	Description
31-5	0	R/W	0h	Must write 0
4	DIS_DYN_CNTRL_2	R/W	0h	0 = Dynamic power mode enabled for die 2 1 = Dynamic power mode disabled for die 2
3-0	0	R/W	0h	Must write 0

8.6.2.4 Register 0Bh (offset = 0Bh) [reset = 0Bh]

Figure 71. Register 0Bh

31	30	29	28	27	26	25	24
0	0	4A_Mode_CNTRL_1	0	0	0	LDO_MODE_G1	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
LDO_MODE_G1		0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 29. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
31-30	0	R/W	0h	Must write 0
29	4A_Mode_CNTRL_1	R/W	0h	0 = Default 5-Level mode 1 = 4.8-A mode 3-Level mode
28-26	0	R/W	0h	Must write 0

Table 29. Register 0Bh Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-22	LDO_MODE_G1	R/W	0h	0000 = LDO in default power mode 1111 = LDO in high power mode Don't use other combination.
21-0	0	R/W	0h	Must write 0

8.6.2.5 Register 0Ch (offset = 0Ch) [reset = 0Ch]

Figure 72. Register 0Ch

31	30	29	28	27	26	25	24
0		TR_SW_OFF_DEL_G2					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0		TR_SW_OFF_DEL_G1					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0		TR_SW_OFF_DEL_G4					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0		TR_SW_OFF_DEL_G3					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 30. Register 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
31-30	0	R/W	0h	Must write 0
29-24	TR_SW_OFF_DEL_G2	R/W	0h	Controls TR switch turnoff delay for B1 to B4 channels. Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.
23-22	0	R/W	0h	Must write 0
21-16	TR_SW_OFF_DEL_G1	R/W	0h	Controls TR switch turnoff delay for A1 to A4 channels. Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.
15-14	0	R/W	0h	Must write 0
13-8	TR_SW_OFF_DEL_G4	R/W	0h	Controls TR switch turnoff delay for B5 to B8 channels. Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.
7-6	0	R/W	0h	Must write 0
5-0	TR_SW_OFF_DEL_G3	R/W	0h	Controls TR switch turnoff delay for A5 to A8 channels. Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.

8.6.2.6 Register 0Fh (offset = 0Fh) [reset = 0Fh]

Figure 73. Register 0Fh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	DIS_DYN_CNTRL_1	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 31. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
31-5	0	R/W	0h	Must write 0
4	DIS_DYN_CNTRL_1	R/W	0h	0 = Dynamic power mode enabled for die 1 1 = Dynamic power mode disabled for die 1
3-0	0	R/W	0h	Must write 0

8.6.2.7 Register 14h (offset = 14h) [reset = 14h]

Figure 74. Register 14h

31	30	29	28	27	26	25	24
0	0	4A_Mode_CNTRL_2	0	0	0	LDO_MODE_G2	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
LDO_MODE_G2		0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 32. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
31-30	0	R/W	0h	Must write 0
29	4A_Mode_CNTRL_2	R/W	0h	0 = Default 5-Level mode 1 = 4.8-A mode 3-Level mode
28-26	0	R/W	0h	Must write 0

Table 32. Register 14h Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-22	LDO_MODE_G2	R/W	0h	0000 = LDO in default power mode 1111 = LDO in high power mode Don't use other combination.
21-0	0	R/W	0h	Must write 0

8.6.2.8 Register 15h (offset = 15h) [reset = 15h]

Figure 75. Register 15h

31	30	29	28	27	26	25	24
0				TR_SW_DEL_G2			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
23	22	21	20	19	18	17	16
TR_SW_DEL_G2							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0				TR_SW_DEL_G4			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
TR_SW_DEL_G4							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 33. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
31-28	0	R/W	0h	Must write 0
27-16	TR_SW_DEL_G2	R/W	100h	Controls TR switch turnon delay for B1 to B4 channels. Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.
15-12	0	R/W	0h	Must write 0
11-0	TR_SW_DEL_G4	R/W	100h	Controls TR switch turnon delay for B5 to B8 channels. Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.

8.6.2.9 Register 16h (offset = 16h) [reset = 16h]

Figure 76. Register 16h

31	30	29	28	27	26	25	24
BF_PROF_SEL_G1				TR_SW_DEL_G1			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
23	22	21	20	19	18	17	16
TR_SW_DEL_G1							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8

BF_PROF_SEL_G2				TR_SW_DEL_G2			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
TR_SW_DEL_G3							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 34. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
31-28	BF_PROF_SEL_G1	R/W	0h	Delay profile select bit for group 1 channels. Refer to *Delay Profile* section for more details.
27-16	TR_SW_DEL_G1	R/W	100h	Controls TR switch turnon delay for A1 to A4 channels. Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.
15-12	BF_PROF_SEL_G2	R/W	0h	Delay profile select bit for group 2 channels. Refer to *Delay Profile* section for more details.
11-0	TR_SW_DEL_G3	R/W	100h	Controls TR switch turnon delay for A5 to A8 channels. Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.

8.6.2.10 Register 17h (offset = 17h) [reset = 17h]

Figure 77. Register 17h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0					PDN_CLK_SYNC_1	PDN_CLK_SYNC_2	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0			DRV_MUX_SEL	DRV_SEL		EN_RESYNC_MUX_SEL	EN_RESYNC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 35. Register 17h Field Descriptions

Bit	Field	Type	Reset	Description
31-30	0	R/W	0h	Must write 0
29-11	0	R/W	0h	Must write 0
10	PDN_CLK_SYNC_1	R/W	0h	0 = Normal operation 1 = Power-down clock and sync buffer for die 1

Table 35. Register 17h Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PDN_CLK_SYNC_2	R/W	0h	0 = Normal operation 1 = Power-down clock and sync buffer for die 2
8-5	0	R/W	0h	Must write 0
4	DRV_MUX_SEL	R/W	0h	0 = Output transistor's current is controlled by DSEL_0/1 pins 1 = Output transistor current is controlled by DRV_SEL bits
3-2	DRV_SEL	R/W	0h	Controls output transistor current drive. Register DRV_MUX_SEL must be set to '1' to use DRV_SEL bits 00 = 1 A current 01 = 0.75 A current 10 = 0.5 A current 11 = 0.25 A current
1	EN_RESYNC_MUX_SEL	R/W	0h	0 = Re-synchronization feature in device is controlled by RESYNC pin 1 = Re-synchronization feature in device is controlled by EN_RESYNC bit
0	EN_RESYNC	R/W	0h	Controls re-synchronization feature of the device. Register EN_RESYNC_MUX_SEL must be set to '1' to use EN_RESYNC bit 0 = Re-sync mode disabled 1 = Re-sync mode enabled

8.6.2.11 Register 18h (offset = 18h) [reset = 18h]

Figure 78. Register 18h

31	30	29	28	27	26	25	24
0					TX_START_DEL		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TX_START_DEL						CW_WAVE_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CW_EN_MUX_SEL	CW_EN_1	CW_EN_2		CW_DAMP_CNT			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	PAT_INV	CLK_DIV			0	TR_SW_DEL_MODE	TX_BF_MODE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 36. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
31-27	0	R/W	0h	Must write 0. Ignore the read value of this field during read operation.
26-18	TX_START_DEL	R/W	0h	Controls the transmit delay. Refer to *Transmit Beam Former (TxBF)* section for more details.
17-16	CW_WAVE_MODE	R/W	0h	00 = Bipolar CW waveform 01 = Only positive polarity waveform 10 = Only negative polarity waveform 11 = Don't use
15	CW_EN_MUX_SEL	R/W	0h	0 = CW mode enable through pin 1 = CW mode enable through register bit 24[13:14]
14	CW_EN_1	R/W	0h	Valid when 24[15] is set to '1' 0 = CW mode disable for die 1 1 = CW mode enable for die 1
13	CW_EN_2	R/W	0h	Valid when 24[15] is set to '1' 0 = CW mode disable for die 2 1 = CW mode enable for die 2
12	0	R/W	0h	Must write 0
11:9	CW_DAMP_CNT	R/W	0h	CW wave damp duration. See *Continuous Wave Mode (CW)* for more details.
8-7	0	R/W	0h	Must write 0
6	PAT_INV	R/W	0h	0 = Normal operation 1 = Invert the output pattern
5-3	CLK_DIV	R/W	0h	Controls the clock division factor in transmit beam former block. Refer to *Transmit Beam Former (TxBF)* section for more details.
2	0	R/W	0h	Must write 0
1	TR_SW_DEL_MODE	R/W	0h	0 = TR switch turn on delay is counted from TR_BF_SYNC pulse 1 = TR switch turn on delay is counted from last pulse transmission Refer to *T/R Switch Control in On-Chip Beam-Forming Mode* section for more details.
0	TX_BF_MODE	R/W	0h	0 = Off-chip beamforming mode 1 = On-chip beamforming mode

8.6.2.12 Register 19h (offset = 19h) [reset = 19h]

Figure 79. Register 19h

31	30	29	28	27	26	25	24
PDN_GBL	EN_DYN_LDO	0		ELASTIC_REPEAT			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ELASTIC_REPEAT							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ELASTIC_REPEAT				EN_ELASTIC_MODE	TAIL_COUNT		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TAIL_COUNT		REPEAT_COUNT					0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 37. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description	
31	PDN_GBL	R/W	0h	0 = Normal operation 1 = Global power down the device	
30	EN_DYN_LDO	R/W	0h	0 = Dynamic power mode for floating LDO disabled 1 = Dynamic power mode for floating LDO enabled	
29-28	0	R/W	0h	Must write 0	
27-12	ELASTIC_REPEAT	R/W	0h	Repeat count for elastic mode.	
11	EN_ELASTIC_MODE	R/W	0h	Enable elastic mode.	
10-6	TAIL_COUNT	R/W	0h	Control the tail count for pattern generator block. Refer to Pattern Generator section for more details.	
5-1	REPEAT_COUNT	R/W	0h	Control the repeat count for pattern generator block. Refer to *Pattern Generator* section for more details.	
0	0	R/W	0h	Must write 0	

8.6.3 Pattern Select Register Map

Table 38. Pattern Select Register Map for 3- and 5-Level Mode

REGISTER ADDRESS		REGISTER DATA											
Hex	Decimal	D31	D30	D29:D24	D23	D22	D21:D16	D15	D14	D13:D8	D7	D6	D5:D0
1C	28	0	0	PAT_SEL_B8	0	0	PAT_SEL_B7	0	0	PAT_SEL_B6	0	0	PAT_SEL_B5
1D	29	0	0	PAT_SEL_B4	0	0	PAT_SEL_B3	0	0	PAT_SEL_B2	0	0	PAT_SEL_B1
1E	30	0	0	PAT_SEL_A8	0	0	PAT_SEL_A7	0	0	PAT_SEL_A6	0	0	PAT_SEL_A5
1F	31	0	0	PAT_SEL_A4	0	0	PAT_SEL_A3	0	0	PAT_SEL_A2	0	0	PAT_SEL_A1

8.6.3.1 Register 28h (offset = 1Ch) [reset = 1Ch]

Figure 80. Register 1Ch

31	30	29	28	27	26	25	24
0		PAT_SEL_B8					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0		PAT_SEL_B7					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0		PAT_SEL_B6					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0		PAT_SEL_B5					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 39. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
31-30	0	R/W	0h	Must write 0
29-24	PAT_SEL_B8	R/W	0h	Pattern select from pattern profile memory for channel B8
23-22	0	R/W	0h	Must write 0
21-16	PAT_SEL_B7	R/W	0h	Pattern select from pattern profile memory for channel B7
15-14	0	R/W	0h	Must write 0
13-8	PAT_SEL_B6	R/W	0h	Pattern select from pattern profile memory for channel B6
7-6	0	R/W	0h	Must write 0
5-0	PAT_SEL_B5	R/W	0h	Pattern select from pattern profile memory for channel B5

8.6.3.2 Register 1Dh (offset = 1Dh) [reset = 1Dh]

Figure 81. Register 1Dh

31	30	29	28	27	26	25	24
0		PAT_SEL_B4					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0		PAT_SEL_B3					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0		PAT_SEL_B2					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0		PAT_SEL_B1					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 40. Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Description
31-30	0	R/W	0h	Must write 0
29-24	PAT_SEL_B4	R/W	0h	Pattern select from pattern profile memory for channel B4
23-22	0	R/W	0h	Must write 0
21-16	PAT_SEL_B3	R/W	0h	Pattern select from pattern profile memory for channel B3
15-14	0	R/W	0h	Must write 0
13-8	PAT_SEL_B2	R/W	0h	Pattern select from pattern profile memory for channel B2
7-6	0	R/W	0h	Must write 0
5-0	PAT_SEL_B1	R/W	0h	Pattern select from pattern profile memory for channel B1

8.6.3.3 Register 1Eh (offset = 1Eh) [reset = 1Eh]

Figure 82. Register 1Eh

31	30	29	28	27	26	25	24
0		PAT_SEL_B4					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0		PAT_SEL_B3					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0		PAT_SEL_B2					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0		PAT_SEL_B1					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 41. Register 1Eh Field Descriptions

Bit	Field	Type	Reset	Description
31-30	0	R/W	0h	Must write 0
29-24	PAT_SEL_A8	R/W	0h	Pattern select from pattern profile memory for channel A8
23-22	0	R/W	0h	Must write 0
21-16	PAT_SEL_A7	R/W	0h	Pattern select from pattern profile memory for channel A7
15-14	0	R/W	0h	Must write 0
13-8	PAT_SEL_A6	R/W	0h	Pattern select from pattern profile memory for channel A6
7-6	0	R/W	0h	Must write 0
5-0	PAT_SEL_A5	R/W	0h	Pattern select from pattern profile memory for channel A5

8.6.3.4 Register 1Fh (offset = 1Fh) [reset = 1Fh]

Figure 83. Register 1Fh

31	30	29	28	27	26	25	24
0		PAT_SEL_A4					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0		PAT_SEL_A3					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0		PAT_SEL_A2					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0		PAT_SEL_A1					
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 42. Register 1Fh Field Descriptions

Bit	Field	Type	Reset	Description
31-30	0	R/W	0h	Must write 0
29-24	PAT_SEL_A4	R/W	0h	Pattern select from pattern profile memory for channel A4
23-22	0	R/W	0h	Must write 0
21-16	PAT_SEL_A3	R/W	0h	Pattern select from pattern profile memory for channel A3
15-14	0	R/W	0h	Must write 0
13-8	PAT_SEL_A2	R/W	0h	Pattern select from pattern profile memory for channel A2
7-6	0	R/W	0h	Must write 0
5-0	PAT_SEL_A1	R/W	0h	Pattern select from pattern profile memory for channel A1

8.6.4 Channel Power Down Register Map

Table 43. Channel Power Down Register Map for 3- and 5- Level Mode

ADDRESS (Hex)	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
1Ah	TR_SW_DIS_B4		TR_SW_DIS_B3		TR_SW_DIS_B2		TR_SW_DIS_B1		TR_SW_DIS_A4		TR_SW_DIS_A3		TR_SW_DIS_A2		TR_SW_DIS_A1	
1Ah	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1Ah	TR_SW_DIS_B8		TR_SW_DIS_B7		TR_SW_DIS_B6		TR_SW_DIS_B5		TR_SW_DIS_A8		TR_SW_DIS_A7		TR_SW_DIS_A6		TR_SW_DIS_A5	
1Bh	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
1Bh	0	0	0	0	0	0	0	0	PDN_PUL_B4	PDN_PUL_B3	PDN_PUL_B2	PDN_PUL_B1	PDN_PUL_A4	PDN_PUL_A3	PDN_PUL_A2	PDN_PUL_A1
1Bh	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1Bh	0	0	0	0	0	0	0	0	PDN_PUL_B8	PDN_PUL_B7	PDN_PUL_B6	PDN_PUL_B5	PDN_PUL_A8	PDN_PUL_A7	PDN_PUL_A6	PDN_PUL_A5

8.6.4.1 Register 1Ah (offset = 1Ah) [reset = 1Ah]

Figure 84. Register 1Ah

31	30	29	28	27	26	25	24
TR_SW_DIS_B4		TR_SW_DIS_B3		TR_SW_DIS_B2		TR_SW_DIS_B1	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TR_SW_DIS_A4		TR_SW_DIS_A3		TR_SW_DIS_A2		TR_SW_DIS_A1	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TR_SW_DIS_B8		TR_SW_DIS_B7		TR_SW_DIS_B6		TR_SW_DIS_B5	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TR_SW_DIS_A8		TR_SW_DIS_A7		TR_SW_DIS_A6		TR_SW_DIS_A5	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 44. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
31-30	TR_SW_DIS_B4	R/W	0h	00 = Normal operation 11 = TR switch for channel B4 is permanently disabled. Do not use any other bit combination.
29-28	TR_SW_DIS_B3	R/W	0h	00 = Normal operation 11 = TR switch for channel B3 is permanently disabled. Do not use any other bit combination.
27-26	TR_SW_DIS_B2	R/W	0h	00 = Normal operation 11 = TR switch for channel B2 is permanently disabled. Do not use any other bit combination.
25-24	TR_SW_DIS_B1	R/W	0h	00 = Normal operation 11 = TR switch for channel B1 is permanently disabled. Do not use any other bit combination.
23-22	TR_SW_DIS_A4	R/W	0h	00 = Normal operation 11 = TR switch for channel A4 is permanently disabled. Do not use any other bit combination.
21-20	TR_SW_DIS_A3	R/W	0h	00 = Normal operation 11 = TR switch for channel A3 is permanently disabled. Do not use any other bit combination.
19-18	TR_SW_DIS_A2	R/W	0h	00 = Normal operation 11 = TR switch for channel A2 is permanently disabled. Do not use any other bit combination.

Table 44. Register 1Ah Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	TR_SW_DIS_A1	R/W	0h	00 = Normal operation 11 = TR switch for channel A1 is permanently disabled. Do not use any other bit combination.
15-14	TR_SW_DIS_B8	R/W	0h	00 = Normal operation 11 = TR switch for channel B8 is permanently disabled. Do not use any other bit combination.
13-12	TR_SW_DIS_B7	R/W	0h	00 = Normal operation 11 = TR switch for channel B7 is permanently disabled. Do not use any other bit combination.
11-10	TR_SW_DIS_B6	R/W	0h	00 = Normal operation 11 = TR switch for channel B6 is permanently disabled. Do not use any other bit combination.
9-8	TR_SW_DIS_B5	R/W	0h	00 = Normal operation 11 = TR switch for channel B5 is permanently disabled. Do not use any other bit combination.
7-6	TR_SW_DIS_A8	R/W	0h	00 = Normal operation 11 = TR switch for channel A8 is permanently disabled. Do not use any other bit combination.
5-4	TR_SW_DIS_A7	R/W	0h	00 = Normal operation 11 = TR switch for channel A7 is permanently disabled. Do not use any other bit combination.
3-2	TR_SW_DIS_A6	R/W	0h	00 = Normal operation 11 = TR switch for channel A6 is permanently disabled. Do not use any other bit combination.
1-0	TR_SW_DIS_A5	R/W	0h	00 = Normal operation 11 = TR switch for channel A5 is permanently disabled. Do not use any other bit combination.

8.6.4.2 Register 1Bh (offset = 1Bh) [reset = 1Bh]

Figure 85. Register 1Bh

31	30	29	28	27	26	25	24
0							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PDN_PUL_B4	PDN_PUL_B3	PDN_PUL_B2	PDN_PUL_B1	PDN_PUL_A4	PDN_PUL_A3	PDN_PUL_A2	PDN_PUL_A1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_PUL_B8	PDN_PUL_B7	PDN_PUL_B6	PDN_PUL_B5	PDN_PUL_A8	PDN_PUL_A7	PDN_PUL_A6	PDN_PUL_A5
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 45. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
31-24	0	R/W	0h	Must write 0
23	PDN_PUL_B4	R/W	0h	0 = Normal operation 1 = Power down pulser of channel B4
22	PDN_PUL_B3	R/W	0h	0 = Normal operation 1 = Power down pulser of channel B3
21	PDN_PUL_B2	R/W	0h	0 = Normal operation 1 = Power down pulser of channel B2
20	PDN_PUL_B1	R/W	0h	0 = Normal operation 1 = Power down pulser of channel B1
19	PDN_PUL_A4	R/W	0h	0 = Normal operation 1 = Power down pulser of channel A4
18	PDN_PUL_A3	R/W	0h	0 = Normal operation 1 = Power down pulser of channel A3
17	PDN_PUL_A2	R/W	0h	0 = Normal operation 1 = Power down pulser of channel A2
16	PDN_PUL_A1	R/W	0h	0 = Normal operation 1 = Power down pulser of channel A1
15-8	0	R/W	0h	Must write 0
7	PDN_PUL_B8	R/W	0h	0 = Normal operation 1 = Power down pulser of channel B8
6	PDN_PUL_B7	R/W	0h	0 = Normal operation 1 = Power down pulser of channel B7
5	PDN_PUL_B6	R/W	0h	0 = Normal operation 1 = Power down pulser of channel B6
4	PDN_PUL_B5	R/W	0h	0 = Normal operation 1 = Power down pulser of channel B5

Table 45. Register 1Bh Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PDN_PUL_A8	R/W	0h	0 = Normal operation 1 = Power down pulser of channel A8
2	PDN_PUL_A7	R/W	0h	0 = Normal operation 1 = Power down pulser of channel A7
1	PDN_PUL_A6	R/W	0h	0 = Normal operation 1 = Power down pulser of channel A6
0	PDN_PUL_A5	R/W	0h	0 = Normal operation 1 = Power down pulser of channel A5

8.6.5 Delay Profile Register Map

Table 46. Delay Profile Register Map for 3-Level Mode

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31	D30	D29	D28:D16	D15	D14	D13	D12:D0
20	32	0	0	0	DEL_B8_1	0	0	0	DEL_B7_1
21	33	0	0	0	DEL_B6_1	0	0	0	DEL_B5_1
22	34	0	0	0	DEL_A8_1	0	0	0	DEL_A7_1
23	35	0	0	0	DEL_A6_1	0	0	0	DEL_A5_1
24	36	0	0	0	DEL_B4_1	0	0	0	DEL_B3_1
25	37	0	0	0	DEL_B2_1	0	0	0	DEL_B1_1
26	38	0	0	0	DEL_A4_1	0	0	0	DEL_A2_1
27	39	0	0	0	DEL_A2_2	0	0	0	DEL_A1_1
28	40	0	0	0	DEL_B8_2	0	0	0	DEL_B7_2
29	41	0	0	0	DEL_B6_2	0	0	0	DEL_B5_2
2A	42	0	0	0	DEL_A8_2	0	0	0	DEL_A7_2
2B	43	0	0	0	DEL_A6_2	0	0	0	DEL_A5_2
2C	44	0	0	0	DEL_B4_2	0	0	0	DEL_B3_2
2D	45	0	0	0	DEL_B2_2	0	0	0	DEL_B1_2
2E	46	0	0	0	DEL_A4_2	0	0	0	DEL_A3_2
2F	47	0	0	0	DEL_A2_2	0	0	0	DEL_A1_2
30	48	0	0	0	DEL_B8_3	0	0	0	DEL_B7_3
31	49	0	0	0	DEL_B6_3	0	0	0	DEL_B5_3
32	50	0	0	0	DEL_A8_3	0	0	0	DEL_A7_3
33	51	0	0	0	DEL_A6_3	0	0	0	DEL_A5_3
34	52	0	0	0	DEL_B4_3	0	0	0	DEL_B3_3
35	53	0	0	0	DEL_B2_3	0	0	0	DEL_B1_3
36	54	0	0	0	DEL_A4_3	0	0	0	DEL_A3_3
37	55	0	0	0	DEL_A2_3	0	0	0	DEL_A1_3
38	56	0	0	0	DEL_B8_4	0	0	0	DEL_B7_4
39	57	0	0	0	DEL_B6_4	0	0	0	DEL_B5_4
3A	58	0	0	0	DEL_A8_4	0	0	0	DEL_A7_4
3B	59	0	0	0	DEL_A6_4	0	0	0	DEL_A5_4
3C	60	0	0	0	DEL_B4_4	0	0	0	DEL_B3_4
3D	61	0	0	0	DEL_B2_4	0	0	0	DEL_B1_4
3E	62	0	0	0	DEL_A4_4	0	0	0	DEL_A3_4
3F	63	0	0	0	DEL_A2_4	0	0	0	DEL_A1_4
40	64	0	0	0	DEL_B8_5	0	0	0	DEL_B7_5
41	65	0	0	0	DEL_B6_5	0	0	0	DEL_B5_5
42	66	0	0	0	DEL_A8_5	0	0	0	DEL_A7_5
43	67	0	0	0	DEL_A6_5	0	0	0	DEL_A5_5
44	68	0	0	0	DEL_B4_5	0	0	0	DEL_B3_5
45	69	0	0	0	DEL_B2_5	0	0	0	DEL_B1_5
46	70	0	0	0	DEL_A4_5	0	0	0	DEL_A3_5
47	71	0	0	0	DEL_A2_5	0	0	0	DEL_A1_5
48	72	0	0	0	DEL_B8_6	0	0	0	DEL_B7_6
49	73	0	0	0	DEL_B6_6	0	0	0	DEL_B5_6
4A	74	0	0	0	DEL_A8_6	0	0	0	DEL_A7_6
4B	75	0	0	0	DEL_A6_6	0	0	0	DEL_A5_6
4C	76	0	0	0	DEL_B4_6	0	0	0	DEL_B3_6
4D	77	0	0	0	DEL_B2_6	0	0	0	DEL_B1_6
4E	78	0	0	0	DEL_A4_6	0	0	0	DEL_A3_6
4F	79	0	0	0	DEL_A2_6	0	0	0	DEL_A1_6
50	80	0	0	0	DEL_B8_7	0	0	0	DEL_B7_7
51	81	0	0	0	DEL_B6_7	0	0	0	DEL_B5_7
52	82	0	0	0	DEL_A8_7	0	0	0	DEL_A7_7
53	83	0	0	0	DEL_A6_7	0	0	0	DEL_A5_7

Table 46. Delay Profile Register Map for 3-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31	D30	D29	D28:D16	D15	D14	D13	D12:D0
54	84	0	0	0	DEL_B4_7	0	0	0	DEL_B3_7
55	85	0	0	0	DEL_B2_7	0	0	0	DEL_B1_7
56	86	0	0	0	DEL_A4_7	0	0	0	DEL_A3_7
57	87	0	0	0	DEL_A2_7	0	0	0	DEL_A1_7
58	88	0	0	0	DEL_B8_8	0	0	0	DEL_B7_8
59	89	0	0	0	DEL_B6_8	0	0	0	DEL_B5_8
5A	90	0	0	0	DEL_A8_8	0	0	0	DEL_A7_8
5B	91	0	0	0	DEL_A6_8	0	0	0	DEL_A5_8
5C	92	0	0	0	DEL_B4_8	0	0	0	DEL_B3_8
5D	93	0	0	0	DEL_B2_8	0	0	0	DEL_B1_8
5E	94	0	0	0	DEL_A4_8	0	0	0	DEL_A3_8
5F	95	0	0	0	DEL_A2_8	0	0	0	DEL_A1_8
60	96	0	0	0	DEL_B8_9	0	0	0	DEL_B7_9
61	97	0	0	0	DEL_B6_9	0	0	0	DEL_B5_9
62	98	0	0	0	DEL_A8_9	0	0	0	DEL_A7_9
63	99	0	0	0	DEL_A6_9	0	0	0	DEL_A5_9
64	100	0	0	0	DEL_B4_9	0	0	0	DEL_B3_9
65	101	0	0	0	DEL_B2_9	0	0	0	DEL_B1_9
66	102	0	0	0	DEL_A4_9	0	0	0	DEL_A3_9
67	103	0	0	0	DEL_A2_9	0	0	0	DEL_A1_9
68	104	0	0	0	DEL_B8_10	0	0	0	DEL_B7_10
69	105	0	0	0	DEL_B6_10	0	0	0	DEL_B5_10
6A	106	0	0	0	DEL_A8_10	0	0	0	DEL_A7_10
6B	107	0	0	0	DEL_A6_10	0	0	0	DEL_A5_10
6C	108	0	0	0	DEL_B4_10	0	0	0	DEL_B3_10
6D	109	0	0	0	DEL_B2_10	0	0	0	DEL_B1_10
6E	110	0	0	0	DEL_A4_10	0	0	0	DEL_A3_10
6F	111	0	0	0	DEL_A2_10	0	0	0	DEL_A1_10
70	112	0	0	0	DEL_B8_11	0	0	0	DEL_B7_11
71	113	0	0	0	DEL_B6_11	0	0	0	DEL_B5_11
72	114	0	0	0	DEL_A8_11	0	0	0	DEL_A7_11
73	115	0	0	0	DEL_A6_11	0	0	0	DEL_A5_11
74	116	0	0	0	DEL_B4_11	0	0	0	DEL_B3_11
75	117	0	0	0	DEL_B2_11	0	0	0	DEL_B1_11
76	118	0	0	0	DEL_A4_11	0	0	0	DEL_A3_11
77	119	0	0	0	DEL_A2_11	0	0	0	DEL_A1_11
78	120	0	0	0	DEL_B8_12	0	0	0	DEL_B7_12
79	121	0	0	0	DEL_B6_12	0	0	0	DEL_B5_12
7A	122	0	0	0	DEL_A8_12	0	0	0	DEL_A7_12
7B	123	0	0	0	DEL_A6_12	0	0	0	DEL_A5_12
7C	124	0	0	0	DEL_B4_12	0	0	0	DEL_B3_12
7D	125	0	0	0	DEL_B2_12	0	0	0	DEL_B1_12
7E	126	0	0	0	DEL_A4_12	0	0	0	DEL_A3_12
7F	127	0	0	0	DEL_A2_12	0	0	0	DEL_A1_12
80	128	0	0	0	DEL_B8_13	0	0	0	DEL_B7_13
81	129	0	0	0	DEL_B6_13	0	0	0	DEL_B5_13
82	130	0	0	0	DEL_A8_13	0	0	0	DEL_A7_13
83	131	0	0	0	DEL_A6_13	0	0	0	DEL_A5_13
84	132	0	0	0	DEL_B4_13	0	0	0	DEL_B3_13
85	133	0	0	0	DEL_B2_13	0	0	0	DEL_B1_13
86	134	0	0	0	DEL_A4_13	0	0	0	DEL_A3_13
87	135	0	0	0	DEL_A2_13	0	0	0	DEL_A1_13
88	136	0	0	0	DEL_B8_14	0	0	0	DEL_B7_14
89	137	0	0	0	DEL_B6_14	0	0	0	DEL_B5_14

Table 46. Delay Profile Register Map for 3-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31	D30	D29	D28:D16	D15	D14	D13	D12:D0
8A	138	0	0	0	DEL_A8_14	0	0	0	DEL_A7_14
8B	139	0	0	0	DEL_A6_14	0	0	0	DEL_A5_14
8C	140	0	0	0	DEL_B4_14	0	0	0	DEL_B3_14
8D	141	0	0	0	DEL_B2_14	0	0	0	DEL_B1_14
8E	142	0	0	0	DEL_A4_14	0	0	0	DEL_A3_14
8F	143	0	0	0	DEL_A2_14	0	0	0	DEL_A1_14
90	144	0	0	0	DEL_B8_15	0	0	0	DEL_B7_15
91	145	0	0	0	DEL_B6_15	0	0	0	DEL_B5_15
92	146	0	0	0	DEL_A8_15	0	0	0	DEL_A7_15
93	147	0	0	0	DEL_A6_15	0	0	0	DEL_A5_15
94	148	0	0	0	DEL_B4_15	0	0	0	DEL_B3_15
95	149	0	0	0	DEL_B2_15	0	0	0	DEL_B1_15
96	150	0	0	0	DEL_A4_15	0	0	0	DEL_A3_15
97	151	0	0	0	DEL_A2_15	0	0	0	DEL_A1_15
98	152	0	0	0	DEL_B8_16	0	0	0	DEL_B7_16
99	153	0	0	0	DEL_B6_16	0	0	0	DEL_B5_16
9A	154	0	0	0	DEL_A8_16	0	0	0	DEL_A7_16
9B	155	0	0	0	DEL_A6_16	0	0	0	DEL_A5_16
9C	156	0	0	0	DEL_B4_16	0	0	0	DEL_B3_16
9D	157	0	0	0	DEL_B2_16	0	0	0	DEL_B1_16
9E	158	0	0	0	DEL_A4_16	0	0	0	DEL_A3_16
9F	159	0	0	0	DEL_A2_16	0	0	0	DEL_A1_16

8.6.5.1 Register 20h (offset = 20h) [reset = 20h]

Figure 86. Register 20h

31	30	29	28	27	26	25	24
0	0	0	DEL_B8_1				
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
23	22	21	20	19	18	17	16
DEL_B8_1							
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
15	14	13	12	11	10	9	8
0	0	0	DEL_B7_1				
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
7	6	5	4	3	2	1	0
DEL_B7_1							
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 47. Register 20h Field Descriptions

Bit	Field	Type	Reset	Description
31-29	0	R/W	Undefined	Must write 0
28-16	DEL_B8_1	R/W	Undefined	Transmit beamforming delay for channel B8, profile 1.
15-13	0	R/W	Undefined	Must write 0
12-0	DEL_B7_1	R/W	Undefined	Transmit beamforming delay for channel B7, profile 1.

8.6.5.2 Register 21h to 9Fh (offset = 21h to 9Fh) [reset = 21h to 9Fh]

In below table register field name are given asDEL_A/Bx1_y and DEL_A/Bx2_y. Where x1 and x2 represents channel number and can vary from A1 to A8 and B1 to B8. and y represents profile number and can vary from 1 to 16 across register addresses in delay profile register map.

Figure 87. Register 21h to 9Fh

31	30	29	28	27	26	25	24
0	0	0	DEL_A/Bx1_y				
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
23	22	21	20	19	18	17	16
DEL_A/Bx1_y							
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
15	14	13	12	11	10	9	8
0	0	0	DEL_A/Bx2_y				
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
7	6	5	4	3	2	1	0
DEL_A/Bx2_y							
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 48. Register 21h to 9Fh Field Descriptions

Bit	Field	Type	Reset	Description
31-29	0	R/W	Undefined	Must write 0
28-16	DEL_A/Bx1_y	R/W	Undefined	Transmit beam forming delay for channel A/Bx1, profile y. x1 represents even numbers from 1 to 8. y represents profile number and can vary from 1 to 16.
15-13	0	R/W	Undefined	Must write 0
12-0	DEL_A/Bx2_y	R/W	Undefined	Transmit beamforming delay for channel A/Bx2, profile y. x2 represents odd numbers from 1 to 8. y represents profile number and can vary from 1 to 16.

Table 49. Delay Profile Register Map for 5-Level Mode

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31	D30	D29	D28:D16	D15	D14	D13	D12:D0
20	32	0	0	0	DEL_A8_1	0	0	0	DEL_A7_1
21	33	0	0	0	DEL_A6_1	0	0	0	DEL_A5_1
22	34	0	0	0	DEL_A4_1	0	0	0	DEL_A3_1
23	35	0	0	0	DEL_A2_1	0	0	0	DEL_A1_1
24	36	0	0	0	DEL_A8_2	0	0	0	DEL_A7_2
25	37	0	0	0	DEL_A6_2	0	0	0	DEL_A5_2
26	38	0	0	0	DEL_A4_2	0	0	0	DEL_A3_2
27	39	0	0	0	DEL_A2_2	0	0	0	DEL_A1_2
28	40	0	0	0	DEL_A8_3	0	0	0	DEL_A7_3
29	41	0	0	0	DEL_A6_3	0	0	0	DEL_A5_3
2A	42	0	0	0	DEL_A4_3	0	0	0	DEL_A3_3
2B	43	0	0	0	DEL_A2_3	0	0	0	DEL_A1_3

Table 49. Delay Profile Register Map for 5-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31	D30	D29	D28:D16	D15	D14	D13	D12:D0
2C	44	0	0	0	DEL_A8_4	0	0	0	DEL_A7_4
2D	45	0	0	0	DEL_A6_4	0	0	0	DEL_A5_4
2E	46	0	0	0	DEL_A4_4	0	0	0	DEL_A3_4
2F	47	0	0	0	DEL_A2_4	0	0	0	DEL_A1_4
30	48	0	0	0	DEL_A8_5	0	0	0	DEL_A7_5
31	49	0	0	0	DEL_A6_5	0	0	0	DEL_A5_5
32	50	0	0	0	DEL_A4_5	0	0	0	DEL_A3_5
33	51	0	0	0	DEL_A2_5	0	0	0	DEL_A1_5
34	52	0	0	0	DEL_A8_6	0	0	0	DEL_A7_6
35	53	0	0	0	DEL_A6_6	0	0	0	DEL_A5_6
36	54	0	0	0	DEL_A4_6	0	0	0	DEL_A3_6
37	55	0	0	0	DEL_A2_6	0	0	0	DEL_A1_6
38	56	0	0	0	DEL_A8_7	0	0	0	DEL_A7_7
39	57	0	0	0	DEL_A6_7	0	0	0	DEL_A5_7
3A	58	0	0	0	DEL_A4_7	0	0	0	DEL_A3_7
3B	59	0	0	0	DEL_A2_7	0	0	0	DEL_A1_7
3C	60	0	0	0	DEL_A8_8	0	0	0	DEL_A7_8
3D	61	0	0	0	DEL_A6_8	0	0	0	DEL_A5_8
3E	62	0	0	0	DEL_A4_8	0	0	0	DEL_A3_8
3F	63	0	0	0	DEL_A2_8	0	0	0	DEL_A1_8
40	64	0	0	0	DEL_A8_9	0	0	0	DEL_A7_9
41	65	0	0	0	DEL_A6_9	0	0	0	DEL_A5_9
42	66	0	0	0	DEL_A4_9	0	0	0	DEL_A3_9
43	67	0	0	0	DEL_A2_9	0	0	0	DEL_A1_9
44	68	0	0	0	DEL_A8_10	0	0	0	DEL_A7_10
45	69	0	0	0	DEL_A6_10	0	0	0	DEL_A5_10
46	70	0	0	0	DEL_A4_10	0	0	0	DEL_A3_10
47	71	0	0	0	DEL_A2_10	0	0	0	DEL_A1_10
48	72	0	0	0	DEL_A8_11	0	0	0	DEL_A7_11
49	73	0	0	0	DEL_A6_11	0	0	0	DEL_A5_11
4A	74	0	0	0	DEL_A4_11	0	0	0	DEL_A3_11
4B	75	0	0	0	DEL_A2_11	0	0	0	DEL_A1_11
4C	76	0	0	0	DEL_A8_12	0	0	0	DEL_A7_12
4D	77	0	0	0	DEL_A6_12	0	0	0	DEL_A5_12
4E	78	0	0	0	DEL_A4_12	0	0	0	DEL_A3_12
4F	79	0	0	0	DEL_A2_12	0	0	0	DEL_A1_12
50	80	0	0	0	DEL_A8_13	0	0	0	DEL_A7_13
51	81	0	0	0	DEL_A6_13	0	0	0	DEL_A5_13
52	82	0	0	0	DEL_A4_13	0	0	0	DEL_A3_13
53	83	0	0	0	DEL_A2_13	0	0	0	DEL_A1_13
54	84	0	0	0	DEL_A8_14	0	0	0	DEL_A7_14
55	85	0	0	0	DEL_A6_14	0	0	0	DEL_A5_14
56	86	0	0	0	DEL_A4_14	0	0	0	DEL_A3_14
57	87	0	0	0	DEL_A2_14	0	0	0	DEL_A1_14
58	88	0	0	0	DEL_A8_15	0	0	0	DEL_A7_15
59	89	0	0	0	DEL_A6_15	0	0	0	DEL_A5_15
5A	90	0	0	0	DEL_A4_15	0	0	0	DEL_A3_15
5B	91	0	0	0	DEL_A2_15	0	0	0	DEL_A1_15
5C	92	0	0	0	DEL_A8_16	0	0	0	DEL_A7_16
5D	93	0	0	0	DEL_A6_16	0	0	0	DEL_A5_16
5E	94	0	0	0	DEL_A4_16	0	0	0	DEL_A3_16
5F	95	0	0	0	DEL_A2_16	0	0	0	DEL_A1_16

8.6.5.3 Register 20h (offset = 20h) [reset = 20h]

Figure 88. Register 20h

31	30	29	28	27	26	25	24
0	0	0	DEL_A8_1				
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
23	22	21	20	19	18	17	16
DEL_A8_1							
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
15	14	13	12	11	10	9	8
0	0	0	DEL_A7_1				
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
7	6	5	4	3	2	1	0
DEL_A7_1							
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 50. Register 20h Field Descriptions

Bit	Field	Type	Reset	Description
31-29	0	R/W	Undefined	Must write 0
28-16	DEL_A8_1	R/W	Undefined	Transmit beamforming delay for channel A8, profile 1.
15-13	0	R/W	Undefined	Must write 0
12-0	DEL_A7_1	R/W	Undefined	Transmit beamforming delay for channel A7, profile 1.

8.6.5.4 Register 21h to 5Fh (offset = 21h to 5Fh) [reset = 21h to 5Fh]

In below table register field name are given as DEL_Ax1_y and DEL_Ax2_y. Where x1 and x2 represents channel number and can vary from A1 to A8. and y represents profile number and can vary from 1 to 16 across register addresses in delay profile register map.

Figure 89. Register 21h to 5Fh

31	30	29	28	27	26	25	24
0	0	0	DEL_Ax1_y				
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
23	22	21	20	19	18	17	16
DEL_Ax1_y							
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
15	14	13	12	11	10	9	8
0	0	0	DEL_Ax2_y				
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
7	6	5	4	3	2	1	0
DEL_Ax2_y							
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 51. Register 21h to 5Fh Field Descriptions

Bit	Field	Type	Reset	Description
31-29	0	R/W	Undefined	Must write 0
28-16	DEL_Ax1_y	R/W	Undefined	Transmit beamforming delay for channel Ax1, profile y. x1 represents an even number from 1 to 8. y represents profile number and can vary from 1 to 16.
15-13	0	R/W	Undefined	Must write 0
12-0	DEL_Ax2_y	R/W	Undefined	Transmit beamforming delay for channel Ax2, profile y. x2 represents an odd number from 1 to 8. y represents profile number and can vary from 1 to 16.

8.6.6 Pattern Profile Register Map

Table 52. Pattern Profile Register Map for 3-Level Mode

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
A0	160	PER_4_1	LVL_4_1	PER_3_1	LVL_3_1	PER_2_1	LVL_2_1	PER_1_1	LVL_1_1
A1	161	PER_8_1	LVL_8_1	PER_7_1	LVL_7_1	PER_6_1	LVL_6_1	PER_5_1	LVL_5_1
A2	162	PER_12_1	LVL_12_1	PER_11_1	LVL_11_1	PER_10_1	LVL_10_1	PER_9_1	LVL_9_1
A3	163	PER_16_1	LVL_16_1	PER_15_1	LVL_15_1	PER_14_1	LVL_14_1	PER_13_1	LVL_13_1
A4	164	PER_4_2	LVL_4_2	PER_3_2	LVL_3_2	PER_2_2	LVL_2_2	PER_1_2	LVL_1_2
A5	165	PER_8_2	LVL_8_2	PER_7_2	LVL_7_2	PER_6_2	LVL_6_2	PER_5_2	LVL_5_2
A6	166	PER_12_2	LVL_12_2	PER_11_2	LVL_11_2	PER_10_2	LVL_10_2	PER_9_2	LVL_9_2
A7	167	PER_16_2	LVL_16_2	PER_15_2	LVL_15_2	PER_14_2	LVL_14_2	PER_13_2	LVL_13_2
A8	168	PER_4_3	LVL_4_3	PER_3_3	LVL_3_3	PER_2_3	LVL_2_3	PER_1_3	LVL_1_3
A9	169	PER_8_3	LVL_8_3	PER_7_3	LVL_7_3	PER_6_3	LVL_6_3	PER_5_3	LVL_5_3
AA	170	PER_12_3	LVL_12_3	PER_11_3	LVL_11_3	PER_10_3	LVL_10_3	PER_9_3	LVL_9_3
AB	171	PER_16_3	LVL_16_3	PER_15_3	LVL_15_3	PER_14_3	LVL_14_3	PER_13_3	LVL_13_3
AC	172	PER_4_4	LVL_4_4	PER_3_4	LVL_3_4	PER_2_4	LVL_2_4	PER_1_4	LVL_1_4
AD	173	PER_8_4	LVL_8_4	PER_7_4	LVL_7_4	PER_6_4	LVL_6_4	PER_5_4	LVL_5_4
AE	174	PER_12_4	LVL_12_4	PER_11_4	LVL_11_4	PER_10_4	LVL_10_4	PER_9_4	LVL_9_4
AF	175	PER_16_4	LVL_16_4	PER_15_4	LVL_15_4	PER_14_4	LVL_14_4	PER_13_4	LVL_13_4
B0	176	PER_4_5	LVL_4_5	PER_3_5	LVL_3_5	PER_2_5	LVL_2_5	PER_1_5	LVL_1_5
B1	177	PER_8_5	LVL_8_5	PER_7_5	LVL_7_5	PER_6_5	LVL_6_5	PER_5_5	LVL_5_5
B2	178	PER_12_5	LVL_12_5	PER_11_5	LVL_11_5	PER_10_5	LVL_10_5	PER_9_5	LVL_9_5
B3	179	PER_16_5	LVL_16_5	PER_15_5	LVL_15_5	PER_14_5	LVL_14_5	PER_13_5	LVL_13_5
B4	180	PER_4_6	LVL_4_6	PER_3_6	LVL_3_6	PER_2_6	LVL_2_6	PER_1_6	LVL_1_6
B5	181	PER_8_6	LVL_8_6	PER_7_6	LVL_7_6	PER_6_6	LVL_6_6	PER_5_6	LVL_5_6
B6	182	PER_12_6	LVL_12_6	PER_11_6	LVL_11_6	PER_10_6	LVL_10_6	PER_9_6	LVL_9_6
B7	183	PER_16_6	LVL_16_6	PER_15_6	LVL_15_6	PER_14_6	LVL_14_6	PER_13_6	LVL_13_6
B8	184	PER_4_7	LVL_4_7	PER_3_7	LVL_3_7	PER_2_7	LVL_2_7	PER_1_7	LVL_1_7
B9	185	PER_8_7	LVL_8_7	PER_7_7	LVL_7_7	PER_6_7	LVL_6_7	PER_5_7	LVL_5_7
BA	186	PER_12_7	LVL_12_7	PER_11_7	LVL_11_7	PER_10_7	LVL_10_7	PER_9_7	LVL_9_7
BB	187	PER_16_7	LVL_16_7	PER_15_7	LVL_15_7	PER_14_7	LVL_14_7	PER_13_7	LVL_13_7
BC	188	PER_4_8	LVL_4_8	PER_3_8	LVL_3_8	PER_2_8	LVL_2_8	PER_1_8	LVL_1_8
BD	189	PER_8_8	LVL_8_8	PER_7_8	LVL_7_8	PER_6_8	LVL_6_8	PER_5_8	LVL_5_8
BE	190	PER_12_8	LVL_12_8	PER_11_8	LVL_11_8	PER_10_8	LVL_10_8	PER_9_8	LVL_9_8
BF	191	PER_16_8	LVL_16_8	PER_15_8	LVL_15_8	PER_14_8	LVL_14_8	PER_13_8	LVL_13_8
C0	192	PER_4_9	LVL_4_9	PER_3_9	LVL_3_9	PER_2_9	LVL_2_9	PER_1_9	LVL_1_9
C1	193	PER_8_9	LVL_8_9	PER_7_9	LVL_7_9	PER_6_9	LVL_6_9	PER_5_9	LVL_5_9
C2	194	PER_12_9	LVL_12_9	PER_11_9	LVL_11_9	PER_10_9	LVL_10_9	PER_9_9	LVL_9_9
C3	195	PER_16_9	LVL_16_9	PER_15_9	LVL_15_9	PER_14_9	LVL_14_9	PER_13_9	LVL_13_9
C4	196	PER_4_10	LVL_4_10	PER_3_10	LVL_3_10	PER_2_10	LVL_2_10	PER_1_10	LVL_1_10
C5	197	PER_8_10	LVL_8_10	PER_7_10	LVL_7_10	PER_6_10	LVL_6_10	PER_5_10	LVL_5_10
C6	198	PER_12_10	LVL_12_10	PER_11_10	LVL_11_10	PER_10_10	LVL_10_10	PER_9_10	LVL_9_10
C7	199	PER_16_10	LVL_16_10	PER_15_10	LVL_15_10	PER_14_10	LVL_14_10	PER_13_10	LVL_13_10
C8	200	PER_4_11	LVL_4_11	PER_3_11	LVL_3_11	PER_2_11	LVL_2_11	PER_1_11	LVL_1_11
C9	201	PER_8_11	LVL_8_11	PER_7_11	LVL_7_11	PER_6_11	LVL_6_11	PER_5_11	LVL_5_11
CA	202	PER_12_11	LVL_12_11	PER_11_11	LVL_11_11	PER_10_11	LVL_10_11	PER_9_11	LVL_9_11
CB	203	PER_16_11	LVL_16_11	PER_15_11	LVL_15_11	PER_14_11	LVL_14_11	PER_13_11	LVL_13_11
CC	204	PER_4_12	LVL_4_12	PER_3_12	LVL_3_12	PER_2_12	LVL_2_12	PER_1_12	LVL_1_12
CD	205	PER_8_12	LVL_8_12	PER_7_12	LVL_7_12	PER_6_12	LVL_6_12	PER_5_12	LVL_5_12
CE	206	PER_12_12	LVL_12_12	PER_11_12	LVL_11_12	PER_10_12	LVL_10_12	PER_9_12	LVL_9_12
CF	207	PER_16_12	LVL_16_12	PER_15_12	LVL_15_12	PER_14_12	LVL_14_12	PER_13_12	LVL_13_12
D0	208	PER_4_13	LVL_4_13	PER_3_13	LVL_3_13	PER_2_13	LVL_2_13	PER_1_13	LVL_1_13
D1	209	PER_8_13	LVL_8_13	PER_7_13	LVL_7_13	PER_6_13	LVL_6_13	PER_5_13	LVL_5_13
D2	210	PER_12_13	LVL_12_13	PER_11_13	LVL_11_13	PER_10_13	LVL_10_13	PER_9_13	LVL_9_13
D3	211	PER_16_13	LVL_16_13	PER_15_13	LVL_15_13	PER_14_13	LVL_14_13	PER_13_13	LVL_13_13

Table 52. Pattern Profile Register Map for 3-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
D4	212	PER_4_14	LVL_4_14	PER_3_14	LVL_3_14	PER_2_14	LVL_2_14	PER_1_14	LVL_1_14
D5	213	PER_8_14	LVL_8_14	PER_7_14	LVL_7_14	PER_6_14	LVL_6_14	PER_5_14	LVL_5_14
D6	214	PER_12_14	LVL_12_14	PER_11_14	LVL_11_14	PER_10_14	LVL_10_14	PER_9_14	LVL_9_14
D7	215	PER_16_14	LVL_16_14	PER_15_14	LVL_15_14	PER_14_14	LVL_14_14	PER_13_14	LVL_13_14
D8	216	PER_4_15	LVL_4_15	PER_3_15	LVL_3_15	PER_2_15	LVL_2_15	PER_1_15	LVL_1_15
D9	217	PER_8_15	LVL_8_15	PER_7_15	LVL_7_15	PER_6_15	LVL_6_15	PER_5_15	LVL_5_15
DA	218	PER_12_15	LVL_12_15	PER_11_15	LVL_11_15	PER_10_15	LVL_10_15	PER_9_15	LVL_9_15
DB	219	PER_16_15	LVL_16_15	PER_15_15	LVL_15_15	PER_14_15	LVL_14_15	PER_13_15	LVL_13_15
DC	220	PER_4_16	LVL_4_16	PER_3_16	LVL_3_16	PER_2_16	LVL_2_16	PER_1_16	LVL_1_16
DD	221	PER_8_16	LVL_8_16	PER_7_16	LVL_7_16	PER_6_16	LVL_6_16	PER_5_16	LVL_5_16
DE	222	PER_12_16	LVL_12_16	PER_11_16	LVL_11_16	PER_10_16	LVL_10_16	PER_9_16	LVL_9_16
DF	223	PER_16_16	LVL_16_16	PER_15_16	LVL_15_16	PER_14_16	LVL_14_16	PER_13_16	LVL_13_16
E0	224	PER_4_17	LVL_4_17	PER_3_17	LVL_3_17	PER_2_17	LVL_2_17	PER_1_17	LVL_1_17
E1	225	PER_8_17	LVL_8_17	PER_7_17	LVL_7_17	PER_6_17	LVL_6_17	PER_5_17	LVL_5_17
E2	226	PER_12_17	LVL_12_17	PER_11_17	LVL_11_17	PER_10_17	LVL_10_17	PER_9_17	LVL_9_17
E3	227	PER_16_17	LVL_16_17	PER_15_17	LVL_15_17	PER_14_17	LVL_14_17	PER_13_17	LVL_13_17
E4	228	PER_4_18	LVL_4_18	PER_3_18	LVL_3_18	PER_2_18	LVL_2_18	PER_1_18	LVL_1_18
E5	229	PER_8_18	LVL_8_18	PER_7_18	LVL_7_18	PER_6_18	LVL_6_18	PER_5_18	LVL_5_18
E6	230	PER_12_18	LVL_12_18	PER_11_18	LVL_11_18	PER_10_18	LVL_10_18	PER_9_18	LVL_9_18
E7	231	PER_16_18	LVL_16_18	PER_15_18	LVL_15_18	PER_14_18	LVL_14_18	PER_13_18	LVL_13_18
E8	232	PER_4_19	LVL_4_19	PER_3_19	LVL_3_19	PER_2_19	LVL_2_19	PER_1_19	LVL_1_19
E9	233	PER_8_19	LVL_8_19	PER_7_19	LVL_7_19	PER_6_19	LVL_6_19	PER_5_19	LVL_5_19
EA	234	PER_12_19	LVL_12_19	PER_11_19	LVL_11_19	PER_10_19	LVL_10_19	PER_9_19	LVL_9_19
EB	235	PER_16_19	LVL_16_19	PER_15_19	LVL_15_19	PER_14_19	LVL_14_19	PER_13_19	LVL_13_19
EC	236	PER_4_20	LVL_4_20	PER_3_20	LVL_3_20	PER_2_20	LVL_2_20	PER_1_20	LVL_1_20
ED	237	PER_8_20	LVL_8_20	PER_7_20	LVL_7_20	PER_6_20	LVL_6_20	PER_5_20	LVL_5_20
EE	238	PER_12_20	LVL_12_20	PER_11_20	LVL_11_20	PER_10_20	LVL_10_20	PER_9_20	LVL_9_20
EF	239	PER_16_20	LVL_16_20	PER_15_20	LVL_15_20	PER_14_20	LVL_14_20	PER_13_20	LVL_13_20
F0	240	PER_4_21	LVL_4_21	PER_3_21	LVL_3_21	PER_2_21	LVL_2_21	PER_1_21	LVL_1_21
F1	241	PER_8_21	LVL_8_21	PER_7_21	LVL_7_21	PER_6_21	LVL_6_21	PER_5_21	LVL_5_21
F2	242	PER_12_21	LVL_12_21	PER_11_21	LVL_11_21	PER_10_21	LVL_10_21	PER_9_21	LVL_9_21
F3	243	PER_16_21	LVL_16_21	PER_15_21	LVL_15_21	PER_14_21	LVL_14_21	PER_13_21	LVL_13_21
F4	244	PER_4_22	LVL_4_22	PER_3_22	LVL_3_22	PER_2_22	LVL_2_22	PER_1_22	LVL_1_22
F5	245	PER_8_22	LVL_8_22	PER_7_22	LVL_7_22	PER_6_22	LVL_6_22	PER_5_22	LVL_5_22
F6	246	PER_12_22	LVL_12_22	PER_11_22	LVL_11_22	PER_10_22	LVL_10_22	PER_9_22	LVL_9_22
F7	247	PER_16_22	LVL_16_22	PER_15_22	LVL_15_22	PER_14_22	LVL_14_22	PER_13_22	LVL_13_22
F8	248	PER_4_23	LVL_4_23	PER_3_23	LVL_3_23	PER_2_23	LVL_2_23	PER_1_23	LVL_1_23
F9	249	PER_8_23	LVL_8_23	PER_7_23	LVL_7_23	PER_6_23	LVL_6_23	PER_5_23	LVL_5_23
FA	250	PER_12_23	LVL_12_23	PER_11_23	LVL_11_23	PER_10_23	LVL_10_23	PER_9_23	LVL_9_23
FB	251	PER_16_23	LVL_16_23	PER_15_23	LVL_15_23	PER_14_23	LVL_14_23	PER_13_23	LVL_13_23
FC	252	PER_4_24	LVL_4_24	PER_3_24	LVL_3_24	PER_2_24	LVL_2_24	PER_1_24	LVL_1_24
FD	253	PER_8_24	LVL_8_24	PER_7_24	LVL_7_24	PER_6_24	LVL_6_24	PER_5_24	LVL_5_24
FE	254	PER_12_24	LVL_12_24	PER_11_24	LVL_11_24	PER_10_24	LVL_10_24	PER_9_24	LVL_9_24
FF	255	PER_16_24	LVL_16_24	PER_15_24	LVL_15_24	PER_14_24	LVL_14_24	PER_13_24	LVL_13_24
100	256	PER_4_25	LVL_4_25	PER_3_25	LVL_3_25	PER_2_25	LVL_2_25	PER_1_25	LVL_1_25
101	257	PER_8_25	LVL_8_25	PER_7_25	LVL_7_25	PER_6_25	LVL_6_25	PER_5_25	LVL_5_25
102	258	PER_12_25	LVL_12_25	PER_11_25	LVL_11_25	PER_10_25	LVL_10_25	PER_9_25	LVL_9_25
103	259	PER_16_25	LVL_16_25	PER_15_25	LVL_15_25	PER_14_25	LVL_14_25	PER_13_25	LVL_13_25
104	260	PER_4_26	LVL_4_26	PER_3_26	LVL_3_26	PER_2_26	LVL_2_26	PER_1_26	LVL_1_26
105	261	PER_8_26	LVL_8_26	PER_7_26	LVL_7_26	PER_6_26	LVL_6_26	PER_5_26	LVL_5_26
106	262	PER_12_26	LVL_12_26	PER_11_26	LVL_11_26	PER_10_26	LVL_10_26	PER_9_26	LVL_9_26
107	263	PER_16_26	LVL_16_26	PER_15_26	LVL_15_26	PER_14_26	LVL_14_26	PER_13_26	LVL_13_26
108	264	PER_4_27	LVL_4_27	PER_3_27	LVL_3_27	PER_2_27	LVL_2_27	PER_1_27	LVL_1_27
109	265	PER_8_27	LVL_8_27	PER_7_27	LVL_7_27	PER_6_27	LVL_6_27	PER_5_27	LVL_5_27

Table 52. Pattern Profile Register Map for 3-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
10A	266	PER_12_27	LVL_12_27	PER_11_27	LVL_11_27	PER_10_27	LVL_10_27	PER_9_27	LVL_9_27
10B	267	PER_16_27	LVL_16_27	PER_15_27	LVL_15_27	PER_14_27	LVL_14_27	PER_13_27	LVL_13_27
10C	268	PER_4_28	LVL_4_28	PER_3_28	LVL_3_28	PER_2_28	LVL_2_28	PER_1_28	LVL_1_28
10D	269	PER_8_28	LVL_8_28	PER_7_28	LVL_7_28	PER_6_28	LVL_6_28	PER_5_28	LVL_5_28
10E	270	PER_12_28	LVL_12_28	PER_11_28	LVL_11_28	PER_10_28	LVL_10_28	PER_9_28	LVL_9_28
10F	271	PER_16_28	LVL_16_28	PER_15_28	LVL_15_28	PER_14_28	LVL_14_28	PER_13_28	LVL_13_28
110	272	PER_4_29	LVL_4_29	PER_3_29	LVL_3_29	PER_2_29	LVL_2_29	PER_1_29	LVL_1_29
111	273	PER_8_29	LVL_8_29	PER_7_29	LVL_7_29	PER_6_29	LVL_6_29	PER_5_29	LVL_5_29
112	274	PER_12_29	LVL_12_29	PER_11_29	LVL_11_29	PER_10_29	LVL_10_29	PER_9_29	LVL_9_29
113	275	PER_16_29	LVL_16_29	PER_15_29	LVL_15_29	PER_14_29	LVL_14_29	PER_13_29	LVL_13_29
114	276	PER_4_30	LVL_4_30	PER_3_30	LVL_3_30	PER_2_30	LVL_2_30	PER_1_30	LVL_1_30
115	277	PER_8_30	LVL_8_30	PER_7_30	LVL_7_30	PER_6_30	LVL_6_30	PER_5_30	LVL_5_30
116	278	PER_12_30	LVL_12_30	PER_11_30	LVL_11_30	PER_10_30	LVL_10_30	PER_9_30	LVL_9_30
117	279	PER_16_30	LVL_16_30	PER_15_30	LVL_15_30	PER_14_30	LVL_14_30	PER_13_30	LVL_13_30
118	280	PER_4_31	LVL_4_31	PER_3_31	LVL_3_31	PER_2_31	LVL_2_31	PER_1_31	LVL_1_31
119	281	PER_8_31	LVL_8_31	PER_7_31	LVL_7_31	PER_6_31	LVL_6_31	PER_5_31	LVL_5_31
11A	282	PER_12_31	LVL_12_31	PER_11_31	LVL_11_31	PER_10_31	LVL_10_31	PER_9_31	LVL_9_31
11B	283	PER_16_31	LVL_16_31	PER_15_31	LVL_15_31	PER_14_31	LVL_14_31	PER_13_31	LVL_13_31
11C	284	PER_4_32	LVL_4_32	PER_3_32	LVL_3_32	PER_2_32	LVL_2_32	PER_1_32	LVL_1_32
11D	285	PER_8_32	LVL_8_32	PER_7_32	LVL_7_32	PER_6_32	LVL_6_32	PER_5_32	LVL_5_32
11E	286	PER_12_32	LVL_12_32	PER_11_32	LVL_11_32	PER_10_32	LVL_10_32	PER_9_32	LVL_9_32
11F	287	PER_16_32	LVL_16_32	PER_15_32	LVL_15_32	PER_14_32	LVL_14_32	PER_13_32	LVL_13_32
120	288	PER_4_33	LVL_4_33	PER_3_33	LVL_3_33	PER_2_33	LVL_2_33	PER_1_33	LVL_1_33
121	289	PER_8_33	LVL_8_33	PER_7_33	LVL_7_33	PER_6_33	LVL_6_33	PER_5_33	LVL_5_33
122	290	PER_12_33	LVL_12_33	PER_11_33	LVL_11_33	PER_10_33	LVL_10_33	PER_9_33	LVL_9_33
123	291	PER_16_33	LVL_16_33	PER_15_33	LVL_15_33	PER_14_33	LVL_14_33	PER_13_33	LVL_13_33
124	292	PER_4_34	LVL_4_34	PER_3_34	LVL_3_34	PER_2_34	LVL_2_34	PER_1_34	LVL_1_34
125	293	PER_8_34	LVL_8_34	PER_7_34	LVL_7_34	PER_6_34	LVL_6_34	PER_5_34	LVL_5_34
126	294	PER_12_34	LVL_12_34	PER_11_34	LVL_11_34	PER_10_34	LVL_10_34	PER_9_34	LVL_9_34
127	295	PER_16_34	LVL_16_34	PER_15_34	LVL_15_34	PER_14_34	LVL_14_34	PER_13_34	LVL_13_34
128	296	PER_4_35	LVL_4_35	PER_3_35	LVL_3_35	PER_2_35	LVL_2_35	PER_1_35	LVL_1_35
129	297	PER_8_35	LVL_8_35	PER_7_35	LVL_7_35	PER_6_35	LVL_6_35	PER_5_35	LVL_5_35
12A	298	PER_12_35	LVL_12_35	PER_11_35	LVL_11_35	PER_10_35	LVL_10_35	PER_9_35	LVL_9_35
12B	299	PER_16_35	LVL_16_35	PER_15_35	LVL_15_35	PER_14_35	LVL_14_35	PER_13_35	LVL_13_35
12C	300	PER_4_36	LVL_4_36	PER_3_36	LVL_3_36	PER_2_36	LVL_2_36	PER_1_36	LVL_1_36
12D	301	PER_8_36	LVL_8_36	PER_7_36	LVL_7_36	PER_6_36	LVL_6_36	PER_5_36	LVL_5_36
12E	302	PER_12_36	LVL_12_36	PER_11_36	LVL_11_36	PER_10_36	LVL_10_36	PER_9_36	LVL_9_36
12F	303	PER_16_36	LVL_16_36	PER_15_36	LVL_15_36	PER_14_36	LVL_14_36	PER_13_36	LVL_13_36
130	304	PER_4_37	LVL_4_37	PER_3_37	LVL_3_37	PER_2_37	LVL_2_37	PER_1_37	LVL_1_37
131	305	PER_8_37	LVL_8_37	PER_7_37	LVL_7_37	PER_6_37	LVL_6_37	PER_5_37	LVL_5_37
132	306	PER_12_37	LVL_12_37	PER_11_37	LVL_11_37	PER_10_37	LVL_10_37	PER_9_37	LVL_9_37
133	307	PER_16_37	LVL_16_37	PER_15_37	LVL_15_37	PER_14_37	LVL_14_37	PER_13_37	LVL_13_37
134	308	PER_4_38	LVL_4_38	PER_3_38	LVL_3_38	PER_2_38	LVL_2_38	PER_1_38	LVL_1_38
135	309	PER_8_38	LVL_8_38	PER_7_38	LVL_7_38	PER_6_38	LVL_6_38	PER_5_38	LVL_5_38
136	310	PER_12_38	LVL_12_38	PER_11_38	LVL_11_38	PER_10_38	LVL_10_38	PER_9_38	LVL_9_38
137	311	PER_16_38	LVL_16_38	PER_15_38	LVL_15_38	PER_14_38	LVL_14_38	PER_13_38	LVL_13_38
138	312	PER_4_39	LVL_4_39	PER_3_39	LVL_3_39	PER_2_39	LVL_2_39	PER_1_39	LVL_1_39
139	313	PER_8_39	LVL_8_39	PER_7_39	LVL_7_39	PER_6_39	LVL_6_39	PER_5_39	LVL_5_39
13A	314	PER_12_39	LVL_12_39	PER_11_39	LVL_11_39	PER_10_39	LVL_10_39	PER_9_39	LVL_9_39
13B	315	PER_16_39	LVL_16_39	PER_15_39	LVL_15_39	PER_14_39	LVL_14_39	PER_13_39	LVL_13_39
13C	316	PER_4_40	LVL_4_40	PER_3_40	LVL_3_40	PER_2_40	LVL_2_40	PER_1_40	LVL_1_40
13D	317	PER_8_40	LVL_8_40	PER_7_40	LVL_7_40	PER_6_40	LVL_6_40	PER_5_40	LVL_5_40
13E	318	PER_12_40	LVL_12_40	PER_11_40	LVL_11_40	PER_10_40	LVL_10_40	PER_9_40	LVL_9_40
13F	319	PER_16_40	LVL_16_40	PER_15_40	LVL_15_40	PER_14_40	LVL_14_40	PER_13_40	LVL_13_40

Table 52. Pattern Profile Register Map for 3-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Dec	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
140	320	PER_4_41	LVL_4_41	PER_3_41	LVL_3_41	PER_2_41	LVL_2_41	PER_1_41	LVL_1_41
141	321	PER_8_41	LVL_8_41	PER_7_41	LVL_7_41	PER_6_41	LVL_6_41	PER_5_41	LVL_5_41
142	322	PER_12_41	LVL_12_41	PER_11_41	LVL_11_41	PER_10_41	LVL_10_41	PER_9_41	LVL_9_41
143	323	PER_16_41	LVL_16_41	PER_15_41	LVL_15_41	PER_14_41	LVL_14_41	PER_13_41	LVL_13_41
144	324	PER_4_42	LVL_4_42	PER_3_42	LVL_3_42	PER_2_42	LVL_2_42	PER_1_42	LVL_1_42
145	325	PER_8_42	LVL_8_42	PER_7_42	LVL_7_42	PER_6_42	LVL_6_42	PER_5_42	LVL_5_42
146	326	PER_12_42	LVL_12_42	PER_11_42	LVL_11_42	PER_10_42	LVL_10_42	PER_9_42	LVL_9_42
147	327	PER_16_42	LVL_16_42	PER_15_42	LVL_15_42	PER_14_42	LVL_14_42	PER_13_42	LVL_13_42
148	328	PER_4_43	LVL_4_43	PER_3_43	LVL_3_43	PER_2_43	LVL_2_43	PER_1_43	LVL_1_43
149	329	PER_8_43	LVL_8_43	PER_7_43	LVL_7_43	PER_6_43	LVL_6_43	PER_5_43	LVL_5_43
14A	330	PER_12_43	LVL_12_43	PER_11_43	LVL_11_43	PER_10_43	LVL_10_43	PER_9_43	LVL_9_43
14B	331	PER_16_43	LVL_16_43	PER_15_43	LVL_15_43	PER_14_43	LVL_14_43	PER_13_43	LVL_13_43
14C	332	PER_4_44	LVL_4_44	PER_3_44	LVL_3_44	PER_2_44	LVL_2_44	PER_1_44	LVL_1_44
14D	333	PER_8_44	LVL_8_44	PER_7_44	LVL_7_44	PER_6_44	LVL_6_44	PER_5_44	LVL_5_44
14E	334	PER_12_44	LVL_12_44	PER_11_44	LVL_11_44	PER_10_44	LVL_10_44	PER_9_44	LVL_9_44
14F	335	PER_16_44	LVL_16_44	PER_15_44	LVL_15_44	PER_14_44	LVL_14_44	PER_13_44	LVL_13_44
150	336	PER_4_45	LVL_4_45	PER_3_45	LVL_3_45	PER_2_45	LVL_2_45	PER_1_45	LVL_1_45
151	337	PER_8_45	LVL_8_45	PER_7_45	LVL_7_45	PER_6_45	LVL_6_45	PER_5_45	LVL_5_45
152	338	PER_12_45	LVL_12_45	PER_11_45	LVL_11_45	PER_10_45	LVL_10_45	PER_9_45	LVL_9_45
153	339	PER_16_45	LVL_16_45	PER_15_45	LVL_15_45	PER_14_45	LVL_14_45	PER_13_45	LVL_13_45
154	340	PER_4_46	LVL_4_46	PER_3_46	LVL_3_46	PER_2_46	LVL_2_46	PER_1_46	LVL_1_46
155	341	PER_8_46	LVL_8_46	PER_7_46	LVL_7_46	PER_6_46	LVL_6_46	PER_5_46	LVL_5_46
156	342	PER_12_46	LVL_12_46	PER_11_46	LVL_11_46	PER_10_46	LVL_10_46	PER_9_46	LVL_9_46
157	343	PER_16_46	LVL_16_46	PER_15_46	LVL_15_46	PER_14_46	LVL_14_46	PER_13_46	LVL_13_46
158	344	PER_4_47	LVL_4_47	PER_3_47	LVL_3_47	PER_2_47	LVL_2_47	PER_1_47	LVL_1_47
159	345	PER_8_47	LVL_8_47	PER_7_47	LVL_7_47	PER_6_47	LVL_6_47	PER_5_47	LVL_5_47
15A	346	PER_12_47	LVL_12_47	PER_11_47	LVL_11_47	PER_10_47	LVL_10_47	PER_9_47	LVL_9_47
15B	347	PER_16_47	LVL_16_47	PER_15_47	LVL_15_47	PER_14_47	LVL_14_47	PER_13_47	LVL_13_47
15C	348	PER_4_48	LVL_4_48	PER_3_48	LVL_3_48	PER_2_48	LVL_2_48	PER_1_48	LVL_1_48
15D	349	PER_8_48	LVL_8_48	PER_7_48	LVL_7_48	PER_6_48	LVL_6_48	PER_5_48	LVL_5_48
15E	350	PER_12_48	LVL_12_48	PER_11_48	LVL_11_48	PER_10_48	LVL_10_48	PER_9_48	LVL_9_48
15F	351	PER_16_48	LVL_16_48	PER_15_48	LVL_15_48	PER_14_48	LVL_14_48	PER_13_48	LVL_13_48

8.6.6.1 Register A0h (offset = A0h) [reset = A0h]

Figure 90. Register A0h

31	30	29	28	27	26	25	24
PER_4_1						LVL_4_1	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
23	22	21	20	19	18	17	16
PER_3_1						LVL_3_1	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
15	14	13	12	11	10	9	8
PER_2_1						LVL_2_1	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
7	6	5	4	3	2	1	0
PER_1_1						LVL_1_1	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 53. Register A0h Field Descriptions

Bit	Field	Type	Reset	Description
31-27	PER_4_1	R/W	Undefined	Period value for 4th transition in pattern profile 1.
26-24	LVL_4_1	R/W	Undefined	Level value for 4th transition in pattern profile 1.
23-19	PER_3_1	R/W	Undefined	Period value for 3rd transition in pattern profile 1.
18-16	LVL_3_1	R/W	Undefined	Level value for 3rd transition in pattern profile 1.
15-11	PER_2_1	R/W	Undefined	Period value for 2nd transition in pattern profile 1.
10-8	LVL_2_1	R/W	Undefined	Level value for 2nd transition in pattern profile 1.
7-3	PER_1_1	R/W	Undefined	Period value for 1st transition in pattern profile 1.
2-0	LVL_1_1	R/W	Undefined	Level value for 1st transition in pattern profile 1.

8.6.6.2 Register A1h to 15Fh (offset = A1h to 15Fh) [reset = A1h to 15Fh]

In below table register field name are given as PER_x1_y, LVL_x1_y, PER_x2_y, LVL_x2_y, PER_x3_y, LVL_x3_y, PER_x4_y, and LVL_x4_y. Where x1, x2, x3 and x4 represents the transition number can vary from 1 to 16 and y represents profile number and can vary from 1 to 48 across register addresses in pattern profile register map.

Figure 91. Register A1h to 15Fh

31	30	29	28	27	26	25	24
PER_x1_y						LVL_x1_y	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
23	22	21	20	19	18	17	16
PER_x2_y						LVL_x2_y	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
15	14	13	12	11	10	9	8
PER_x3_y						LVL_x3_y	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
7	6	5	4	3	2	1	0
PER_x4_y						LVL_x4_y	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 54. Register A1h to 15Fh Field Descriptions

Bit	Field	Type	Reset	Description
31-27	PER_x1_y	R/W	Undefined	Period value for x1th transition in pattern profile y.
26-24	LVL_x1_y	R/W	Undefined	Level value for x1th transition in pattern profile y.

Table 54. Register A1h to 15Fh Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-19	PER_x2_y	R/W	Undefined	Period value for x2nd transition in pattern profile y.
18-16	LVL_x2_y	R/W	Undefined	Level value for x2nd transition in pattern profile y.
15-11	PER_x3_y	R/W	Undefined	Period value for x3rd transition in pattern profile y.
10-8	LVL_x3_y	R/W	Undefined	Level value for x3rd transition in pattern profile y.
7-3	PER_x4_y	R/W	Undefined	Period value for x4th transition in pattern profile y.
2-0	LVL_x4_y	R/W	Undefined	Level value for x4th transition in pattern profile y.

Table 55. Pattern Profile Register Map for 5-Level Mode

REGISTER ADDRESS		REGISTER DATA							
Hex	Decimal	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
60	96	PER_4_1	LVL_4_1	PER_3_1	LVL_3_1	PER_2_1	LVL_2_1	PER_1_1	LVL_1_1
61	97	PER_8_1	LVL_8_1	PER_7_1	LVL_7_1	PER_6_1	LVL_6_1	PER_5_1	LVL_5_1
62	98	PER_12_1	LVL_12_1	PER_11_1	LVL_11_1	PER_10_1	LVL_10_1	PER_9_1	LVL_9_1
63	99	PER_16_1	LVL_16_1	PER_15_1	LVL_15_1	PER_14_1	LVL_14_1	PER_13_1	LVL_13_1
64	100	PER_20_1	LVL_20_1	PER_19_1	LVL_19_1	PER_18_1	LVL_18_1	PER_17_1	LVL_17_1
65	101	PER_24_1	LVL_24_1	PER_23_1	LVL_23_1	PER_22_1	LVL_22_1	PER_21_1	LVL_21_1
66	102	PER_28_1	LVL_28_1	PER_27_1	LVL_27_1	PER_26_1	LVL_26_1	PER_25_1	LVL_25_1
67	103	PER_32_1	LVL_32_1	PER_31_1	LVL_31_1	PER_30_1	LVL_30_1	PER_29_1	LVL_29_1
68	104	PER_4_2	LVL_4_2	PER_3_2	LVL_3_2	PER_2_2	LVL_2_2	PER_1_2	LVL_1_2
69	105	PER_8_2	LVL_8_2	PER_7_2	LVL_7_2	PER_6_2	LVL_6_2	PER_5_2	LVL_5_2
6A	106	PER_12_2	LVL_12_2	PER_11_2	LVL_11_2	PER_10_2	LVL_10_2	PER_9_2	LVL_9_2
6B	107	PER_16_2	LVL_16_2	PER_15_2	LVL_15_2	PER_14_2	LVL_14_2	PER_13_2	LVL_13_2
6C	108	PER_20_2	LVL_20_2	PER_19_2	LVL_19_2	PER_18_2	LVL_18_2	PER_17_2	LVL_17_2
6D	109	PER_24_2	LVL_24_2	PER_23_2	LVL_23_2	PER_22_2	LVL_22_2	PER_21_2	LVL_21_2
6E	110	PER_28_2	LVL_28_2	PER_27_2	LVL_27_2	PER_26_2	LVL_26_2	PER_25_2	LVL_25_2
6F	111	PER_32_2	LVL_32_2	PER_31_2	LVL_31_2	PER_30_2	LVL_30_2	PER_29_2	LVL_29_2
70	112	PER_4_3	LVL_4_3	PER_3_3	LVL_3_3	PER_2_3	LVL_2_3	PER_1_3	LVL_1_3
71	113	PER_8_3	LVL_8_3	PER_7_3	LVL_7_3	PER_6_3	LVL_6_3	PER_5_3	LVL_5_3
72	114	PER_12_3	LVL_12_3	PER_11_3	LVL_11_3	PER_10_3	LVL_10_3	PER_9_3	LVL_9_3
73	115	PER_16_3	LVL_16_3	PER_15_3	LVL_15_3	PER_14_3	LVL_14_3	PER_13_3	LVL_13_3
74	116	PER_20_3	LVL_20_3	PER_19_3	LVL_19_3	PER_18_3	LVL_18_3	PER_17_3	LVL_17_3
75	117	PER_24_3	LVL_24_3	PER_23_3	LVL_23_3	PER_22_3	LVL_22_3	PER_21_3	LVL_21_3
76	118	PER_28_3	LVL_28_3	PER_27_3	LVL_27_3	PER_26_3	LVL_26_3	PER_25_3	LVL_25_3
77	119	PER_32_3	LVL_32_3	PER_31_3	LVL_31_3	PER_30_3	LVL_30_3	PER_29_3	LVL_29_3
78	120	PER_4_4	LVL_4_4	PER_3_4	LVL_3_4	PER_2_4	LVL_2_4	PER_1_4	LVL_1_4
79	121	PER_8_4	LVL_8_4	PER_7_4	LVL_7_4	PER_6_4	LVL_6_4	PER_5_4	LVL_5_4
7A	122	PER_12_4	LVL_12_4	PER_11_4	LVL_11_4	PER_10_4	LVL_10_4	PER_9_4	LVL_9_4
7B	123	PER_16_4	LVL_16_4	PER_15_4	LVL_15_4	PER_14_4	LVL_14_4	PER_13_4	LVL_13_4
7C	124	PER_20_4	LVL_20_4	PER_19_4	LVL_19_4	PER_18_4	LVL_18_4	PER_17_4	LVL_17_4
7D	125	PER_24_4	LVL_24_4	PER_23_4	LVL_23_4	PER_22_4	LVL_22_4	PER_21_4	LVL_21_4
7E	126	PER_28_4	LVL_28_4	PER_27_4	LVL_27_4	PER_26_4	LVL_26_4	PER_25_4	LVL_25_4
7F	127	PER_32_4	LVL_32_4	PER_31_4	LVL_31_4	PER_30_4	LVL_30_4	PER_29_4	LVL_29_4
80	128	PER_4_5	LVL_4_5	PER_3_5	LVL_3_5	PER_2_5	LVL_2_5	PER_1_5	LVL_1_5

Table 55. Pattern Profile Register Map for 5-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Decimal	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
81	129	PER_8_5	LVL_8_5	PER_7_5	LVL_7_5	PER_6_5	LVL_6_5	PER_5_5	LVL_5_5
82	130	PER_12_5	LVL_12_5	PER_11_5	LVL_11_5	PER_10_5	LVL_10_5	PER_9_5	LVL_9_5
83	131	PER_16_5	LVL_16_5	PER_15_5	LVL_15_5	PER_14_5	LVL_14_5	PER_13_5	LVL_13_5
84	132	PER_20_5	LVL_20_5	PER_19_5	LVL_19_5	PER_18_5	LVL_18_5	PER_17_5	LVL_17_5
85	133	PER_24_5	LVL_24_5	PER_23_5	LVL_23_5	PER_22_5	LVL_22_5	PER_21_5	LVL_21_5
86	134	PER_28_5	LVL_28_5	PER_27_5	LVL_27_5	PER_26_5	LVL_26_5	PER_25_5	LVL_25_5
87	135	PER_32_5	LVL_32_5	PER_31_5	LVL_31_5	PER_30_5	LVL_30_5	PER_29_5	LVL_29_5
88	136	PER_4_6	LVL_4_6	PER_3_6	LVL_3_6	PER_2_6	LVL_2_6	PER_1_6	LVL_1_6
89	137	PER_8_6	LVL_8_6	PER_7_6	LVL_7_6	PER_6_6	LVL_6_6	PER_5_6	LVL_5_6
8A	138	PER_12_6	LVL_12_6	PER_11_6	LVL_11_6	PER_10_6	LVL_10_6	PER_9_6	LVL_9_6
8B	139	PER_16_6	LVL_16_6	PER_15_6	LVL_15_6	PER_14_6	LVL_14_6	PER_13_6	LVL_13_6
8C	140	PER_20_6	LVL_20_6	PER_19_6	LVL_19_6	PER_18_6	LVL_18_6	PER_17_6	LVL_17_6
8D	141	PER_24_6	LVL_24_6	PER_23_6	LVL_23_6	PER_22_6	LVL_22_6	PER_21_6	LVL_21_6
8E	142	PER_28_6	LVL_28_6	PER_27_6	LVL_27_6	PER_26_6	LVL_26_6	PER_25_6	LVL_25_6
8F	143	PER_32_6	LVL_32_6	PER_31_6	LVL_31_6	PER_30_6	LVL_30_6	PER_29_6	LVL_29_6
90	144	PER_4_7	LVL_4_7	PER_3_7	LVL_3_7	PER_2_7	LVL_2_7	PER_1_7	LVL_1_7
91	145	PER_8_7	LVL_8_7	PER_7_7	LVL_7_7	PER_6_7	LVL_6_7	PER_5_7	LVL_5_7
92	146	PER_12_7	LVL_12_7	PER_11_7	LVL_11_7	PER_10_7	LVL_10_7	PER_9_7	LVL_9_7
93	147	PER_16_7	LVL_16_7	PER_15_7	LVL_15_7	PER_14_7	LVL_14_7	PER_13_7	LVL_13_7
94	148	PER_20_7	LVL_20_7	PER_19_7	LVL_19_7	PER_18_7	LVL_18_7	PER_17_7	LVL_17_7
95	149	PER_24_7	LVL_24_7	PER_23_7	LVL_23_7	PER_22_7	LVL_22_7	PER_21_7	LVL_21_7
96	150	PER_28_7	LVL_28_7	PER_27_7	LVL_27_7	PER_26_7	LVL_26_7	PER_25_7	LVL_25_7
97	151	PER_32_7	LVL_32_7	PER_31_7	LVL_31_7	PER_30_7	LVL_30_7	PER_29_7	LVL_29_7
98	152	PER_4_8	LVL_4_8	PER_3_8	LVL_3_8	PER_2_8	LVL_2_8	PER_1_8	LVL_1_8
99	153	PER_8_8	LVL_8_8	PER_7_8	LVL_7_8	PER_6_8	LVL_6_8	PER_5_8	LVL_5_8
9A	154	PER_12_8	LVL_12_8	PER_11_8	LVL_11_8	PER_10_8	LVL_10_8	PER_9_8	LVL_9_8
9B	155	PER_16_8	LVL_16_8	PER_15_8	LVL_15_8	PER_14_8	LVL_14_8	PER_13_8	LVL_13_8
9C	156	PER_20_8	LVL_20_8	PER_19_8	LVL_19_8	PER_18_8	LVL_18_8	PER_17_8	LVL_17_8
9D	157	PER_24_8	LVL_24_8	PER_23_8	LVL_23_8	PER_22_8	LVL_22_8	PER_21_8	LVL_21_8
9E	158	PER_28_8	LVL_28_8	PER_27_8	LVL_27_8	PER_26_8	LVL_26_8	PER_25_8	LVL_25_8
9F	159	PER_32_8	LVL_32_8	PER_31_8	LVL_31_8	PER_30_8	LVL_30_8	PER_29_8	LVL_29_8
A0	160	PER_4_9	LVL_4_9	PER_3_9	LVL_3_9	PER_2_9	LVL_2_9	PER_1_9	LVL_1_9
A1	161	PER_8_9	LVL_8_9	PER_7_9	LVL_7_9	PER_6_9	LVL_6_9	PER_5_9	LVL_5_9
A2	162	PER_12_9	LVL_12_9	PER_11_9	LVL_11_9	PER_10_9	LVL_10_9	PER_9_9	LVL_9_9
A3	163	PER_16_9	LVL_16_9	PER_15_9	LVL_15_9	PER_14_9	LVL_14_9	PER_13_9	LVL_13_9
A4	164	PER_20_9	LVL_20_9	PER_19_9	LVL_19_9	PER_18_9	LVL_18_9	PER_17_9	LVL_17_9
A5	165	PER_24_9	LVL_24_9	PER_23_9	LVL_23_9	PER_22_9	LVL_22_9	PER_21_9	LVL_21_9
A6	166	PER_28_9	LVL_28_9	PER_27_9	LVL_27_9	PER_26_9	LVL_26_9	PER_25_9	LVL_25_9
A7	167	PER_32_9	LVL_32_9	PER_31_9	LVL_31_9	PER_30_9	LVL_30_9	PER_29_9	LVL_29_9
A8	168	PER_4_10	LVL_4_10	PER_3_10	LVL_3_10	PER_2_10	LVL_2_10	PER_1_10	LVL_1_10
A9	169	PER_8_10	LVL_8_10	PER_7_10	LVL_7_10	PER_6_10	LVL_6_10	PER_5_10	LVL_5_10
AA	170	PER_12_10	LVL_12_10	PER_11_10	LVL_11_10	PER_10_10	LVL_10_10	PER_9_10	LVL_9_10
AB	171	PER_16_10	LVL_16_10	PER_15_10	LVL_15_10	PER_14_10	LVL_14_10	PER_13_10	LVL_13_10
AC	172	PER_20_10	LVL_20_10	PER_19_10	LVL_19_10	PER_18_10	LVL_18_10	PER_17_10	LVL_17_10
AD	173	PER_24_10	LVL_24_10	PER_23_10	LVL_23_10	PER_22_10	LVL_22_10	PER_21_10	LVL_21_10
AE	174	PER_28_10	LVL_28_10	PER_27_10	LVL_27_10	PER_26_10	LVL_26_10	PER_25_10	LVL_25_10
AF	175	PER_32_10	LVL_32_10	PER_31_10	LVL_31_10	PER_30_10	LVL_30_10	PER_29_10	LVL_29_10
B0	176	PER_4_11	LVL_4_11	PER_3_11	LVL_3_11	PER_2_11	LVL_2_11	PER_1_11	LVL_1_11
B1	177	PER_8_11	LVL_8_11	PER_7_11	LVL_7_11	PER_6_11	LVL_6_11	PER_5_11	LVL_5_11
B2	178	PER_12_11	LVL_12_11	PER_11_11	LVL_11_11	PER_10_11	LVL_10_11	PER_9_11	LVL_9_11
B3	179	PER_16_11	LVL_16_11	PER_15_11	LVL_15_11	PER_14_11	LVL_14_11	PER_13_11	LVL_13_11
B4	180	PER_20_11	LVL_20_11	PER_19_11	LVL_19_11	PER_18_11	LVL_18_11	PER_17_11	LVL_17_11
B5	181	PER_24_11	LVL_24_11	PER_23_11	LVL_23_11	PER_22_11	LVL_22_11	PER_21_11	LVL_21_11
B6	182	PER_28_11	LVL_28_11	PER_27_11	LVL_27_11	PER_26_11	LVL_26_11	PER_25_11	LVL_25_11

Table 55. Pattern Profile Register Map for 5-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Decimal	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
B7	183	PER_32_11	LVL_32_11	PER_31_11	LVL_31_11	PER_30_11	LVL_30_11	PER_29_11	LVL_29_11
B8	184	PER_4_12	LVL_4_12	PER_3_12	LVL_3_12	PER_2_12	LVL_2_12	PER_1_12	LVL_1_12
B9	185	PER_8_12	LVL_8_12	PER_7_12	LVL_7_12	PER_6_12	LVL_6_12	PER_5_12	LVL_5_12
BA	186	PER_12_12	LVL_12_12	PER_11_12	LVL_11_12	PER_10_12	LVL_10_12	PER_9_12	LVL_9_12
BB	187	PER_16_12	LVL_16_12	PER_15_12	LVL_15_12	PER_14_12	LVL_14_12	PER_13_12	LVL_13_12
BC	188	PER_20_12	LVL_20_12	PER_19_12	LVL_19_12	PER_18_12	LVL_18_12	PER_17_12	LVL_17_12
BD	189	PER_24_12	LVL_24_12	PER_23_12	LVL_23_12	PER_22_12	LVL_22_12	PER_21_12	LVL_21_12
BE	190	PER_28_12	LVL_28_12	PER_27_12	LVL_27_12	PER_26_12	LVL_26_12	PER_25_12	LVL_25_12
BF	191	PER_32_12	LVL_32_12	PER_31_12	LVL_31_12	PER_30_12	LVL_30_12	PER_29_12	LVL_29_12
C0	192	PER_4_13	LVL_4_13	PER_3_13	LVL_3_13	PER_2_13	LVL_2_13	PER_1_13	LVL_1_13
C1	193	PER_8_13	LVL_8_13	PER_7_13	LVL_7_13	PER_6_13	LVL_6_13	PER_5_13	LVL_5_13
C2	194	PER_12_13	LVL_12_13	PER_11_13	LVL_11_13	PER_10_13	LVL_10_13	PER_9_13	LVL_9_13
C3	195	PER_16_13	LVL_16_13	PER_15_13	LVL_15_13	PER_14_13	LVL_14_13	PER_13_13	LVL_13_13
C4	196	PER_20_13	LVL_20_13	PER_19_13	LVL_19_13	PER_18_13	LVL_18_13	PER_17_13	LVL_17_13
C5	197	PER_24_13	LVL_24_13	PER_23_13	LVL_23_13	PER_22_13	LVL_22_13	PER_21_13	LVL_21_13
C6	198	PER_28_13	LVL_28_13	PER_27_13	LVL_27_13	PER_26_13	LVL_26_13	PER_25_13	LVL_25_13
C7	199	PER_32_13	LVL_32_13	PER_31_13	LVL_31_13	PER_30_13	LVL_30_13	PER_29_13	LVL_29_13
C8	200	PER_4_14	LVL_4_14	PER_3_14	LVL_3_14	PER_2_14	LVL_2_14	PER_1_14	LVL_1_14
C9	201	PER_8_14	LVL_8_14	PER_7_14	LVL_7_14	PER_6_14	LVL_6_14	PER_5_14	LVL_5_14
CA	202	PER_12_14	LVL_12_14	PER_11_14	LVL_11_14	PER_10_14	LVL_10_14	PER_9_14	LVL_9_14
CB	203	PER_16_14	LVL_16_14	PER_15_14	LVL_15_14	PER_14_14	LVL_14_14	PER_13_14	LVL_13_14
CC	204	PER_20_14	LVL_20_14	PER_19_14	LVL_19_14	PER_18_14	LVL_18_14	PER_17_14	LVL_17_14
CD	205	PER_24_14	LVL_24_14	PER_23_14	LVL_23_14	PER_22_14	LVL_22_14	PER_21_14	LVL_21_14
CE	206	PER_28_14	LVL_28_14	PER_27_14	LVL_27_14	PER_26_14	LVL_26_14	PER_25_14	LVL_25_14
CF	207	PER_32_14	LVL_32_14	PER_31_14	LVL_31_14	PER_30_14	LVL_30_14	PER_29_14	LVL_29_14
D0	208	PER_4_15	LVL_4_15	PER_3_15	LVL_3_15	PER_2_15	LVL_2_15	PER_1_15	LVL_1_15
D1	209	PER_8_15	LVL_8_15	PER_7_15	LVL_7_15	PER_6_15	LVL_6_15	PER_5_15	LVL_5_15
D2	210	PER_12_15	LVL_12_15	PER_11_15	LVL_11_15	PER_10_15	LVL_10_15	PER_9_15	LVL_9_15
D3	211	PER_16_15	LVL_16_15	PER_15_15	LVL_15_15	PER_14_15	LVL_14_15	PER_13_15	LVL_13_15
D4	212	PER_20_15	LVL_20_15	PER_19_15	LVL_19_15	PER_18_15	LVL_18_15	PER_17_15	LVL_17_15
D5	213	PER_24_15	LVL_24_15	PER_23_15	LVL_23_15	PER_22_15	LVL_22_15	PER_21_15	LVL_21_15
D6	214	PER_28_15	LVL_28_15	PER_27_15	LVL_27_15	PER_26_15	LVL_26_15	PER_25_15	LVL_25_15
D7	215	PER_32_15	LVL_32_15	PER_31_15	LVL_31_15	PER_30_15	LVL_30_15	PER_29_15	LVL_29_15
D8	216	PER_4_16	LVL_4_16	PER_3_16	LVL_3_16	PER_2_16	LVL_2_16	PER_1_16	LVL_1_16
D9	217	PER_8_16	LVL_8_16	PER_7_16	LVL_7_16	PER_6_16	LVL_6_16	PER_5_16	LVL_5_16
DA	218	PER_12_16	LVL_12_16	PER_11_16	LVL_11_16	PER_10_16	LVL_10_16	PER_9_16	LVL_9_16
DB	219	PER_16_16	LVL_16_16	PER_15_16	LVL_15_16	PER_14_16	LVL_14_16	PER_13_16	LVL_13_16
DC	220	PER_20_16	LVL_20_16	PER_19_16	LVL_19_16	PER_18_16	LVL_18_16	PER_17_16	LVL_17_16
DD	221	PER_24_16	LVL_24_16	PER_23_16	LVL_23_16	PER_22_16	LVL_22_16	PER_21_16	LVL_21_16
DE	222	PER_28_16	LVL_28_16	PER_27_16	LVL_27_16	PER_26_16	LVL_26_16	PER_25_16	LVL_25_16
DF	223	PER_32_16	LVL_32_16	PER_31_16	LVL_31_16	PER_30_16	LVL_30_16	PER_29_16	LVL_29_16
E0	224	PER_4_17	LVL_4_17	PER_3_17	LVL_3_17	PER_2_17	LVL_2_17	PER_1_17	LVL_1_17
E1	225	PER_8_17	LVL_8_17	PER_7_17	LVL_7_17	PER_6_17	LVL_6_17	PER_5_17	LVL_5_17
E2	226	PER_12_17	LVL_12_17	PER_11_17	LVL_11_17	PER_10_17	LVL_10_17	PER_9_17	LVL_9_17
E3	227	PER_16_17	LVL_16_17	PER_15_17	LVL_15_17	PER_14_17	LVL_14_17	PER_13_17	LVL_13_17
E4	228	PER_20_17	LVL_20_17	PER_19_17	LVL_19_17	PER_18_17	LVL_18_17	PER_17_17	LVL_17_17
E5	229	PER_24_17	LVL_24_17	PER_23_17	LVL_23_17	PER_22_17	LVL_22_17	PER_21_17	LVL_21_17
E6	230	PER_28_17	LVL_28_17	PER_27_17	LVL_27_17	PER_26_17	LVL_26_17	PER_25_17	LVL_25_17
E7	231	PER_32_17	LVL_32_17	PER_31_17	LVL_31_17	PER_30_17	LVL_30_17	PER_29_17	LVL_29_17
E8	232	PER_4_18	LVL_4_18	PER_3_18	LVL_3_18	PER_2_18	LVL_2_18	PER_1_18	LVL_1_18
E9	233	PER_8_18	LVL_8_18	PER_7_18	LVL_7_18	PER_6_18	LVL_6_18	PER_5_18	LVL_5_18
EA	234	PER_12_18	LVL_12_18	PER_11_18	LVL_11_18	PER_10_18	LVL_10_18	PER_9_18	LVL_9_18
EB	235	PER_16_18	LVL_16_18	PER_15_18	LVL_15_18	PER_14_18	LVL_14_18	PER_13_18	LVL_13_18
EC	236	PER_20_18	LVL_20_18	PER_19_18	LVL_19_18	PER_18_18	LVL_18_18	PER_17_18	LVL_17_18

Table 55. Pattern Profile Register Map for 5-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Decimal	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
ED	237	PER_24_18	LVL_24_18	PER_23_18	LVL_23_18	PER_22_18	LVL_22_18	PER_21_18	LVL_21_18
EE	238	PER_28_18	LVL_28_18	PER_27_18	LVL_27_18	PER_26_18	LVL_26_18	PER_25_18	LVL_25_18
EF	239	PER_32_18	LVL_32_18	PER_31_18	LVL_31_18	PER_30_18	LVL_30_18	PER_29_18	LVL_29_18
F0	240	PER_4_19	LVL_4_19	PER_3_19	LVL_3_19	PER_2_19	LVL_2_19	PER_1_19	LVL_1_19
F1	241	PER_8_19	LVL_8_19	PER_7_19	LVL_7_19	PER_6_19	LVL_6_19	PER_5_19	LVL_5_19
F2	242	PER_12_19	LVL_12_19	PER_11_19	LVL_11_19	PER_10_19	LVL_10_19	PER_9_19	LVL_9_19
F3	243	PER_16_19	LVL_16_19	PER_15_19	LVL_15_19	PER_14_19	LVL_14_19	PER_13_19	LVL_13_19
F4	244	PER_20_19	LVL_20_19	PER_19_19	LVL_19_19	PER_18_19	LVL_18_19	PER_17_19	LVL_17_19
F5	245	PER_24_19	LVL_24_19	PER_23_19	LVL_23_19	PER_22_19	LVL_22_19	PER_21_19	LVL_21_19
F6	246	PER_28_19	LVL_28_19	PER_27_19	LVL_27_19	PER_26_19	LVL_26_19	PER_25_19	LVL_25_19
F7	247	PER_32_19	LVL_32_19	PER_31_19	LVL_31_19	PER_30_19	LVL_30_19	PER_29_19	LVL_29_19
F8	248	PER_4_20	LVL_4_20	PER_3_20	LVL_3_20	PER_2_20	LVL_2_20	PER_1_20	LVL_1_20
F9	249	PER_8_20	LVL_8_20	PER_7_20	LVL_7_20	PER_6_20	LVL_6_20	PER_5_20	LVL_5_20
FA	250	PER_12_20	LVL_12_20	PER_11_20	LVL_11_20	PER_10_20	LVL_10_20	PER_9_20	LVL_9_20
FB	251	PER_16_20	LVL_16_20	PER_15_20	LVL_15_20	PER_14_20	LVL_14_20	PER_13_20	LVL_13_20
FC	252	PER_20_20	LVL_20_20	PER_19_20	LVL_19_20	PER_18_20	LVL_18_20	PER_17_20	LVL_17_20
FD	253	PER_24_20	LVL_24_20	PER_23_20	LVL_23_20	PER_22_20	LVL_22_20	PER_21_20	LVL_21_20
FE	254	PER_28_20	LVL_28_20	PER_27_20	LVL_27_20	PER_26_20	LVL_26_20	PER_25_20	LVL_25_20
FF	255	PER_32_20	LVL_32_20	PER_31_20	LVL_31_20	PER_30_20	LVL_30_20	PER_29_20	LVL_29_20
100	256	PER_4_21	LVL_4_21	PER_3_21	LVL_3_21	PER_2_21	LVL_2_21	PER_1_21	LVL_1_21
101	257	PER_8_21	LVL_8_21	PER_7_21	LVL_7_21	PER_6_21	LVL_6_21	PER_5_21	LVL_5_21
102	258	PER_12_21	LVL_12_21	PER_11_21	LVL_11_21	PER_10_21	LVL_10_21	PER_9_21	LVL_9_21
103	259	PER_16_21	LVL_16_21	PER_15_21	LVL_15_21	PER_14_21	LVL_14_21	PER_13_21	LVL_13_21
104	260	PER_20_21	LVL_20_21	PER_19_21	LVL_19_21	PER_18_21	LVL_18_21	PER_17_21	LVL_17_21
105	261	PER_24_21	LVL_24_21	PER_23_21	LVL_23_21	PER_22_21	LVL_22_21	PER_21_21	LVL_21_21
106	262	PER_28_21	LVL_28_21	PER_27_21	LVL_27_21	PER_26_21	LVL_26_21	PER_25_21	LVL_25_21
107	263	PER_32_21	LVL_32_21	PER_31_21	LVL_31_21	PER_30_21	LVL_30_21	PER_29_21	LVL_29_21
108	264	PER_4_22	LVL_4_22	PER_3_22	LVL_3_22	PER_2_22	LVL_2_22	PER_1_22	LVL_1_22
109	265	PER_8_22	LVL_8_22	PER_7_22	LVL_7_22	PER_6_22	LVL_6_22	PER_5_22	LVL_5_22
10A	266	PER_12_22	LVL_12_22	PER_11_22	LVL_11_22	PER_10_22	LVL_10_22	PER_9_22	LVL_9_22
10B	267	PER_16_22	LVL_16_22	PER_15_22	LVL_15_22	PER_14_22	LVL_14_22	PER_13_22	LVL_13_22
10C	268	PER_20_22	LVL_20_22	PER_19_22	LVL_19_22	PER_18_22	LVL_18_22	PER_17_22	LVL_17_22
10D	269	PER_24_22	LVL_24_22	PER_23_22	LVL_23_22	PER_22_22	LVL_22_22	PER_21_22	LVL_21_22
10E	270	PER_28_22	LVL_28_22	PER_27_22	LVL_27_22	PER_26_22	LVL_26_22	PER_25_22	LVL_25_22
10F	271	PER_32_22	LVL_32_22	PER_31_22	LVL_31_22	PER_30_22	LVL_30_22	PER_29_22	LVL_29_22
110	272	PER_4_23	LVL_4_23	PER_3_23	LVL_3_23	PER_2_23	LVL_2_23	PER_1_23	LVL_1_23
111	273	PER_8_23	LVL_8_23	PER_7_23	LVL_7_23	PER_6_23	LVL_6_23	PER_5_23	LVL_5_23
112	274	PER_12_23	LVL_12_23	PER_11_23	LVL_11_23	PER_10_23	LVL_10_23	PER_9_23	LVL_9_23
113	275	PER_16_23	LVL_16_23	PER_15_23	LVL_15_23	PER_14_23	LVL_14_23	PER_13_23	LVL_13_23
114	276	PER_20_23	LVL_20_23	PER_19_23	LVL_19_23	PER_18_23	LVL_18_23	PER_17_23	LVL_17_23
115	277	PER_24_23	LVL_24_23	PER_23_23	LVL_23_23	PER_22_23	LVL_22_23	PER_21_23	LVL_21_23
116	278	PER_28_23	LVL_28_23	PER_27_23	LVL_27_23	PER_26_23	LVL_26_23	PER_25_23	LVL_25_23
117	279	PER_32_23	LVL_32_23	PER_31_23	LVL_31_23	PER_30_23	LVL_30_23	PER_29_23	LVL_29_23
118	280	PER_4_24	LVL_4_24	PER_3_24	LVL_3_24	PER_2_24	LVL_2_24	PER_1_24	LVL_1_24
119	281	PER_8_24	LVL_8_24	PER_7_24	LVL_7_24	PER_6_24	LVL_6_24	PER_5_24	LVL_5_24
11A	282	PER_12_24	LVL_12_24	PER_11_24	LVL_11_24	PER_10_24	LVL_10_24	PER_9_24	LVL_9_24
11B	283	PER_16_24	LVL_16_24	PER_15_24	LVL_15_24	PER_14_24	LVL_14_24	PER_13_24	LVL_13_24
11C	284	PER_20_24	LVL_20_24	PER_19_24	LVL_19_24	PER_18_24	LVL_18_24	PER_17_24	LVL_17_24
11D	285	PER_24_24	LVL_24_24	PER_23_24	LVL_23_24	PER_22_24	LVL_22_24	PER_21_24	LVL_21_24
11E	286	PER_28_24	LVL_28_24	PER_27_24	LVL_27_24	PER_26_24	LVL_26_24	PER_25_24	LVL_25_24
11F	287	PER_32_24	LVL_32_24	PER_31_24	LVL_31_24	PER_30_24	LVL_30_24	PER_29_24	LVL_29_24
120	288	PER_4_25	LVL_4_25	PER_3_25	LVL_3_25	PER_2_25	LVL_2_25	PER_1_25	LVL_1_25
121	289	PER_8_25	LVL_8_25	PER_7_25	LVL_7_25	PER_6_25	LVL_6_25	PER_5_25	LVL_5_25
122	290	PER_12_25	LVL_12_25	PER_11_25	LVL_11_25	PER_10_25	LVL_10_25	PER_9_25	LVL_9_25

Table 55. Pattern Profile Register Map for 5-Level Mode (continued)

REGISTER ADDRESS		REGISTER DATA							
Hex	Decimal	D31:D27	D26:D24	D23:D19	D18:D16	D15:D11	D10:D8	D7:D3	D2:D0
123	291	PER_16_25	LVL_16_25	PER_15_25	LVL_15_25	PER_14_25	LVL_14_25	PER_13_25	LVL_13_25
124	292	PER_20_25	LVL_20_25	PER_19_25	LVL_19_25	PER_18_25	LVL_18_25	PER_17_25	LVL_17_25
125	293	PER_24_25	LVL_24_25	PER_23_25	LVL_23_25	PER_22_25	LVL_22_25	PER_21_25	LVL_21_25
126	294	PER_28_25	LVL_28_25	PER_27_25	LVL_27_25	PER_26_25	LVL_26_25	PER_25_25	LVL_25_25
127	295	PER_32_25	LVL_32_25	PER_31_25	LVL_31_25	PER_30_25	LVL_30_25	PER_29_25	LVL_29_25
128	296	PER_4_26	LVL_4_26	PER_3_26	LVL_3_26	PER_2_26	LVL_2_26	PER_1_26	LVL_1_26
129	297	PER_8_26	LVL_8_26	PER_7_26	LVL_7_26	PER_6_26	LVL_6_26	PER_5_26	LVL_5_26
12A	298	PER_12_26	LVL_12_26	PER_11_26	LVL_11_26	PER_10_26	LVL_10_26	PER_9_26	LVL_9_26
12B	299	PER_16_26	LVL_16_26	PER_15_26	LVL_15_26	PER_14_26	LVL_14_26	PER_13_26	LVL_13_26
12C	300	PER_20_26	LVL_20_26	PER_19_26	LVL_19_26	PER_18_26	LVL_18_26	PER_17_26	LVL_17_26
12D	301	PER_24_26	LVL_24_26	PER_23_26	LVL_23_26	PER_22_26	LVL_22_26	PER_21_26	LVL_21_26
12E	302	PER_28_26	LVL_28_26	PER_27_26	LVL_27_26	PER_26_26	LVL_26_26	PER_25_26	LVL_25_26
12F	303	PER_32_26	LVL_32_26	PER_31_26	LVL_31_26	PER_30_26	LVL_30_26	PER_29_26	LVL_29_26
130	304	PER_4_27	LVL_4_27	PER_3_27	LVL_3_27	PER_2_27	LVL_2_27	PER_1_27	LVL_1_27
131	305	PER_8_27	LVL_8_27	PER_7_27	LVL_7_27	PER_6_27	LVL_6_27	PER_5_27	LVL_5_27
132	306	PER_12_27	LVL_12_27	PER_11_27	LVL_11_27	PER_10_27	LVL_10_27	PER_9_27	LVL_9_27
133	307	PER_16_27	LVL_16_27	PER_15_27	LVL_15_27	PER_14_27	LVL_14_27	PER_13_27	LVL_13_27
134	308	PER_20_27	LVL_20_27	PER_19_27	LVL_19_27	PER_18_27	LVL_18_27	PER_17_27	LVL_17_27
135	309	PER_24_27	LVL_24_27	PER_23_27	LVL_23_27	PER_22_27	LVL_22_27	PER_21_27	LVL_21_27
136	310	PER_28_27	LVL_28_27	PER_27_27	LVL_27_27	PER_26_27	LVL_26_27	PER_25_27	LVL_25_27
137	311	PER_32_27	LVL_32_27	PER_31_27	LVL_31_27	PER_30_27	LVL_30_27	PER_29_27	LVL_29_27
138	312	PER_4_28	LVL_4_28	PER_3_28	LVL_3_28	PER_2_28	LVL_2_28	PER_1_28	LVL_1_28
139	313	PER_8_28	LVL_8_28	PER_7_28	LVL_7_28	PER_6_28	LVL_6_28	PER_5_28	LVL_5_28
13A	314	PER_12_28	LVL_12_28	PER_11_28	LVL_11_28	PER_10_28	LVL_10_28	PER_9_28	LVL_9_28
13B	315	PER_16_28	LVL_16_28	PER_15_28	LVL_15_28	PER_14_28	LVL_14_28	PER_13_28	LVL_13_28
13C	316	PER_20_28	LVL_20_28	PER_19_28	LVL_19_28	PER_18_28	LVL_18_28	PER_17_28	LVL_17_28
13D	317	PER_24_28	LVL_24_28	PER_23_28	LVL_23_28	PER_22_28	LVL_22_28	PER_21_28	LVL_21_28
13E	318	PER_28_28	LVL_28_28	PER_27_28	LVL_27_28	PER_26_28	LVL_26_28	PER_25_28	LVL_25_28
13F	319	PER_32_28	LVL_32_28	PER_31_28	LVL_31_28	PER_30_28	LVL_30_28	PER_29_28	LVL_29_28

8.6.6.3 Register 60h (offset = 60h) [reset = 60h]

Figure 92. Register 60h

31	30	29	28	27	26	25	24
PER_4_1						LVL_4_1	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
23	22	21	20	19	18	17	16
PER_3_1						LVL_3_1	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
15	14	13	12	11	10	9	8
PER_2_1						LVL_2_1	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
7	6	5	4	3	2	1	0
PER_1_1						LVL_1_1	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 56. Register 60h Field Descriptions

Bit	Field	Type	Reset	Description
31-27	PER_4_1	R/W	Undefined	Period value for 4th transition in pattern profile 1.
26-24	LVL_4_1	R/W	Undefined	Level value for 4th transition in pattern profile 1.
23-19	PER_3_1	R/W	Undefined	Period value for 3rd transition in pattern profile 1.
18-16	LVL_3_1	R/W	Undefined	Level value for 3rd transition in pattern profile 1.
15-11	PER_2_1	R/W	Undefined	Period value for 2nd transition in pattern profile 1.
10-8	LVL_2_1	R/W	Undefined	Level value for 2nd transition in pattern profile 1.
7-3	PER_1_1	R/W	Undefined	Period value for 1st transition in pattern profile 1.
2-0	LVL_1_1	R/W	Undefined	Level value for 1st transition in pattern profile 1.

8.6.6.4 Register 61h to 13Fh (offset = 61h to 13Fh) [reset = 61h to 13Fh]

In below table register field name are given as PER_x1_y, LVL_x1_y, PER_x2_y, LVL_x2_y, PER_x3_y, LVL_x3_y, PER_x4_y, and LVL_x4_y. Where x1, x2, x3 and x4 represents the transition number can vary from 1 to 32 and y represents profile number and can vary from 1 to 28 across register addresses in pattern profile register map.

Figure 93. Register 61h to 13Fh

31	30	29	28	27	26	25	24
PER_x1_y						LVL_x1_y	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
23	22	21	20	19	18	17	16
PER_x2_y						LVL_x2_y	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
15	14	13	12	11	10	9	8
PER_x3_y						LVL_x3_y	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U
7	6	5	4	3	2	1	0
PER_x4_y						LVL_x4_y	
R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U	R/W-U

LEGEND: R = Read/Write; W = Write only; -n = value after reset

Table 57. Register 61h to 13Fh Field Descriptions

Bit	Field	Type	Reset	Description
31-27	PER_x1_y	R/W	Undefined	Period value for x1th transition in pattern profile y.

Table 57. Register 61h to 13Fh Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-24	LVL_x1_y	R/W	Undefined	Level value for x1th transition in pattern profile y.
23-19	PER_x2_y	R/W	Undefined	Period value for x2nd transition in pattern profile y.
18-16	LVL_x2_y	R/W	Undefined	Level value for x2nd transition in pattern profile y.
15-11	PER_x3_y	R/W	Undefined	Period value for x3rd transition in pattern profile y.
10-8	LVL_x3_y	R/W	Undefined	Level value for x3rd transition in pattern profile y.
7-3	PER_x4_y	R/W	Undefined	Period value for x4th transition in pattern profile y.
2-0	LVL_x4_y	R/W	Undefined	Level value for x4th transition in pattern profile y.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

To get the best performance and lowest power from the device follow the guideline given in the below section:

9.1.1 Guidelines for Selecting the Device Power Mode for Both Off-chip and On-chip Beamforming Mode

Hardware configuration: Consider an ultrasound system with multiple TX7316 ICs; see Figure 40. In such system it is recommended to keep TR_EN* signal separate across devices. It gives flexibility to control the power mode of individual IC independently to achieve lowest system level power.

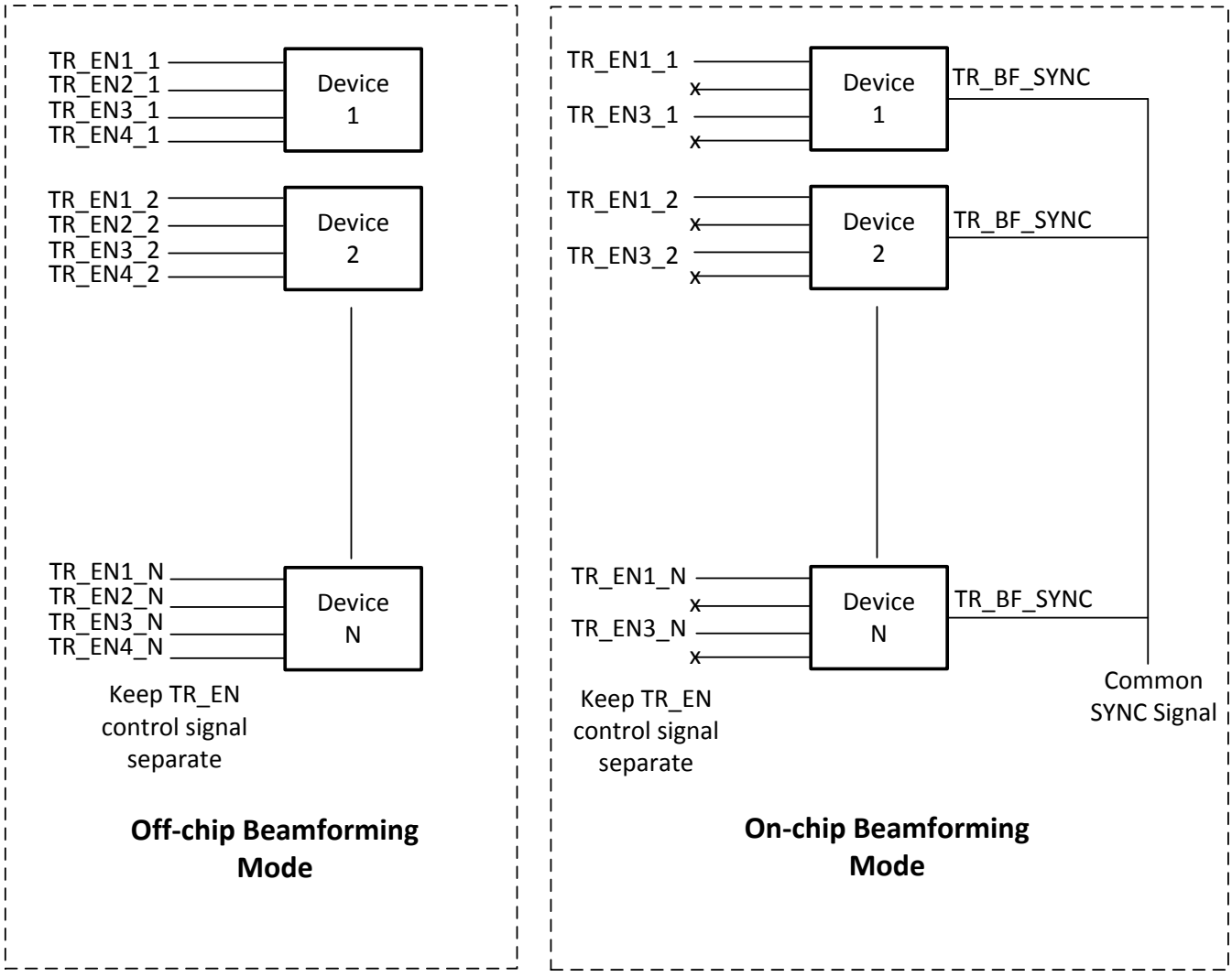


Figure 94. System Configuration Example

Configure the device as per suggestion below in the ultrasound systems:

1. *When device is both transmitting and receiving (transmit-receive mode):* This scenario occurs in B, PW mode

Application Information (continued)

of imaging. Configure the device either in default or dynamic power mode. Dynamic power mode gives lower power as compared to default mode however TR_EN* signals must be toggled at a minimum rate of 200 Hz in dynamic power mode. Dynamic power mode also allows exciting more than 4 cycles and PRF higher than 10 kHz in the output waveform without affecting the performance.

2. *When device is not transmitting but only receiving echo (T/R switch needs to be switched OFF during transmit phase and ON in receive phase):* This scenario occurs in B, PW mode of imaging. Configure the device either in default or dynamic power mode. To disable the transmit the pulser can be powered down. Dynamic power mode gives lower power as compared to default mode however TR_EN* signals must be toggled at a minimum rate of 200 Hz in dynamic power mode. Dynamic power mode also allows exciting more than 4 cycles and PRF higher than 10 kHz in the output waveform without affecting the performance.
3. *When device is continuously transmitting (minimum one channel is transmitting continuously)*: This scenario occurs in CW mode of imaging. In CW mode half of the channels in the system keep transmitting the waveform and other half keeps receiving echo from the body. For such a use case configure the device in CW power mode.
4. *When device is continuously receiving echoes (CW receive only mode — TR switch of all the channels are always ON):* This scenario occurs in CW mode of imaging. In CW mode half of the channels in the system keep transmitting the waveform and other half keeps receiving echo from the body. In such scenario, configure the device in default power mode. Default power mode is higher as compared to other power modes but it is the quietest power mode because it doesn't involve toggling of TR_EN* signal, therefore does not affect the receiving echo signals.
5. *When device is not transmitting but only receiving echoes for short duration (B-mode receive only mode — If TR switch of all the channels shall be kept always ON):* This scenario occurs if TR switch of the device is used as multiplexer or limited numbers of channels in the system are transmitting but TR switch is turned ON for more number of channels to receive echo from the body. In such cases configure the device either in default or transmit-less power mode. Transmit-less power mode gives lower power compared to default mode; however, TR_EN* signals must be toggled at a minimum rate of 200 Hz in dynamic power mode. Toggle TR_EN* signal when echo is not being received by the device.
6. *When device is neither transmitting nor receiving (Idle mode) but requires quick wake-up time:* This scenario occurs when in the system there are 128 channels but only few of the channels are used for transmit and receive. During scanning of multiple lines different devices are used for transmit and receive, therefore requires quick wake-up time and consumes less power when not in use. In such scenario configure the device either in transmit-less power mode or default power or standby mode. Transmit-less power mode offers the lowest power and fast wake-up time.
7. *When device is neither transmitting nor receiving with large wake-up time:* This scenario occurs when system is not performing any imaging and must shut down to save power. In such scenario use the global power down mode.

9.1.2 Option to Reduce System Clock Power

To reduce the power from the clock driving circuit generating clock for the device, the clock driving circuit can be disabled and enabled dynamically. Device doesn't need the clock when TR switch of all the channels are ON so external clock driving circuit can be disabled during that duration. Enable the clock again before 10 µs of applying TR_BF_SYNC pulse.

9.1.3 Color Noise

To get the good color mode image in the ultrasound systems, it is important to get the good repeatable performance from the device transmitting high voltage pulses. To measure the repeatability performance of TX7316 below experiment is performed:

1. Supply condition: A- and B-side high voltage supplies = ±100V.
2. Input to the device:
   a. BF_CLK clock frequency = 200 MHz
   b. TR_BF_SYNC = Configured in burst mode to generate 100 pulses of 5 kHz pulse repetition frequency (PRF) and repeating it after 1 sec (Referred as super PRF)
   c. Pulser output load: 1 kΩ || 220 pF

Application Information (continued)

d. All the channels are transmitting.

3. Device setting:
   a. Device is configured in 3-level, on-chip beam forming mode.
   b. Performance is measured across default and dynamic power mode and results are same.
   c. Device is configured to generate the waveform as shown in Figure 95.

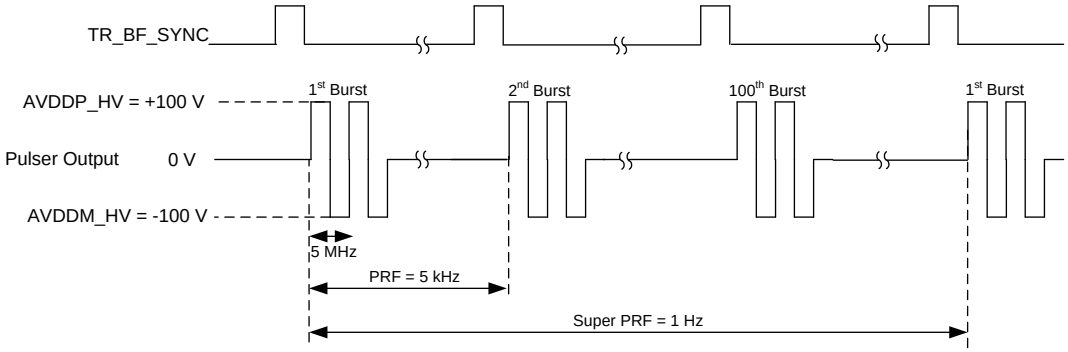


Figure 95. Color Noise Experiment Waveform

4. Measurement result:
   a. To measure the repeatability, puler output data is sampled at PRF rate on the data points shown in the Figure 96.
   b. The Figure 97 shows the FFT of the data on different points sampled at PRF.
   c. To estimate the device performance the FFT on point A is taken as reference. As at this point device is not transmitting so it is limited by scope noise. It is observed that points B, D, and F shows higher noise only for frequency less than 500 Hz, which can be easily filtered out using HPF without affecting the signal bandwidth. For frequency >500 Hz noise level is same as noise level of point A. For points C and E shows FFT same as point A proving no noise from these points. In ultrasound system the signal of interest lies for the frequency range >1 kHz.

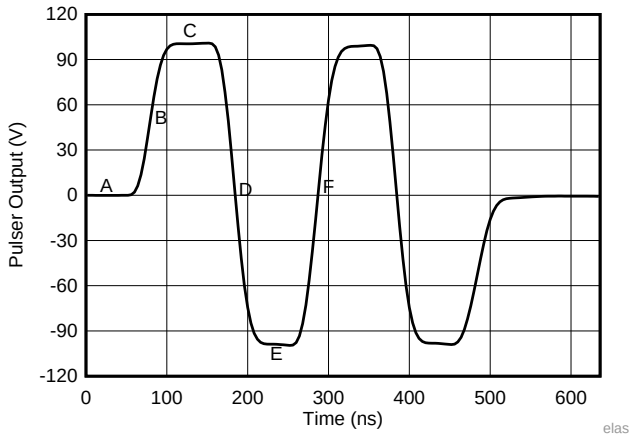


Figure 96. Repeatability Data

Application Information (continued)

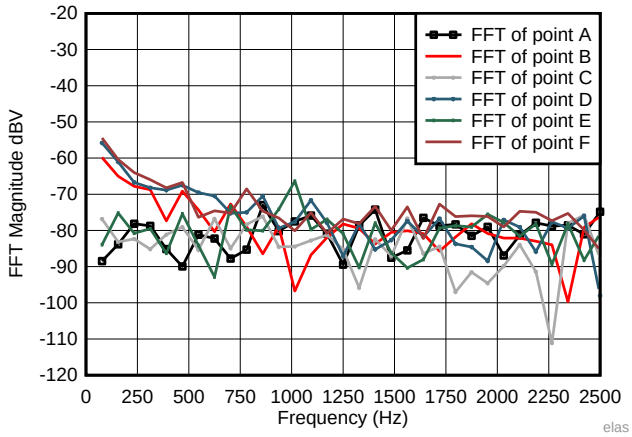


Figure 97. FFT of Different Points on Repeatability Waveform

9.1.4 Power Supply Design

1. See TIDA-01592 for high voltage low current design. This is useful for B-mode, PW mode and CW mode.
2. See TIDA-01352 and TIDA-01371 for high voltage high current designs. This is useful for Elastography or Shearwave mode Clocking Design .
3. See SNAA311 for the clocking section design.

9.1.5 Register Configuration Example

Refer to different register configuration example given below to configure device in different modes:

9.1.5.1 Default Power Mode

TR_ENx signal shall be kept low permanently

Table 58. Default Mode Register Configuration Example

Address (Hex)	Register Value (Hex)	Comment
00	0x00000001	Software reset the device
06	0x00000010	Enabling bit DIS_DYN_CNTRL_2
0F	0x00000010	Enabling bit DIS_DYN_ CNTRL_1
20h to 15Fh for 3-level mode 20h to 13Fh for 5-level mode	Xxxx	Program user defined pattern profile, delay profile and profile select registers
18	0x008C0003	- [26:18] Writes TX_START_DEL to get a minimum delay of 2us. - [1] TR_SW_DEL_MODE to enable TR switch at the end of pattern - [0] Enabling the TX_BF_MODE

9.1.5.2 Dynamic Power Mode

Apply TR_ENx at least 8 µs before TR_BF_SYNC pulse.

Table 59. Dynamic Power Mode Register Configuration Example

Address (Hex)	Register Value (Hex)	Comment
00	0x00000001	Software reset the device
19	0x40000000	EN_DYN_LDO is enabled
20h to 15Fh for 3-level mode 20h to 13Fh for 5-level mode	Xxxx	Program user defined pattern profile, delay profile and profile select registers

Table 59. Dynamic Power Mode Register Configuration Example (continued)

Address (Hex)	Register Value (Hex)	Comment
18	0x008C0003	- [26:18] Writes TX_START_DEL to get a minimum delay of 2us. - [1] TR_SW_DEL_MODE to enable TR switch at the end of pattern - [0] Enabling the TX_BF_MODE

9.1.5.3 Transmit-less Power Mode

Apply TR_ENx at least once in 5 ms.

Table 60. Transmit-less Mode Register Configuration Example

Address (Hex)	Register Value (Hex)	Comment
00	0x00000001	Software reset the device
17	0x00000600	Enabling PDN_CLK_SYNC_1 and PDN_CLK_SYNC_2
19	0x40000000	EN_DYN_LDO is enabled
18	0x00000001	Enabling the TX_BF_MODE

9.1.5.4 CW Mode

TR_ENx shall be kept low permanently. Below configuration configures all the 16 channels in continuous transmit mode. To configure any channel in receive mode, enable the TR switch of that particular channel.

Table 61. CW Mode Register Configuration Example

Address (Hex)	Register Value (Hex)	Comment
00	0x00000001	Software reset the device
06	0x00000010	Enabling bit DIS_DYN_CNTRL_2
0F	0x00000010	Enabling bit DIS_DYN_CNTRL_1
19	0xFFFFFFFF	Disabling all the TR switches.
20h to 9Fh for 3-level mode 20h to 5Fh for 5-level mode	Xxxx	Program user defined delay profiles.
18	0x008CE003	- [26:18] Writes TX_START_DEL to get a minimum delay of 2 us. - [17:16] CW_WAVE_MODE can be configured as per user requirement - [15:13] Enables CW_EN_MUX_SEL and CW_EN_1 and CW_EN_2. - [11:9] CW_DAMP_CNT can be configured as per user requirement - [1] TR_SW_DEL_MODE to enable TR switch at the end of pattern - [0] Enabling the TX_BF_MODE

9.1.5.5 4.8-A Mode

Both AVDDP/M_HV_A and AVDDP/M_HV_B has to be shorted in this mode.

Table 62. 4.8-A Mode Register Configuration Example

Address (Hex)	Data (Hex)	Comment
0	0x00000001	Software reset the device
0B	0x20000000	Enabling bit 4A_Mode_CNTRL_1
14	0x20000000	Enabling bit 4A_Mode_CNTRL_2
20 to 15F	Xxxx	Program user defined pattern profile, delay profile and profile select registers (3-level mode)

Table 62. 4.8-A Mode Register Configuration Example (continued)

Address (Hex)	Data (Hex)	Comment
18	0x008C0003	[26:18] Writes TX_START_DEL to get a minimum delay of 2 us. -[1] TR_SW_DEL_MODE to enable TR switch at the end of pattern -[0] Enabling the TX_BF_MODE

9.2 Typical Applications

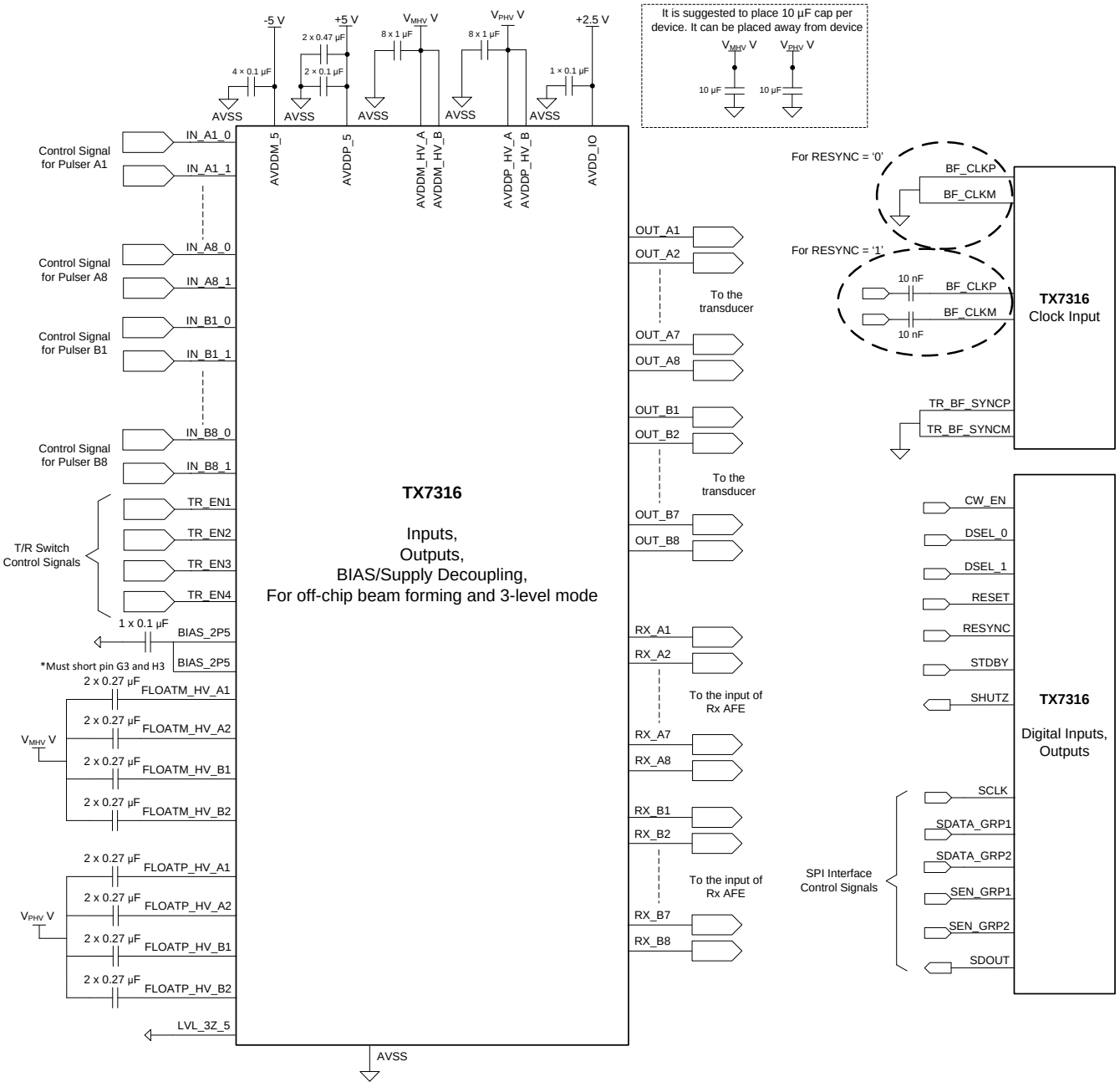


Figure 98. Application Circuit for 3-Level, Off-Chip Beamforming Mode

Typical Applications (continued)

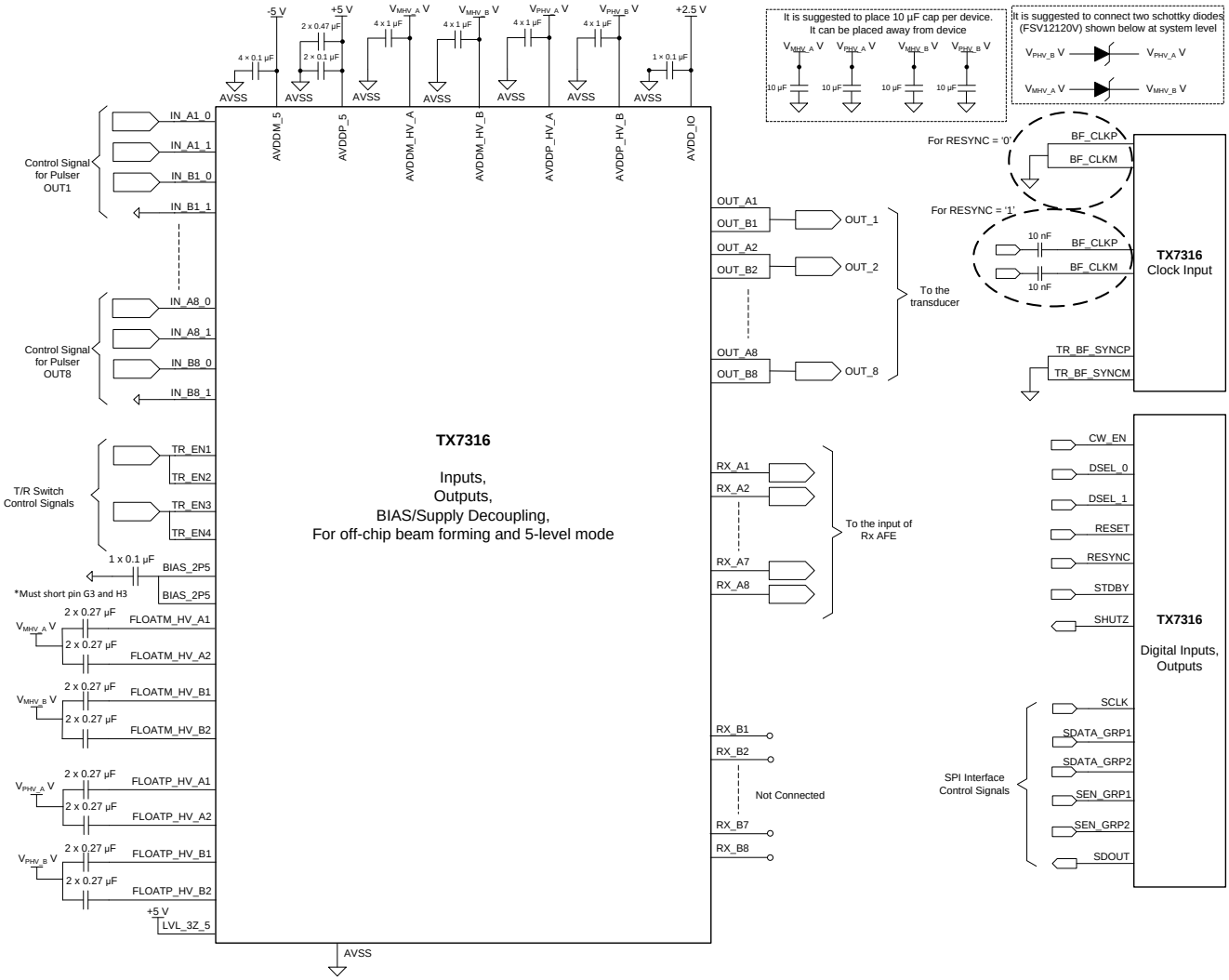


Figure 99. Application Circuit for 5-Level, Off-Chip Beamforming Mode

Typical Applications (continued)

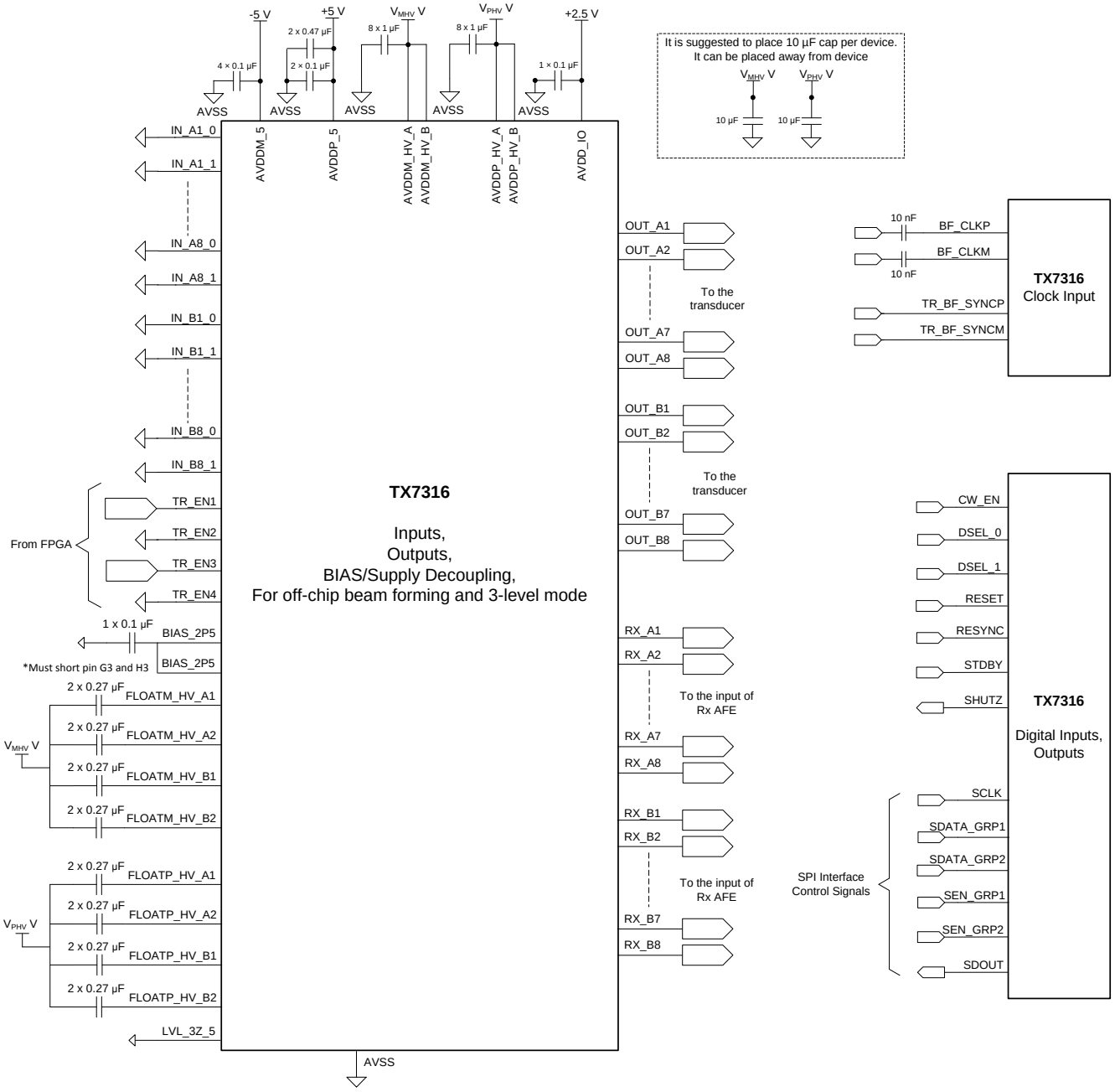


Figure 100. Application Circuit for 3-Level, On-Chip Beamforming Mode

Typical Applications (continued)

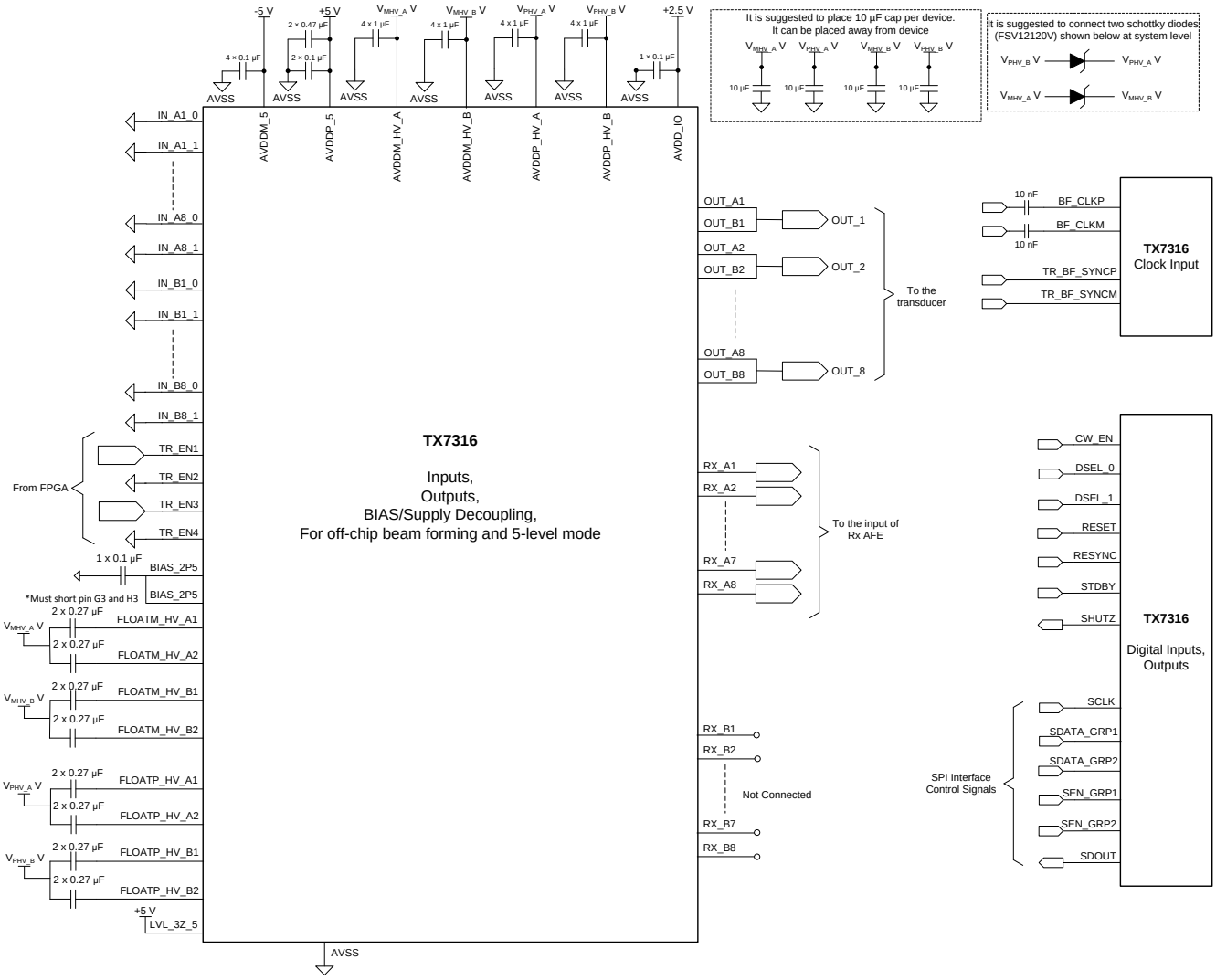


Figure 101. Application Circuit for 5-Level, On-Chip Beamforming Mode

9.2.1 Design Requirements

Table 63 list down the different capacitor specifications connected to different pins of the device.

Table 63. Capacitor Specifications

DEVICE PIN	CAPACITOR VALUE IN (µF)	SIZE	VOLTAGE RATING (V)	TOLERANCE
AVDDP_HV_A, AVDDM_HV_A AVDDP_HV_B, AVDDM_HV_B	1	0805	100	10%
FLOAT* pins to corresponding high voltage supplies	0.27	0402	6.3	10%
AVDDP_5	0.47	0402	6.3	10%
	0.1	0402	6.3	10%
AVDDM_5	0.1	0402	6.3	10%
AVDD_IO	0.1	0402	6.3	10%
BIAS_2P5	0.1	0402	6.3	10%

9.2.2 Detailed Design Procedure

Table 64 lists the schematic check list. Review the system schematic using Table 64.

Table 64. Schematic Checklist

PIN NAME	TI RECOMMENDATION FOR OFF-CHIP BEAMFORMING MODE	TI RECOMMENDATION FOR ON-CHIP BEAMFORMING MODE	VERIFIED YES/NO
BF_CLKP, BF_CLKM	Required if re-synchronization feature is used. Otherwise; connect both BF_CLKP and BF_CLKM to ground For differential input mode: - AC couple BF_CLKP and BF_CLKM signal - 100-Ω differential termination is required - Maximum frequency supported 200 MHz	For differential input mode: - AC couple BF_CLKP and BF_CLKM signal - 100-Ω differential termination is required - Maximum frequency supported 200 MHz	
	For single-ended input mode: - Connect BF_CLKM to AVDDP_5 supply - Apply BF_CLKP with AVDD_IO logic level - maximum frequency supported is 100 MHz	For single-ended input mode: - Connect BF_CLKM to AVDDP_5 supply - Apply BF_CLKP with AVDD_IO logic level - Maximum frequency supported is 100 MHz	
	For multiple devices in system, it should be separate for separate device	For multiple devices in system, it should be separate for separate device	
TR_BF_SYNCP, TR_BF_SYNCM	Connect TR_BF_SYNCP/M to ground	For differential input mode: - DC couple TR_BF_SYNCP and TR_BF_SYNCM signal - 100-Ω differential termination is required	
	Connect TR_BF_SYNCP/M to ground	For single-ended input mode: - Connect TR_BF_SYNCM to AVDDP_5 supply - Apply TR_BF_SYNCP with AVDD_IO logic level	
	Connect TR_BF_SYNCP/M to ground	Keep the same for all the devices driven by single driver	
BIAS_2P5	Make sure both the BIAS_2P5 pins (K1, L1) are shorted and connected to ground with minimum of 0.1-µF capacitance.	Make sure both the BIAS_2P5 pins (K1, L1) are shorted and connected to ground with minimum of 0.1-µF capacitance.	
FLOAT* pins	Make sure FLOAT_MHV* decaps are referred to MHV supplies and FLOAT_PHV* decaps are referred to PHV supplies. Use 2 × 0.27-µF capacitors.	Make sure FLOAT_MHV* decaps are referred to MHV supplies and FLOAT_PHV* decaps are referred to PHV supplies. Use 2 × 0.27-µF capacitors.	
IN* control signals	Apply control signal from FPGA with AVDD_IO level.	Connect to ground	
RESET	Connect to FPGA to reset the device.	Connect to FPGA to reset the device	
RESYNC	Connect to AVDD_IO if re-sync feature is required. Otherwise connect to ground.	Connect to AVDD_IO supply	
SPI signals	Connect all the SPI signals to FPGA.	Connect all the SPI signals to FPGA	
SHUTZ	2-kΩ resistor to AVDD_IO	2-kΩ resistor to AVDD_IO	
TR_EN* signals	Connect all the TR_EN* pins to FPGA to control TR switch.	Connect TR_EN1 and TR_EN3 to FPGA. Ground TR_EN2 and TR_EN4 pins. These pins are useful to get lowest power from device.	
	In case of system having multiple devices, keep TR_EN1/2/3/4 signal separate for separate device. This allows to turn ON and turn OFF instant of TR switch independently across devices.	For systems having multiple devices, keep TR_EN1/3 signal separate for separate device. Power of the device must be optimized at system level by controlling individual device using these pins.	
AVDDM_5	Voltage level has to be –5 V. Connect minimum of 4 × 0.1-µF capacitors of 0402 size.	Voltage level has to be -–5 V. Connect minimum of 4 × 0.1-µF capacitors of 0402 size.	

Table 64. Schematic Checklist (continued)

PIN NAME	TI RECOMMENDATION FOR OFF-CHIP BEAMFORMING MODE	TI RECOMMENDATION FOR ON-CHIP BEAMFORMING MODE	VERIFIED YES/NO
AVDDM_HV_A	If supply voltage is >90V then use minimum of 4 x 0.1µF cap of >100V rating with 0805 size. If supply voltage is <90V then use minimum of 4 x 1-µF cap of 100V rating with 0805 size.	If supply voltage is >90V then use minimum of 4 x 0.1-µF cap of >100V rating with 0805 size. If supply voltage is <90V then use minimum of 4 x 1-µF cap of 100V rating with 0805 size.	
AVDDM_HV_B	If supply voltage is >90V then use minimum of 4 x 0.1-µF cap of >100V rating with 0805 size. If supply voltage is <90V then use minimum of 4x1-ƒF cap of 100V rating with 0805 size.	If supply voltage is >90V then use minimum of 4 x 0.1-µF cap of >100V rating with 0805 size. If supply voltage is <90V then use minimum of 4 x 1uF cap of 100V rating with 0805 size.	
AVDDM_HV_A and AVDDM_HV_B supply protection	For 5-level mode connect schottky diode FSV12120V, between AVDDM_HV_A and AVDDM_HV_B with its anode connected to AVDDM_HV_A and cathode connected to AVDDM_HV_B.	For 5-level mode connect schottky diode FSV12120V, between AVDDM_HV_A and AVDDM_HV_B with its anode connected to AVDDM_HV_A and cathode connected to AVDDM_HV_B.	
AVDDP_5	Voltage level must be 5 V. Connect minimum of 2 × 0.47-µF, 2 × 0.1-µF capacitors of 0402 size.	Voltage level must be 5 V. Connect minimum of 2 × 0.47-µF, 2 × 0.1-µF capacitors of 0402 size.	
AVDDP_HV_A	If supply voltage is >90V then use minimum of 4x0.1µF cap of >100V rating with 0805 size. If supply voltage is <90V then use minimum of 4 x 1-µF cap of 100V rating with 0805 size.	If supply voltage is >90V then use minimum of 4x0.1-µF cap of >100V rating with 0805 size. If supply voltage is <90V then use minimum of 4 x 1-µF cap of 100V rating with 0805 size.	
AVDDP_HV_B	If supply voltage is >90V then use minimum of 4x0.1µF cap of >100V rating with 0805 size. If supply voltage is <90V then use minimum of 4 x 1-µF cap of 100V rating with 0805 size.	If supply voltage is >90V then use minimum of 4x0.1-µF cap of >100V rating with 0805 size. If supply voltage is <90V then use minimum of 4 x 1-µF cap of 100V rating with 0805 size.	
AVDDP_HV_A and AVDDP_HV_B supply protection	For 5-level mode connect schottky diode FSV12120V, between AVDDP_HV_A and AVDDP_HV_B with its anode connected to AVDDP_HV_B and cathode connected to AVDDP_HV_A.	For 5-level mode connect schottky diode FSV12120V, between AVDDP_HV_A and AVDDP_HV_B with its anode connected to AVDDP_HV_B and cathode connected to AVDDP_HV_A.	
AVDD_IO	Use either 1.8-V or 2.5-V supply. Connect minimum of 1 × 0.1-µF capacitor.	Use either 1.8-V or 2.5-V supply. Connect minimum of 1 × 0.1-µF capacitor.	

9.3 Application Curves

This section outlines the trends described in *Typical Characteristics* from an application perspective.

Figure 3 illustrates the total power in mW versus pulse repetition time (PRT). To measure the power, device is configured to generate patterns shown in Figure 2 on all the 8 channels with 0 transmit delay beamforming. For the on-chip beam forming mode PRT is same as TR_BF_SYNC signal period. When PRT reduces, the high voltage pulses are fired more often therefore the device power increases. The power difference between off-chip and on-chip beam forming is very small therefore Figure 3 is applicable for both the beamforming modes. The power difference between default and dynamic power mode is more significant for the PRT > 200 µs because the internal floating LDO is powered up less often in dynamic power mode causing lower power consumption.

Figure 4 illustrates the total power in mW v/s high voltage supply. The |AVDDP/M_HV_B| supplies are kept at 50 V and |AVDDP/M_HV_A| supplies are swept from 50 V to 100 V. The device is configured to generate patterns shown in Figure 2 on all the 8 channels with 0 transmit delay beam forming. As the power supply magnitude increases, the load current increases which results in increase of the device power.

Figure 5 illustrates the time domain result of pulse inversion test. A single channel pulser of the device is first excited with the positive polarity waveform followed by negative polarity waveform of frequency 5 MHz. Both the waveforms are captured on scope and summed to get the second harmonic component in the waveform. This test estimates the quality of second harmonic imaging used in ultrasound system.

Figure 6 illustrates the FFT of signals shown in Figure 5. The fundamental power cancels out on summing OUT_A1 and OUT_A2 waveforms but second harmonic adds up and increases the HD2 power by 6 dB. The device achieves fundamental cancellation and HD2 > 45 dBc.

Application Curves (continued)

Figure 7 illustrates the rise time for ground to AVDDP_HV_A transition and fall time for ground to AVDDM_HV_A transition across AVDDP/M_HV_A supply for |AVDDP/M_HV_B| kept at 10 V. The plot shows that the rise and fall are matched within 1 ns across high voltage supply range. This matching is critical to meet the HD2 performance across supply.

Figure 8 illustrates the rise time for AVDDM_HV_A to AVDDP_HV_A transition and fall time for AVDDP_HV_A to AVDDM_HV_A transition across AVDDP/M_HV_A supply for |AVDDP/M_HV_B| kept at 10 V. The plot shows that the rise and fall are matched very close (≈1 ns) across high voltage supply range. This matching is critical to meet the HD2 performance across supply.

Figure 9 illustrates the rise time for AVDDM_HV_A to ground transition and fall time for AVDDP_HV_A to ground transition across AVDDP/M_HV_A supply for |AVDDP/M_HV_B| kept at 10 V. The plot shows that the rise and fall are matched very close (≈1.5 ns) across high voltage supply range. This matching is critical to meet the HD2 performance across supply.

Figure 10 illustrates the rise time for ground to AVDDP_HV_B transition and fall time for ground to AVDDM_HV_B transition across AVDDP/M_HV_B supply for |AVDDP/M_HV_A| kept at 100 V. When the voltage difference between A side and B side supply changes, it results in more mismatch between the rise and fall time. In case of 3-level mode when A and B side supply is kept same the B-side pulser shows the same behavior as shown in Figure 7, Figure 8, and Figure 9.

Figure 11 illustrates the rise time for AVDDM_HV_B to AVDDP_HV_B transition and fall time for AVDDP_HV_B to AVDDM_HV_B transition across AVDDP/M_HV_B supply for |AVDDP/M_HV_A| kept at 100 V. When the voltage difference between A side and B side supply changes, it results in more mismatch between the rise and fall time. In case of 3-level mode when A and B side supply is kept same the B-side pulser shows the same behavior as shown in Figure 7, Figure 8, and Figure 9.

Figure 12 illustrates the rise time for AVDDM_HV_B to ground transition and fall time for AVDDP_HV_B to ground transition across AVDDP/M_HV_B supply for |AVDDP/M_HV_A| kept at 100 V. When the voltage difference between A side and B side supply changes, it results in more mismatch between the rise and fall time. In case of 3-level mode when A and B side supply is kept same the B-side pulser shows the same behavior as shown in Figure 7, Figure 8, and Figure 9.

Figure 13 illustrates the HD2 performance of pulser output at 5 MHz across AVDDP/M_HV_B supplies for different AVDDP/M_HV_A supplies. AVDDP/M_HV_B supplies are always less than AVDDP/M_HV_A supplies. The pattern used is a 3-Level waveform pulsing between AVDDP_HV_A and AVDDM_HV_A. To measure HD2 single channel is excited at a time. Good HD2 across supply is required in ultrasound system to get good harmonic imaging. We see that changing AVDDP/M_HV_B supplies do not affect the HD2 of the A-side pulser.

Figure 14 illustrates the HD2 performance of pulser output at 5 MHz across AVDDP/M_HV_B supplies for different AVDDP/M_HV_A supplies. AVDDP/M_HV_B supplies are always less than AVDDP/M_HV_A supplies. The pattern used is a 3-Level waveform pulsing between AVDDP_HV_B and AVDDM_HV_B. To measure HD2 single channel is excited at a time. When the voltage difference between A side and B side supply changes, it results in HD2 performance degradation. In case of 3-level mode when A and B side supply is kept same the B-side pulser shows the same behavior as shown in Figure 13.

Figure 15 illustrates the HD2 performance of pulser output for AVDDP/M_HV_A at ±100 V and AVDDP/M_HV_B at 50 V, across frequency. The pattern used is 3-Level waveform pulsing between AVDDP/M_HV_A. To measure HD2 single channel is excited at a time.

Figure 16 illustrates the HD2 distribution measured across 6160 channels. It shows close distribution of HD2 performance with mean around 45 dBc.

Figure 17 illustrates the HD2 performance of pulser output at 5 MHz across high voltage supply for different temperature condition. The plot represents average HD2 performance measured across all the 8 channels on 30 devices. To measure HD2 single channel is excited at a time. Good HD2 across supply and temperature is required in ultrasound system to get good harmonic imaging.

Application Curves (continued)

Figure 18 illustrates the HD2 performance of A group pulser output at 5 MHz across A group high voltage supply for B group supply voltage kept fixed at ±10 V. To measure HD2, single channel is excited at a time. Good HD2 across supply is required in ultrasound system to get good harmonic imaging. The A group HD2 is not dependent on B group supply level. So same HD2 performance is applicable for other values of B group HV supply. The three plots represent the typical, minimum, and maximum HD2 observed after characterizing the performance on 3 devices.

Figure 19 illustrates the pulser normalized amplitude across frequency for different AVDDP/M_HV_A supplies. To perform this measurement the peak to peak amplitude of pulser output is measured across frequency and normalized it with respect to peak to peak amplitude at 1 MHz for different high voltage supply values. As the high voltage supply value reduces, the pulser peak to peak swing also reduces that helps in getting the higher bandwidth for lower supply voltage.

Figure 20 illustrates the pulser peak-to-peak voltage v/s time in elastography mode. Device is configured to generate continuous pulses for 1-ms duration with signal frequency of 5 MHz. Such 1-ms duration pulses are repeated after every 1 second. All the 8 channels are excited together. As shown in Figure 20 the peak-to-peak voltage reduces slightly with time. This is because of increase in ON resistance of output transistor due to change in temperature.

Figure 21 illustrates the pulser rise and fall time v/s time in elastography mode. Device is configured to generate continuous pulses for 1-ms duration with signal frequency of 5 MHz. Such 1-ms duration pulses are repeated after every 1 second. All the 8 channels are excited together. As shown in Figure 21 the rise and fall time changes with time. This is because of change in output transistor behavior due to change in temperature.

Figure 22 illustrates the AVDDP_HV_A/B and AVDDM_HV_A/B power supply rejection ratio (PSRR) across frequency. The PSRR of the device is measure by applying a known amplitude signal at high voltage supply across frequency and measuring the same frequency component amplitude at RX_n node. The pulser is programmed in high impedance mode and TR switch is kept ON while performing PSRR measurement. For measuring PSRR, RX_A/Bn node is connected to 50 Ω resistance in parallel with 20-pF capacitance and OUT_A/Bn node connected to 1-kΩ resistance in parallel with 220-pF capacitance. The PSRR of AVDDM_HV_A supply scales directly with the total load connected at OUT_An and RX_An node. At system level the RX_An node gets connected to the input of very high gain ultrasound analog front end. So total channel gain and PSRR of the device should be considered while deciding the power supply noise level.

Figure 23 illustrates the AVDDP_5 and AVDDM_5 power supply rejection ratio (PSRR) across frequency. The PSRR of the device is measure by applying a known amplitude signal at corresponding supply across frequency and measuring the same frequency component amplitude at RX_A/Bn node. The pulser is programmed in high impedance mode and TR switch is kept ON while performing PSRR measurement. For measuring PSRR, RX_A/Bn node is connected to 50-Ω resistance in parallel with 20-pF capacitance and OUT_A/Bn node connected to 1-kΩ resistance in parallel with 220-pF capacitance. The PSRR of AVDDP_5 supply scales directly with the total load connected at OUT_A/Bn and RX_A/Bn node. At system level the RX_A/Bn node gets connected to the input of very high gain ultrasound analog front end. So total channel gain and PSRR of the device should be considered while deciding the power supply noise level.

Figure 24 illustrates the time domain waveform at pulser output node (OUT_A/Bn) when TR switch turns ON. The last small glitch in the waveform at ≈500 ns time instant is the time when TR switch completely turns ON.

Figure 25 illustrates the time domain waveform at pulser output node (OUT_A/Bn) when TR switch turns OFF. The last small glitch in the waveform at ≈1700 ns time instant is the time when TR switch completely turns OFF.

Figure 26 illustrates the time domain waveform measured at RX_A/Bn node when pulser generates the large voltage output. This data shows the good isolation performance from TR switch.

Figure 27 illustrates the second harmonic distortion (HD2) performance of TR switch v/s frequency. To measure the HD2 performance, a signal is applied at pulser output (OUT_A/Bn node) with 50 ohms source impedance and HD2 is measured for the signal at RX_A/Bn node. To measure the linearity signal amplitude is kept as 1 V_{PP} at RX_A/Bn node .

Figure 28 illustrates the phase noise performance of pulser in CW mode. To measure CW phase noise device is configured to generate 5-MHz continuous signal (5 V -> -5 V -> 5 V ....) with AVDDP_HV_A/B = 5 V and AVDDM_HV_A/B = –5 V. The x axis in the plot represents the frequency offset with respect to signal of frequency 5 MHz and y-axis represents noise level measured with respect to fundamental carrier power.

9.4 Do's and Don'ts

Take care of following points while working with the TX7332 device:

1. The content of delay and pattern profile register maps are undefined on power up and applying a reset. Users must configure delay and pattern profile register maps as per requirements.
2. Make sure that TX_START_DEL setting is written such that TX_DEL delay become greater than 2 μs. This 2-μs time is required to switch Off the TR switch.
3. Make sure that T/R switch is configured in OFF state for the duration where high voltage pulses from pulser are being transmitted. Otherwise, pulser output gets disabled.
4. While probing the device supply or any node take extra precaution. Shorting any node to any other node while probing shall damage the device.
5. In elastography mode if drop in the pulser output peak-to-peak voltage is observed then it can be because of the AVDDP_HV_A/B and AVDDM_HV_/B power supplies. So as a first debug point probe the positive and negative high voltage power supplies and make sure that there is no drop in the HV supply.
6. Keep absolute voltage level of AVDDP/M_HV_A supplies always greater than AVDDP/M_HV_B.

9.5 Initialization Set Up

To initialize device in off-chip beamforming mode, follow these steps:

1. Bring up all the power supplies.
2. After all the supplies are up wait for 1 μs.
3. Apply a pulse on the RESET pin with minimum pulse duration of 1 μs.
4. Keep TR_ENx and IN_* control signals at logic level '0'.
5. Wait for 1 ms.
6. Apply user defined register settings.
7. Apply control signals to control pulser and TR switch.

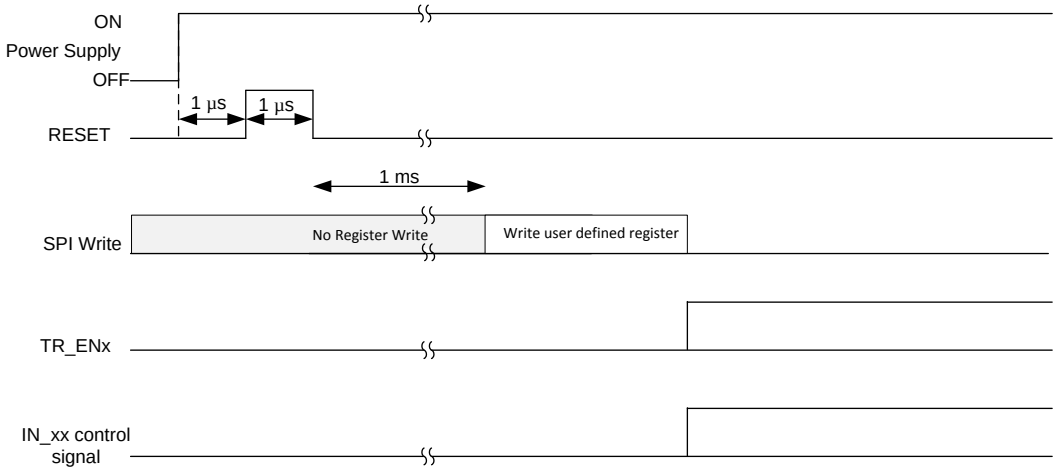


Figure 102. Initialization Sequence in Off-chip Beamforming Mode

To initialize the device in on-chip beamforming mode follow below step:

1. Bring up all the power supplies.
2. After all the supplies are up wait for 1 μs.
3. Apply a pulse on the RESET pin with minimum pulse duration of 1 μs.
4. Wait for 1 ms.
5. Write register set 1 as suggested below. If this step is not followed then enabling the TX_BF_MODE bit shall generate unknown HV pulses on the pulser output even without applying TR_BF_SYNC signal. If that's not the concern in the system then step described in points 5 and 6 can be omitted.
    1. Write 0 to address 20h to 2Fh. It will set the delay value for all the channels to 0.

Initialization Set Up (continued)

2. Write 00000078h to register address 120h.
3. Write 00000001h to register address 18h.

6. Wait for 200 BF_CLK clock cycles.
7. Write user defined register setting.
8. Apply TR_BF_SYNC pulse signal. Device operates as per the user-defined settings.

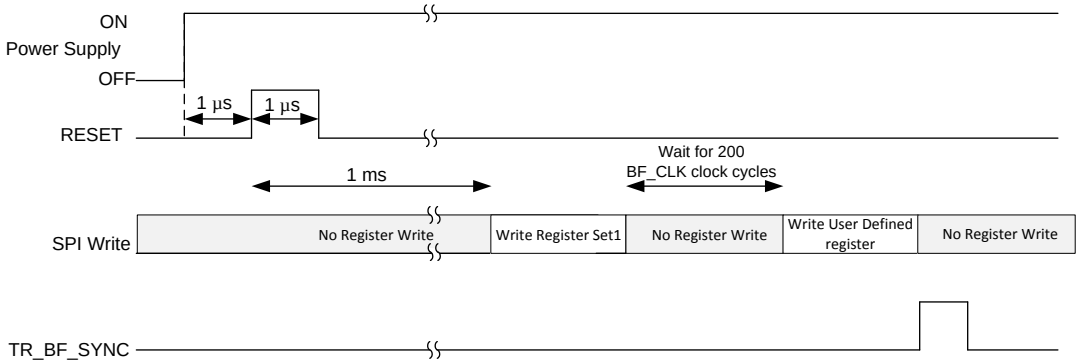


Figure 103. Initialization Sequence in On-chip Beamforming Mode

10 Power Supply Recommendations

10.1 3-level mode

In 3-level mode no specific power sequencing is required. Device shall be powered-up and powered-down in any sequence. For AVDDDP/M_HV_A/B supplies the maximum slew rate allowed is 200 V/ms.

10.2 5-Level Mode

In 5-level mode the power sequencing has only one constraint. At any point of time during power up or power down, the AVDDP_HV_A supply voltage level has to be equal or greater than AVDDP_HV_B and AVDDM_HV_A supply absolute voltage level has to be equal or greater than AVDDM_HV_B. For AVDDP/M_HV_A/B supplies the maximum slew rate allowed is 200 V/ms.

11 Layout

11.1 Layout Guidelines

In high-voltage, high-speed devices, most of the switching currents are provided by external decoupling capacitors. Hence, any inductance on the supply path can affect the device performance. For the device, care must be taken to ensure that the supply decoupling capacitors are as close to the device as possible. Also, the current return path must be short as possible. Place multiple vias on the supply path whenever possible.

TX7316EVM layout can be used as a reference. Layout diagrams of the EVM top and bottom layer are shown in Figure 104 and Figure 105 respectively.

Table 65 lists the TI recommended placement and routing strategy. It is assumed that the device is place on the top layer.

Table 65. Placement and Routing Checklist

PIN NAME	TI RECOMMENDED PLACEMENT AND ROUTING STRATEGY	VERIFIED YES/NO
AVDDP/M_HV	Place all the HV decoupling capacitors on the top layer. In the system, the supply planes can be couple of layers apart from the external layers and the via inductance can be significant. Hence, there should be a HV supply patch just below the device plane. This ensures that HV supply return current has the lowest inductance path. See Figure 106 for reference.	
FLOAT pins	Place the two decoupling capacitors on the top layer as close to the device as possible.	
AVDDP/M_5	Place the decoupling capacitor as close to the device as possible, either in the top layer or the bottom layer.	
BF_CLK and TR_BF_SYNC pins	Route the pair as differential 100-Ω trace when used in differential mode (length matched to 5 mils(1) within the pair). In single-ended mode route the signal as 50-Ω trace. Length match the TR_BF_SYNC signal routing to BF_CLK signal routing(2).	
OUT pins	Avoid routing two OUT signals parallel to each other in adjacent layers. This is to limit the parasitic capacitor between different OUT signals to get good cross talk performance. For 220-pF load capacitance a small parasitic capacitance of 1 pF between the two OUT signals can degrade cross talk to -47 dBc.	
IN control pins	If the device is used in off-chip beamforming mode, signals IN_n_0 and IN_n_1 must be length matched(2).	
SPI control pins	Need to take care of signal integrity to ensure SPI works till 100-MHz frequency. Length match the SCLK and SDATA* signals to meet timing(2).	
RX pins	Take care of signal integrity to avoid reflection because of echo signal coming from the transducer. TI recommends to terminate the RX* signal near to RX device with source (and trace) matching impedance.	

(1) 1 mil = 0.001 inch
(2) Length matching tolerance is within 100 mils if not specified.

11.2 Layout Examples

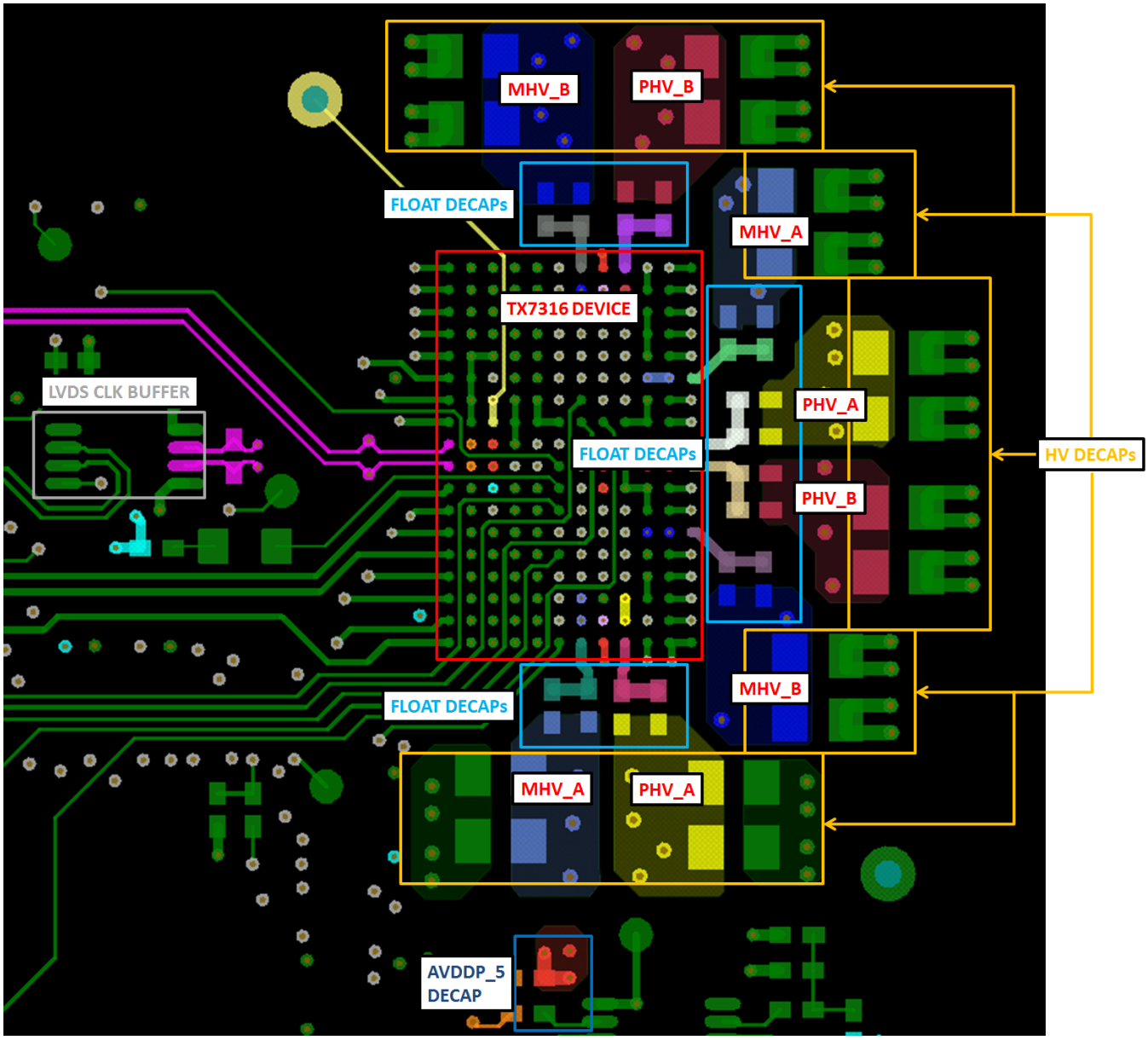


Figure 104. Top Layer of the EVM

Layout Examples (continued)

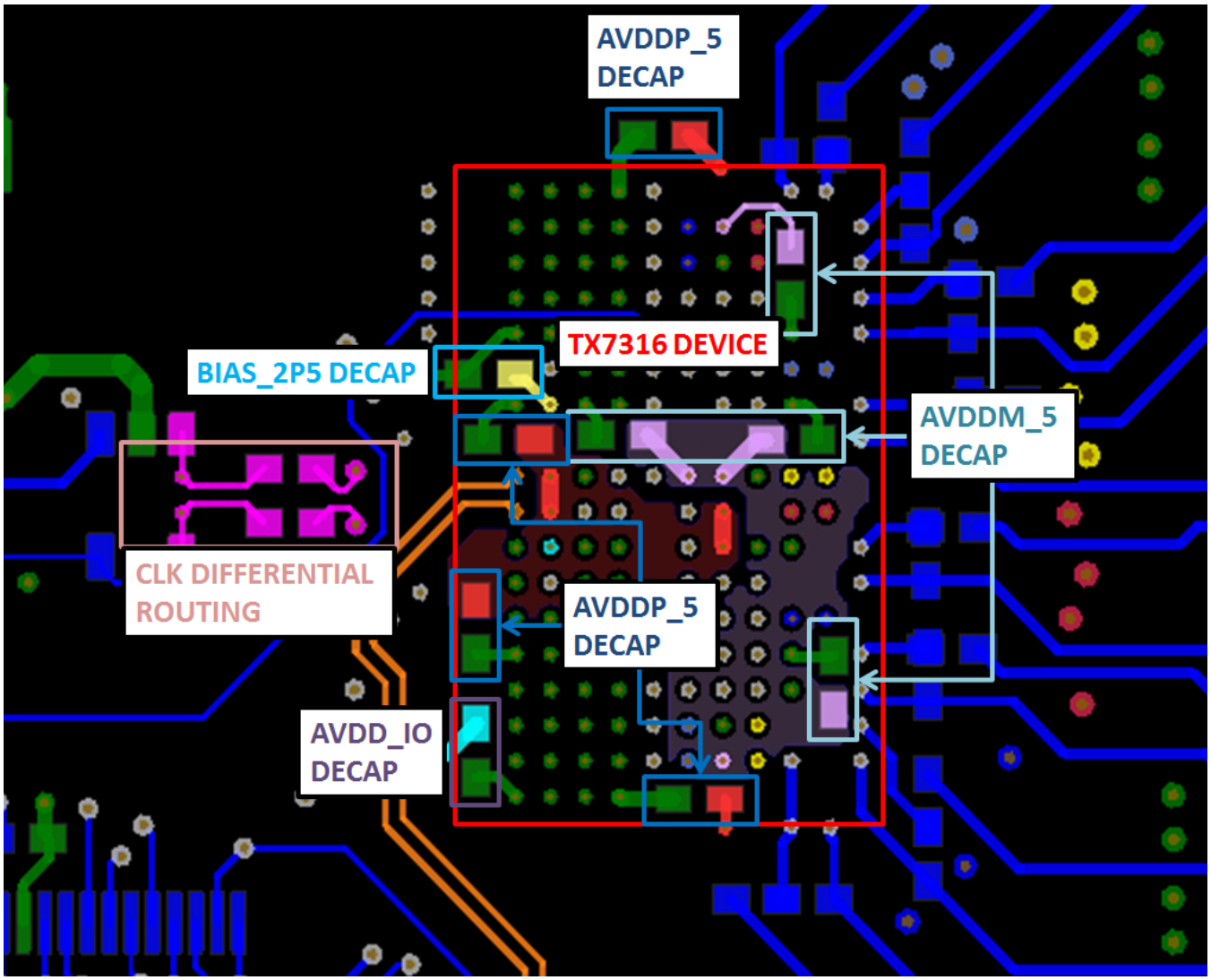


Figure 105. Bottom Layer of the EVM

Layout Examples (continued)

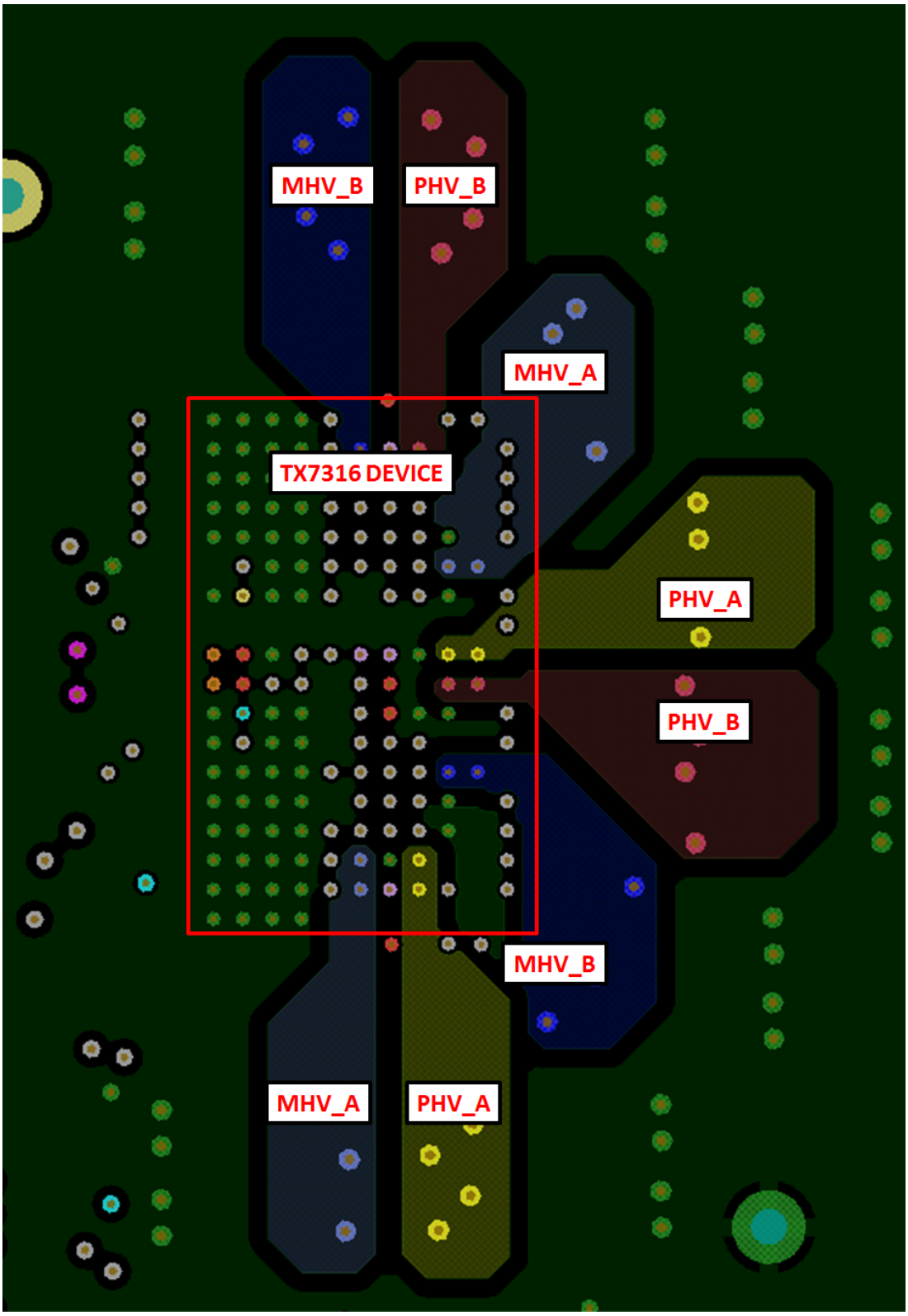


Figure 106. HV Supply Patch in the Adjacent Layer Below the Device Layer - Reduces Return Current Path for the HV Supply Current

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

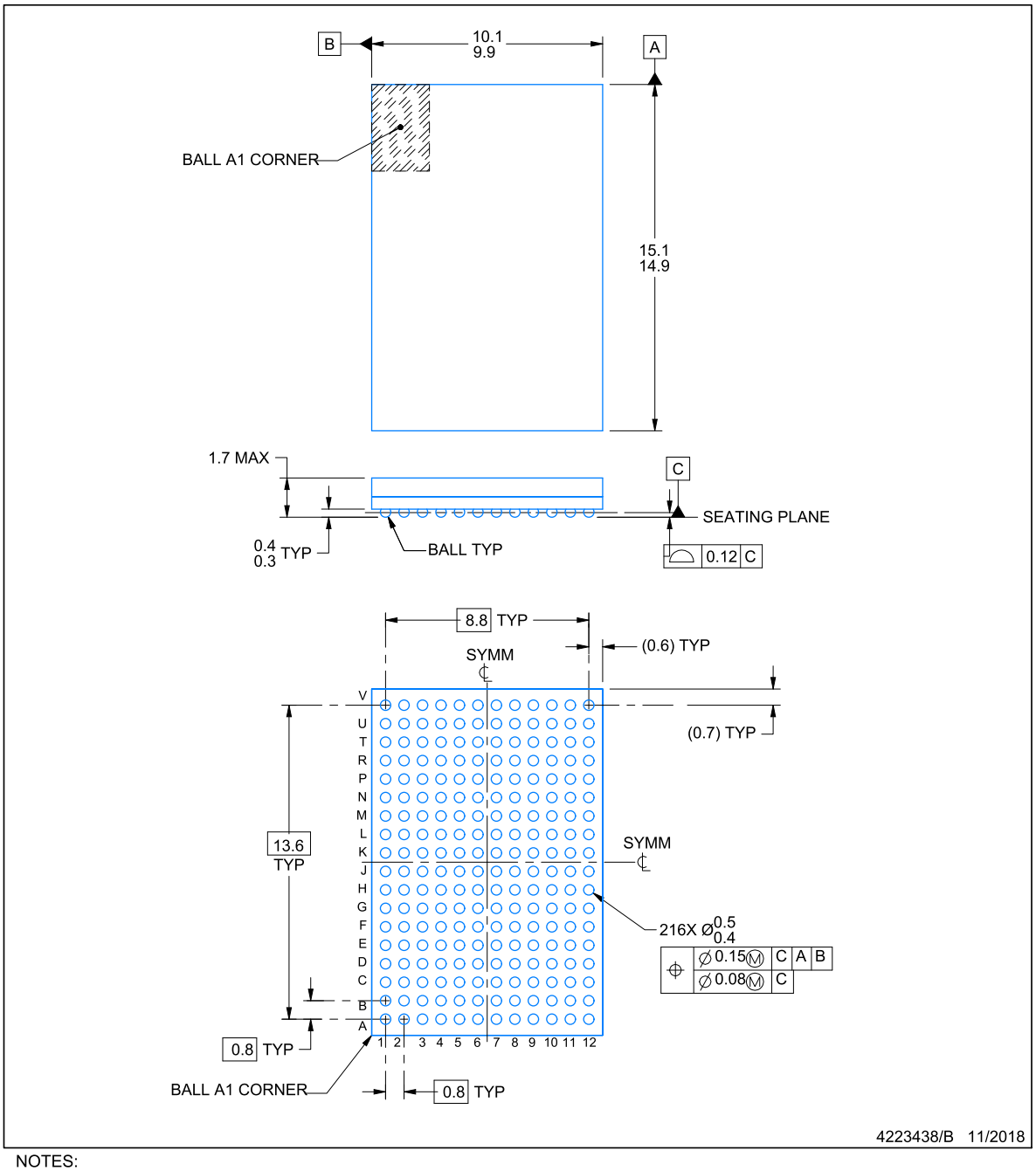
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

ZCX0216A

NFBGA - 1.7 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

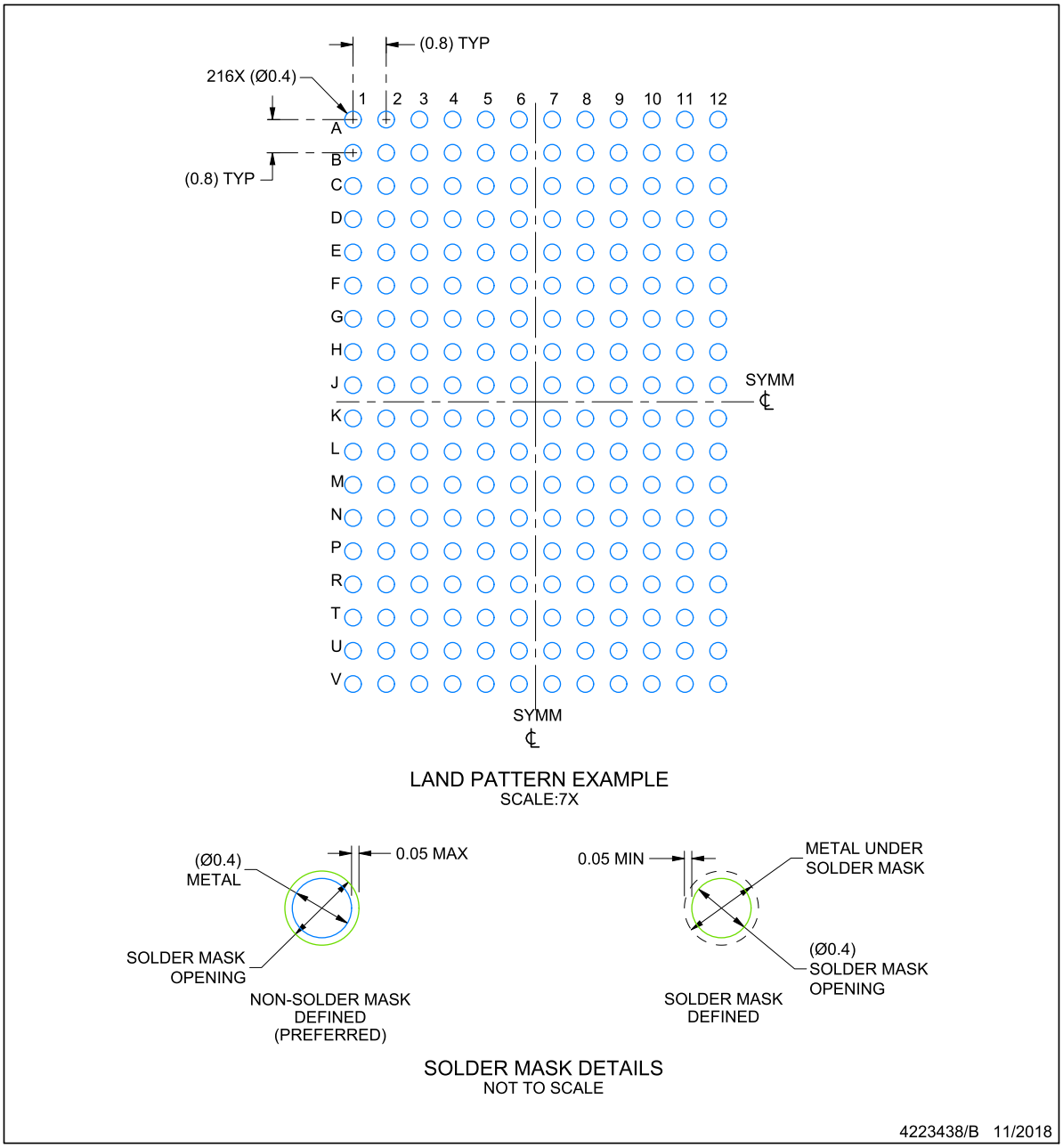
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ZCX0216A

NFBGA - 1.7 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

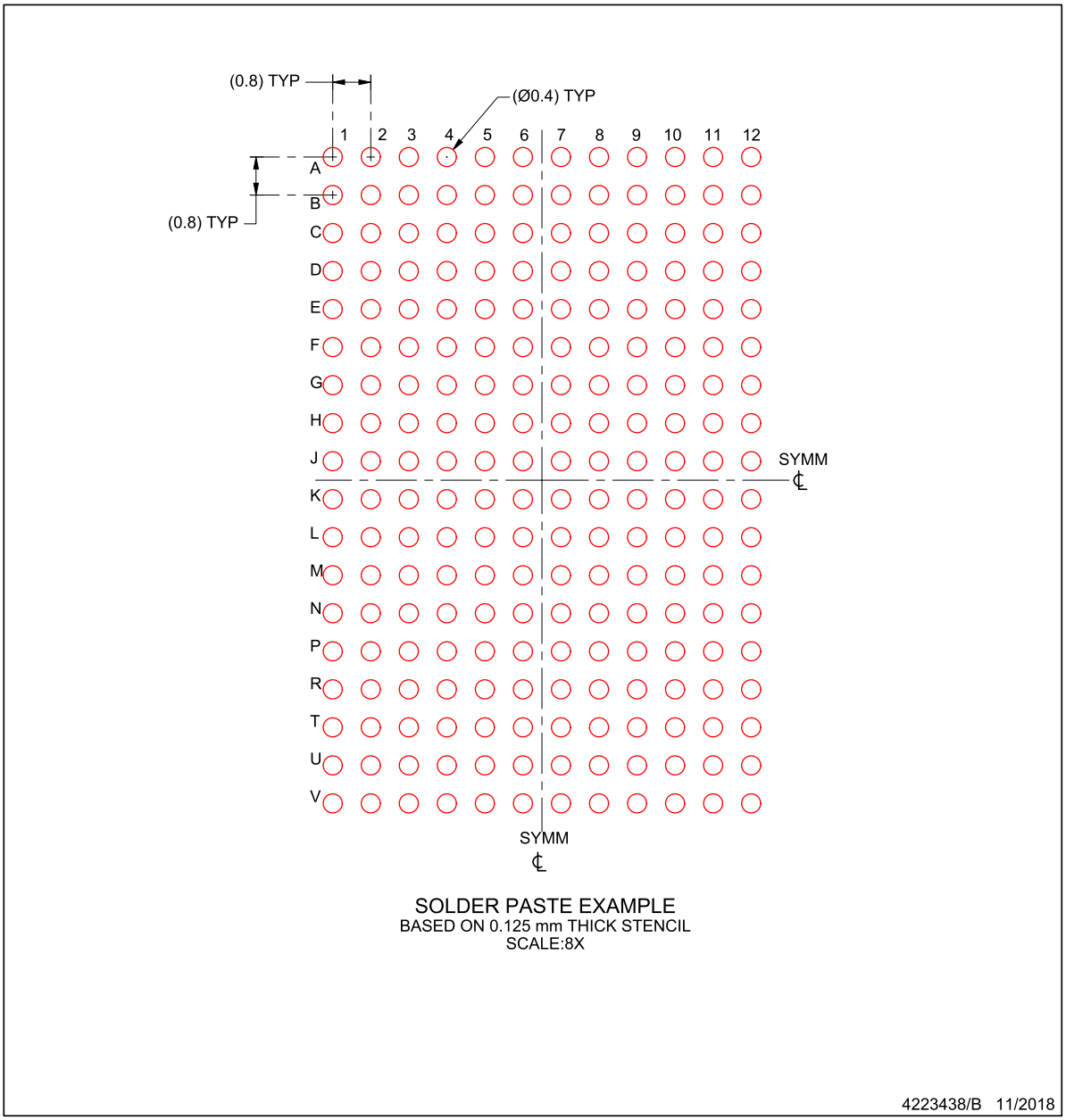
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZCX0216A

NFBGA - 1.7 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4223438/B 11/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4)(5)
PTX7316ZCX	ACTIVE	nFBGA	ZCX	216		Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	PTX7316

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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