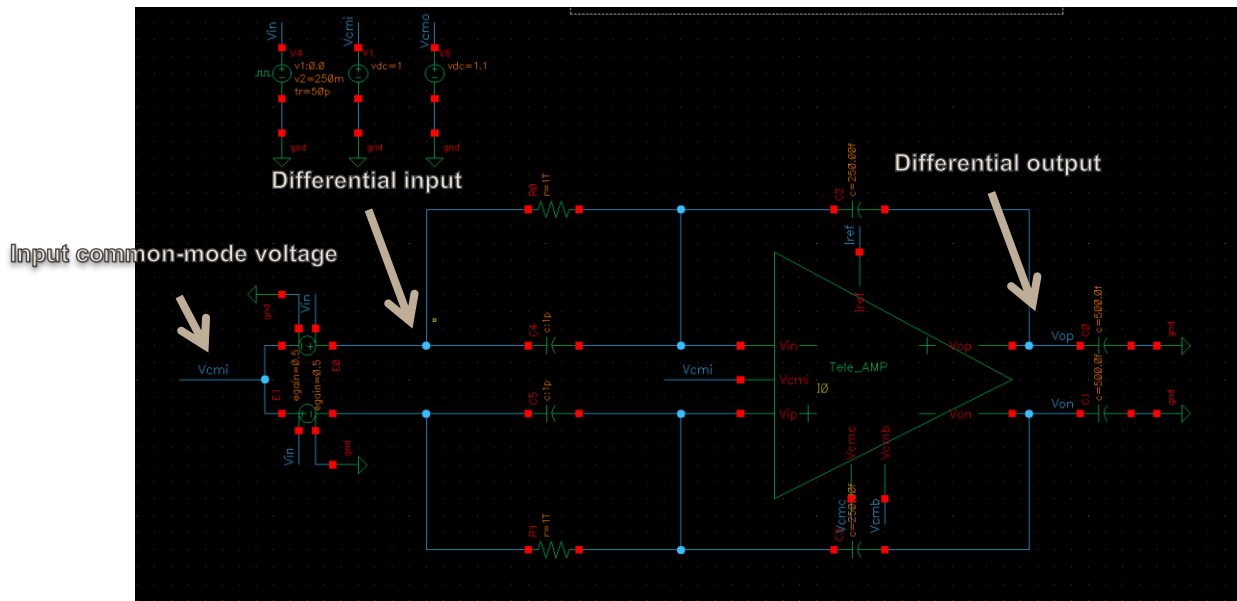
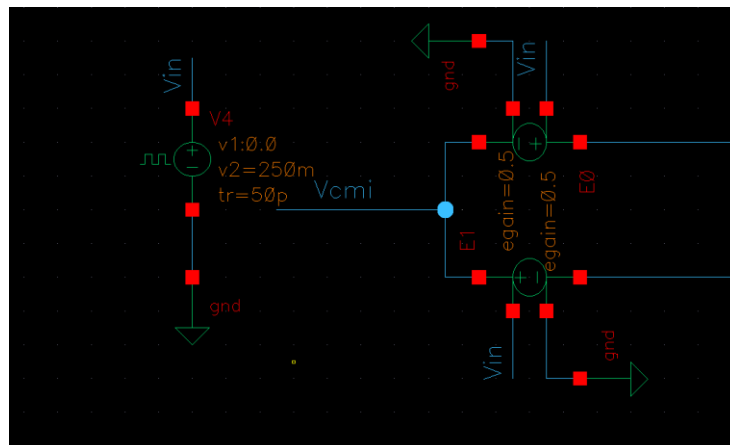


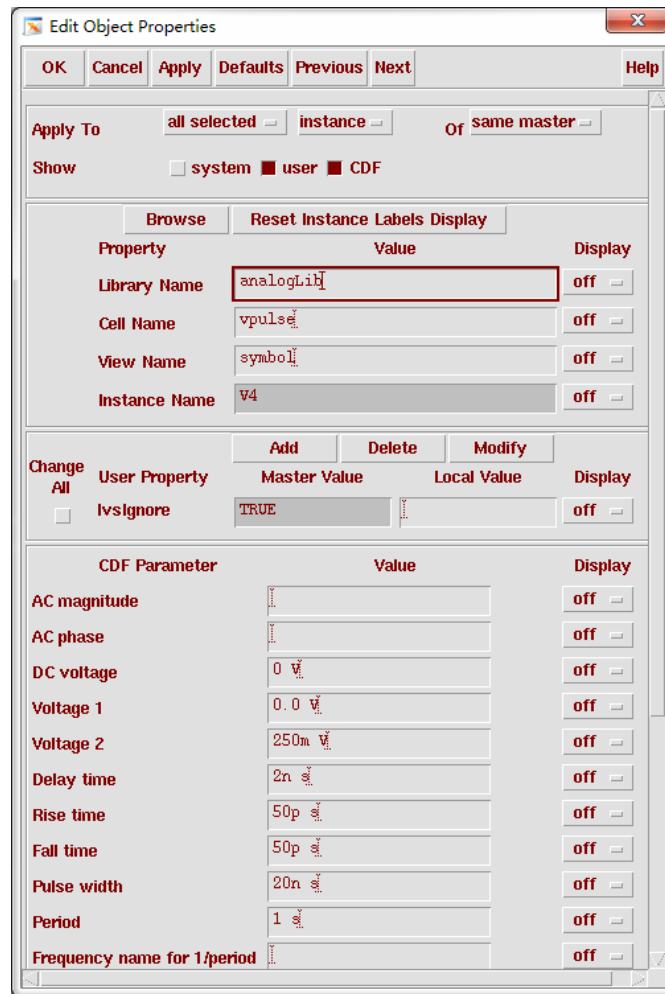
Settling time measurement



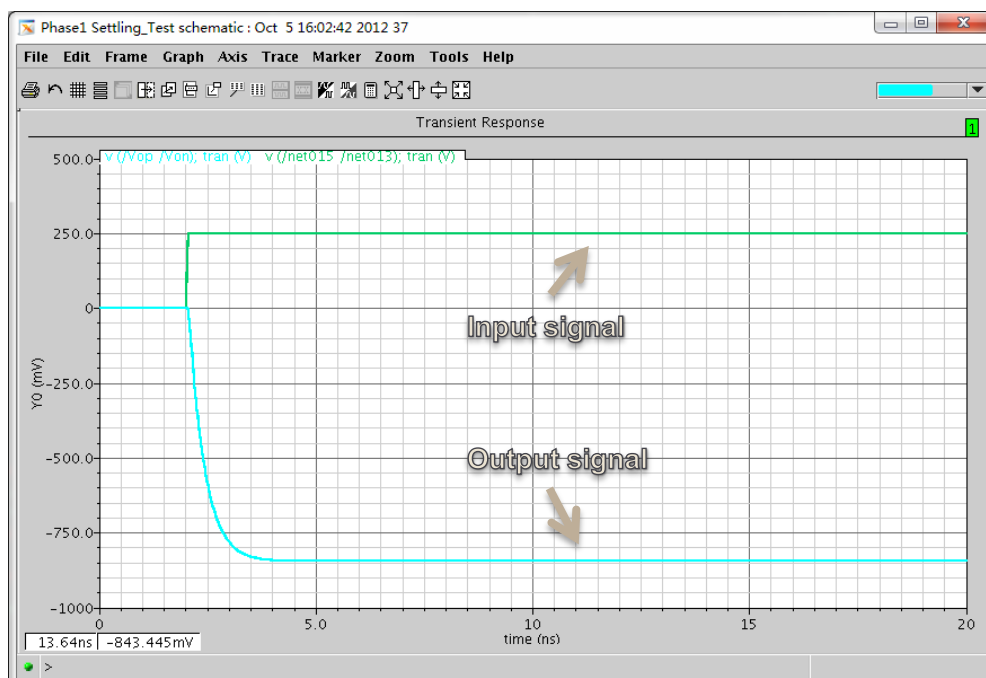
- Two VCVS from analogLib are used to generate differential input.
- Two $1T$ resistance are used to set input common mode of the amplifier



The input signal is a step signal at 2ns. Its setup is shown as follows.

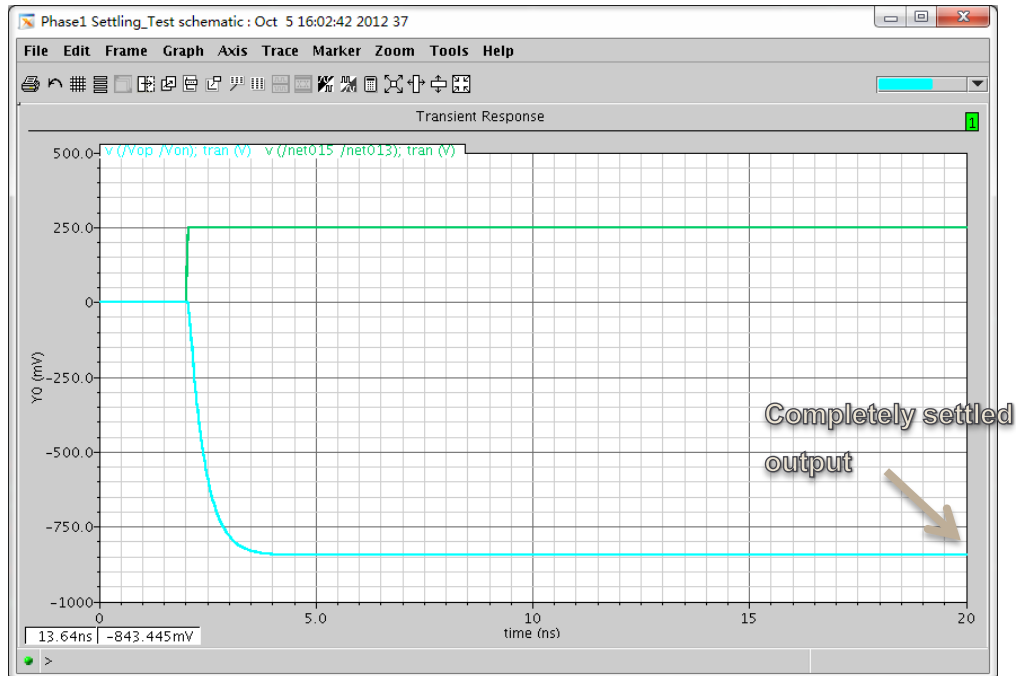


After transient simulation is done, you should see the following input and output signal.



You could see the output magnitude is almost 4x larger the input magnitude.

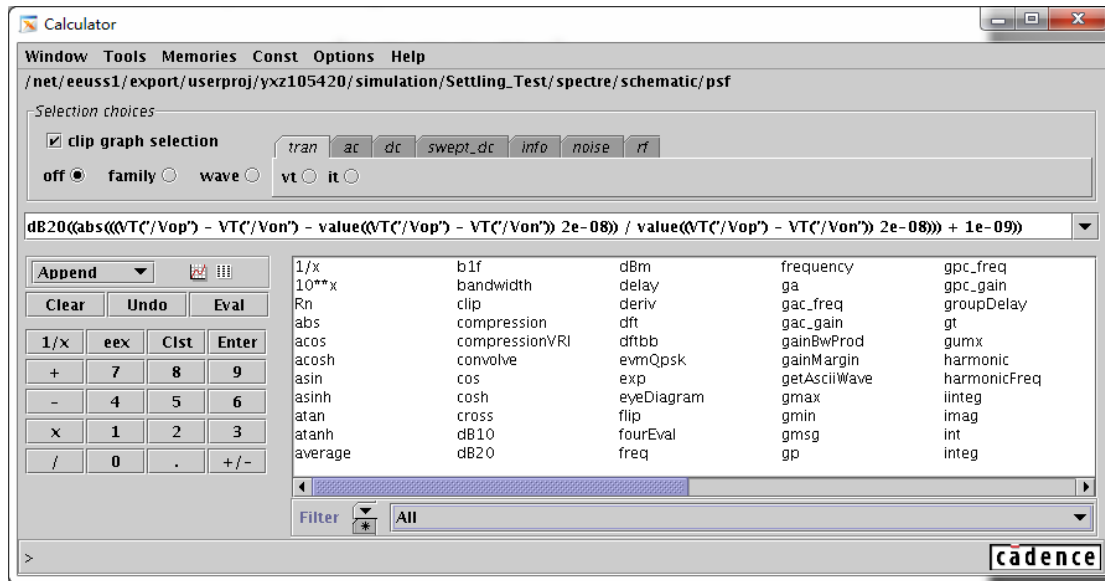
The next step is to generate settling error vs. time plot. Based on that, we could tell how long the settling time is.



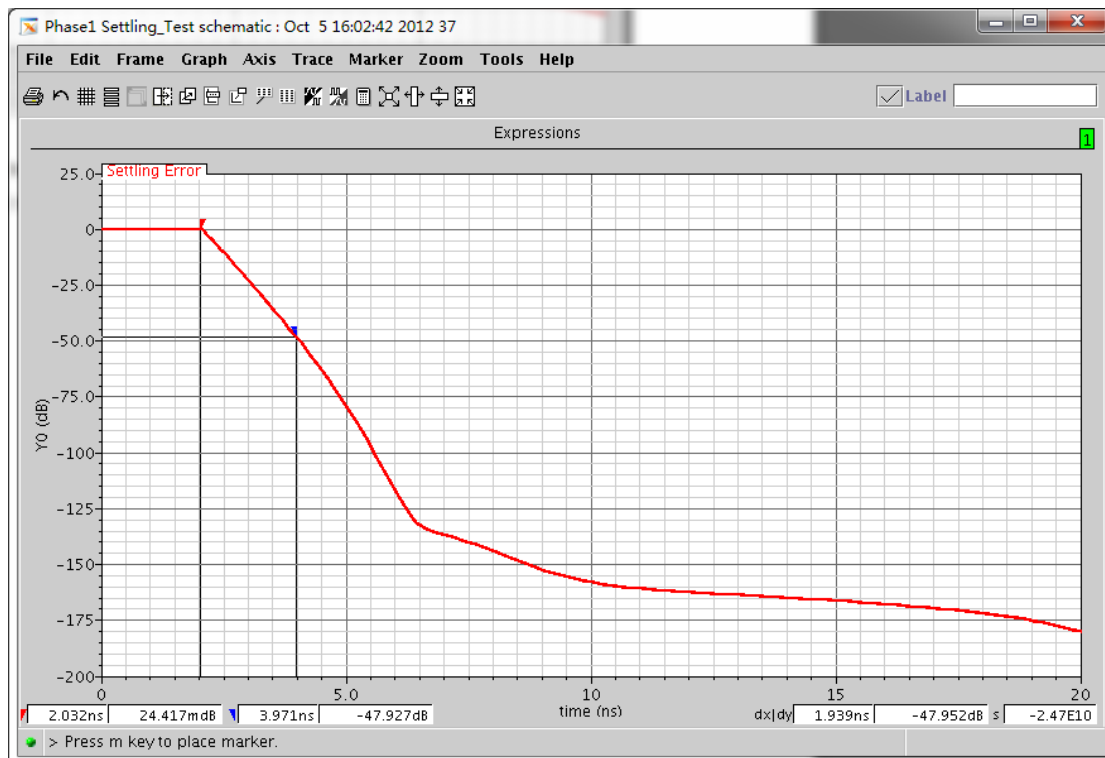
If we assume the output completely settles at 20nS, we could use the output at 20ns as the ideal amplifier output. The settling error will be calculated based on

$$E(t) = \text{abs} \left(\frac{V_{\text{out}}(t) - V_{\text{out}}(t = 20\text{ns})}{V_{\text{out}}(t = 20\text{ns})} \right)$$

We could use calculator to generate settling error in dB.



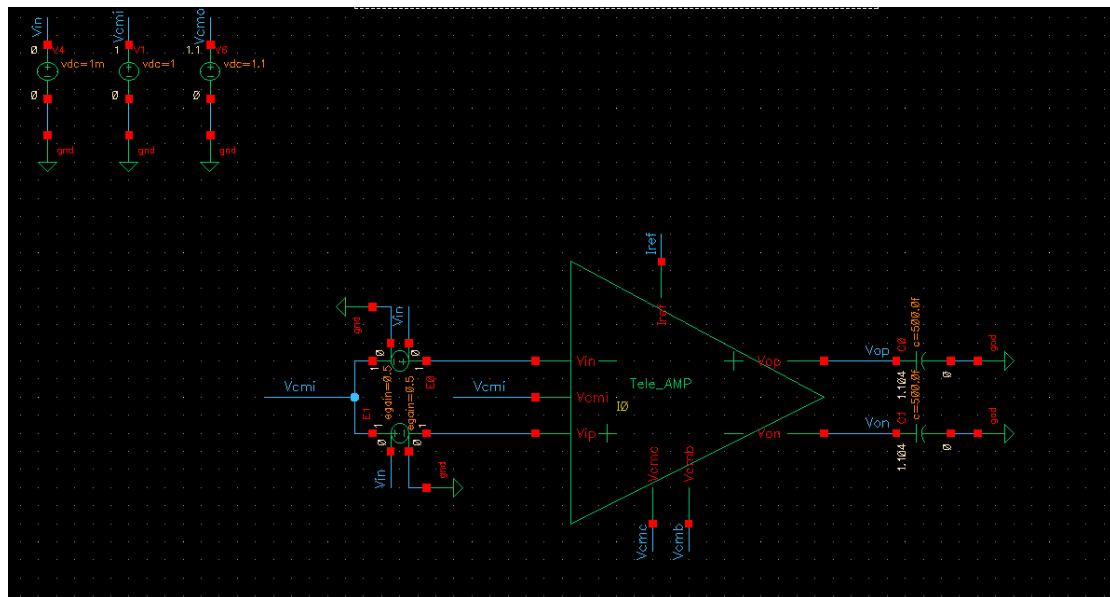
A small offset 1e-9 is added to prevent minus infinite settling error at 20ns.



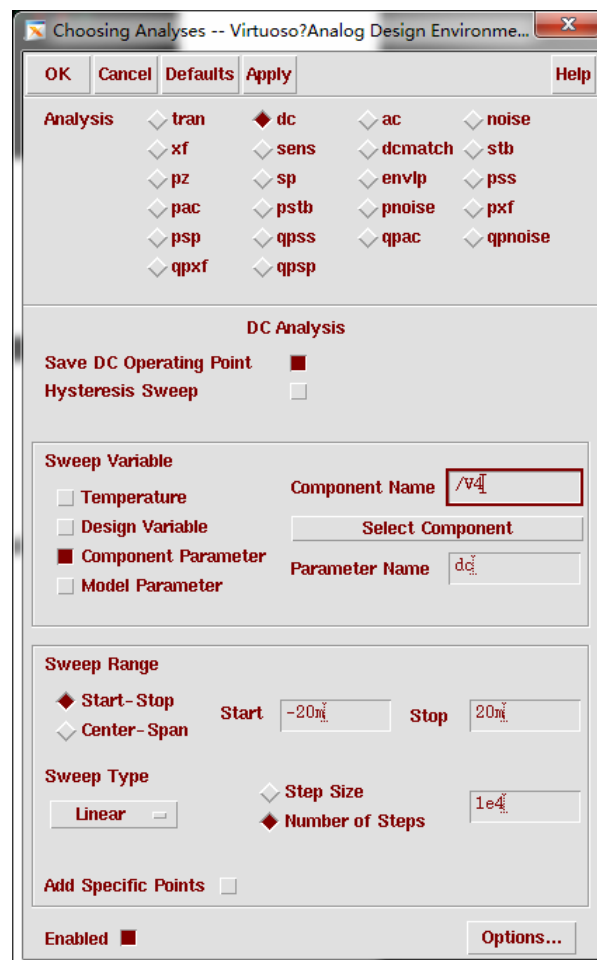
In order measure the settling time corresponding to 8 bit settling error, just find the time point where settling error = $-20 \cdot \log(1/2^8) = 48$ dB. For this example, settling time is about 1.939 ns.

Gain measurement

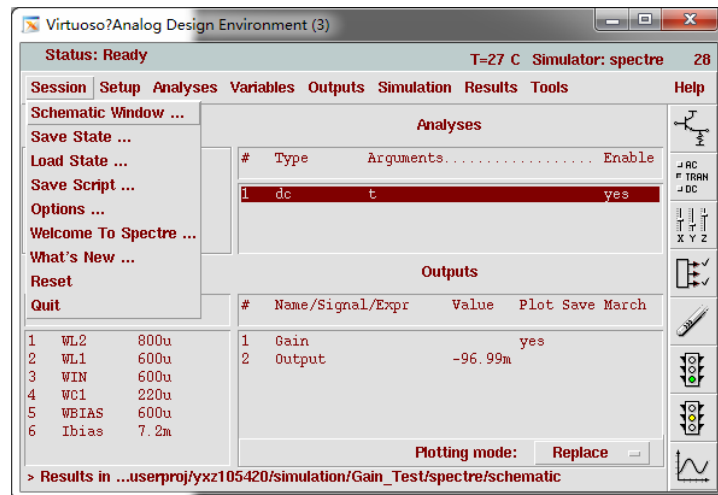
The test circuit setup is similar. The feedback part is removed.



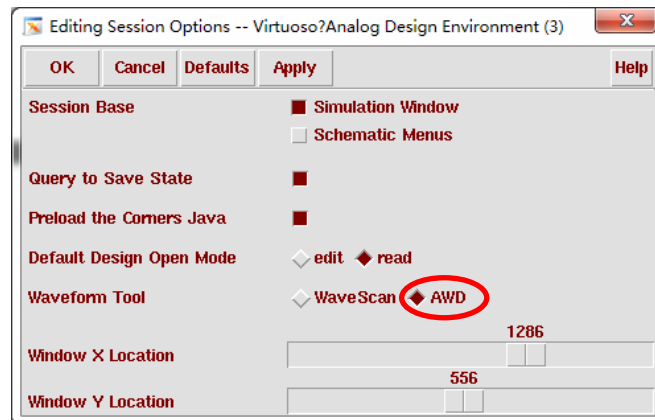
Here input is a DC voltage source. We use DC analysis to sweep its value from -20 mV to 20 mV.



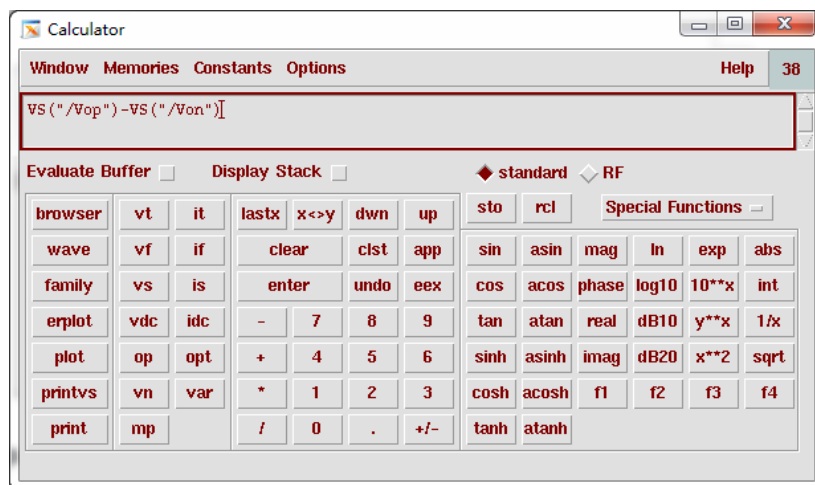
In order to generate gain vs. output plot, we need to use AWD as waveform tool.



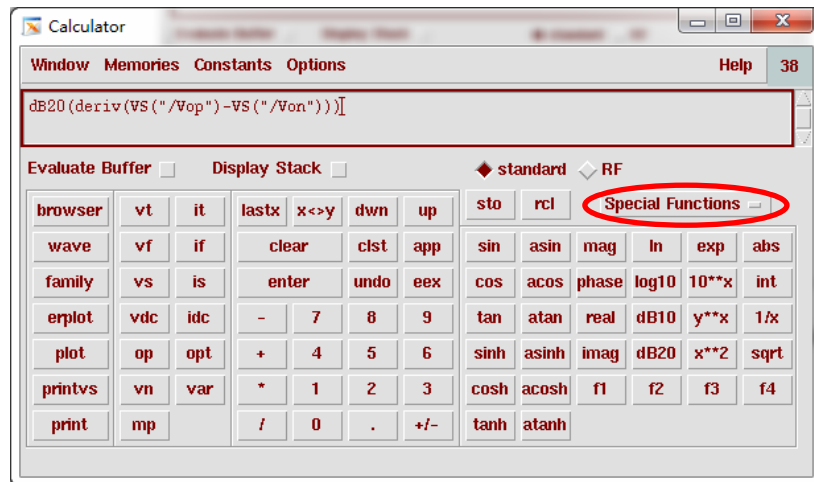
Go to Session -> Options



First plot the output voltage vs. input voltage



Then plot the open loop gain vs. input voltage using deriv function in Special Functions list



Double click the x axis, choose plot vs. (vop-von)

