Method for Measuring MOSFET Parameters

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Summary: This quick manual is involved with some simple tricks for measuring MOSFET Parameters, and also some plots of the characteristics of MOSFETs. All the examples are for just nMOS FET test only, and the readers can follow it when they deal with pMOS.

Keywords: MOSFET, transconductance efficiency.

I n this manual, we use IBM 7HP which is 0.18 BiCMOS technology, and the simple details are just as below. [2]

IBM 180-nm Technology Highlights

Category	Base Technology CMOS 7SF	Related Technologies CMOS 7RF	BiCMOS 7WL	BiCMOS 7HP
Process	Industry-standard 180-nm CMOS	CMOS 7SF with passive devices	CMOS 7RF with 60-GHz bipolar devices	CMOS 7SF with120-GHz bipolar devices
Wiring	Copper or aluminum	Copper and aluminum with analog metal	Copper and aluminum with analog metal	Copper with analog metal
Bipolar devices	N/A	N/A	3 HBTs, wireless focus	2 HBTs, high-speed optical/digital focus

Table.01 IBM 0.18um Technology Highlights.

Due to the specs in the IBM document, we can get the information as Table. [2]So BiCMOS 7HP includes the Base Technology CMOS 7SF CMOS devices libraries. Then the test result shall be same.

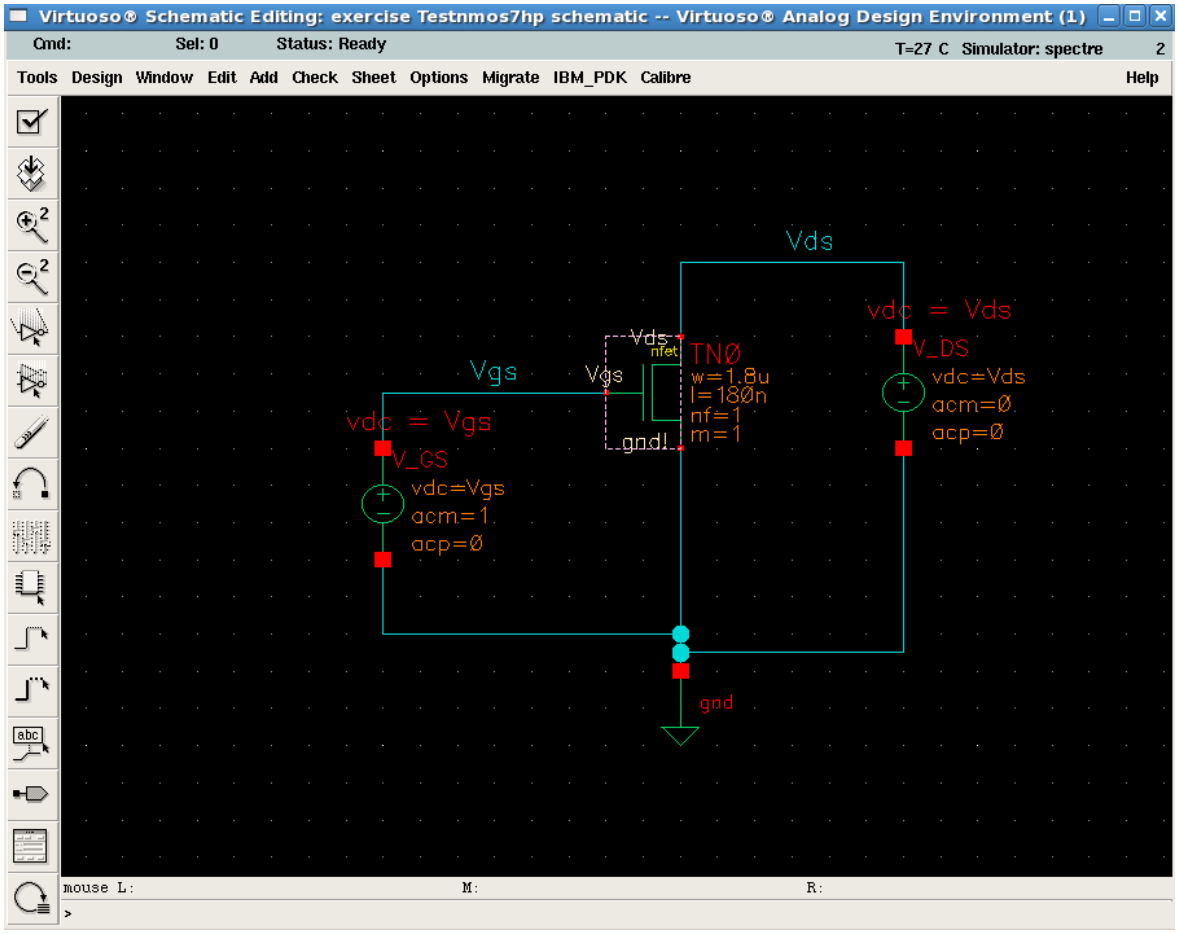


FIG 01. The Testing Circuit, Nmos From IBM7HP

The whole circuit is just settled as above. The specs are just as below,

W=1.8um, L=180nm

Substrate node is connected to the gnd! (which is ground global).

Two Vdcs are settled as Vgs and Vds.

Then “Check and Save” the circuit you just settled. After you have done this, then enter the Analog Design Environment to begin with setting up the simulation environment.

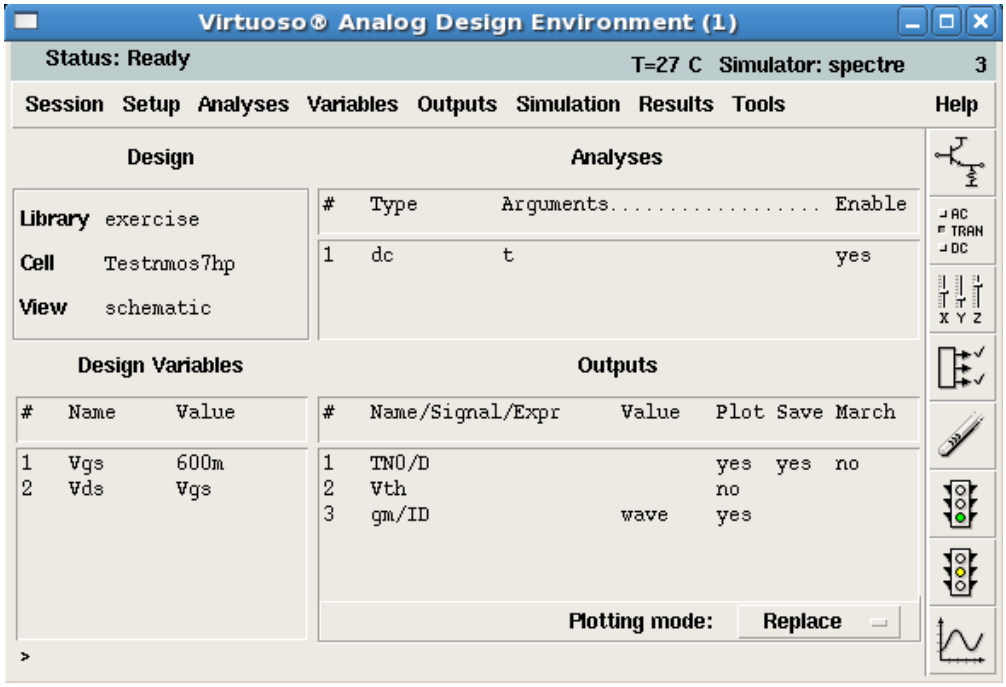
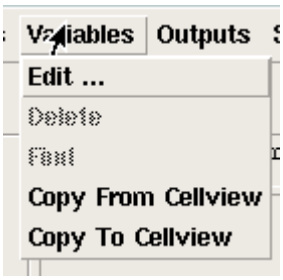
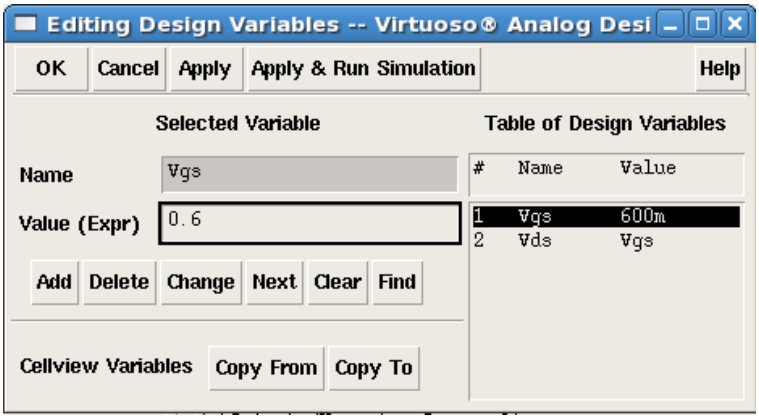


Fig. 02. ADE Setting.



The variables Vgs and Vds are the ones you just set in the schematic and you can get them into ADE by just click on Variables --- Copy From Cellview.

And you shall give the Vgs and Vds an initial value. I just set the Vds = = Vgs and Vgs with an initial value equal to 600mV, since we estimate by experience that the Vth for this nMOS shall be around 460 to 520mV, and we want to keep this circuit working in the status of moderate inversion and saturation area.



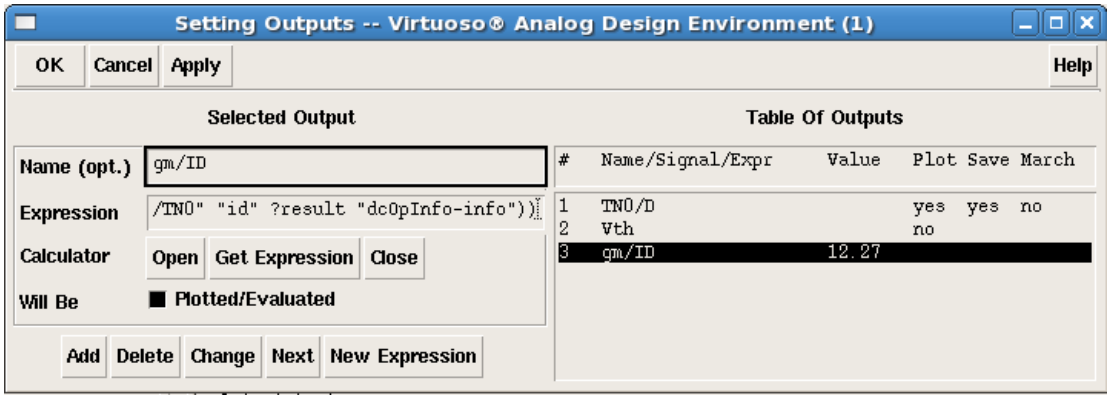
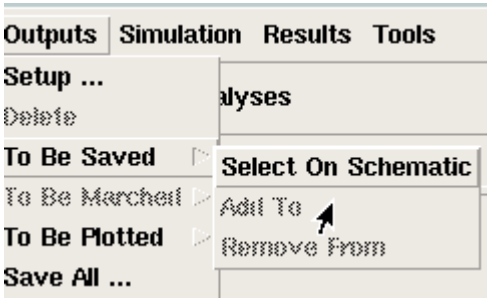


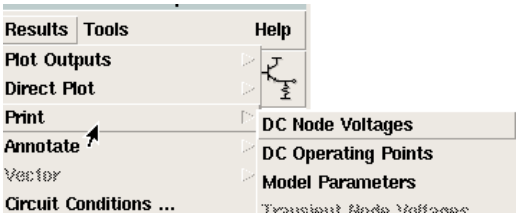
Fig. Setting of Outputs

Setting of the outputs of the design as following, To Be Saved the ID, which you just click on the drain pin of the transistor TN0, and you might not select to plot it.



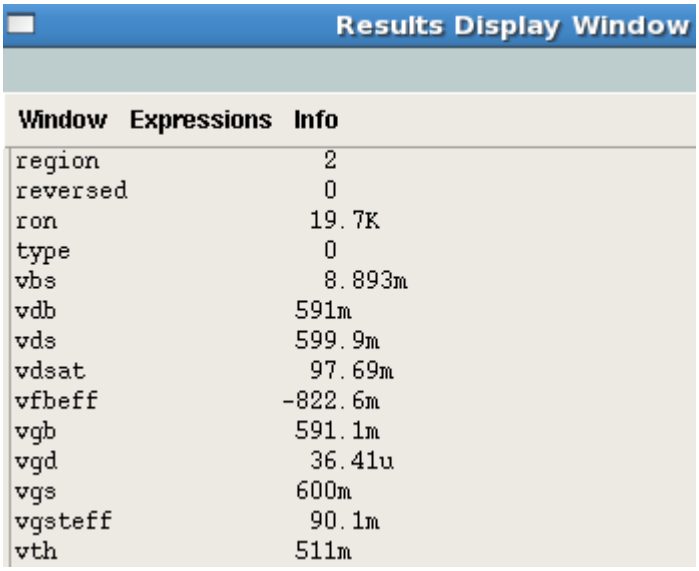
And then the first step is done.

Netlist and Run the design.



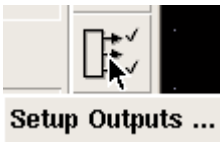
If everything goes well, then you would get no error or strange things happening.

Click on Results----Print----DC Operating Points, and then select the TN0, which is the nMOS in schematic we just draw. And then we can get the dc parameter in this operating point.

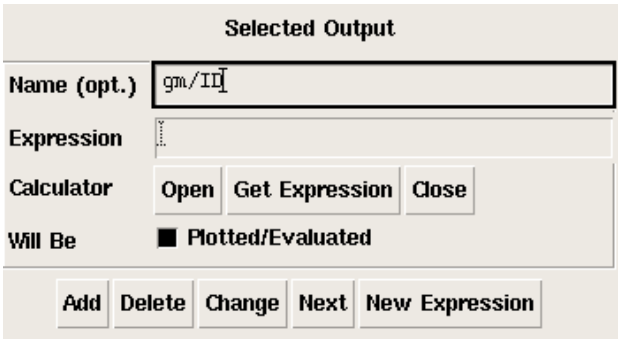


And we can find that the Vth is 511mV, so the VEFF = 600Mv-511Mv=89mV, in the region of moderate inversion area [1, P114], and the region is 2 which is saturation area in cadence.

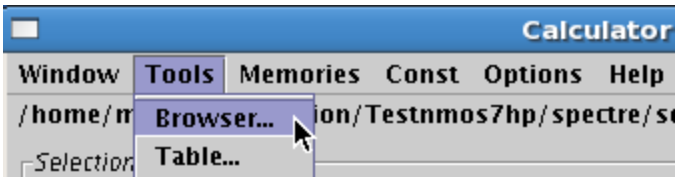
In the next step, we shall deal with setting for plotting transconductance efficiency, which is gm/ID. Then click on the Setup Outputs.



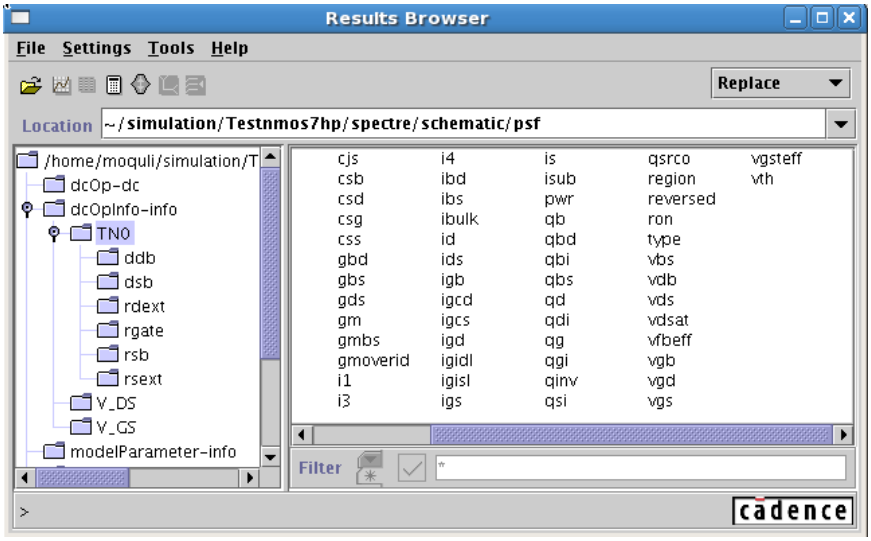
Name the transconductance efficiency as gm/ID just as [1] mentioned. Then click on the Calculator --- Open button below.



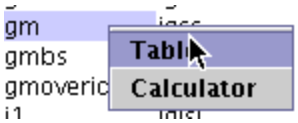
Then the calculator will show above all the windows. We want to find the gm, so click on Tools --- Brower to find the parameters we saved before in cadence files.

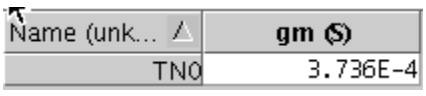


Then we can see lots of catalogs in the left area of the browser, just like gds, vth and other stuff, they just have an operating point value which is static value but not range value if you select the Design Variable in Sweep Variable when you set the Choosing Analyses.

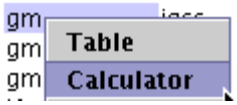


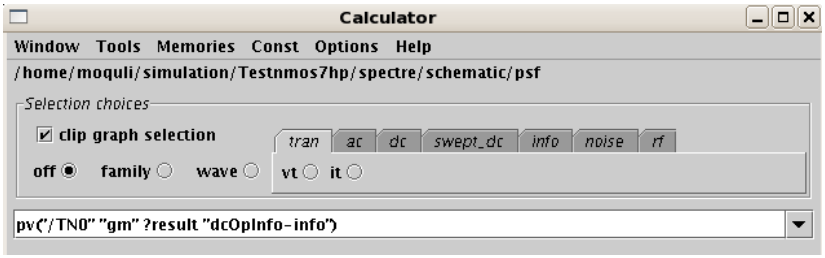
You can try this by right clicking on the gm and select Table, and you will get the table value of gm (S) as the one on the right.



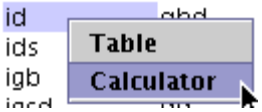


In here, we care about the gm, so we right click on the gm and select Calculator. Then the expression of the gm has been added in the calculator.

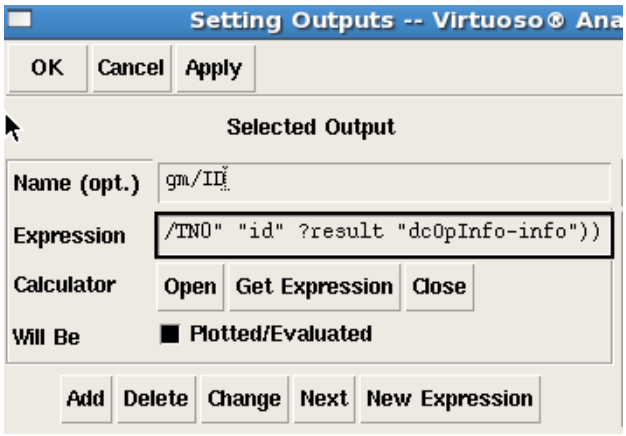




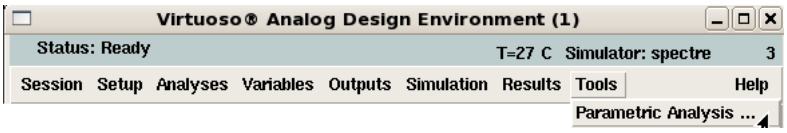
Then we can use "/" for division, and in the same method above we can add the Id in the position of denominator.

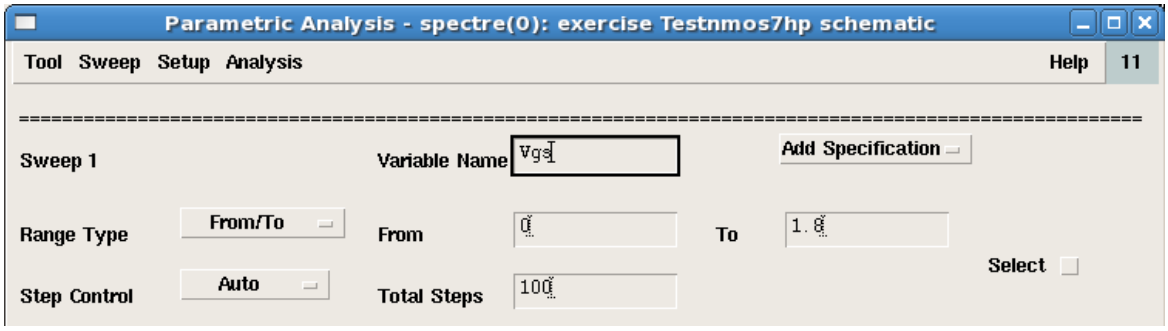


Then let the Setting Outputs window show up in the front, click on Get Expression button then click on the Add button below. Then we finish editing the expression of transconductance efficiency as gm/ID in cadence.

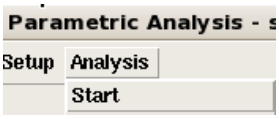


Now, you shall click on Tools --- Parametric Analysis, and you can get the window right as below.

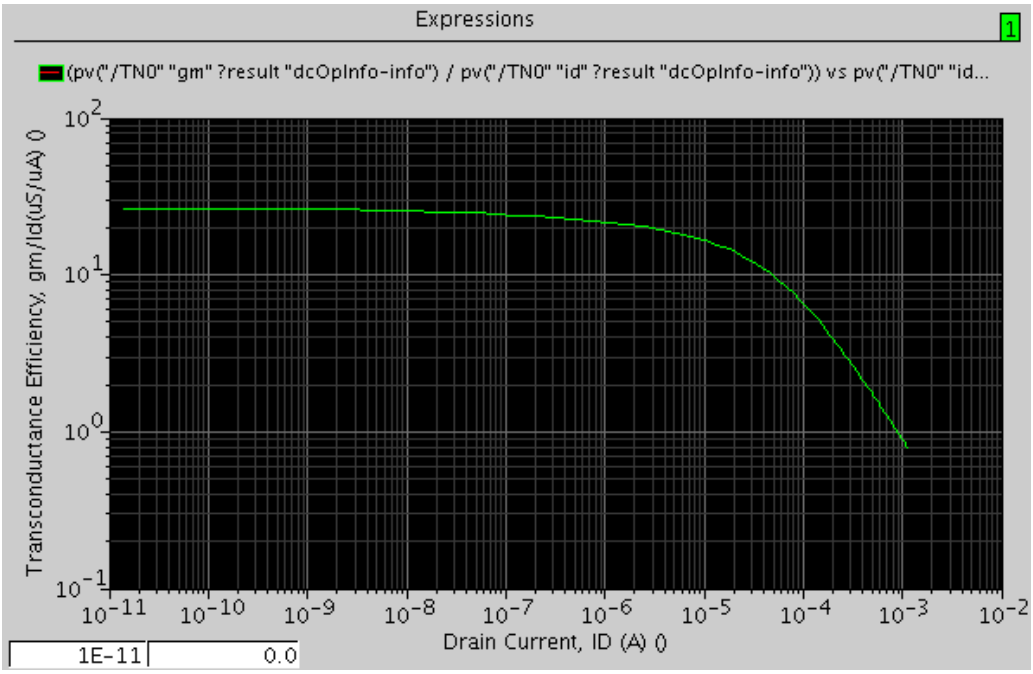


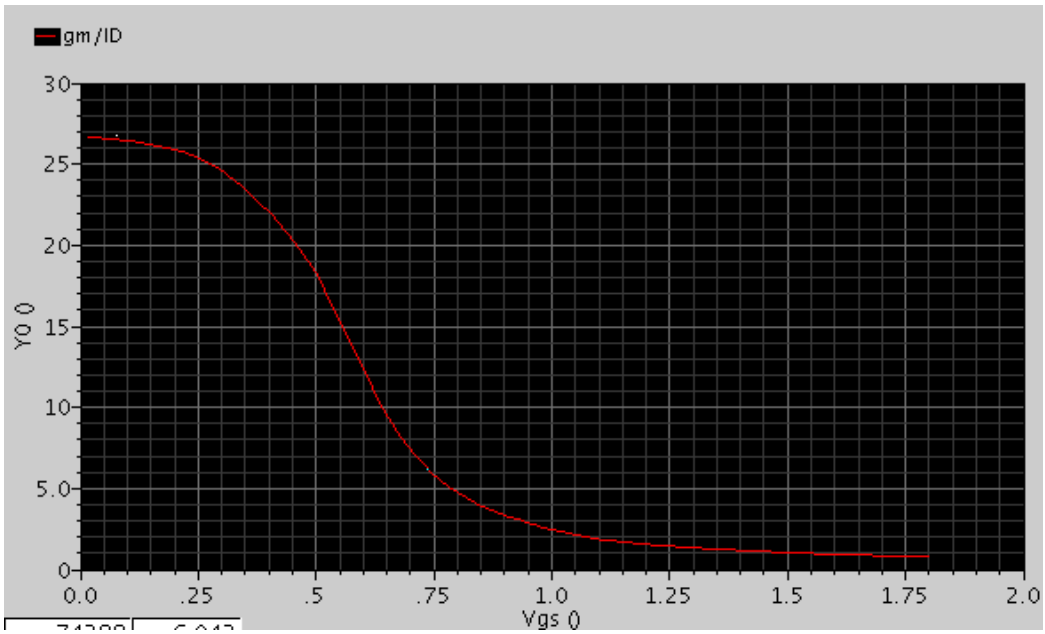


We want Vgs to change from 0V to 1.8V and want to check the Vgs in 100 steps, and click on Analysis --- Start to run the testing.



After the running of the measurement, and we can change the Axis in X and Y into logarithm scaling then we can get the testing result just as below.





Also, we can get gm/Id versus Vgs like above.

References

[1] David M. Binkley, *Tradeoffs and Optimization in Analog CMOS Design*, John Wiley and Sons Ltd., 2008.

[2] Foundry technologies, 180-nm CMOS, RF CMOS and SiGe BiCMOS, High-performance devices for a wide range of applications, http://rfic.eecs.berkeley.edu/files/180nm-techbrief02.pdf.