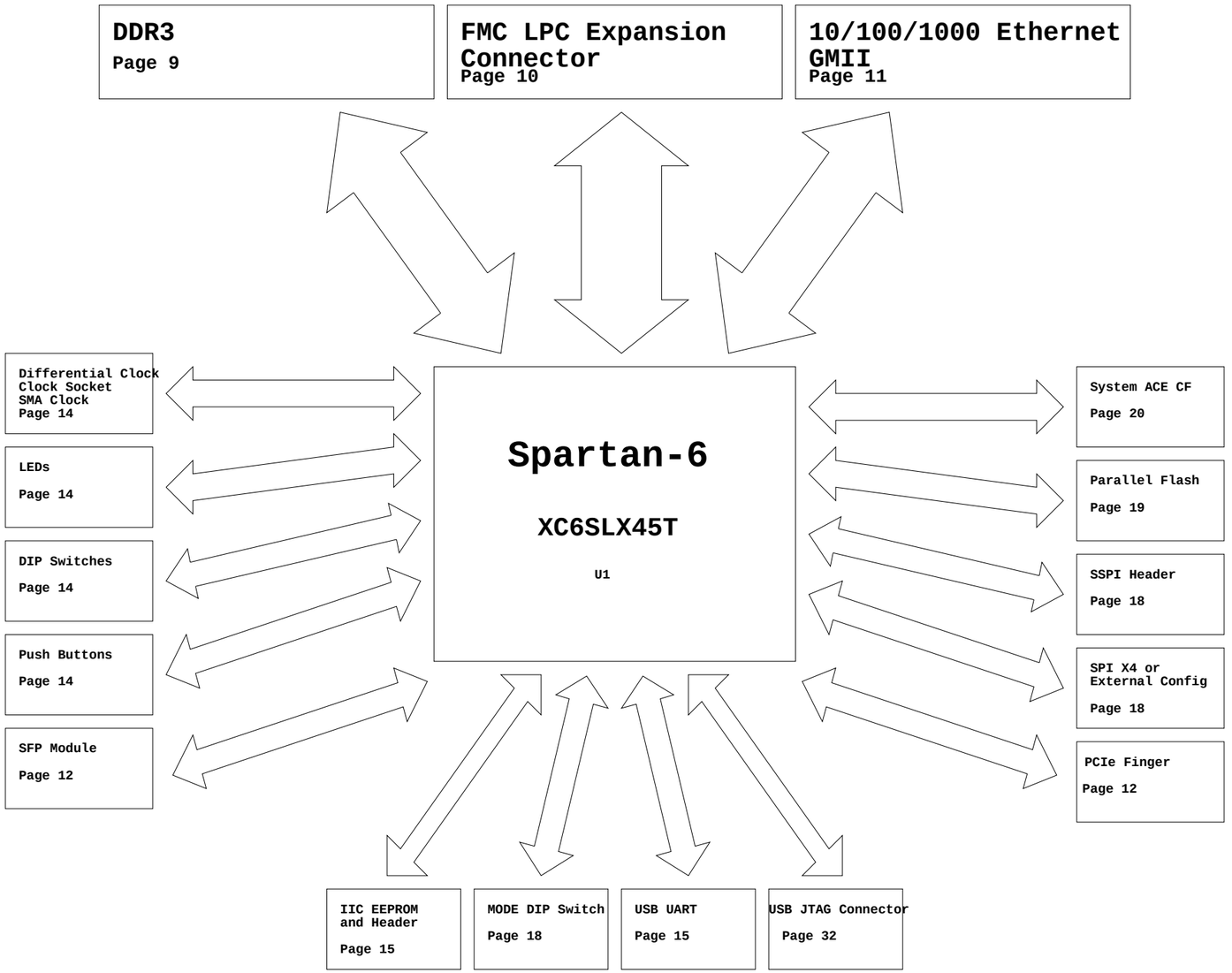
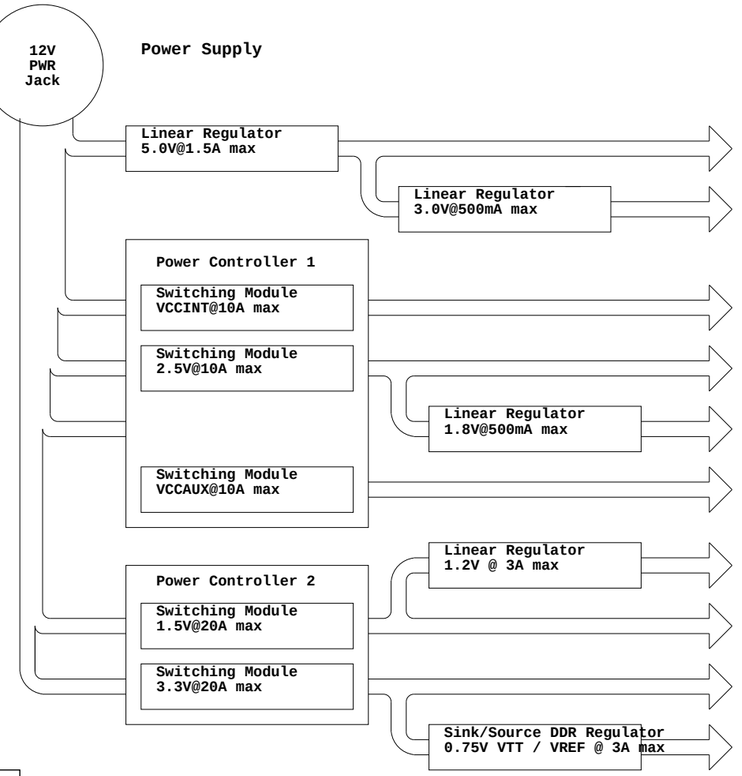
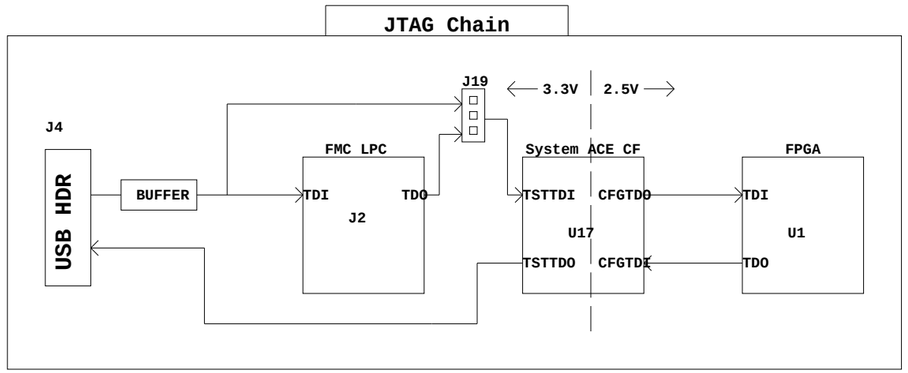


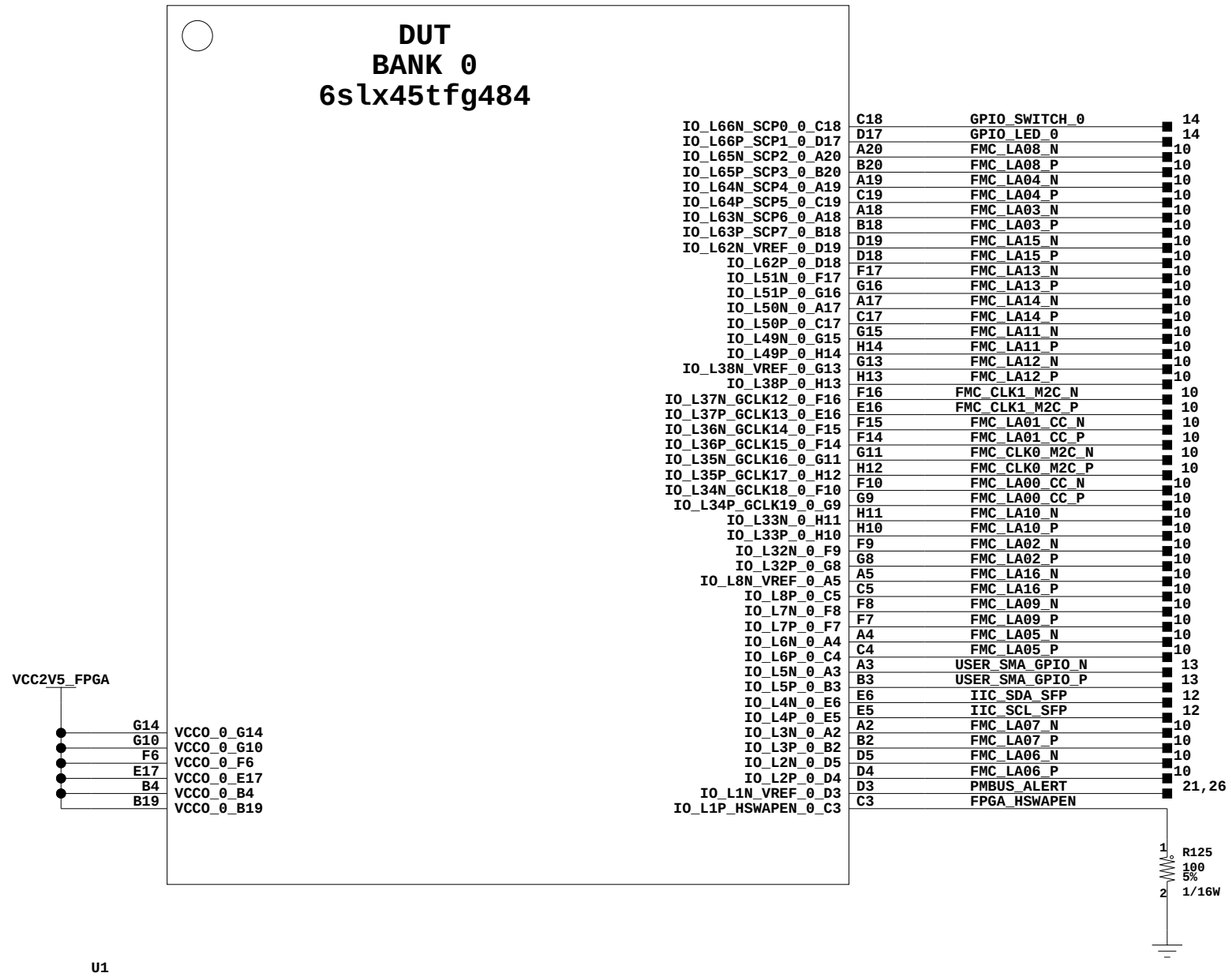




IIC Addressing	
U4	0b1010100
J2	EEPROM: 0b1010010 Other Devices: 0bXXXXX10

XILINX

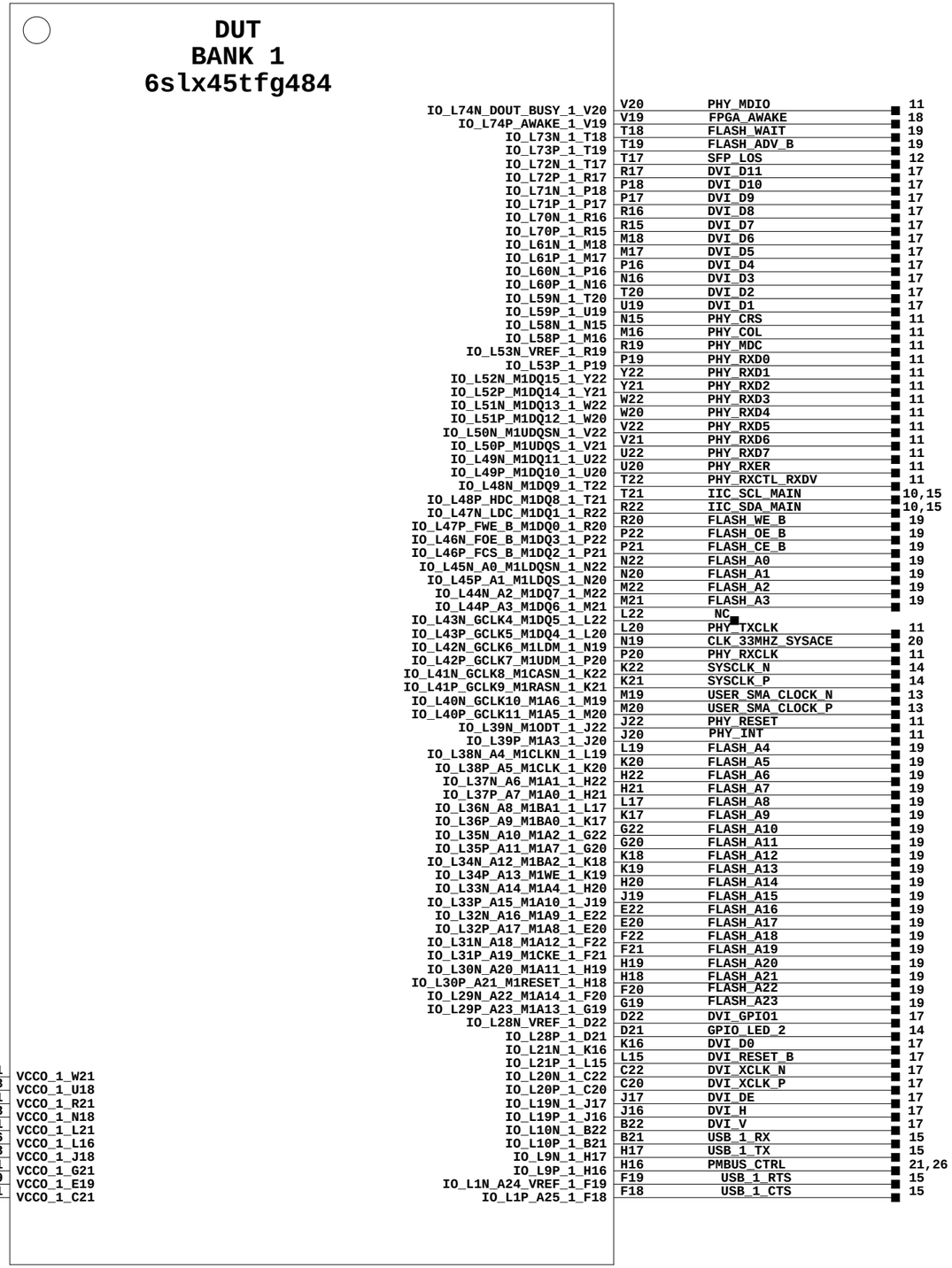
Title:	SP605 Block Diagram SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-25-2009_10:32	Ver:	D
Sheet Size: B		Rev:	02
Sheet	1 of 35	Drawn By	BF



FPGA Bank 0

XILINX

Title:	FPGA Bank 0 SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:04	Ver:	D
Sheet Size: B		Rev:	02
Sheet	2 of 35	Drawn By	BF



FPGA Bank 1

Title:	FPGA Bank 1 SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:04	Ver:	D
Sheet Size: B		Rev:	02
Sheet	3 of 35	Drawn By	BF

DUT
BANK 2
6slx45tfg484

IO_L65N_CSO_B_2_AA3	AA3	SPI_CS_B	18
IO_L65P_INIT_B_2_Y4	Y4	FPGA_INIT_B	14,20
IO_L64N_D9_2_U6	U6	FLASH_D9	19
IO_L64P_D8_2_T7	T7	FLASH_D8	19
IO_L63N_2_AB4	AB4	GPIO_LED_1	14
IO_L63P_2_AA4	AA4	IIC_SDA_DVI	16,17
IO_L62N_D6_2_AB5	AB5	FLASH_D6	19
IO_L62P_D5_2_Y5	Y5	FLASH_D5	19
IO_L60N_2_Y6	Y6	GPIO_SWITCH_1	14
IO_L60P_2_W6	W6	GPIO_SWITCH_2	14
IO_L59N_2_R8	R8	FMC_LA20_N	10
IO_L59P_2_R9	R9	FMC_LA20_P	10
IO_L58N_2_W8	W8	FMC_LA22_N	10
IO_L58P_2_V7	V7	FMC_LA22_P	10
IO_L57N_2_U8	U8	PHY_TXER	11
IO_L57P_2_T8	T8	PHY_TXCTL_TXEN	11
IO_L50N_2_V9	V9	FMC_LA23_N	10
IO_L50P_2_U9	U9	FMC_LA23_P	10
IO_L49N_D4_2_AB6	AB6	FLASH_D4	19
IO_L49P_D3_2_AA6	AA6	FLASH_D3	19
IO_L48N_RDWR_B_VREF_2_Y8	Y8	SFP_TX_DISABLE_FPGA	12
IO_L48P_D7_2_W9	W9	FLASH_D7	19
IO_L47N_2_AB7	AB7	PHY_TXC_GTXCLK	11
IO_L47P_2_Y7	Y7	NC	
IO_L46N_2_U10	U10	PHY_TXD0	11
IO_L46P_2_T10	T10	PHY_TXD1	11
IO_L45N_2_AB8	AB8	PHY_TXD2	11
IO_L45P_2_AA8	AA8	PHY_TXD3	11
IO_L44N_2_Y10	Y10	PMBUS_DATA	21,26
IO_L44P_2_W10	W10	PMBUS_CLK	21,26
IO_L43N_2_AB9	AB9	PHY_TXD4	11
IO_L43P_2_Y9	Y9	PHY_TXD5	11
IO_L42N_2_W11	W11	FMC_LA21_N	10
IO_L42P_2_V11	V11	FMC_LA21_P	10
IO_L41N_VREF_2_AB10	AB10	FMC_LA27_N	10
IO_L41P_2_AA10	AA10	FMC_LA27_P	10
IO_L40N_2_Y12	Y12	PHY_TXD6	11
IO_L40P_2_W12	W12	PHY_TXD7	11
IO_L32N_GCLK28_2_AB11	AB11	FMC_LA17_CC_N	10
IO_L32P_GCLK29_2_Y11	Y11	FMC_LA17_CC_P	10
IO_L31N_GCLK30_D15_2_AB12	AB12	FLASH_D15	19
IO_L31P_GCLK31_D14_2_AA12	AA12	FLASH_D14	19
IO_L30N_GCLK0_USERCCLK_2_AB13	AB13	USER_CLOCK	14
IO_L30P_GCLK1_D13_2_Y13	Y13	FLASH_D13	19
IO_L29N_GCLK2_2_U12	U12	FMC_LA18_CC_N	10
IO_L29P_GCLK3_2_T12	T12	FMC_LA18_CC_P	10
IO_L23N_2_U15	U15	FMC_LA29_N	10
IO_L23P_2_T15	T15	FMC_LA29_P	10
IO_L22N_2_T11	T11	FMC_LA19_N	10
IO_L22P_2_R11	R11	FMC_LA19_P	10
IO_L21N_2_AB15	AB15	FMC_LA30_N	10
IO_L21P_2_Y15	Y15	FMC_LA30_P	10
IO_L20N_2_Y14	Y14	FMC_LA25_N	10
IO_L20P_2_W14	W14	FMC_LA25_P	10
IO_L19N_2_AB16	AB16	FMC_LA28_N	10
IO_L19P_2_AA16	AA16	FMC_LA28_P	10
IO_L18N_2_W13	W13	IIC_SCL_DVI	16,17
IO_L18P_2_V13	V13	FMC_PWR_GOOD_FLASH_RST_B	7,10,19
IO_L17N_2_W15	W15	GPIO_LED_3	14
IO_L17P_2_Y16	Y16	FMC_PRSNT_M2C_L	10
IO_L16N_VREF_2_U13	U13	FMC_LA26_N	10
IO_L16P_2_U14	U14	FMC_LA26_P	10
IO_L15N_2_AB17	AB17	FMC_LA33_N	10
IO_L15P_2_Y17	Y17	FMC_LA33_P	10
IO_L14N_D12_2_AB18	AB18	FLASH_D12	19
IO_L14P_D11_2_AA18	AA18	FLASH_D11	19
IO_L13N_D10_2_AB19	AB19	FLASH_D10	19
IO_L13P_M1_2_Y19	Y19	FPGA_M1	18
IO_L12N_D2_MISO3_2_T14	T14	FPGA_D2_MISO3	18,19
IO_L12P_D1_MISO2_2_R13	R13	FPGA_D1_MISO2	18,19
IO_L6N_2_AB14	AB14	FMC_LA24_N	10
IO_L6P_2_AA14	AA14	FMC_LA24_P	10
IO_L5N_2_Y18	Y18	FMC_LA32_N	10
IO_L5P_2_W17	W17	FMC_LA32_P	10
IO_L4N_VREF_2_V15	V15	FMC_LA31_N	10
IO_L4P_2_U16	U16	FMC_LA31_P	10
IO_L3N_MOSI_CSI_B_MISO0_2_AB20	AB20	FPGA_MOSI_CSI_B_MISO0	18
IO_L3P_D0_DIN_MISO1_2_AA20	AA20	FPGA_D0_DIN_MISO_MISO1	18,19
IO_L2N_CMPMOSI_2_W18	W18	FPGA_CMP_MOSI	18
IO_L2P_CMPCLK_2_V17	V17	FPGA_CMP_CLK	18
IO_L1N_M0_CMPMISO_2_AA21	AA21	FPGA_M0_CMP_MISO	18
IO_L1P_CCLK_2_Y20	Y20	FPGA_CCLK	18

VCC2V5

R10 4.7K 5% 1/16W

R285 140 1% 1/16W

C260 NPO 50V 120PF

VCC2V5_FPGA

W5	VCCO_2_W5
V8	VCCO_2_V8
V16	VCCO_2_V16
V12	VCCO_2_V12
T9	VCCO_2_T9
T13	VCCO_2_T13
AB3	VCCO_2_AB3
AA7	VCCO_2_AA7
AA19	VCCO_2_AA19
AA15	VCCO_2_AA15
AA11	VCCO_2_AA11

U1

FPGA Bank 2

XILINX

Title:	FPGA Bank 2 SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
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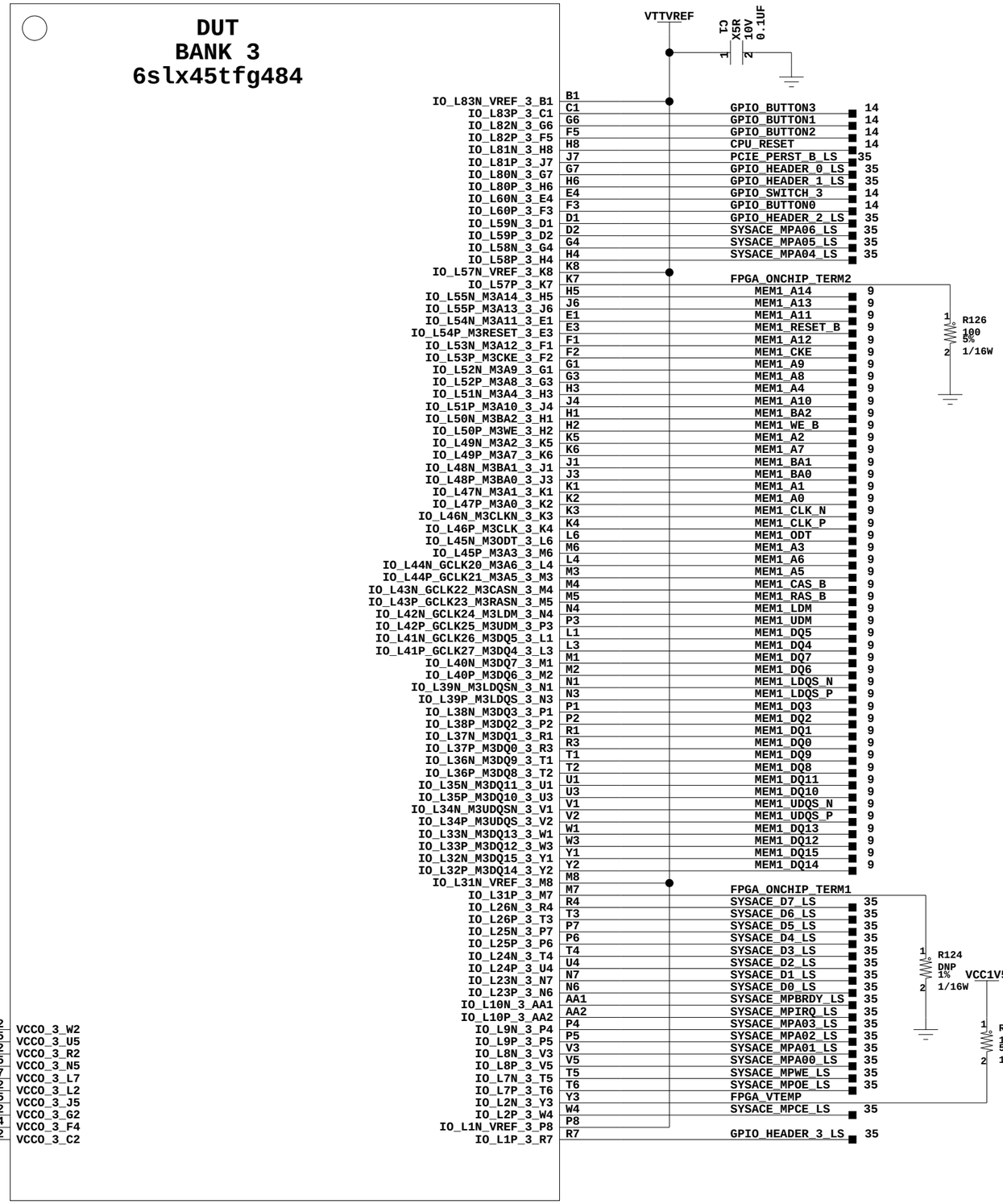
Sheet Size: B		Rev:	02
Sheet	4 of 35	Drawn By	BF



FPGA Bank 3

XILINX

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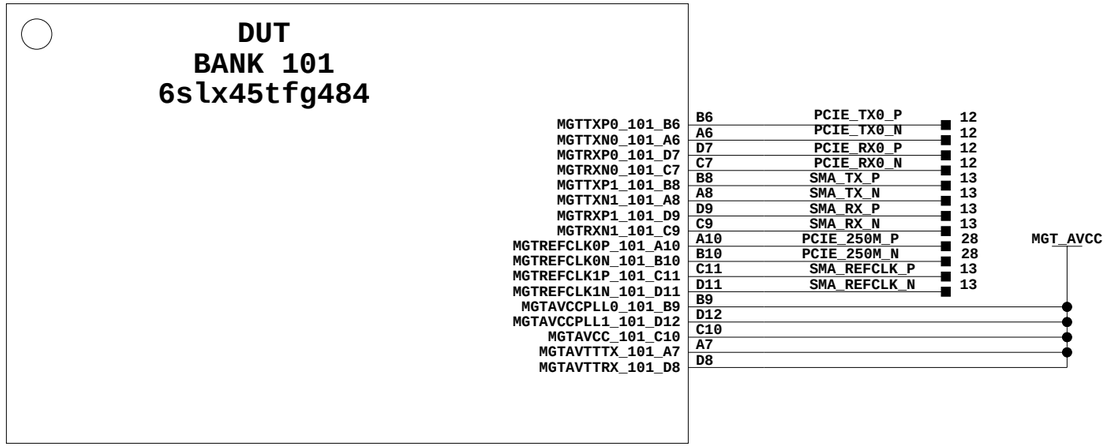
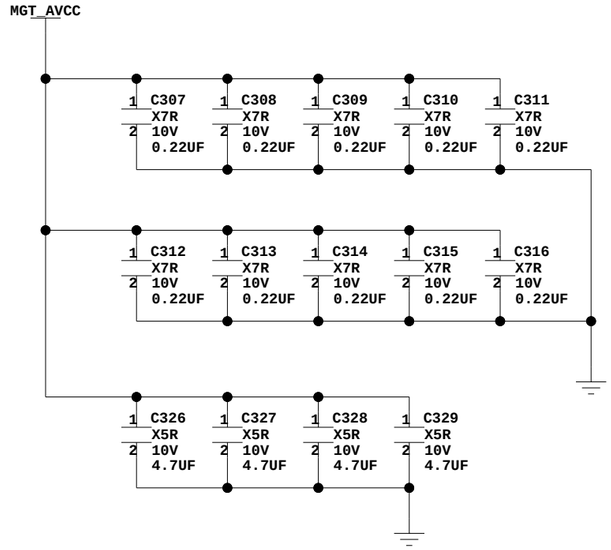
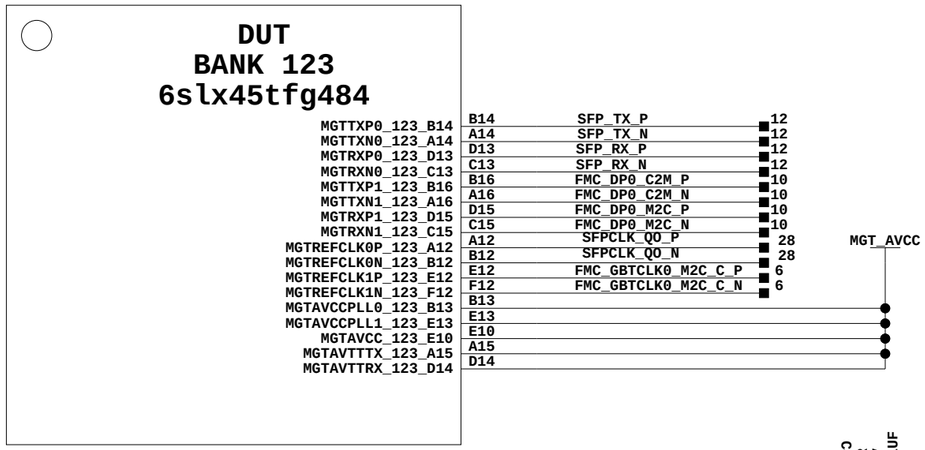
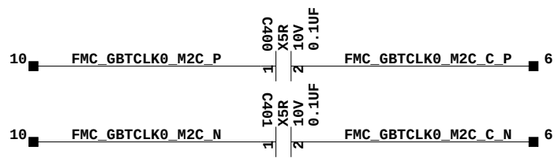
Date:	9-18-2009_15:04	Ver:	D
Sheet Size: B		Rev:	02
Sheet	5 of 35	Drawn By	BF





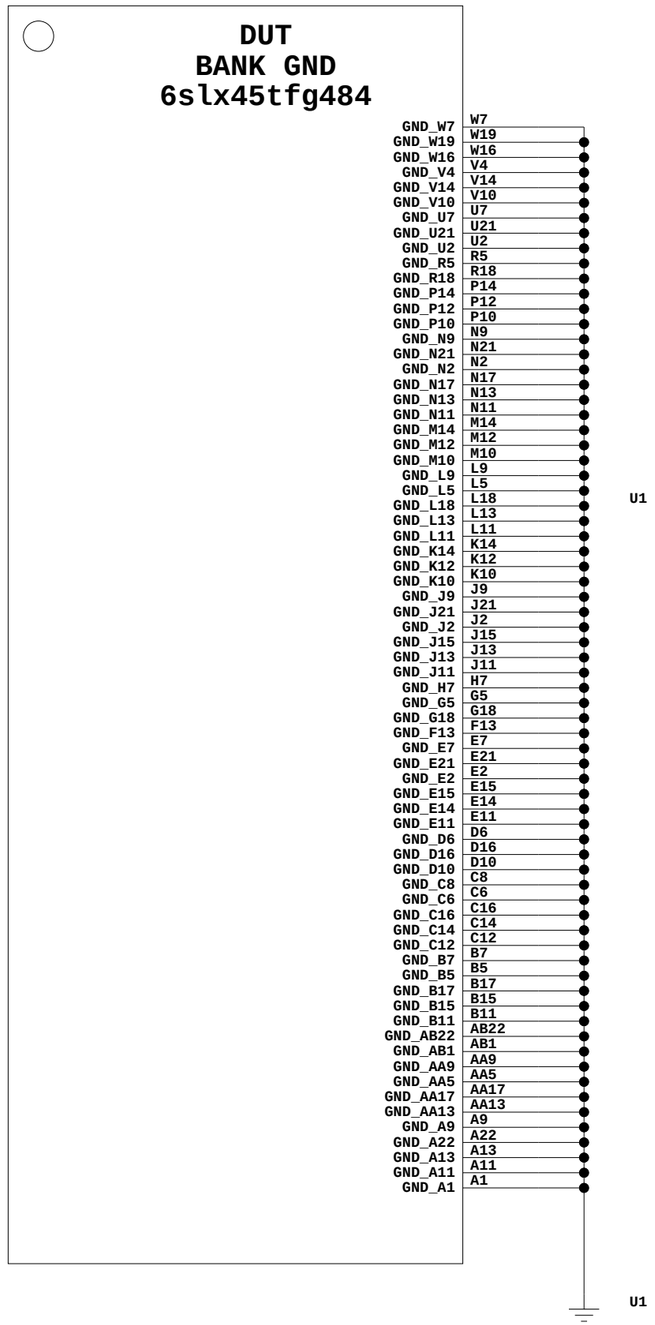


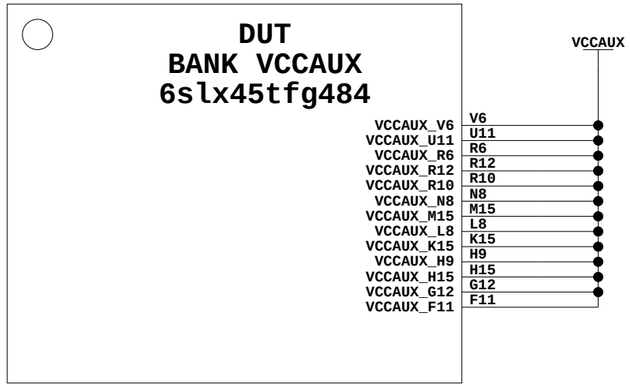


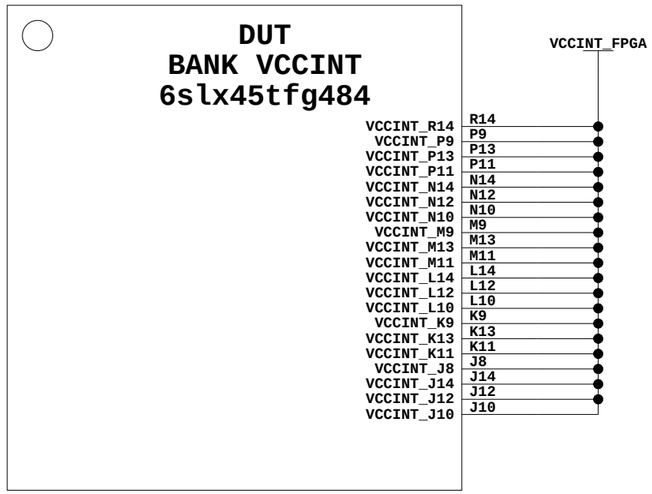
MGT Banks

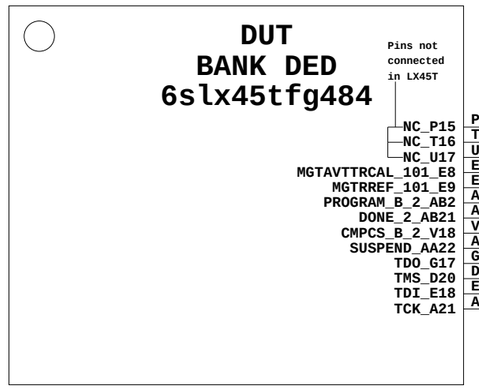
XILINX

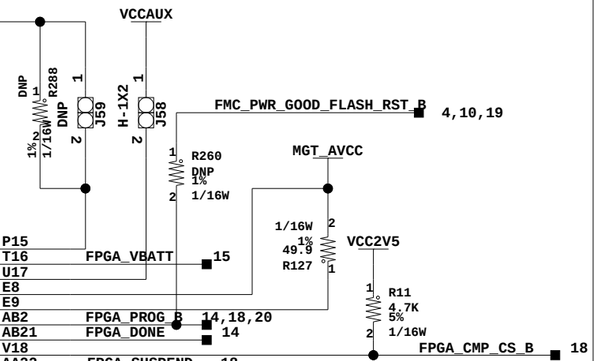
Title:	MGT Banks SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:04	Ver:	D
Sheet Size: B		Rev:	02
Sheet	6 of 35	Drawn By	BF



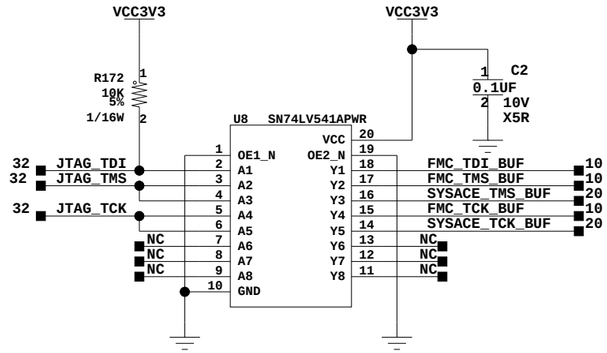








Trace length from the resistor pins to the FPGA pins MGTRREF and MGTV must be equal in length.

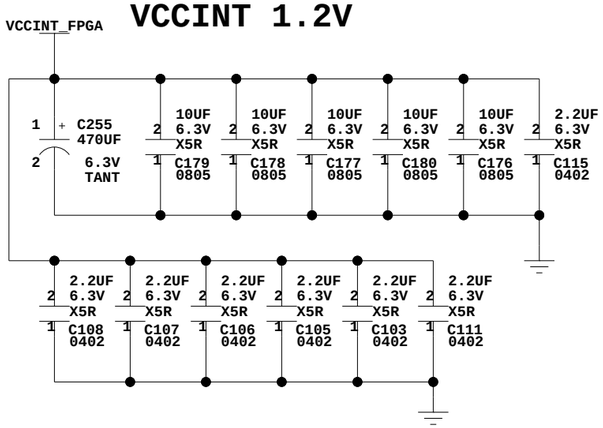


Power, GND, and Dedicated Banks

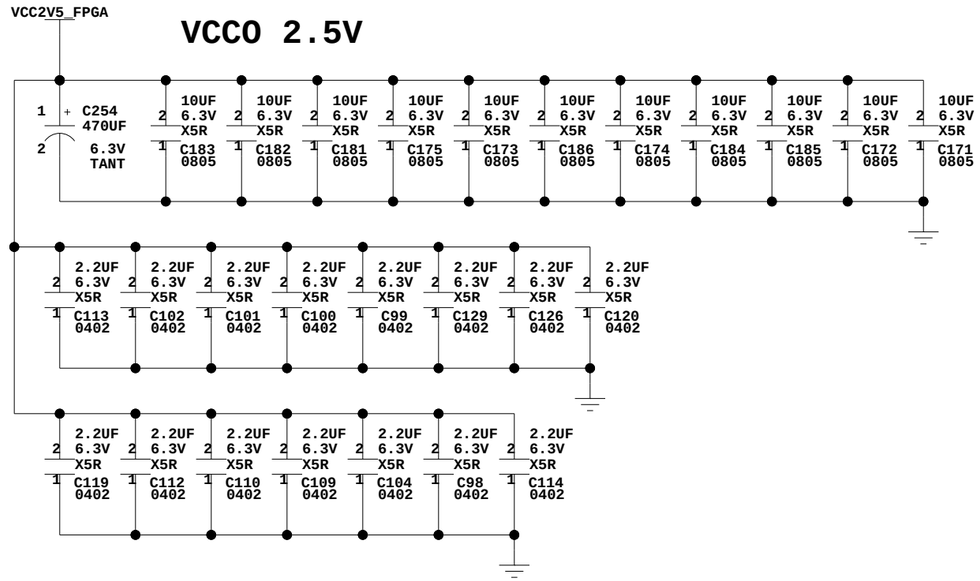
XILINX

Title:	Power, GND, and Dedicated Banks SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_14:59	Ver:	D
Sheet Size: B		Rev:	02
Sheet	7 of 35	Drawn By	BF

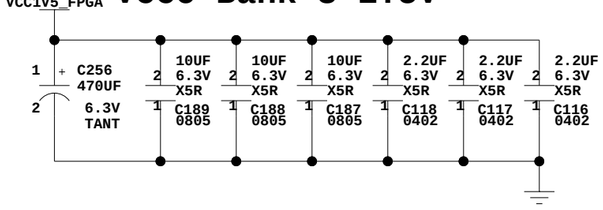
VCCINT 1.2V



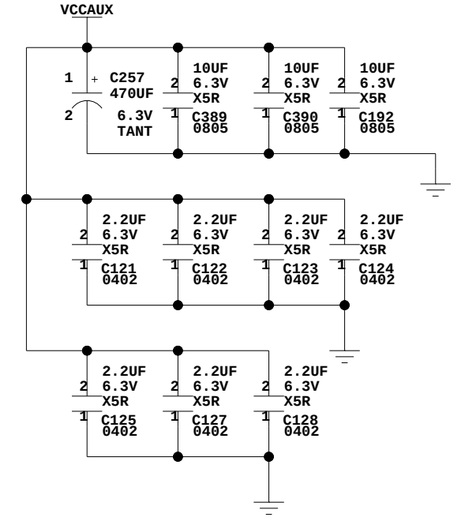
VCCO 2.5V



VCCO Bank 3 1.5V



VCCAUX 2.5V



FPGA Decoupling

XILINX

Title:	FPGA Decoupling SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
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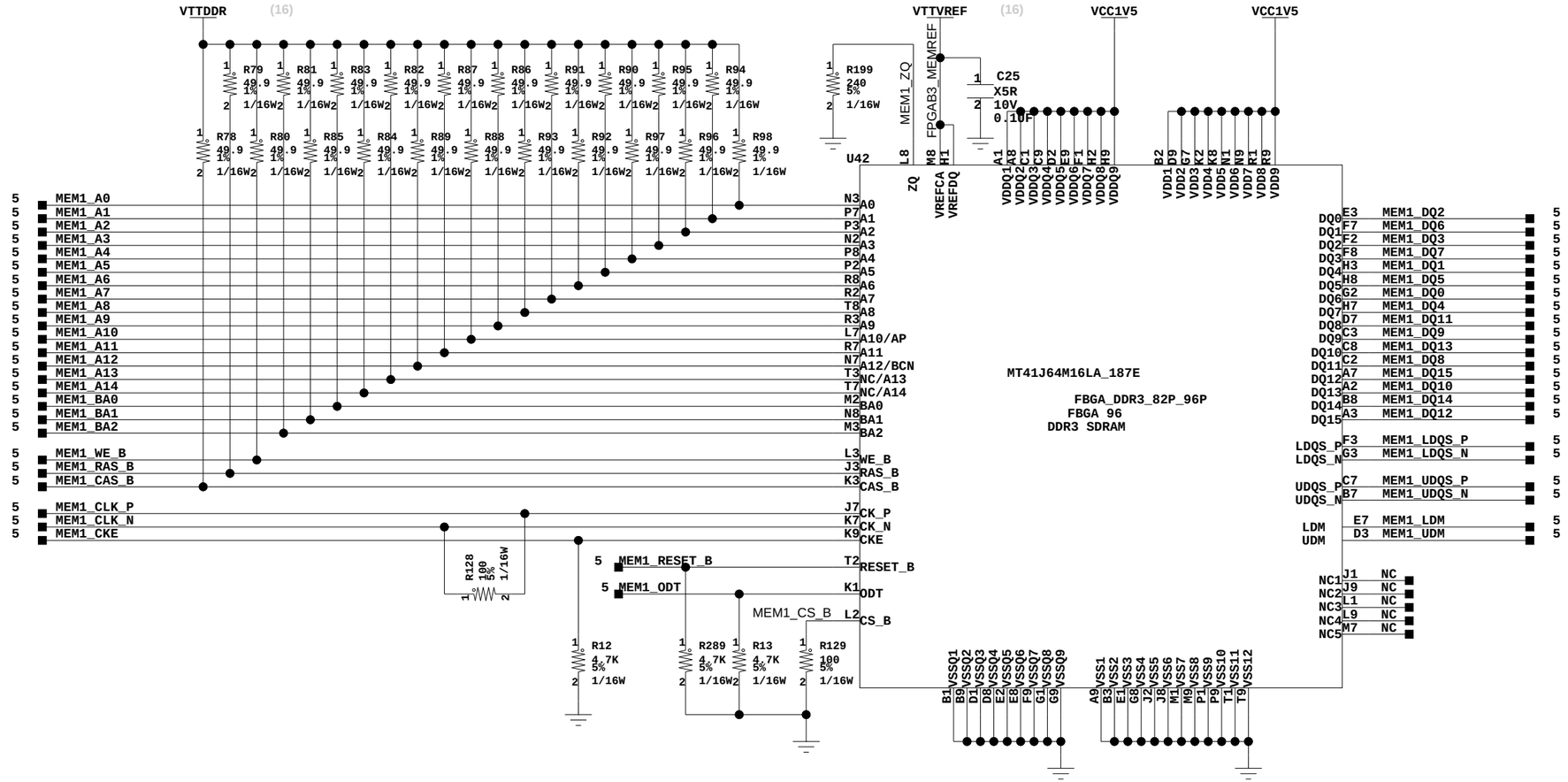
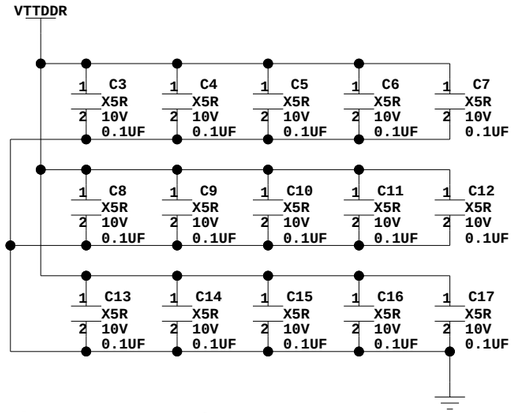
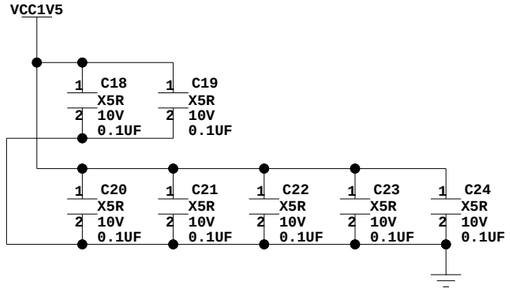
Sheet	8 of 35	Drawn By	BF





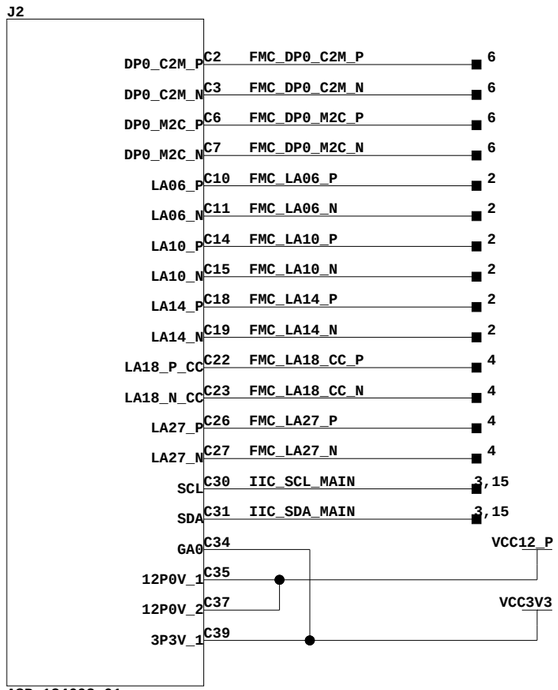


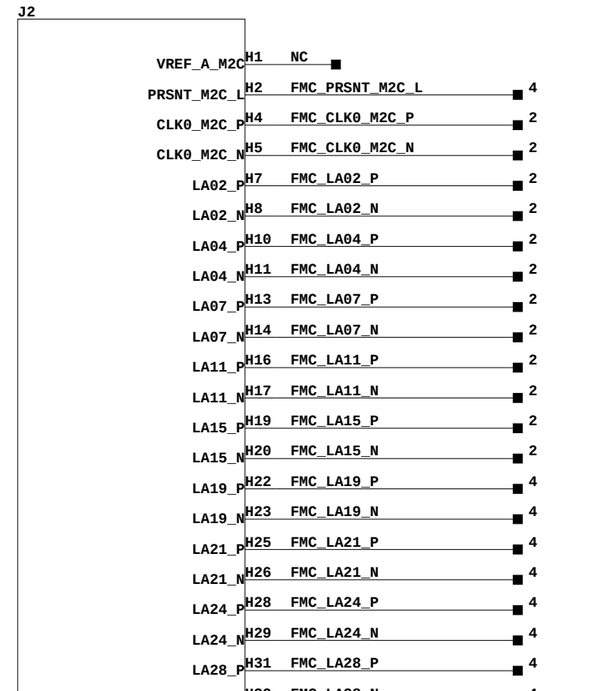
VCCOB3 remote sense pair connects from here back to (10)

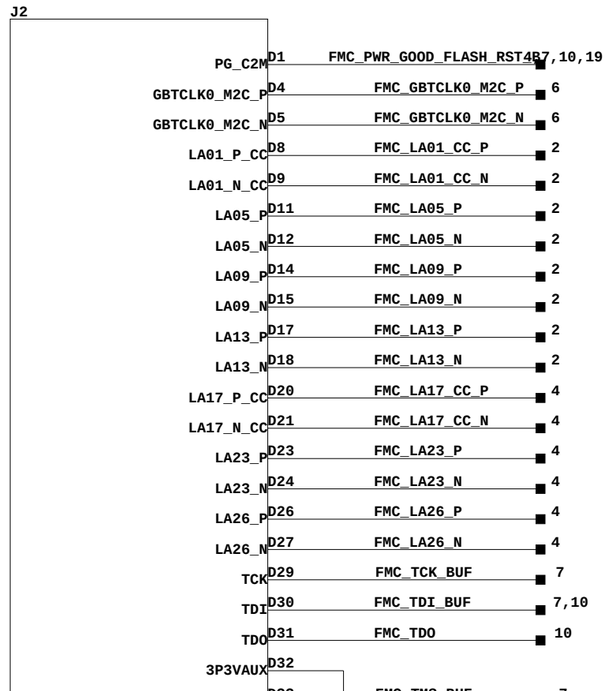
DDR3

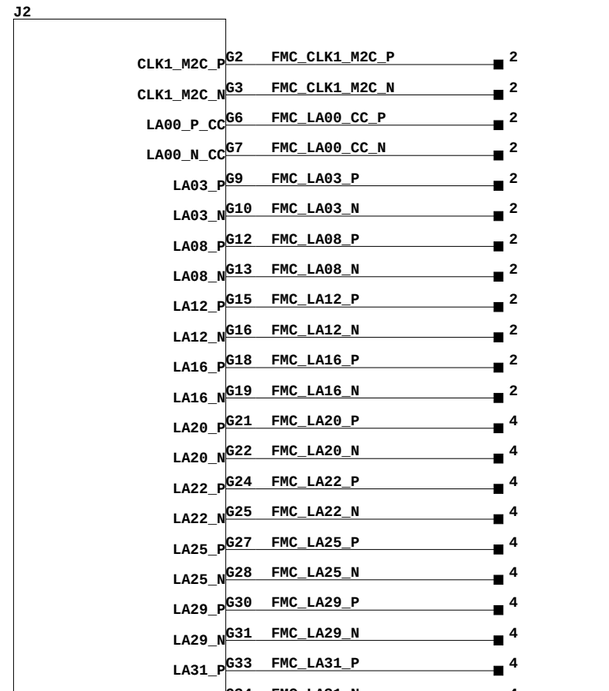
XILINX

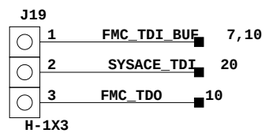
Title:	DDR3 SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	9 of 35	Drawn By	BF



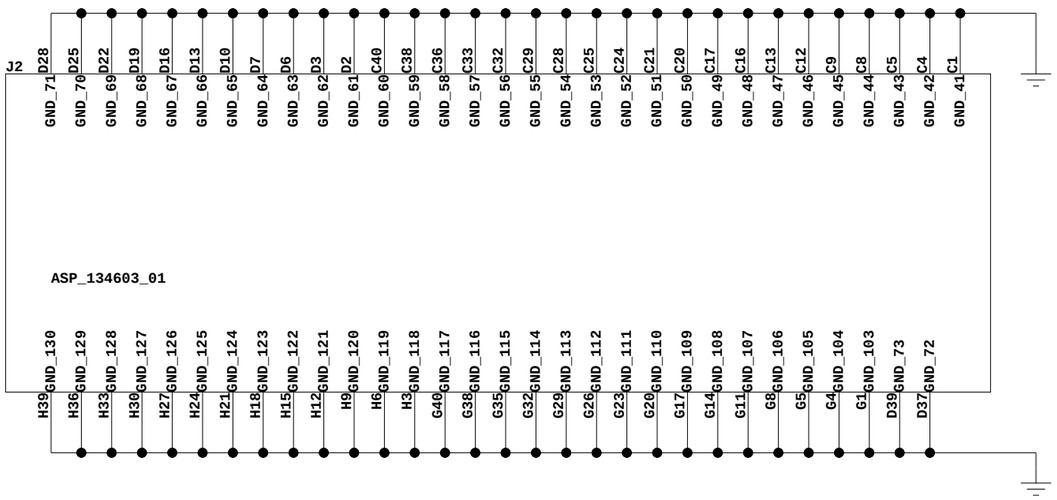


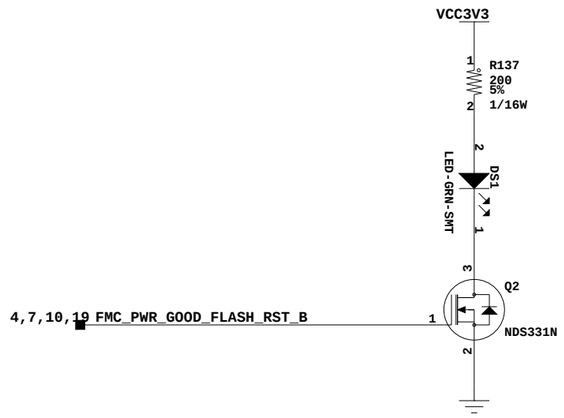




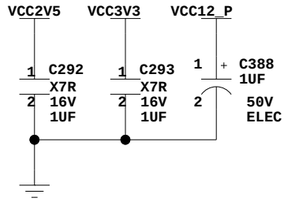


Jumper to include FMC in JTAG chain





FMC Power Good LED



ANSI/VITA 57.1-2008 Version 1.1 FMC LPC Connector

XILINX

Title:	FMC LPC Connector SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-25-2009_10:32	Ver:	D
Sheet Size: B		Rev:	02
Sheet	10 of 35	Drawn By	BF

The PHY MDIP Pins below are
Media Dependent Interface Pins (MDIP),
and are all bidirectional pins.

Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

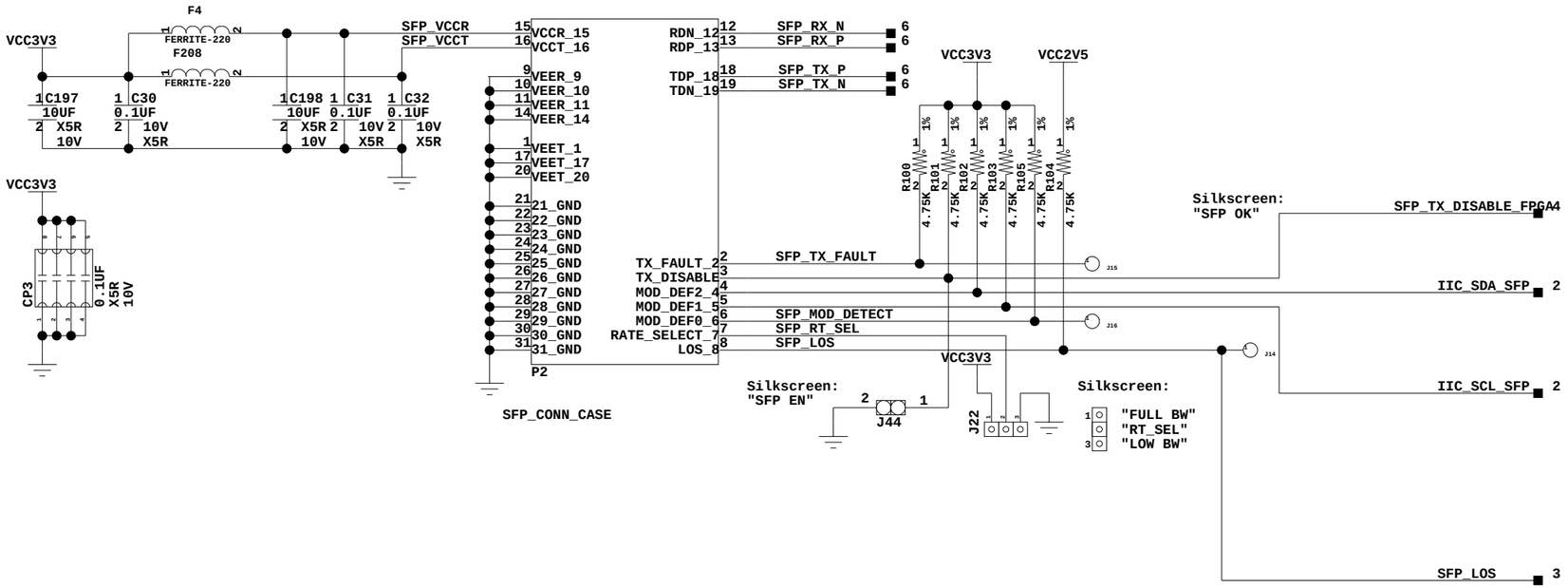
Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

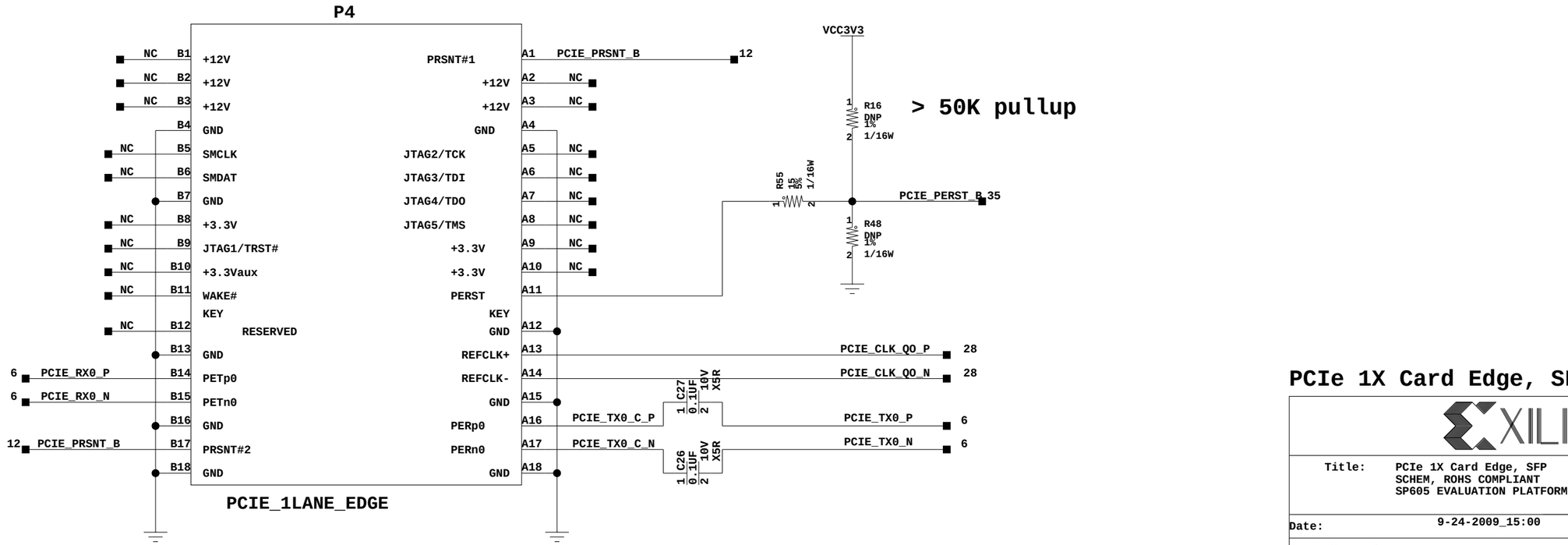
10/100/1000 PHY

XILINX

Title:	10/100/1000 PHY SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	ASSY P/N:	0431540
		PCB P/N:	1280479
		SCH P/N:	0381311
Date:	9-24-2009_15:30	Ver:	D
Sheet Size: B		Rev:	02
Sheet	11 of 35	Drawn By	BF

SFP MODULE



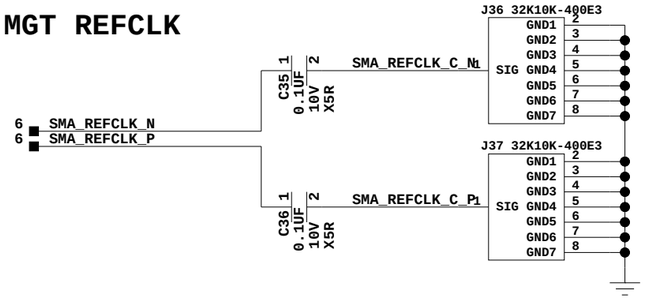


PCIe 1X Card Edge, SFP

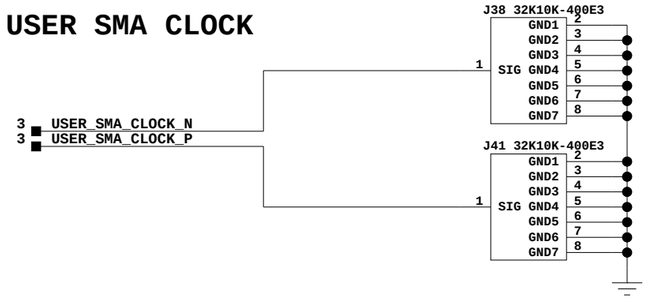
XILINX

Title:	PCIe 1X Card Edge, SFP SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	12 of 35	Drawn By	BF

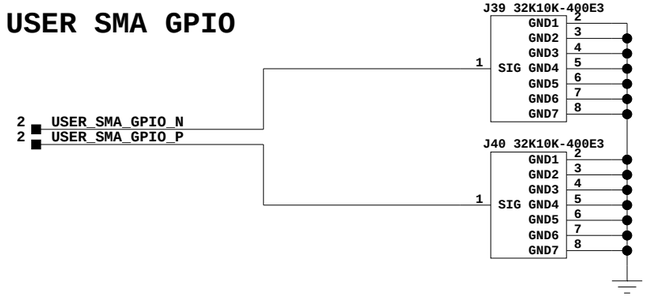
MGT REFCLK



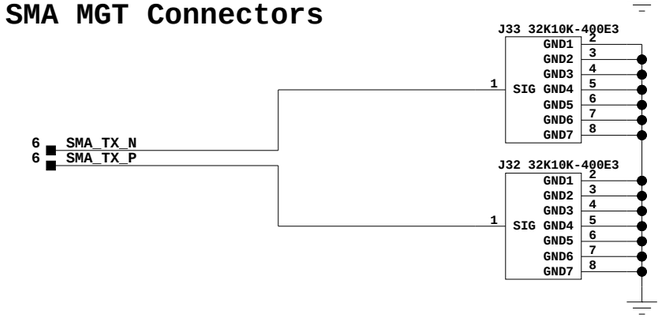
USER SMA CLOCK



USER SMA GPIO



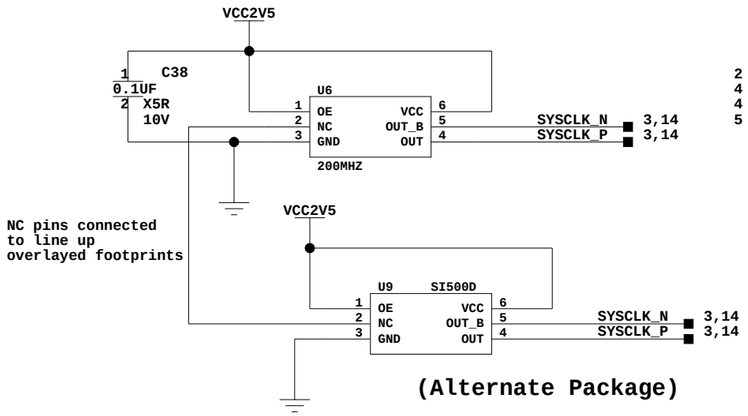
SMA MGT Connectors



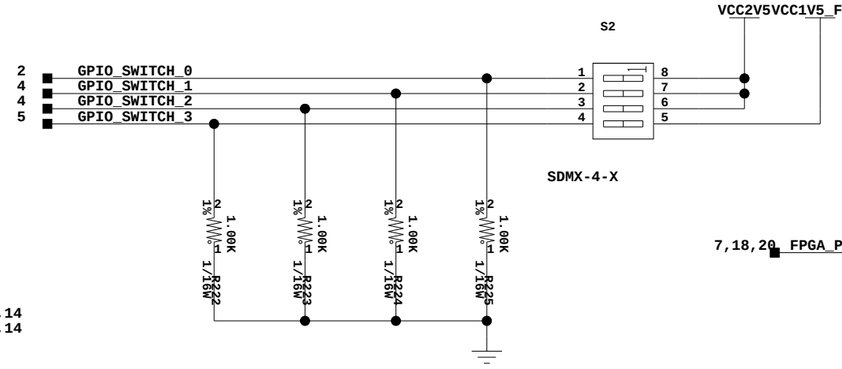
SMA Connectors

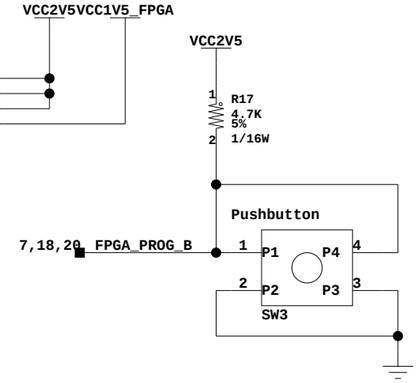
XILINX

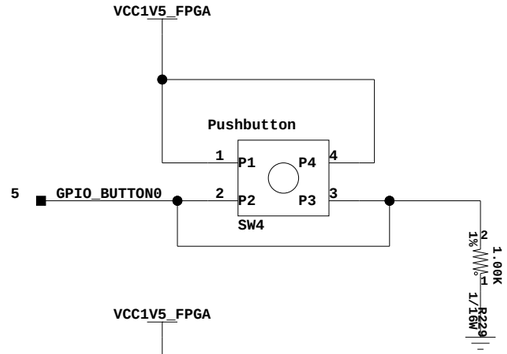
Title:	SMA Connectors SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date: 9-18-2009_15:04		Ver: D	
Sheet Size: B		Rev: 02	
Sheet 13 of 35		Drawn By BF	

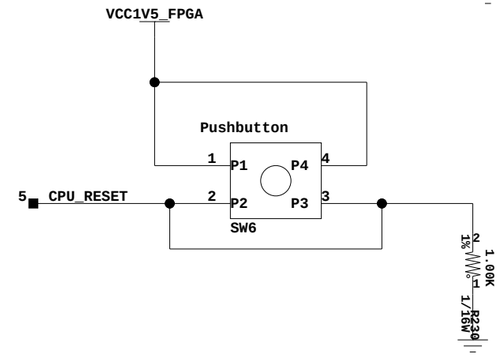


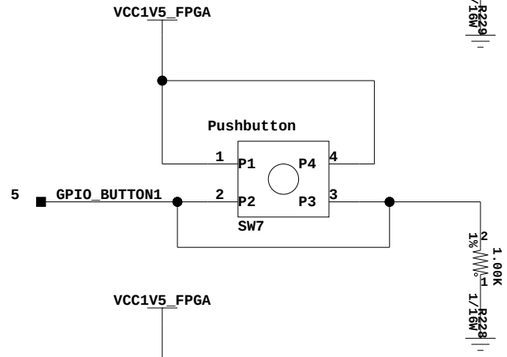
Differential System Clock

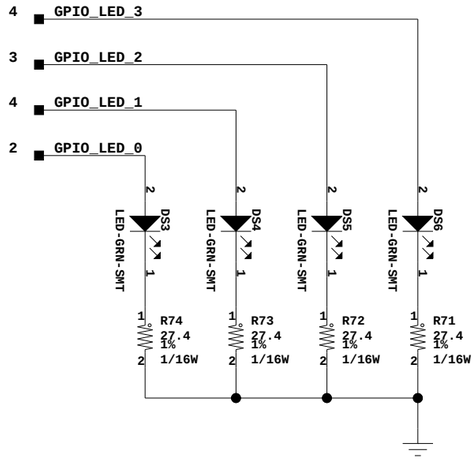


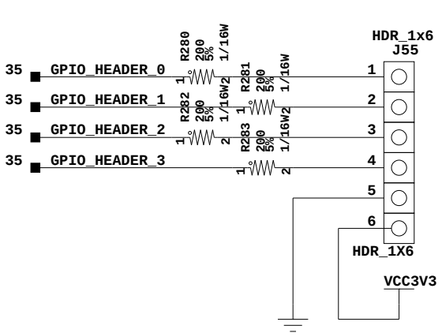


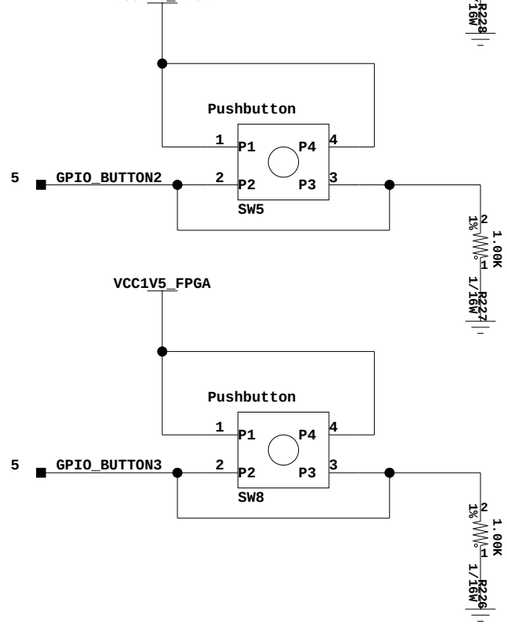


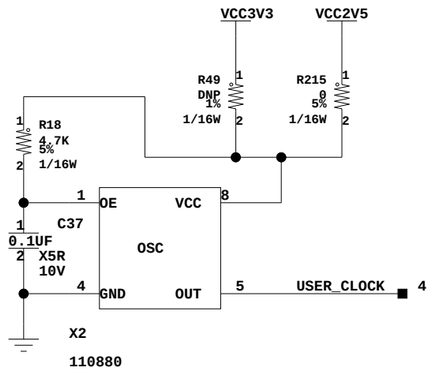




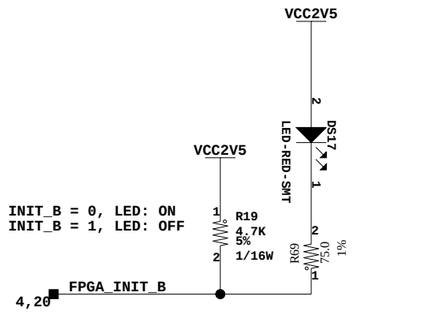


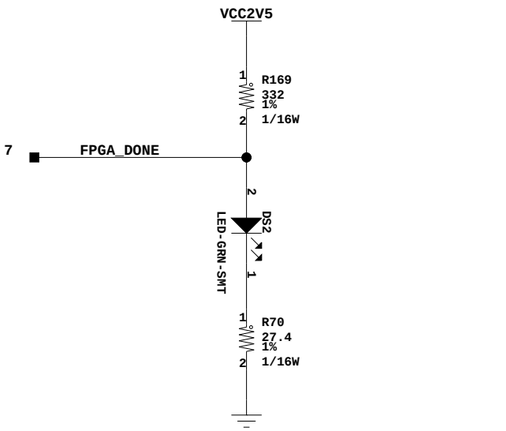






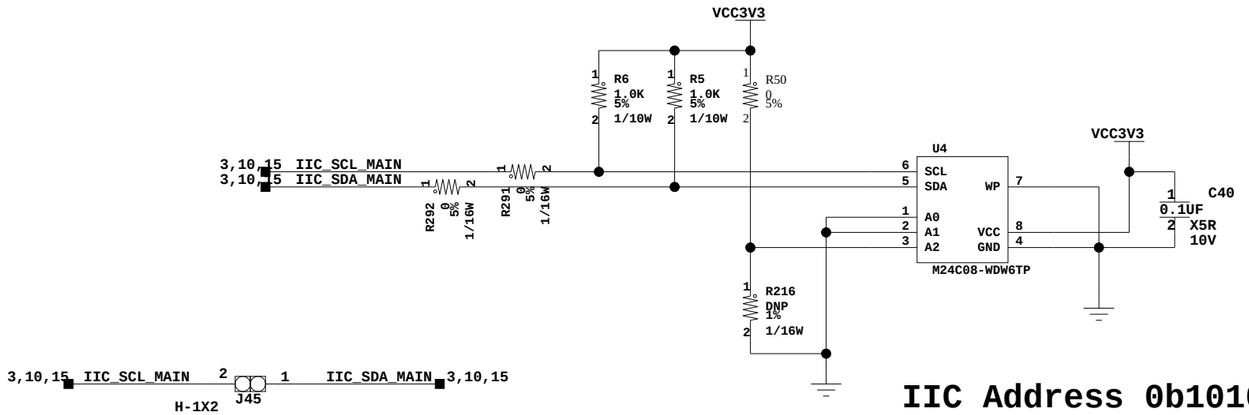
Single Ended User Clock



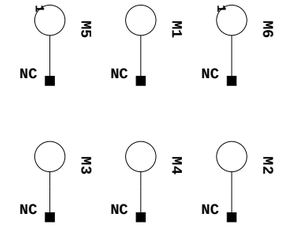


Clocks, LEDs, Buttons, Switches

Title:	Clocks, LEDs, Buttons, Switches SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:04	Ver:	D
Sheet Size: B		Rev:	02
Sheet	14 of 35	Drawn By	BF

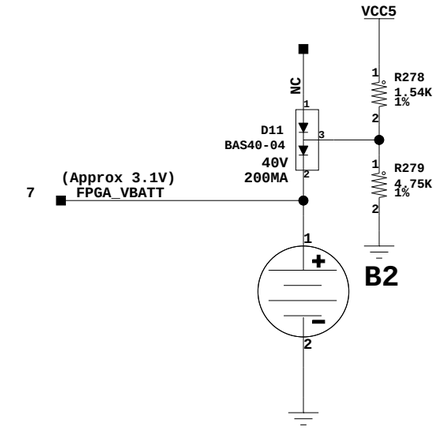


IIC Address 0b1010100



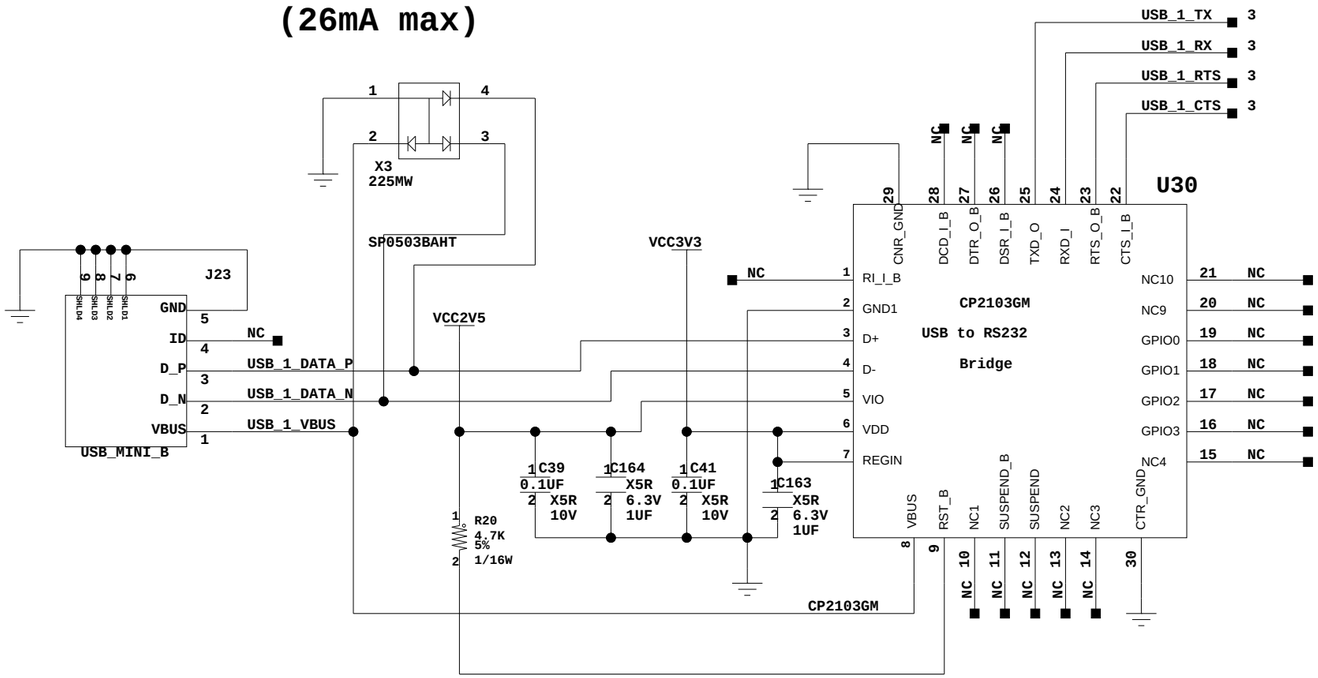
Fiducials

Rechargeable Battery



CP2103 USB Self-Powered

(26mA max)

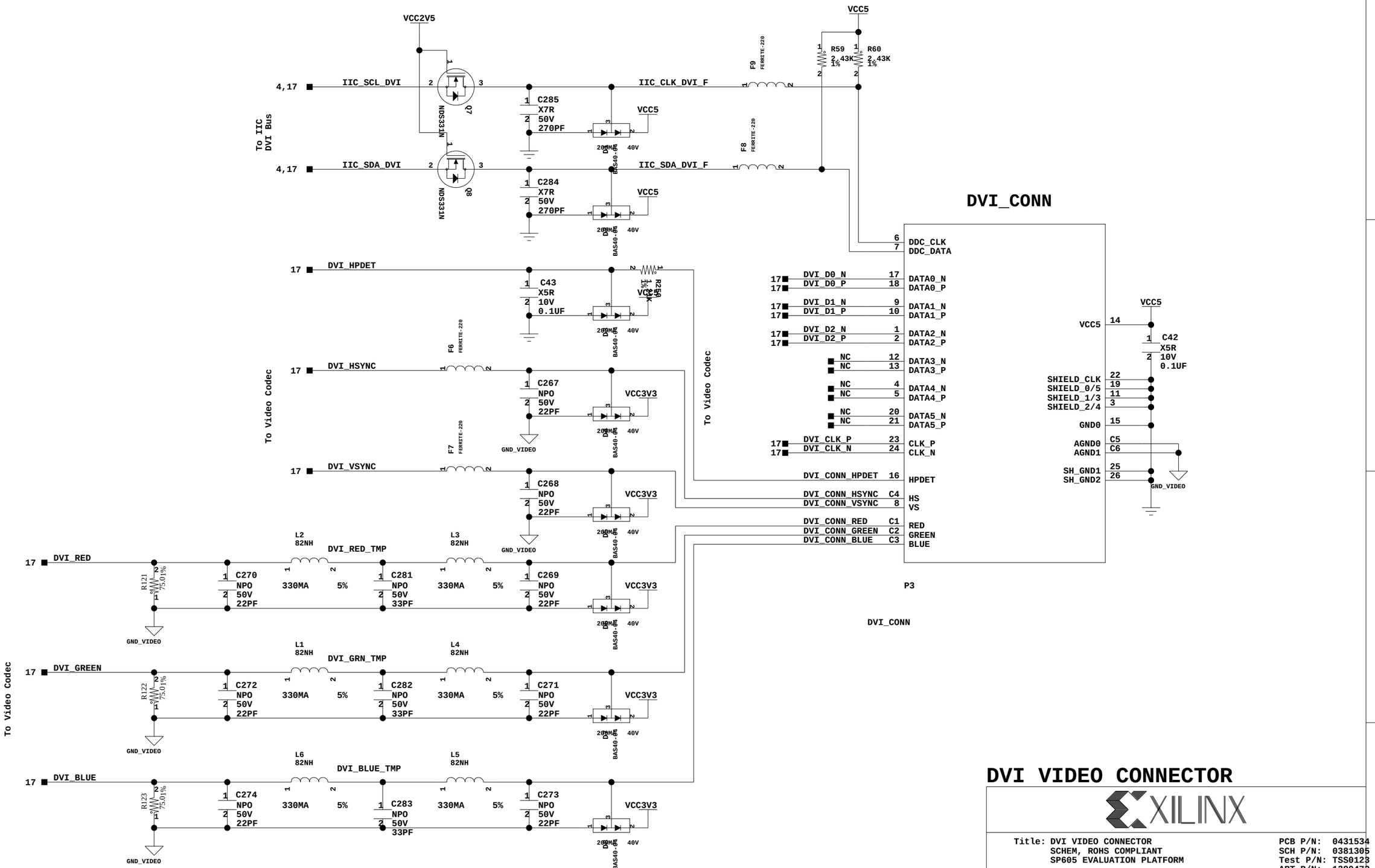


The VIO voltage must match the appropriate bank IO voltage

UART, IIC Header/EEPROM

XILINX

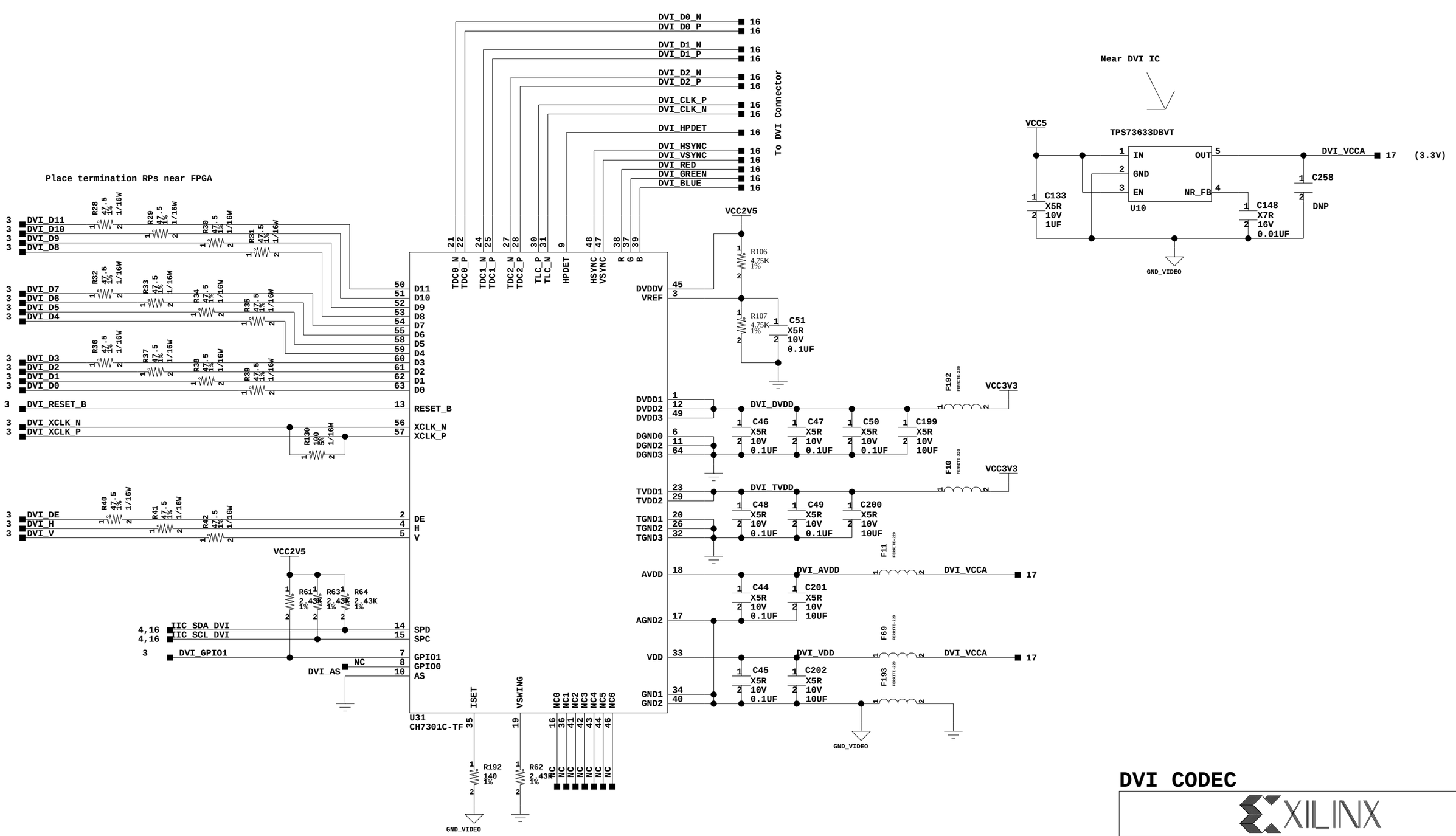
Title:	UART, IIC Header/EEPROM SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	15 of 35	Drawn By	BF



DVI VIDEO CONNECTOR

XILINX

Title: DVI VIDEO CONNECTOR SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
Date: 9-18-2009_15:03	Ver: D
Sheet Size: B	Rev: 02
Sheet 16 of 35	Drawn By BF

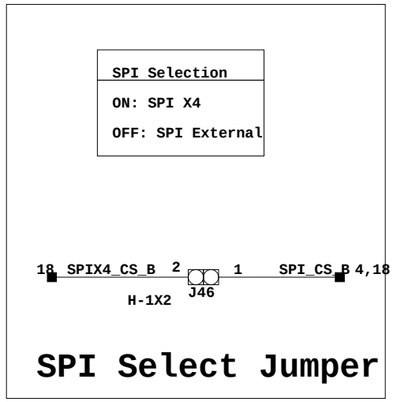


IIC Address = 0x76

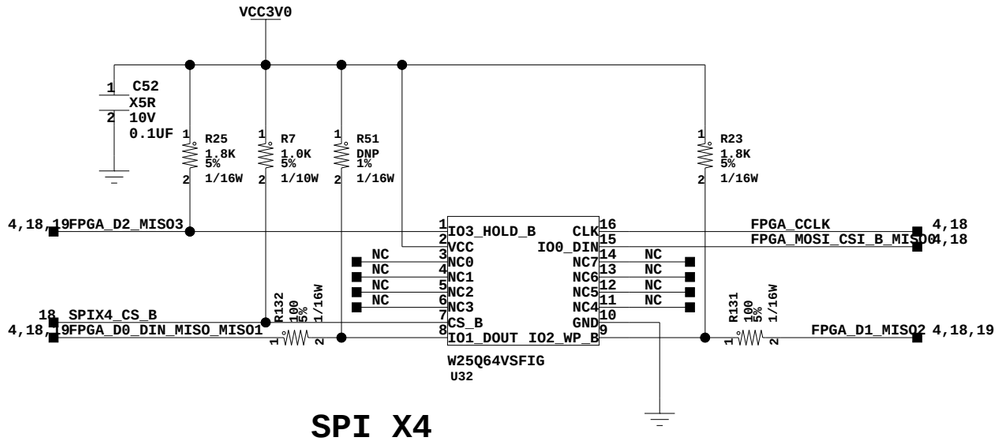
DVI CODEC

XILINX

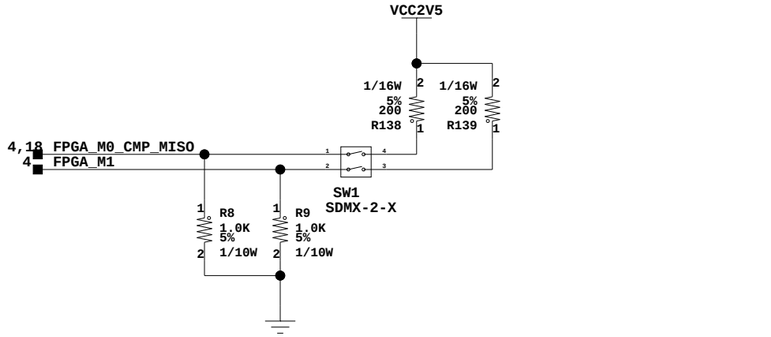
Title:	DVI CODEC SCHEM, ROHS COMPLIANT, SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date: 9-18-2009_15:03		Ver:	D
Sheet Size: B		Rev:	02
Sheet 17 of 35		Drawn By	BF



SPI Select Jumper

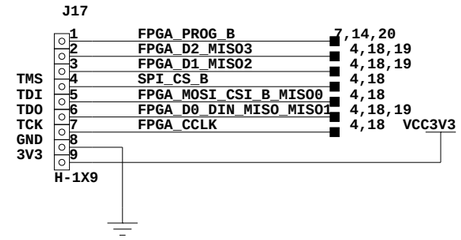


SPI X4

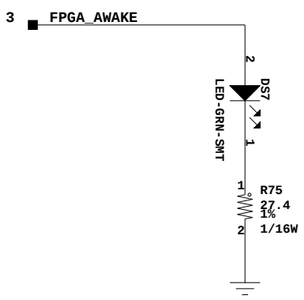


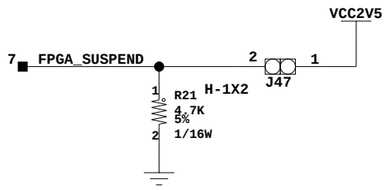
Mode pin DIP switches

Silkscreen:

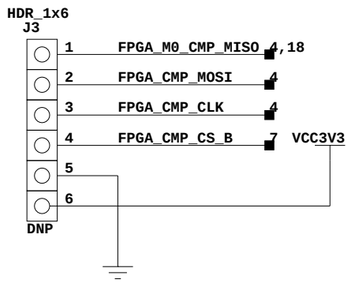


SPI Program Header





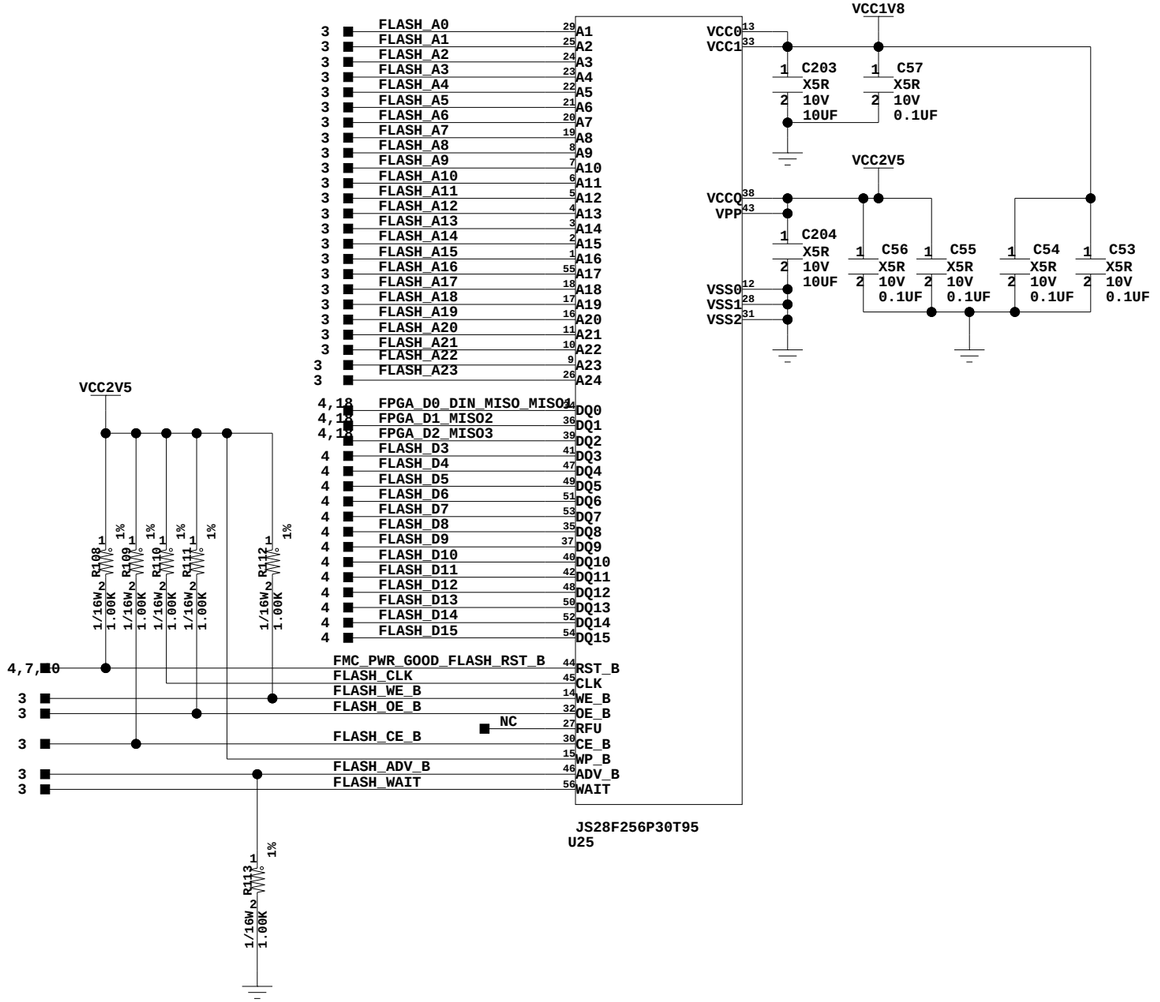
Suspend Jumper



SPI, CMP, Mode, and Suspend

Title:	SPI, CMP, Mode, and Suspend SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	18 of 35	Drawn By	BF

Silkscreen:
"Strata FLASH"
"256 MBit"



Synchronous mode not supported

ASYNC. SRAM FLASH

XILINX

Title:	ASYNC. SRAM FLASH SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:03	Ver:	D
Sheet Size: B		Rev:	02
Sheet	19 of 35	Drawn By	BF

SYSTEMACE TQFP144 (DIE DOWN)

PARTS=1
LEVEL=STD
XCCACE-TQ144I
U17

CP4 0.1UF X5R 10V
CP5 0.1UF X5R 10V
CP6 0.1UF X5R 10V

VCC3V3

VCC2V5

VCC3V3

SYSACE_RESET_B 20

Silkscreen: "SYSACE RESET"
Pushbutton
SW9

VCC2V5
SysACE Failsafe Mode Jumpers
OR = Failsafe Mode Enabled

R116 4.75K 1%

SYSACE_ERR_LED — H-1X2 J49 — 1 SYSACE_RESET_B — 20
7,14,18 FPGA_PROG_B — H-1X2 J48 — 1 SYSACE_ERR_LED — 20

NC	2	NC1
NC	14	NC2
NC	16	NC3
NC	19	NC4
NC	20	NC5
NC	21	NC6
NC	22	NC7
NC	23	NC8
NC	24	NC9
NC	27	NC10
NC	28	NC11
NC	29	NC12
NC	30	NC13
NC	31	NC14
NC	32	NC15

35 SYSACE_MPBRDY	39	MPBRDY
35 SYSACE_MPIRQ	41	MPIRQ
35 SYSACE_MPCE	42	MPCE
35 SYSACE_MPA06	43	MPA06
35 SYSACE_MPA05	44	MPA05
35 SYSACE_MPA04	45	MPA04

NC	47	MPD15
NC	48	MPD14
NC	49	MPD13
NC	50	MPD12
NC	51	MPD11
NC	52	MPD10
NC	53	MPD09
NC	56	MPD08

35 SYSACE_D7	58	MPD07
35 SYSACE_D6	59	MPD06
35 SYSACE_D5	60	MPD05
35 SYSACE_D4	61	MPD04
35 SYSACE_D3	62	MPD03
35 SYSACE_D2	63	MPD02
35 SYSACE_D1	65	MPD01
35 SYSACE_D0	66	MPD00
35 SYSACE_MPA03	67	MPA03
35 SYSACE_MPA02	68	MPA02
35 SYSACE_MPA01	69	MPA01
35 SYSACE_MPA00	70	MPA00
35 SYSACE_MPWE	76	MPWE
35 SYSACE_MPOE	77	MPOE

NC	34	NC16
NC	36	NC17
NC	38	NC18
NC	40	NC19
NC	71	NC20
NC	90	NC21
NC	122	NC22
NC	124	NC23
NC	127	NC24
NC	143	NC25

VCCL_10 10, VCCL_15 15, VCCL_25 25, VCCL_57 57, VCCL_84 84, VCCL_94 94, VCCL_99 99, VCCL_126 126
VCCH_1 1, VCCH_17 17, VCCH_37 37, VCCH_55 55, VCCH_92 92, VCCH_73 73, VCCH_109 109, VCCH_128 128
RESET_B 33
POR_BYPASS 108, POR_TEST 74, POR_RESET 72

4,14	FPGA_INIT_B	CFGINIT 78
7	FPGA_TDI	CFGPROG 79
7	FPGA_TMS	CFGTDO 82
7	FPGA_TCK	CFGTMS 85
		CFGTCK 80
7	SYSACE_CFGTDI	CFGTDI 81
20	SYSACE_CFGADDR0	CFGADDR0 86
20	SYSACE_CFGADDR1	CFGADDR1 87
20	SYSACE_CFGADDR2	CFGADDR2 88
20	SYSACE_CFGMODEPIN	CFGMODEPIN 89
3	CLK_33MHZ_SYSACE	CLK 93
		STATLED 95
		ERRLED 96
		TSTTMS 98
		TSTTCK 101
		TSTTDO 97
		TSTTDI 102

35 GND 26 GND 18 GND 9 GND 144 GND 136 GND 129 GND 120 GND 111 GND 46 GND 54 GND 64 GND 83 GND 75 GND 91 GND 100 GND 112 GND 110 GND

VCC3V3 — R115 4.75K 1%

N7E50-7516PG-20

CFCD2	13	SYSACE_CFCD2	25	25_CD2
CFD10	12	SYSACE_CFD10	49	49_D10
CFD09	11	SYSACE_CFD09	48	48_D09
CFD02	8	SYSACE_CFD02	23	23_D02
CFD08	7	SYSACE_CFD08	47	47_D08
CFD01	6	SYSACE_CFD01	22	22_D01
CFD00	5	SYSACE_CFD00	21	21_D00
CFA00	4	SYSACE_CFA00	20	20_A00
CFREG	3	SYSACE_CFREG	44	44_REG
CFA01	142	SYSACE_CFA01	19	19_A01
CFA02	141	SYSACE_CFA02	18	18_A02
CFWAIT	140	SYSACE_CFWAIT	42	42_WAIT
CFA03	139	SYSACE_CFA03	17	17_A03
CFA04	137	SYSACE_CFA04	16	16_A04
CFA05	135	SYSACE_CFA05	15	15_A05
CFA06	134	SYSACE_CFRDBSY	14	14_A06
CFGRSVD	133		37	37_RDY/BSY
CFA07	132	SYSACE_CFA07	12	12_A07
CFWE	131	SYSACE_CFWE	36	36_WE
CFA08	130	SYSACE_CFA08	11	11_A08
CFA09	125	SYSACE_CFA09	10	10_A09
CFOE	123	SYSACE_CFDE	9	9_OEI
CFA10	121	SYSACE_CFA10	8	8_A10
CFCE2	138	SYSACE_CFCE2	32	32_CE2
CFCE1	119	SYSACE_CFCE1	7	7_CE1I
CFD15	118	SYSACE_CFD15	31	31_D15
CFD07	117	SYSACE_CFD07	6	6_D07
CFD14	116	SYSACE_CFD14	30	30_D14
CFD06	115	SYSACE_CFD06	5	5_D06
CFD13	114	SYSACE_CFD13	29	29_D13
CFD05	113	SYSACE_CFD05	4	4_D05
CFD12	107	SYSACE_CFD12	28	28_D12
CFD04	106	SYSACE_CFD04	3	3_D04
CFD11	105	SYSACE_CFD11	27	27_D11
CFD03	104	SYSACE_CFD03	2	2_D03
CFCD1	103	SYSACE_CFCD1	26	26_CD1

U37

VCC3V3

38_VCC	38	
13_VCC	13	
35_IOWR	35	R117 4.75K 1%
34_IORD	34	R118 4.75K 1%
46_BVD1	46	NC
45_BVD2	45	NC
40_VS2	40	NC
33_VS1	33	NC
24_WP	24	NC
43_INPACK	43	NC
39_CSEL	39	
41_RESET	41	R251 1.21K 1%; R252 1.21K 1%
50_GND	50	
1_GND	1	

VCC2V5

S1 SDMX-4-X

20 SYSACE_CFGADDR0	1	8
20 SYSACE_CFGADDR1	2	7
20 SYSACE_CFGADDR2	3	6
20 SYSACE_CFGMODEPIN	4	5

R133 200 5% 1/16W; R134 200 5% 1/16W; R135 200 5% 1/16W; R136 200 5% 1/16W
R218 1.00K 1% 1/16W; R219 1.00K 1% 1/16W; R220 1.00K 1% 1/16W; R221 1.00K 1% 1/16W

Combined FPGA & CPU PC4 Connector

U29 32.000MHZ
NC — TRI — VCC — VCC2V5
GND — OUT
50PPM
C58 0.1UF 10V X5R

Silkscreen "System ACE" "Status LED"
VCC3V3 — DS8 LED-GRN-SMT — R193 180 5% 1/16W — SYSACE_STAT_LED

Silkscreen "System ACE" "Error LED"
DS18 LED-RED-SMT — R194 180 5% 1/16W — SYSACE_ERR_LED — 20

Disable SysACE Error LED
H-1X2 J60

SYSACE_TDI	10	JTAG_TDO
SYSACE_TCK_BUF	32	
SYSACE_TMS_BUF	7	
	7	

System ACE CF

XILINX

Title:	SYSTEM ACE CF SCHEM, ROHS COMPLIANT, SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	20 of 35	Drawn By	BF

PMBus Address is calculated as follows:

PMBus Address = 12 × Value(ADDRSEN1) + Value(ADDRSEN0)

Example: ADDRSEN1 R=27.4k and ADDRSEN0 R=27.4k

PMBus Address = (12 x 4) + 4 = 52 decimal

ADDRSENx Value	RPMBus
Open	-
11	210k
10	158k
9	115k
8	84.5k
7	63.4k
6	47.5k
5	36.5k
4	27.4k
3	21.5k
2	16.9k
1	13.0k
0	10.2k
Short	-

Note:

Do not use PMBus Addresses 0, 1, 2, 3, 12, 126 or 127

VCCxxxx_EAP/N are remote sense pairs wired back from power plane connections at FPGA

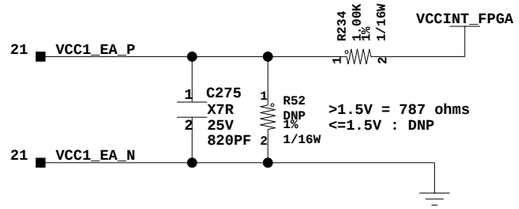
PMBus Connector

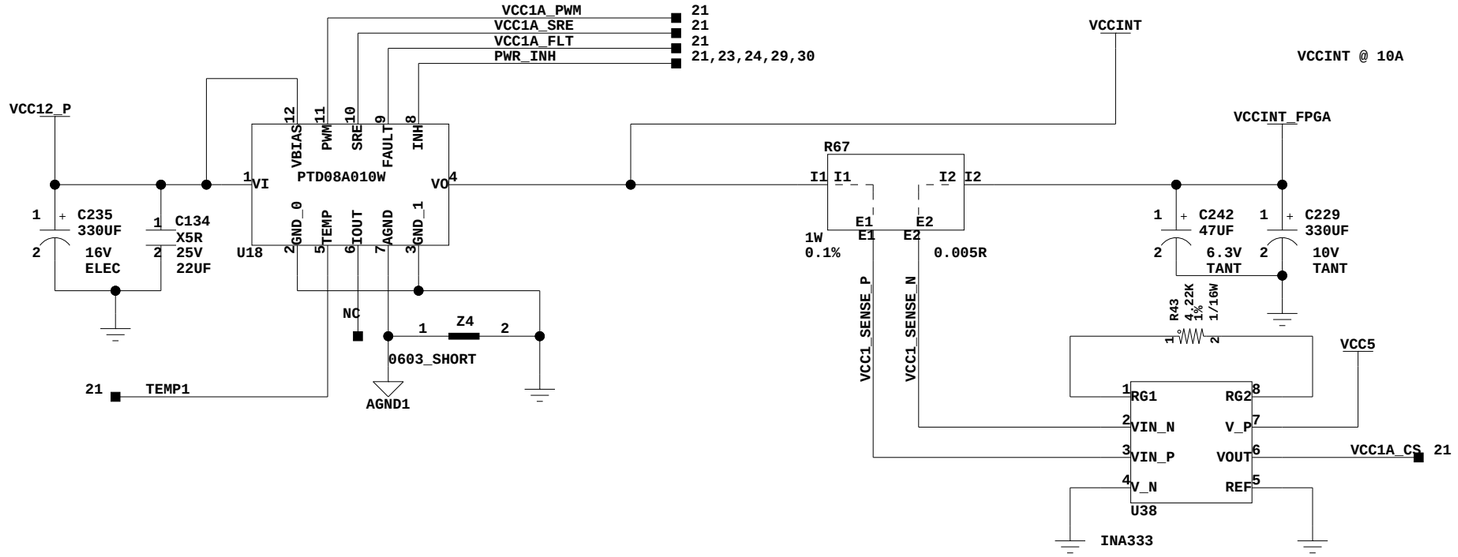
AGND should be a copper island underneath the 9240 and every associated module

FPGA PMBus Regulator Shutdown (shuts off regulators)

FPGA UCD9240 PMBus Controller

Title:	TI UCD9240 Power System SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	21 of 35	Drawn By	BF

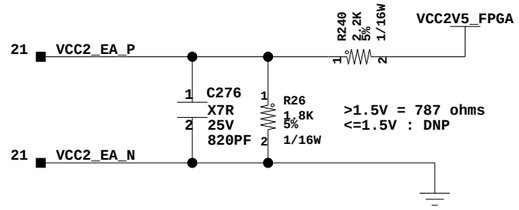


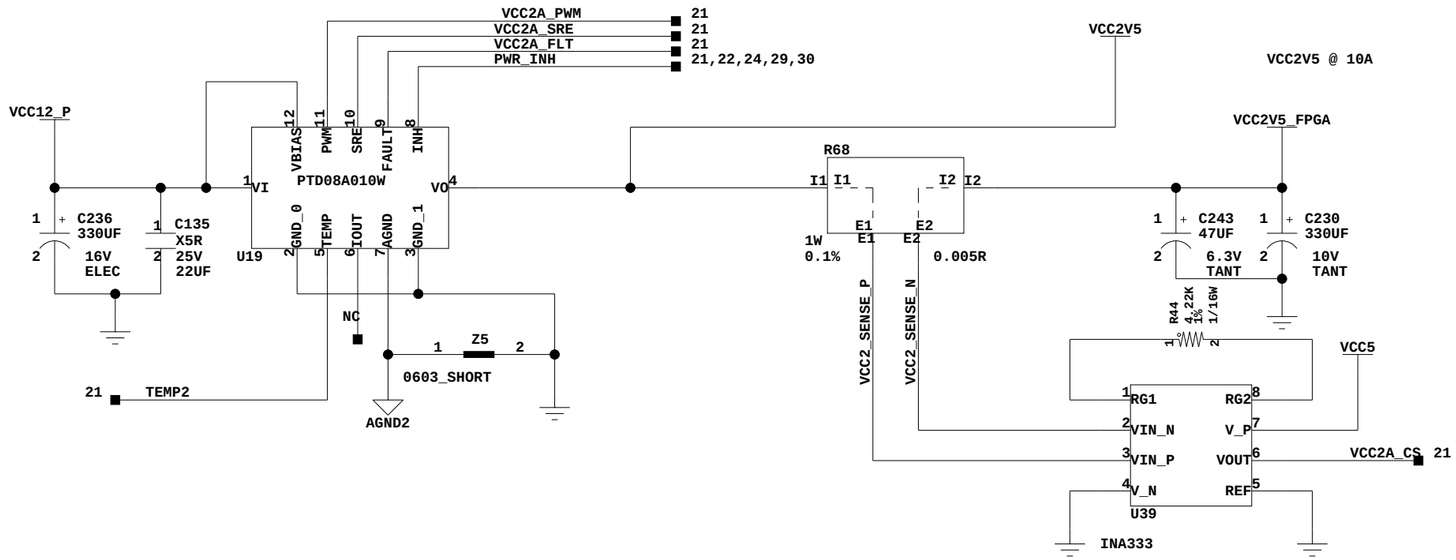


PTD08A010W 10A Max. Power Channel

XILINX

Title:	PTD08A010W 10A Max. Power Channel SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:03	Ver:	D
Sheet Size: B		Rev:	02
Sheet	22 of 35	Drawn By	BF

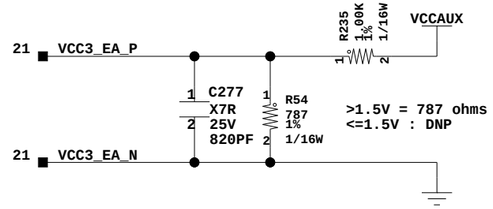


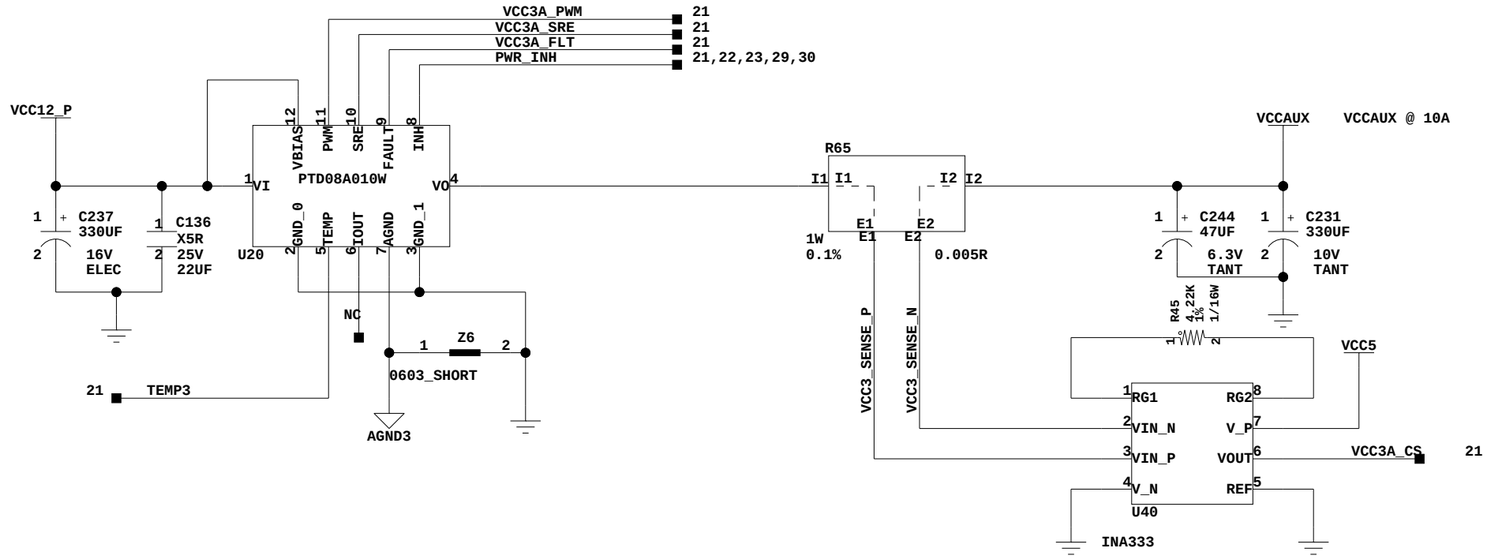


PTD08A010W 10A Max. Power Channel

XILINX

Title:	PTD08A010W 20A Max. Power Channel SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:03	Ver:	D
Sheet Size: B		Rev:	02
Sheet	23 of 35	Drawn By	BF

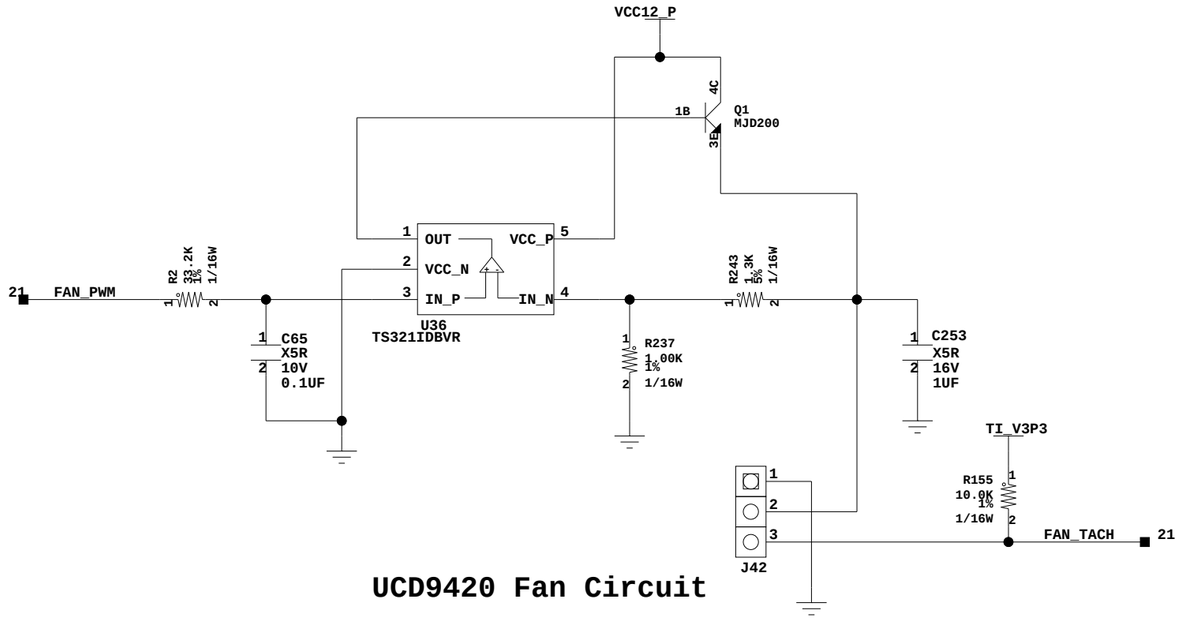




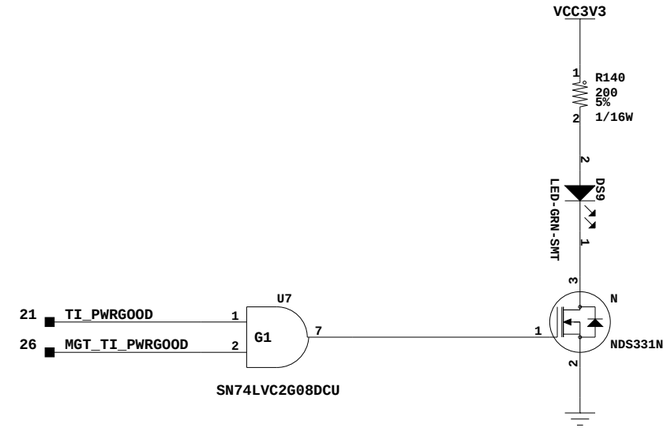
PTD08A010W 10A Max. Power Channel

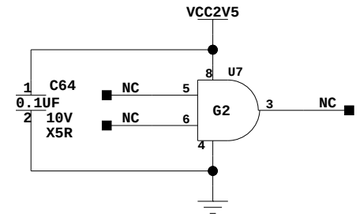
XILINX

Title:	PTD08A010W 10A Max. Power Channel SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	24 of 35	Drawn By	BF

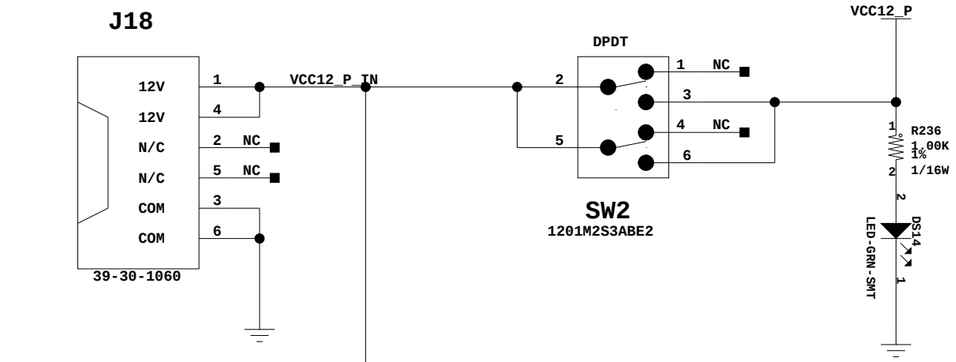


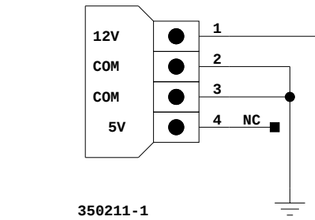
UCD9420 Fan Circuit





SP605 Power Good

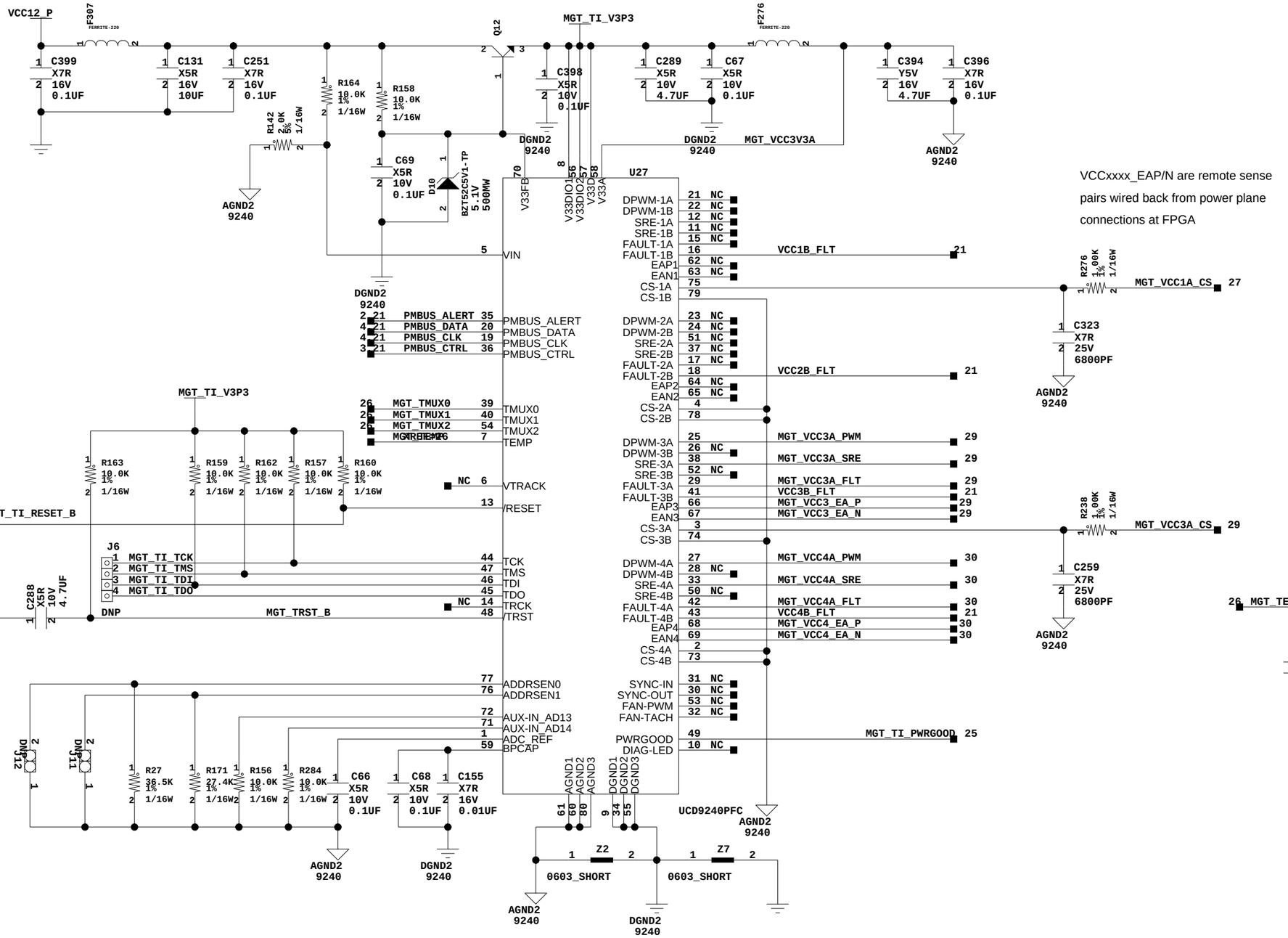




12V Power Jacks, 12V Fan

XILINX

Title:	TI UCD9240 Power System SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	25 of 35	Drawn By	BF



VCCxxxx_EAP/N are remote sense pairs wired back from power plane connections at FPGA

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Example: ADDRSEN1 R=27.4k and ADDRSEN0 R=27.4k

PMBus Address = (12 x 4) + 4 = 52 decimal

ADDRSENx Value	RPMBus
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3	21.5k
2	16.9k
1	13.0k
0	10.2k
Short	-

Note:

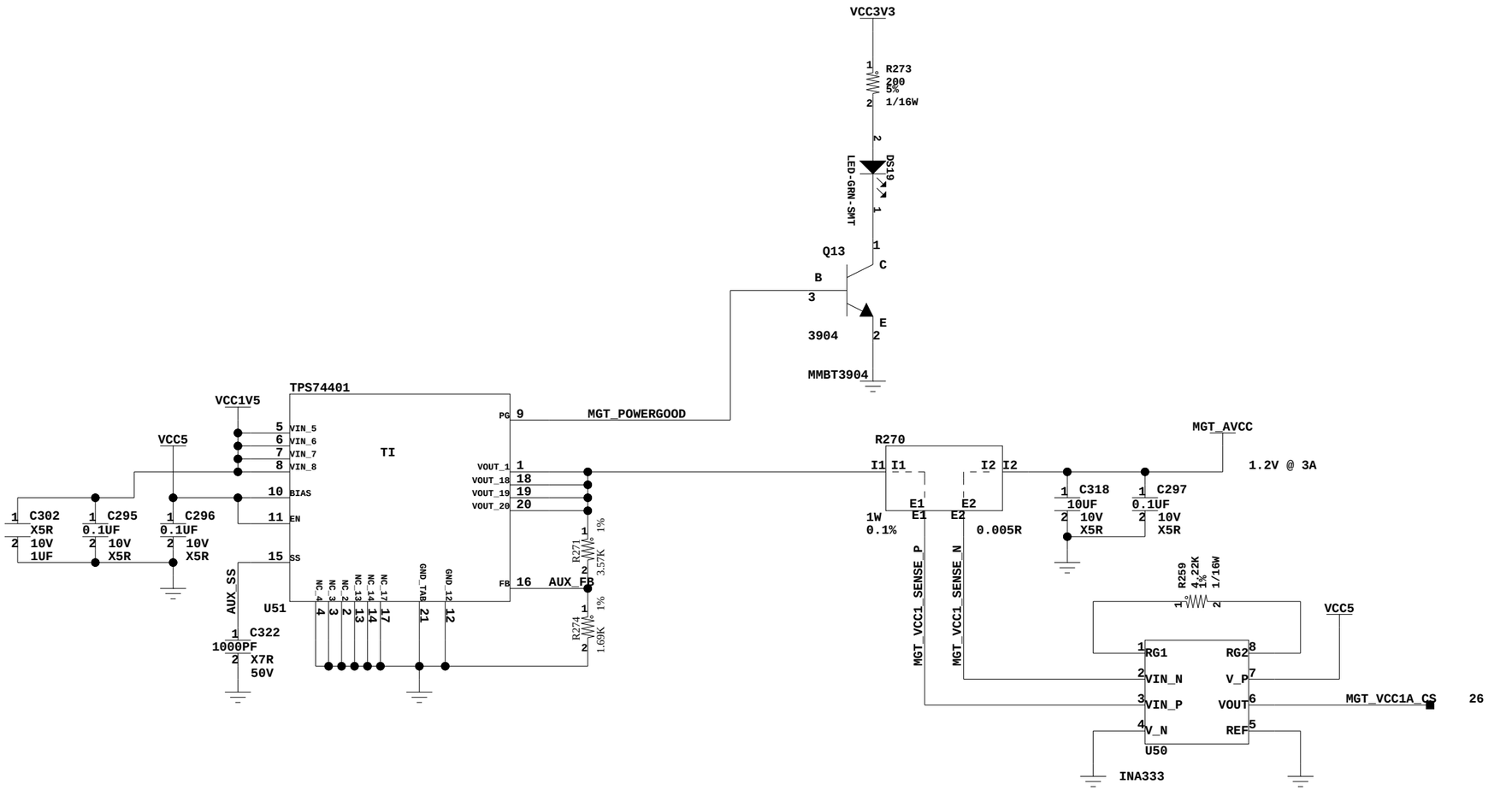
Do not use PMBus Addresses 0, 1, 2, 3, 12, 126 or 127

AGND should be a copper island underneath the 9240 and every associated module

FPGA UCD9240 PMBus Controller

XILINX

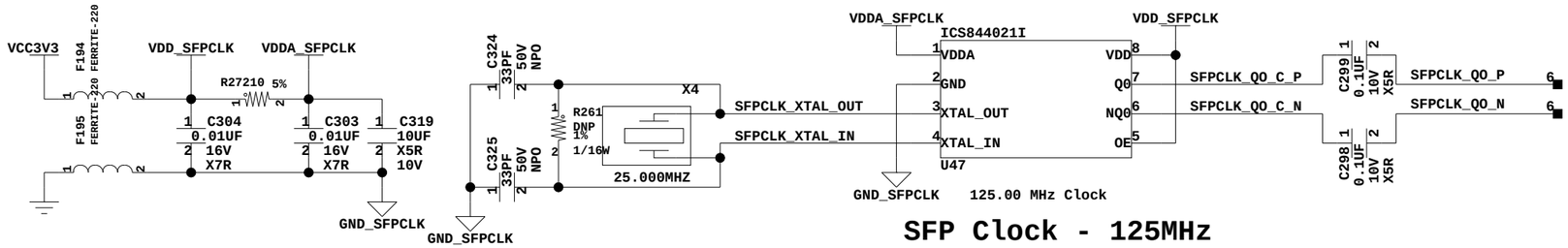
Title:	TI UCD9240 Power System SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	26 of 35	Drawn By	BF



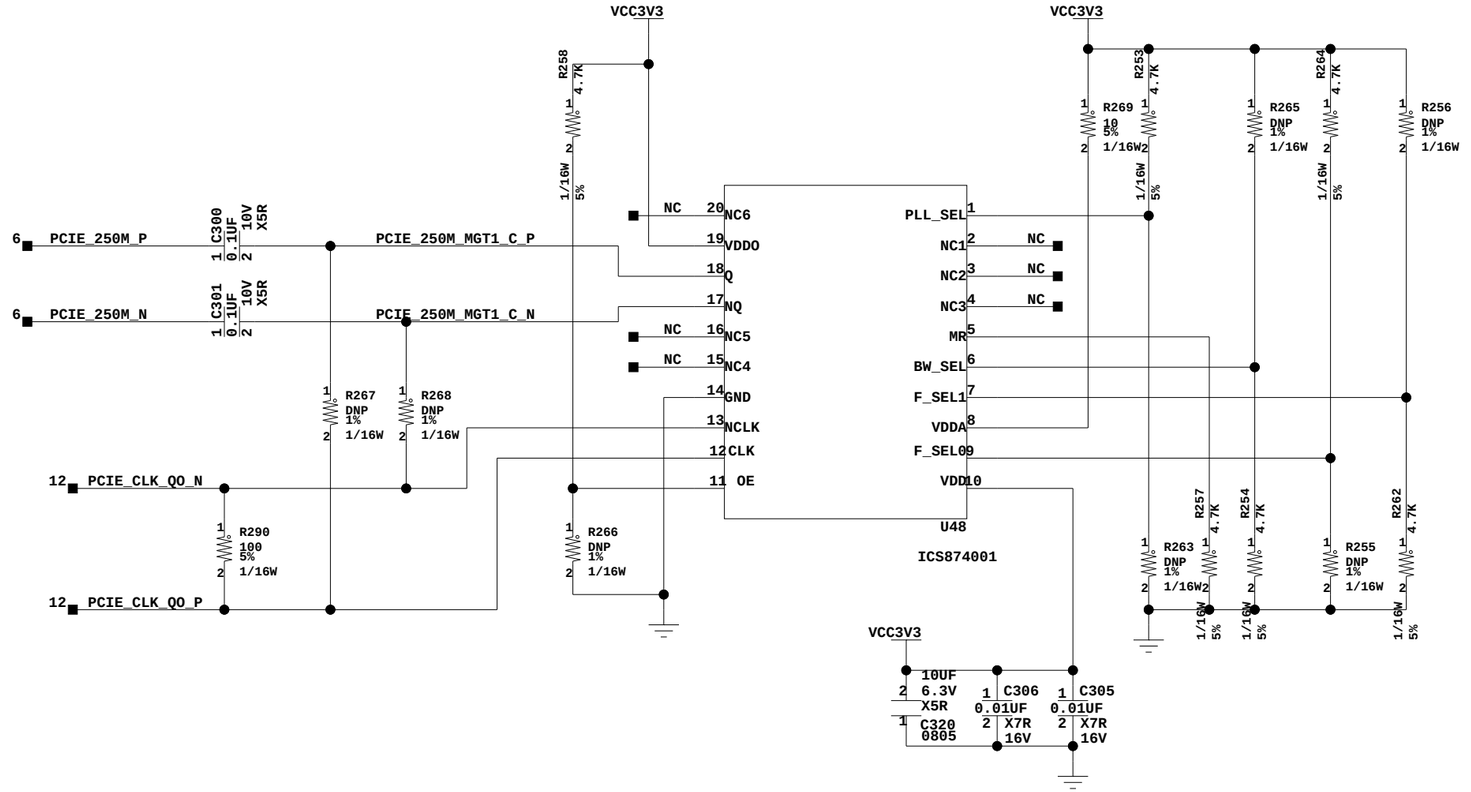
TPS74401 3A Max MGT Power

XILINX

Title:	TPS74401 3A Max MGT Power SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:03	Ver:	D
Sheet Size: B		Rev:	02
Sheet	27 of 35	Drawn By	BF



SFP Clock - 125MHz



MGT Clocks

XILINX

Title:	MGT Clocks SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:30	Ver:	D
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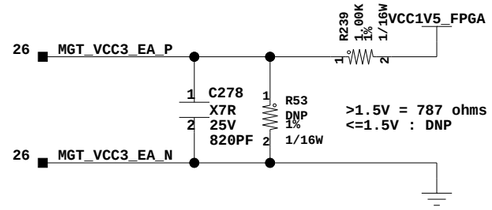
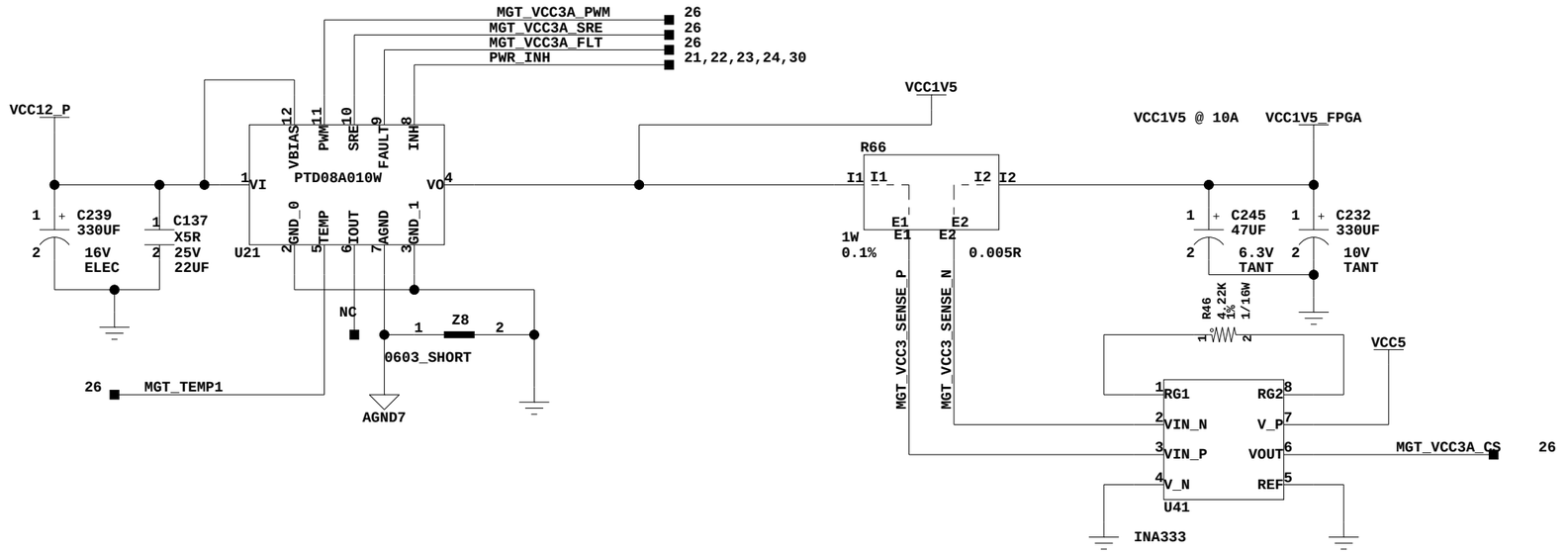
Sheet	28 of 35	Drawn By	BF

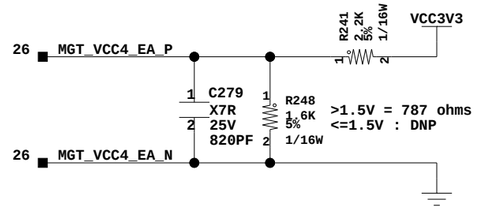


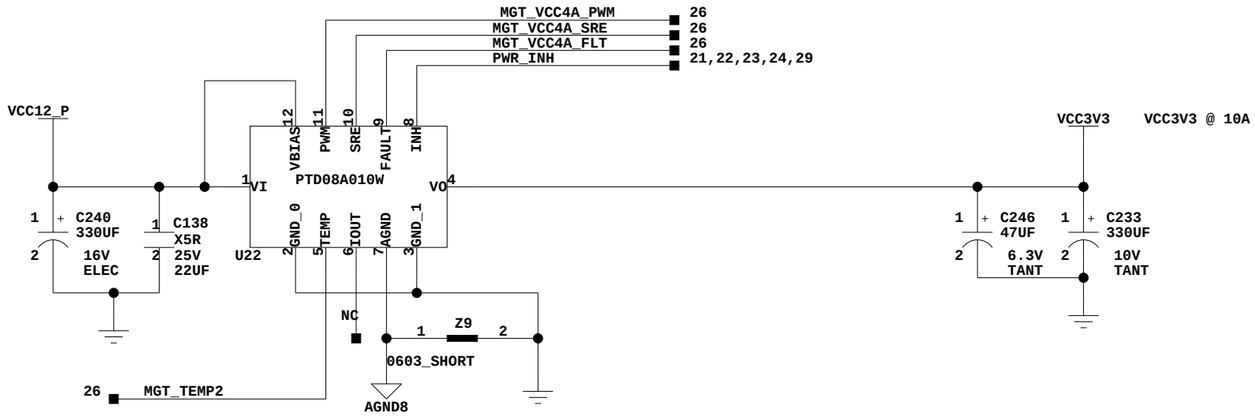


PTD08A010W 10A Max. Power Channel

XILINX

Title:	PTD08A010W 10A Max. Power Channel SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:03	Ver:	D
Sheet Size: B		Rev:	02
Sheet	29 of 35	Drawn By	BF

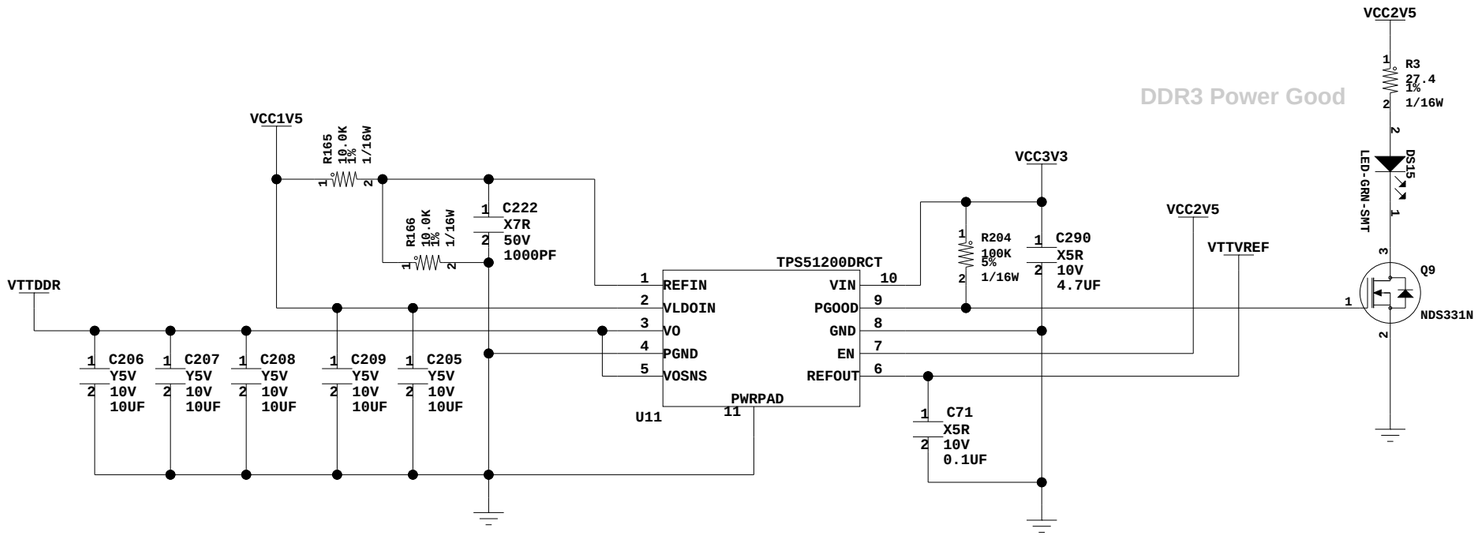




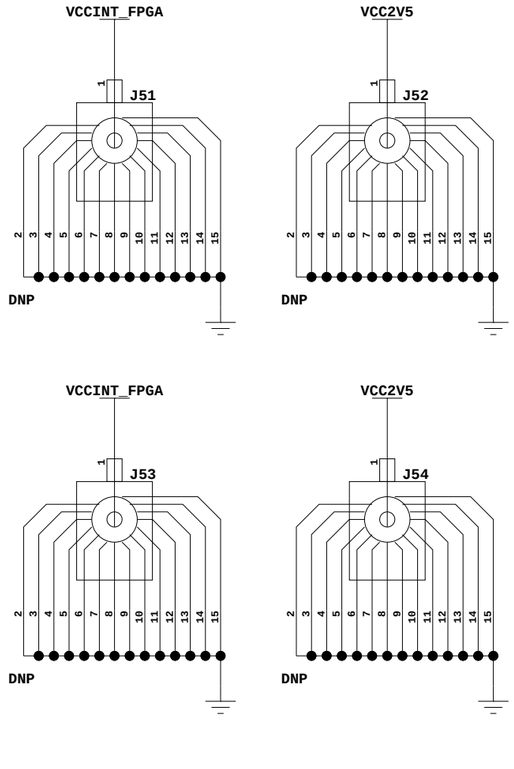
PTD08A010W 10A Max. Power Channel

Title:	PTD08A010W 10A Max. Power Channel SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-18-2009_15:03	Ver:	D
Sheet Size: B		Rev:	02
Sheet	30 of 35	Drawn By	BF

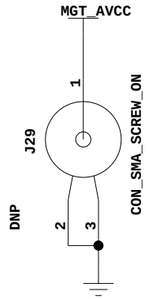
DDR3 Power Good

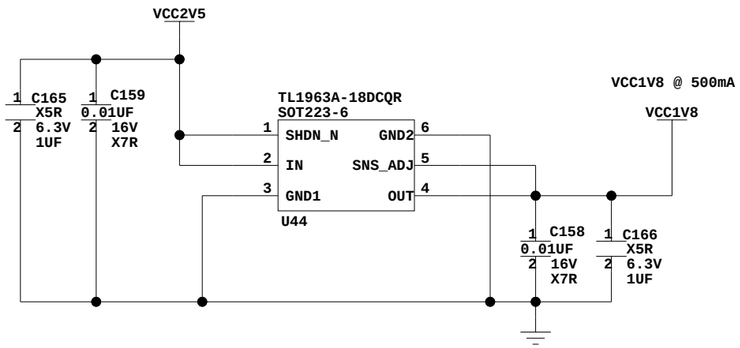


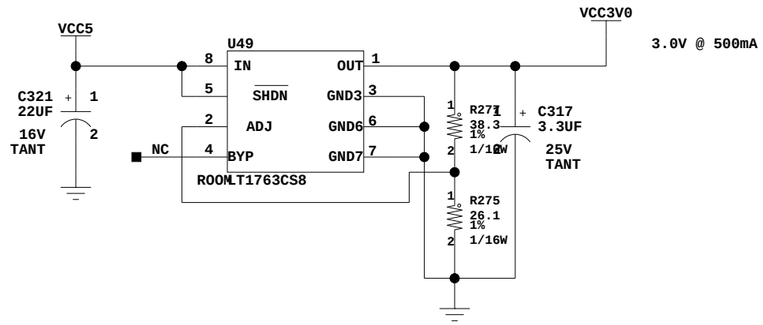
VCCINT_FPGA, VCCAUX Power Probe Channels



MGT Power Probe Channel







DDR3 Termination Regulator, power prob

Title:	DDR3 Termination Regulator SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-24-2009_15:00	Ver:	D
Sheet Size: B		Rev:	02
Sheet	31 of 35	Drawn By	BF

The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

U28

PART_NUMBER=CY7C68013A
TQFP100

USB CONTROLLER

USB CONNECTOR

USB TYPE B RECEPTACLE

NOTE: EMBEDDED VERSION IS NOT BUS POWERED

USB_MINI_B
VBUS 1 NC
D_N 2 → 18 D-
D_P 3 → 17 D+
ID 4 NC
GND 5
J4

VCC3V3
C132 3.3UF 10V
C72 X5R 10V 0.1UF
AVCC 9
AGND 12
XTALIN 11
XTALOUT 10
24MHZ
C264 NPO 50V 11PF
C263 NPO 50V 11PF

VCC3V3
R180 10K 5% 1/16W
WR 32 NC
RD 31 NC
BKPT 28 NC
INT5 84
INT4 22
T0 23
T1 24
T2 25
RXD0 41
TXD0 40 NC
RXD1 43
TXD1 42 NC
SCL 29 USB_SCL 33
SDA 30 USB_SDA 33
RESET 77 POR 33
6 PLACES

PORT E	PE0_T0OUT	86	SERIAL_NUMBER → 33
	PE1_T1OUT	87	
PORT A	PA3_WU2	70	NC
	PA2_SLOE	69	VREF_DETECT → N/C
	PA1_INT1	68	LED_RED → 33
	PA0_INT0	67	LED_GRN → 33
PORT E	PE2_T2OUT	88	VERSION_REQUEST → 56 VERSION
PORT A	PA4_FIFOADR0	71	TMS_LEVEL → 60 TMS_LEVEL
	PA5_FIFOADR1	72	BUFFER_OE → 61 BUFFER_OE
	PA6_PKTEND	73	LAST_WORD → 58 LAST_WORD
	PA7_FLAGD	74	JTP_CMD3 → 24 EXTEND
PORT B	PB0_FD0	34	GPIF_D00 → 32 GPIF_D00
	PB1_FD1	35	GPIF_D01 → 33 GPIF_D01
	PB2_FD2	36	GPIF_D02 → 34 GPIF_D02
	PB3_FD3	37	GPIF_D03 → 35 GPIF_D03
	PB4_FD4	44	GPIF_D04 → 36 GPIF_D04
	PB5_FD5	45	GPIF_D05 → 37 GPIF_D05
	PB6_FD6	46	GPIF_D06 → 39 GPIF_D06
	PB7_FD7	47	GPIF_D07 → 40 GPIF_D07
PORT D	PD0_FD8	80	GPIF_D08 → 41 GPIF_D08
	PD1_FD9	81	GPIF_D09 → 42 GPIF_D09
	PD2_FD10	82	GPIF_D10 → 43 GPIF_D10
	PD3_FD11	83	GPIF_D11 → 44 GPIF_D11
	PD4_FD12	95	GPIF_D12 → 46 GPIF_D12
	PD5_FD13	96	GPIF_D13 → 49 GPIF_D13
	PD6_FD14	97	GPIF_D14 → 50 GPIF_D14
	PD7_FD15	98	GPIF_D15 → 52 GPIF_D15
GPIF	CTL0_FLAGA	54	BIT_CLOCK → 22 BIT_CLOCK
	CTL1_FLAGB	55	GPIF_START → 53 START
	CTL2_FLAGC	56	CTRL2 → 54 CTRL1
	CTL3	51	CTRL3 → 55 CTRL2
	CTL4	52	NC
	CTL5	76	NC
PORT C	PC0_GPIFADR0	57	COUNT0 → 14 COUNT0
	PC1_GPIFADR1	58	COUNT1 → 15 COUNT1
	PC2_GPIFADR2	59	COUNT2 → 16 COUNT2
	PC3_GPIFADR3	60	COUNT3 → 17 COUNT3
	PC4_GPIFADR4	61	COUNT4 → 18 COUNT4
	PC5_GPIFADR5	62	JTP_CMD0 → 19 JTP_CMD0
	PC6_GPIFADR6	63	JTP_CMD1 → 29 JTP_CMD1
	PC7_GPIFADR7	64	JTP_CMD2 → 30 JTP_CMD2
	CLKOUT	100	TDO_SAMPLE_CLK → 23 TDO_SAMPLE_CLOCK
	IFCLK	26	
PORT E	PE3_RXD0OUT	89	CPLD_TCK 33 → 48 TCK
	PE4_RXD1OUT	90	CPLD_TMS 33 → 47 TMS
	PE6_T2EX	92	CPLD_TDI 33 → 45 TDI
	PE5_INT6	91	CPLD_TDO 33 → 83 TDO
	PE7_GPIFADR8	93	SPARE_COM → 9 SPARE_COM
GPIF	RDY0	3	GPIF_DONE → 63 DONE
	RDY1	4	RDY1 → 64 RDY1
	RDY2	5	RDY2 → 59 RDY2
	RDY3	6	
	RDY4	7	
	RDY5	8	
	NC1	13	NC
	NC2	14	NC
	NC3	15	NC
	WAKEUP	79	
	RESERVED	27	

R178 10K 5% 1/16W
R179 10K 5% 1/16W
2 PLACES

R177 10K 5% 1/16W
R188 10K 5% 1/16W
R170 10K 5% 1/16W
R171 10K 5% 1/16W
R172 10K 5% 1/16W
R173 10K 5% 1/16W
R174 10K 5% 1/16W
R175 10K 5% 1/16W
R176 10K 5% 1/16W
R187 10K 5% 1/16W
R186 10K 5% 1/16W
R185 10K 5% 1/16W
R184 10K 5% 1/16W
R183 10K 5% 1/16W
R182 10K 5% 1/16W

VCCINT VCC3V3;1,16,20,33,38
VCC3V3;49,53,66,78,85
GND;65,75,94,99
GND;2,19,21,39,48,50

3 PLACES

R169 4.42K 1%

U24

XC2C256

VQFP100

BANK 2	TAP_STATE0	1	NC
	TAP_STATE1	13	NC
	TAP_STATE2	11	NC
	TAP_STATE3	12	NC
	IDLE_FLAG	72	NC
	SPARE_P065	65	NC
	SPARE_P071	71	NC
	SPARE_P073	73	NC
	SPARE_P074	74	NC
	SPARE_P076	76	NC
	SPARE_P077	77	NC
BANK 1	TCK_CCLK	66	USBHDR_TCK_R → JTAG_TCK 7
	TMS_PROG	67	USBHDR_TMS_R → JTAG_TMS 7
	TDI_DIN	68	USBHDR_TDI_R → JTAG_TDI 7
	INIT_OUT	70	
BANK 2	SPARE_P078	78	NC
	SPARE_P079	79	NC
	SPARE_P080	80	NC
	SPARE_P081	81	NC
	SPARE_P082	82	NC
	SPARE_P085	85	NC
	SPARE_P086	86	NC
	SPARE_P087	87	NC
BANK 1	INIT_IN	28	EMBEDDED_INIT
BANK 2	SPARE_P089	89	NC
	SPARE_P090	90	NC
	SPARE_P091	91	NC
	SPARE_P092	92	NC
	SPARE_P099	99	NC
	SHIFT_CLK	10	NC
	LAST_BIT	4	NC
	BUS_ENABLE	2	NC
BANK 1	TDO_B	27	JTAG_TDO → 20
BANK 2	DOWN_CNT0	97	NC
	DOWN_CNT1	96	NC
	DOWN_CNT2	95	NC
	DOWN_CNT3	94	NC
	DOWN_CNT4	93	NC
	DONE_SM0	3	NC
	DONE_SM1	6	NC
	DONE_SM2	7	NC
	DONE_INH	8	

VCC3V3
R190 10K 5% 1/16W
R189 10K 5% 1/16W
R197 10K 5% 1/16W
3 PLACES

FPGA_TCK
R85 10K 5% 1/16W
R87 10K 5% 1/16W
R88 10K 5% 1/16W

VCC3V3
R195 10K 5% 1/16W
VCC3V3
R196 10K 5% 1/16W
VCC3V3
R181 10K 5% 1/16W

PARALLEL TO SERIAL CONVERTER

TARGET INTERFACE CONNNECTIONS	
FROM	TO JTAG
FPGA_TCK	TCK ALL DEVICES
FPGA_TMS	TMS ALL DEVICES
USB_HEADER_TDI	FIRST DEVICE TDI
JTAG_TDO	LAST DEVICE TDO
EMBEDDED_INIT	NO CONNECTION

3.3V INTERFACE TO LOCAL JTAG OR SLAVE-SERIAL DEVICE CHAIN.
FOR LONG CHAINS OR TRACES, DISTRIBUTE EMBEDDED_TCK
AND EMBEDDED_TMS WITH LVDS BUFFERS.

LEGEND:

- (J1) OPTIONAL NETS ROUTED IN PARALLEL TO LOCAL 2MM CABEL CONNECTOR J1.
- ● COMPONENTS TO BE LOADED FOR THE PRODUCTION ASSEMBLY VERSION ONLY.
- ● OPTIONAL COMPONENTS THAT SUPPORT DEBUG AND/OR DIAGNOSTICS.

NOTE:

MAKE PARALLEL CONNECTIONS TO J1 (OPTION B) AT EACH OF THE NETS MARKED (J1) TO FACILITATE FASTER IN-CIRCUIT RE-PROGRAMMING OF THE CPLD DURING BOARD TEST.
J1 DOES NOT NEED TO BE POPULATED DURING PRODUCTION, BUT THE ASSEMBLY FOOTPRINT IS RECOMMENDED FOR THE PWB LAYOUT.

Embedded USB JTAG: USB Controller, CPLD

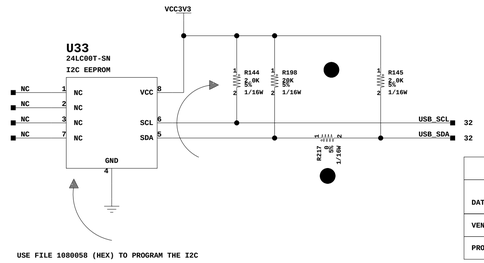
PCB P/N: 043153A
SCH P/N: 0381385
Test P/N: TSS0123
ART P/N: 1280473

Drawing Number: 0381242
Date: 14-JUNE-2006 Ver: C
Sheet Size: D Rev: 02
Sheet 32 of 35 Drawn By SCHWEIGLER

LAST REVISION: 9-24-2009_15:56

The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

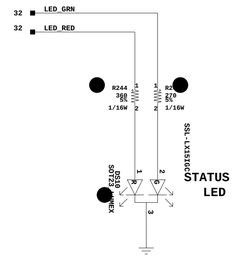
DEFAULT PID/VID EEPROM



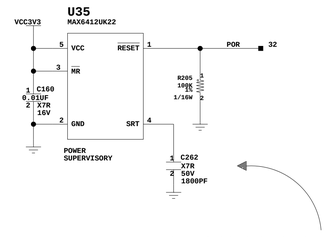
USE FILE 1080058 (HEX) TO PROGRAM THE I2C PROM PRIOR TO ASSEMBLY.

LOW POWER BOOT CONDITIONS		
DATA FIELD	CYPRESS DEFAULT	XILINX EMBEDDED
VENDOR ID	0x004B4	0x03FD
PRODUCT ID	0xB613	0x000D

STATUS LEDS (OPTION A)

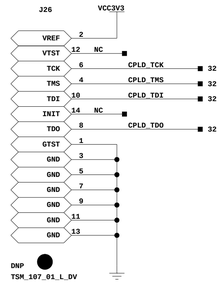


POWER-ON RESET

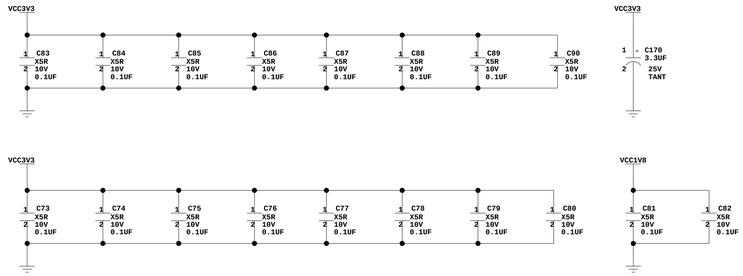


NOTE: PRODUCES 5MS POWER-ON RESET

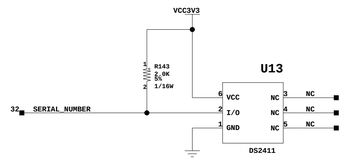
PC4 JTAG CONNECTOR (OPTION B)



BYPASS CAPACITORS



ELECTRONIC SERIAL NUMBER



Embedded USB JTAG: IIC, POR, Decoupling, LED, JTAG Header, Serial Number

Drawing Number: 0381242		PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
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MS1

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MS5

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MS4

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MS2

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MS3

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MN1

NUT_SS_4-40

MN5

NUT_SS_4-40

MN3

NUT_SS_4-40

MN2

NUT_SS_4-40

MN4

NUT_SS_4-40

MSO2

MSO5

MSO3

MSO1

MSO4

MRB3

RUBBER_BUMPER

MRB5

RUBBER_BUMPER

MRB2

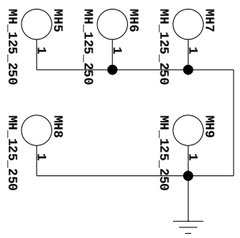
RUBBER_BUMPER

MRB1

RUBBER_BUMPER

MRB4

RUBBER_BUMPER



MJB1

JUMPER_BLOCK_2-PIN

MJB3

JUMPER_BLOCK_2-PIN

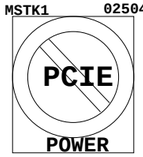
MJB4

JUMPER_BLOCK_2-PIN

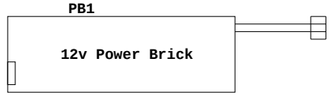
MJB2

JUMPER_BLOCK_2-PIN

MSTK1 0250446



PB1



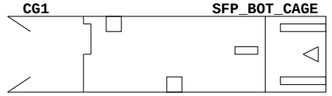
CBL1

Power Cord

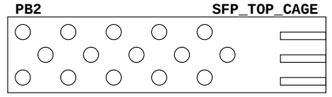
CBL2

USB Mini-B Cable

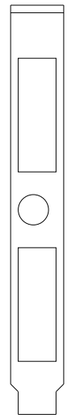
CG1



PB2



PL1

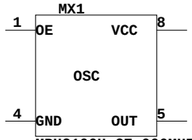


3650017

MJS2

MJS1

MX1



MBH2100H-27.000MHZ

Half Size Oscillator

Mechanical Components

XILINX

Title:	Mechanical Components SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date:	9-25-2009_10:34	Ver:	D
Sheet Size: B		Rev:	02
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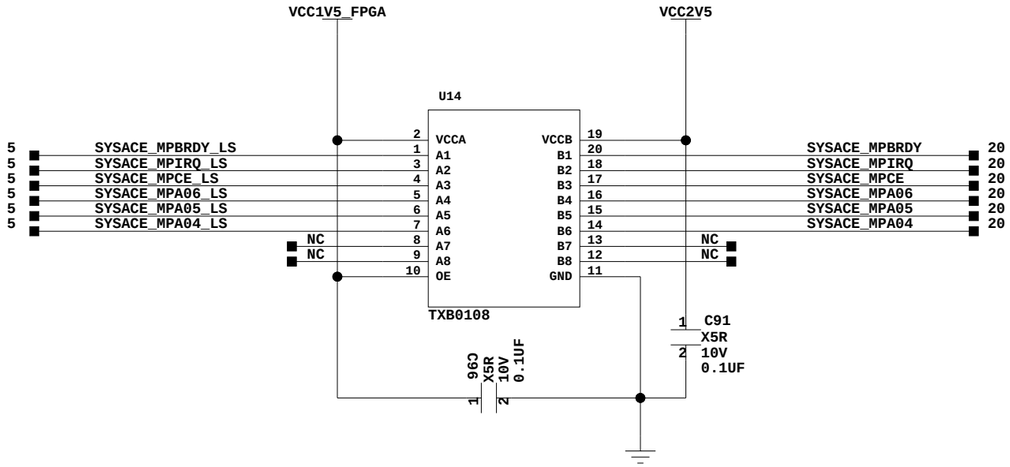

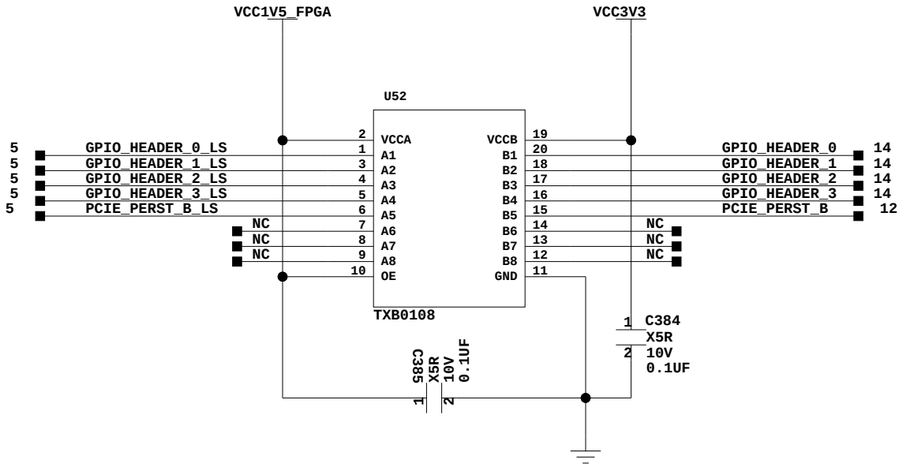

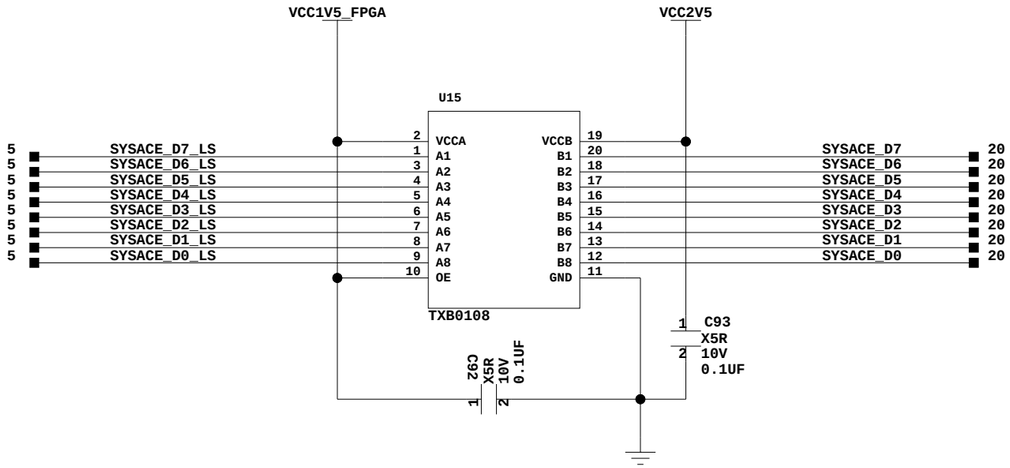

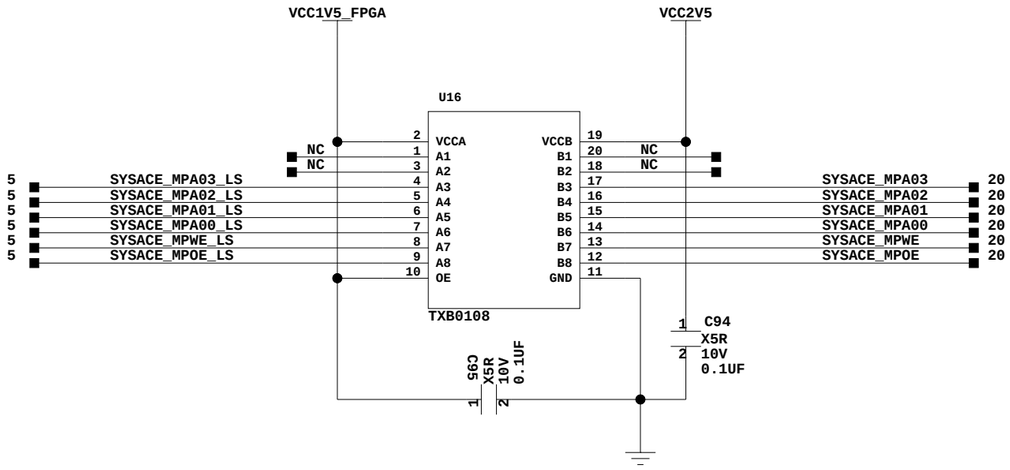

Level Shifters

XILINX

Title:	Level Shifters SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: SCH P/N: Test P/N: ART P/N:	0431534 0381305 TSS0123 1280473
Date: 9-24-2009_15:00		Ver:	D
Sheet Size: B		Rev:	02
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