



Base I/O Library SMIC 0.13 μ m G Process

User Guide

Revision A01

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Chapter 1 Introduction and Nomenclature

This user guide provides the necessary information to build an effective and reliable pad ring using Virage Logic's SMIC 0.13um I/O library. This document will frequently refer to the following power and ground supplies, including other "aliases" to which they may be referred:

VDDIO I/O Power Supply also referred to as VD33 and VDDQ

VSSIO I/O Ground Supply, also referred to as VSSPST

VDD Core CMOS Power Supply

VSS Core CMOS Ground Supply

All Virage I/O Pad Cell names have a prefix designating which SMIC process option is used. These prefixes are as follows:

Table 1-1

Core Oxide	I/O Oxide	Core Transistor	Dielectric Type	I/O Product Prefix
1.2V	2.5V	Normal	(FSG)	sm13ugfsio45b25
1.2V	3.3V	Normal	(FSG)	sm13ugfsio45b33

Chapter 2 Electromigration Guidelines

An analysis of the DC current requirements of the Virage Logic SMIC 0.13um I/O family has been completed. All SPICE simulations were run with Fast P/Fast N models, maximum supply voltages, and 125C temperature, which is the worst case condition for electromigration.

Only the DC, unterminated I/O pad cell current is analyzed. The bi-directional switching AC current electromigration limits are much higher than the DC values, thus only DC current is considered. Keep in mind that this analysis is based only on electromigration constraints. Simultaneous switching (SSO) supply integrity is not considered here. This is highly dependent on load and package considerations. For a fully differential family such as the LVDS drivers and receivers, these guidelines should prove sufficient.

Table 2-1 summarizes these results..

Table 2-1 Virage I/O Family Power/Ground Pad Ratios¹

Cell Type	DC Current (mA)				Single Connect				Double Connect			
					S:Power Ratio		S:Ground Ratio		S:Power Ratio		S:Ground Ratio	
	VDDIO	VDD	VSS	VSSIO	VDDIO	VDD	VSS	VSSIO	VDDIO	VDD	VSS	VSSIO
SSTL2C1	1.88	0.01	0.01	1.88	42.6	500	500	42.6	85.2	1000	1000	85.2
SSTL2C2	3.76	0.01	0.01	3.76	21.3	500	500	21.3	42.6	1000	1000	42.6
HSTL15C1	1.78	0.01	0.01	1.78	45	500	500	45	90	1000	1000	90
HSTL15C2	3.57	0.01	0.01	3.57	22.4	500	500	22.4	44.8	1000	1000	44.8
HSTL18C1	1.78	0.01	0.01	1.78	45	500	500	45	90	1000	1000	90
HSTL18C2	3.57	0.01	0.01	3.57	22.4	500	500	22.4	44.8	1000	1000	44.8
BD25LV_2	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_4	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_6	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_8	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_10	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_12	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_14	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_16	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_18	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000
BD25LV_20	0.01	0.01	0.01	0.01	500	500	500	500	1000	1000	1000	1000

¹ Note: A fundamental assumption made in this analysis is that the bumps can supply a maximum of 80mA of current. This value for the bump current specification must be supplied by the bump and/or package vendor.

The data under the "Current Power I/O" columns refer to the DC current (mA) measured under worst-case electromigration conditions (Fast process, VDDIO=3.6V, T=110 C) for each I/O cell. The current is broken out between the VDDIO, VDD, VSSIO, and VSS supplies, based on how the circuits are actually connected in each design.

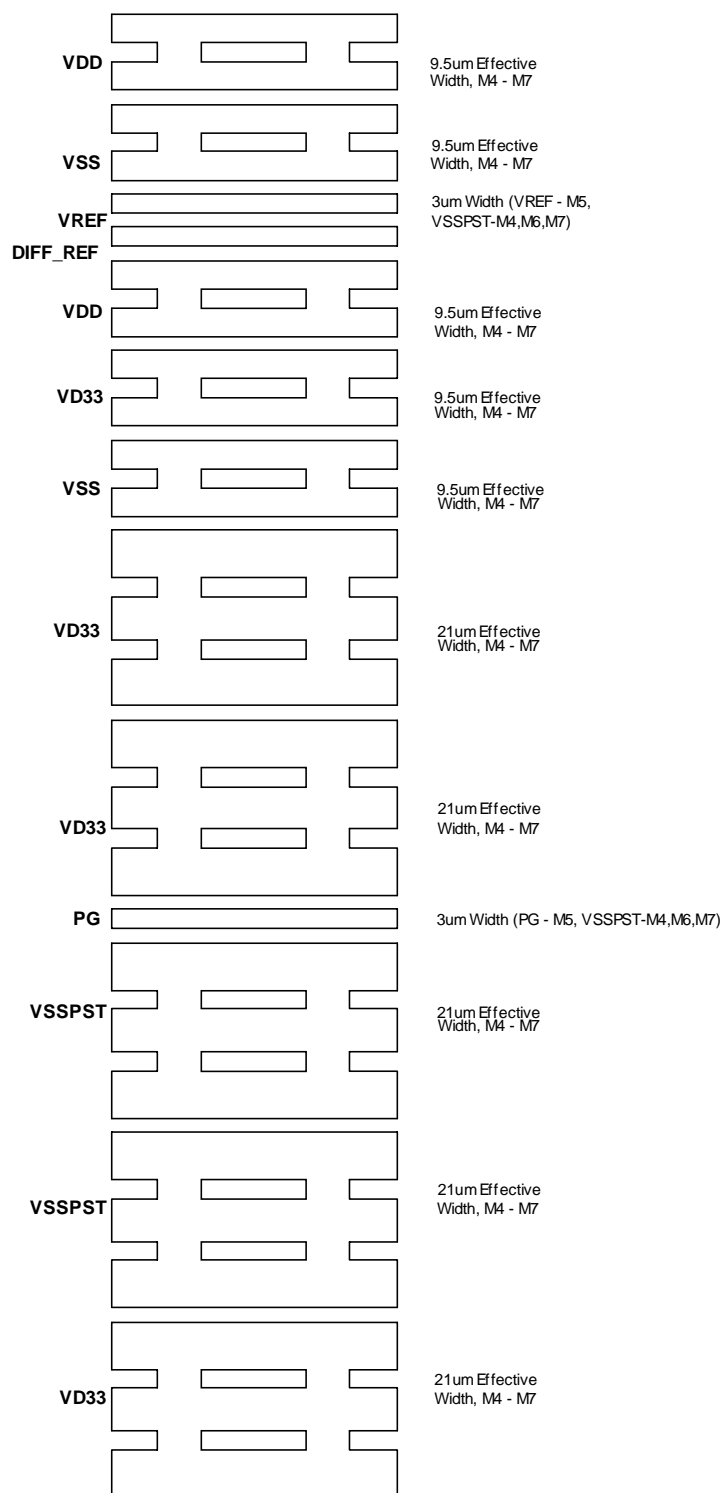
The second and third set of columns are broken out for a single bump/wire bond connected pad cell, or double bump connected pad cell. Virage Logic's power and ground pad cells supply connection points on the top and bottom of each cell, thus current can be supplied from two bumps (if feasible from a bump pattern standpoint). Each column contains the signal pad to power/ground ratio, broken out separately for I/O and core power and ground pads.

Using the HSTL15C1 cell as an example, the VDDIO requirement is 1.78 mA, while the ground current is split between the VSSIO and VSS (core) supplies. Assuming a single bump connection for each power/ground pad, a single VDDIO pad cell can supply 45 driver cells, and a single VDD pad cell can supply 500 driver cells.

2.1 Power Rail Structure

Figure 1 shows the actual widths and location of the multiple VDDIO (referred to as VD33), VSSIO (referred to as VSSPST), VDD, and VSS power buses that pass through each Virage 0.13um library I/O pad cell. The effective width (subtracting out the notch width) on each metal layer of each bus, and the rail it is connected to is indicated on the figure. These bus widths and the current density limits in the SMIC design rules are used to calculate the amount current supplied by (and through) each power/ground pad cell.

Figure 2-1 Virage Logic SMIC 0.13um I/O Pad Cell Power Rail Structure



Chapter 3 Pad Ring Assembly Guidelines

This section contains guidelines on pad ring assembly for individual I/O families based on interface specific applications. The I/O pad ring power structure is assembled by abutment of the I/O cells with each other, including power cells, spacer cells and corner cells. These guidelines cover the usage of VDDIO, VSSIO, VDD, and VSS power pad cells to correctly deliver power to each type of I/O family, and to interface between different I/O families.

All of Virage Logic's I/O pads come as single width, standard height cells. The dimensions of these cells are 45um (width) x 240um (height). The only exception is for the PWR_DIOHV_BK and PWRALL_DIOHV_BK break cells described later in this document. These two tall height cells are 45um (width) x 300um (height).

Specific guidelines concerning analog/reference signals such as vref (SSTL and HSTL) and diff_ref (SSTL) are covered in the I/O family specific sections.

3.1 General Guidelines

The general pad ring assembly guidelines cover the usage of power and ground pad cells, corner cells, and spacer cells.

3.1.1 Power, Ground, Break, and End Cap Cells

The Virage I/O library contains dedicated power and ground cells with built in ESD protection to provide VDDIO (I/O power), VSSIO (I/O ground), VDD (core power), and VSS (core ground). There are also several variations of break cells between separate VDDIO and VSSIO supplies. All available break cells and end cap cells are described in Table 3-1.

The following guidelines should be followed when using the break cells to ensure robust ESD performance.

1. Between 1.2V and 2.5V supplies, or between 2.5V and 3.3V supplies:

Use either the PWR_DIO_BK or PWRALL_DIO_BK break cell. These cells have 4 diodes cross-connected in series between the two different VDDIO supplies, and a single diode connected between the separate VSSIO supplies. Figure 4 Depicts this example.

2. Between 1.2V and 3.3V supplies:

Use two PWR_DIO_BK or PWRALL_DIO_BK break cells connected in series (this will provide 8 diodes cross-connected in series between the 1.2v and 3.3v supplies). See Figure 5 for how this is accomplished.

- a. When only a single wide (45um wide), standard height (240um tall) cell can be used as a break, use the PWR_DIOVSSIO_BK or PWRALL_DIOVSSIO_BK break cell. This cell has only a diode between the two separate VSSIO supplies. There is a full break, with no diode connections between the separate VDDIO supplies. Some ESD performance is sacrificed by not having series diode connections between VDDIO supplies.
- b. When restricted to a single wide (45um wide) cell, but a height of greater than the standard 240um can be used, use the PWR_DIOHV_BK or PWRALL_DIOHV_BK break cell. These cells have 6 diodes cross-connected in series between the two different VDDIO supplies, and a single diode connected between the separate VSSIO supplies. Using this cell will result in improved ESD performance compared to the PWR_DIOVSSIO_BK/PWRALL_DIOVSSIO_BK break cells.

3. Between digital pad ring and a quiet analog VDD/VSS “island”:

Use the ANALOG_BK cell. You must still have a VDDIO and VSSIO supply source (using a PVDDIO and PVSSIO cell on the digital side of any ANALOG_BK cell (assuming you are using PVDDC and PVSSC for analog VDD/ VSS).

4. To cap off the end of a non-continuous section of a pad ring:

Use the ENDCAP_RT (right edge) or ENDCAP_LT (left edge). An ENDCAP cell is required at points where the pad ring is completely broken. Figure 3-5 graphically details the end cap cells.

Table 3-1 Power, Ground, and Break Pad Cell Information

Power/Ground Pad Cell Type	Cell Name	 Buses that have Breaks
VDDIO	PVDDIO	None
VSSIO	PVSSIO	None
VDD	PVDDC	None
VSS	PVSSC	None
Break Cell	ANALOG_BK	Breaks only VDD and VSS, Use for Analog supplies for PLLs, etc.
Break Cell	PWR_DIO_BK	VDDIO, VSSIO, VREF, DIFF_REF, PG (series diode connections between VDDIO/ VSSIO supplies, can support up to a MAX difference of 1.4V between VDDIO supplies)
Break Cell	PWRALL_DIO_BK	VDDIO, VSSIO, VDD, VSS, VREF, DIFF_REF, PG (series diode connections between VDDIO/VSSIO supplies, can support up to a MAX difference of 1.4V between VDDIO supplies)
Break Cell	PWR_DIOVSSIO_BK	VDDIO, VSSIO, VREF, DIFF_REF, PG (diode connection between ONLY VSSIO supplies, for use between 1.2v and 3.3v supplies, when only standard footprint, single wide cell can be used)
Break Cell	PWRALL_DIOVSSIO_BK	VDDIO, VSSIO, VDD, VSS, VREF, DIFF_REF, PG (diode connection between ONLY VSSIO supplies, for use between 1.2v and 3.3v supplies, when only standard footprint, single wide cell can be used)
Break Cell	PWR_DIOHV_BK	VDDIO, VSSIO, VREF, DIFF_REF, PG (series diode connections between VDDIO/VSSIO supplies, to be used between 1.2 and 3.3v supplies)
Break Cell	PWRALL_DIOHV_BK	VDDIO, VSSIO, VDD, VSS, VREF, DIFF_REF, PG (series diode connections between VDDIO/VSSIO supplies, to be used between 1.2 and 3.3v supplies)
End Cap Cell	ENDCAP_RT	Used at the right edge of a pad ring section that is not continuous
End Cap Cell	ENDCAP_LT	Used at the left edge of a pad ring section that is not continuous
Bridge Cell	BRIDGE	Used to bridge standard cells heights to tall cell heights

Figure 3-1 and Figure 3-2 contain additional information regarding the different types of breaker cells. Figure 2 shows the schematics for each breaker cell; keep in mind that there is no difference in the schematics between the *PWR* and *PWRALL* cells. Figure 3-2 shows that the only difference is in the breaking of the power buses.

Figure 3-1 Schematics showing diode connections for each type of Breaker Cell

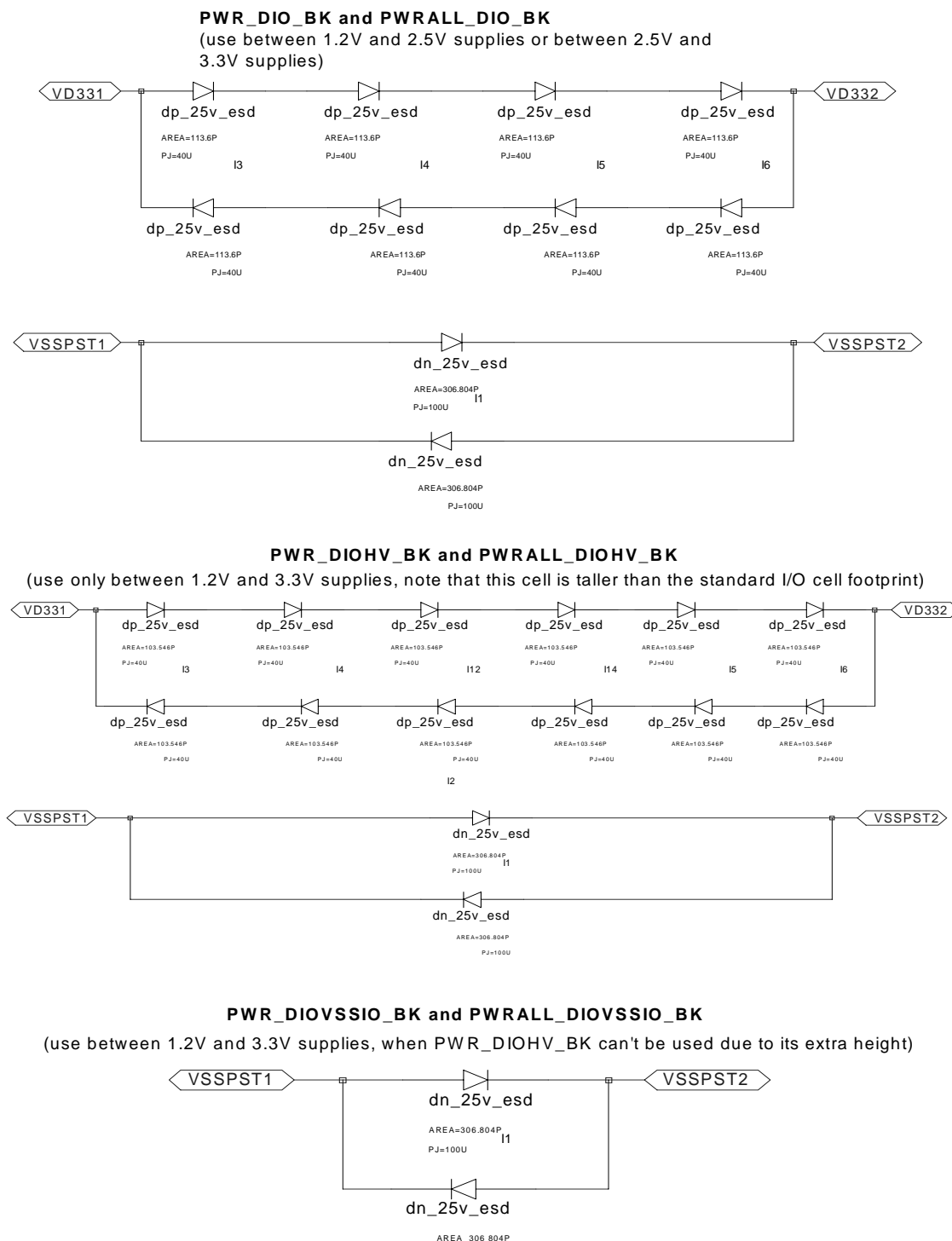


Figure 3-2 Comparison of PWR_DIO*_BK to _PWRALL_DIO*_BK (break all supplies)

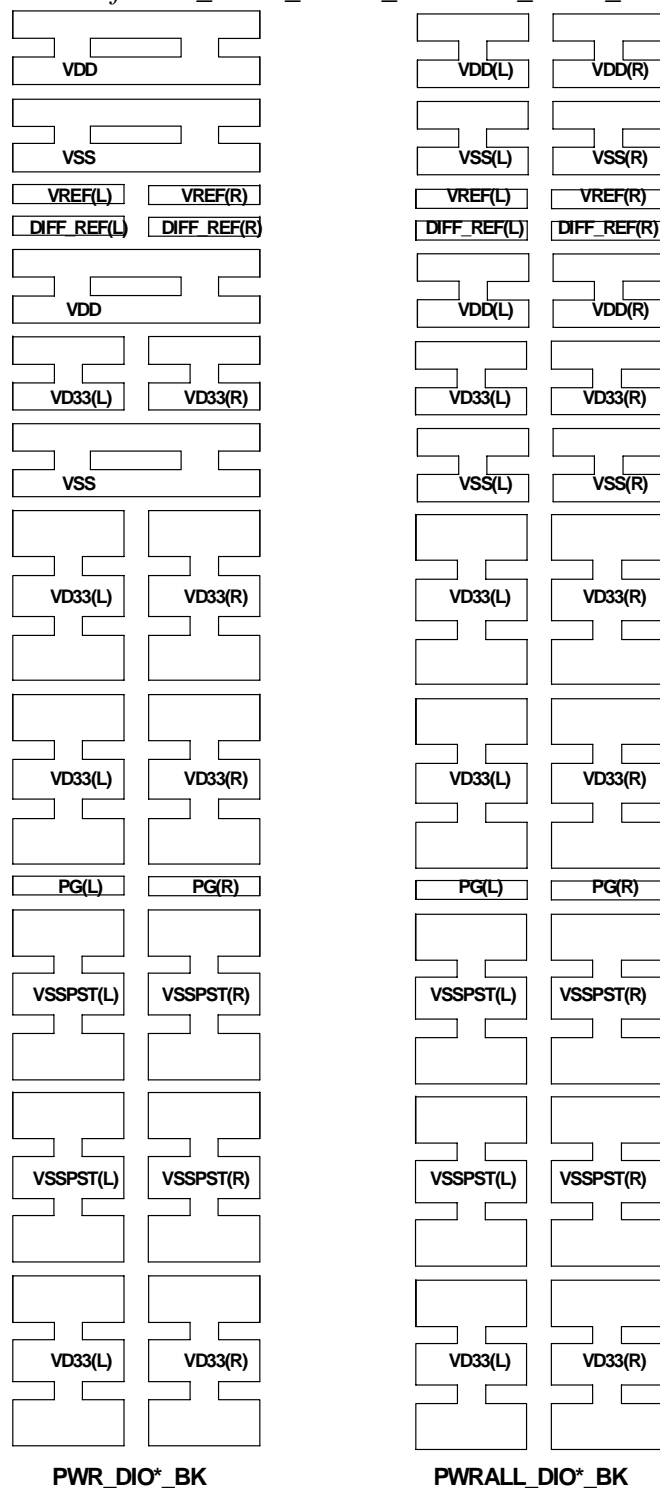


Figure 3-3 depicts a simple example where a break is necessary when an SSTL-2 DRAM I/O interface (requires a 2.5V I/O supply voltage) must be adjacent to a PCI-X I/O interface (requires a 3.3V I/O supply voltage) on the same edge of a pad ring.

Figure 3-3 PWR_DIO_BK I/O power break cell between different I/O power domains (2.5V SSTL - 3.3V PCI-X)

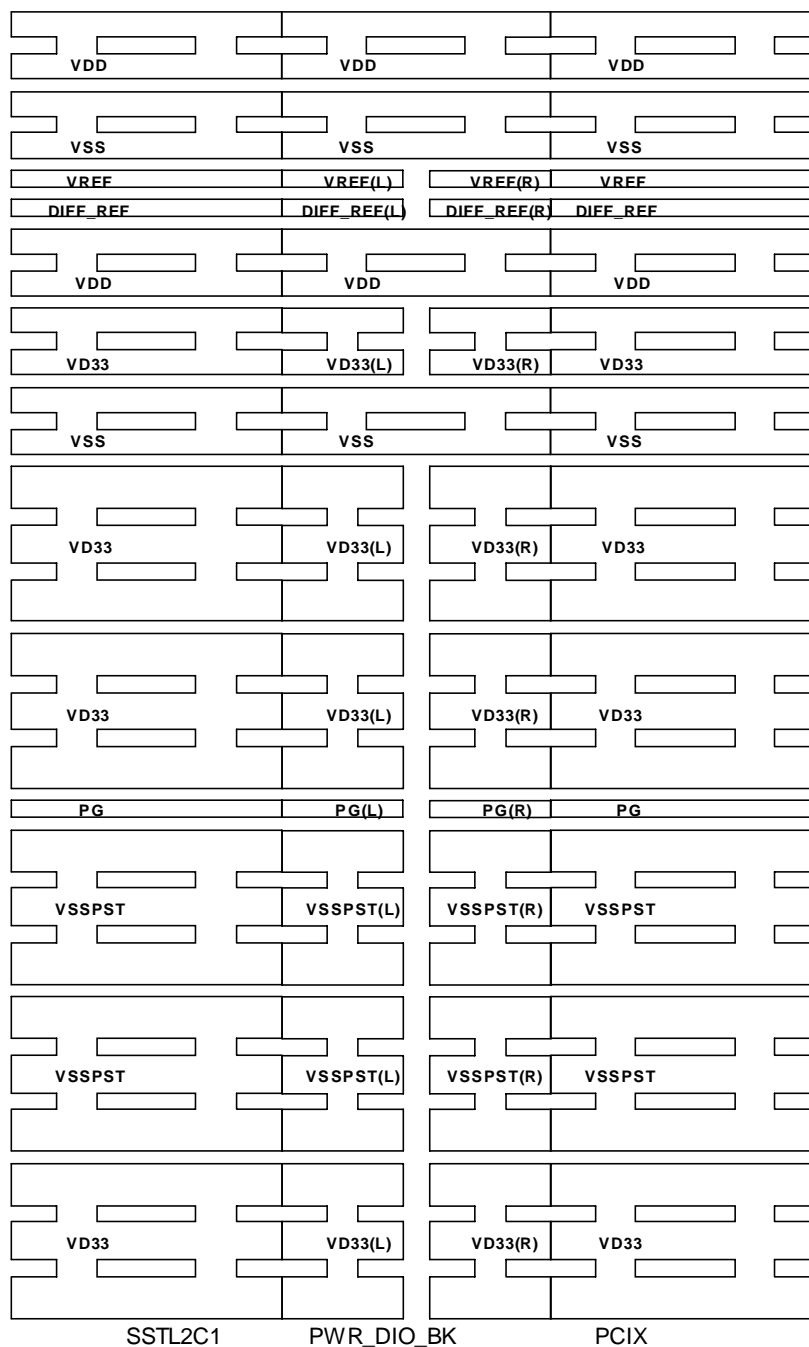


Figure 3-4 Two PWRALL_DIO_BK I/O power break cells between different I/O power domains
(1.5V HSTL - 3.3V PCI-X)

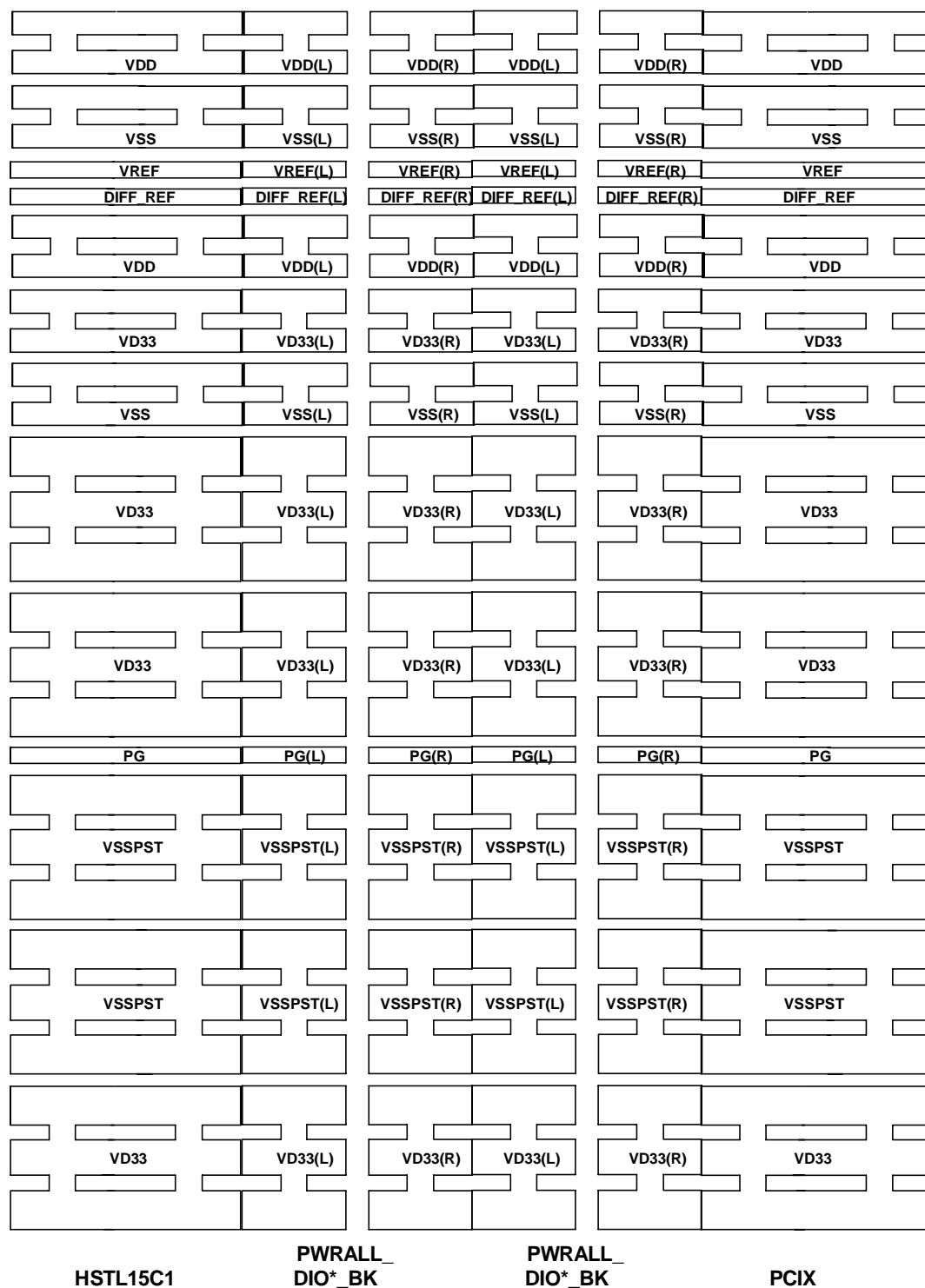
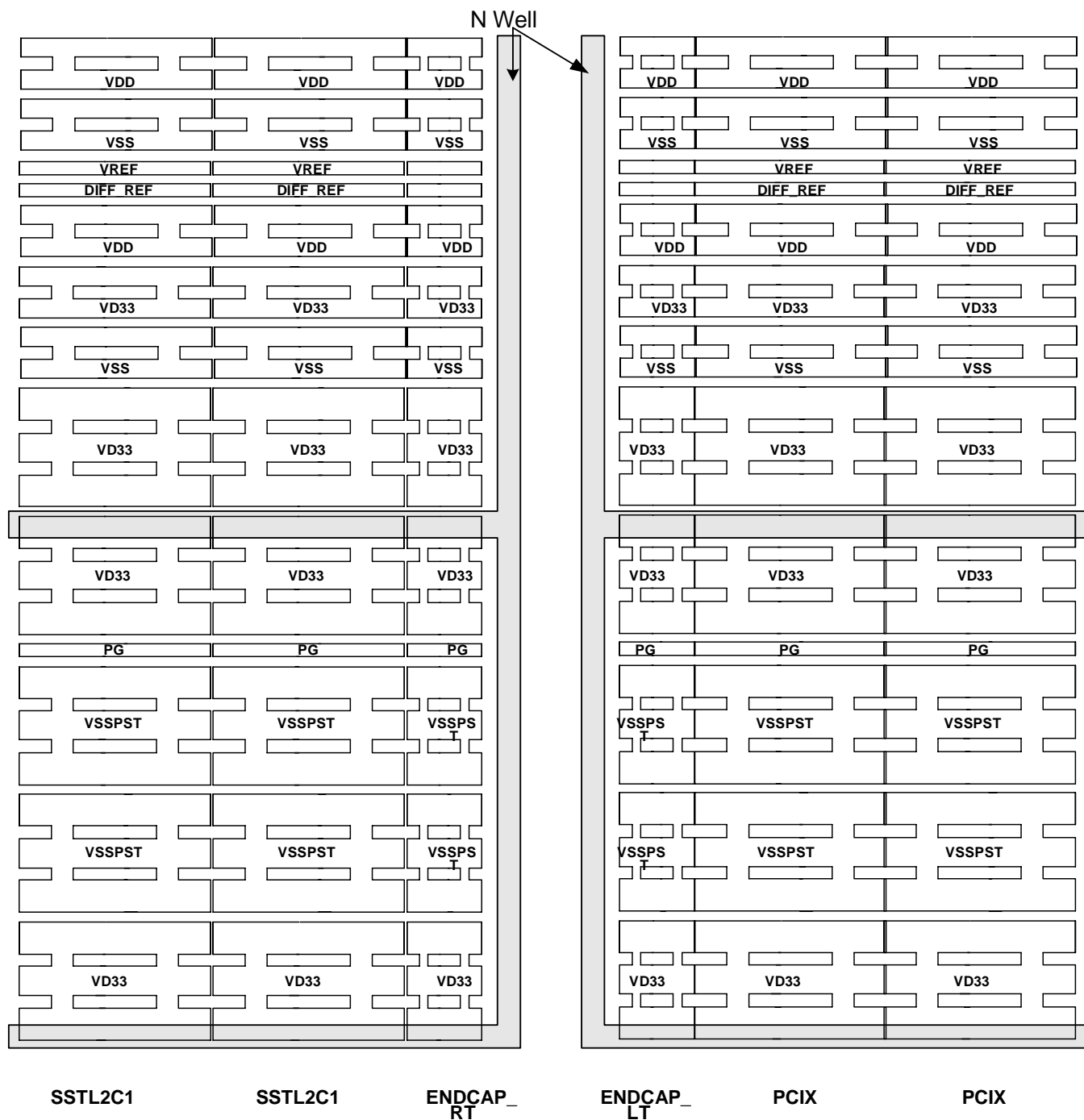


Figure 3-5 End Cap cells - Capping off non-continuous sections of the pad ring



3.1.1.1 Layout Versus Schematic (LVS) Considerations

Global text is attached to the power and ground cells to separate multi-power/ground routing, and for LVS consideration. The pad text attached for LVS is described in Table 3-2.

Table 3-2Table 3: LVS Information for Power/Ground Cells

Power/GroundCells	Pad Text For LVS
PVDDIO	VD33
PVSSIO	VSSPST
PVDDC	VDD
PVSSC	VSS

3.1.2 Spacer/Filler Cells

Spacer cells (also known as filler cells) are used if the pad pitch does not perfectly align. These spacer cells go between I/O cells. Table 3-3 documents the spacer cell names and widths that are currently available. Any number of spacer cells may be combined in any order to fill gaps in between I/O cells. There is one exception to the use of spacer cell SP01, it can not be used alone as the minimum space between two I/O cells is 0.38 microns due to DRC errors.

Table 3-3 Spacer Cell Information

Spacer Cell Name	Spacer Cell Width	Spacer Cell Height
SP01	0.1um space	240um
SP05	0.5um space	240um
SP1	1.0um space	240um
SP2	2.0um space	240um
SP4	4.0um space	240um
SP8	8.0um space	240um
SP16	16um space	240um
SP32	32um space	240um
SP45	45um space	240um

3.2 SSTL-2 Class I and II I/O Reference Bus Guidelines

The SSTL-2 I/O family requires two analog reference signal buses, VREF and DIFF_REF. VREF is used as reference for internal differential amplifiers in the PAD to OUT input receiver path on the SSTL2C* pad cells. DIFF_REF is also used as reference for an internal differential amplifier in the IN to PAD output driver path on all three cells.

The SSTL2REFGEN cell provides both the VREF and DIFF_REF signals. Connection is guaranteed via abutment within a Virage 0.13um I/O family pad ring.

3.2.1 DIFF_REF Reference Bus Guidelines

A SSTL2REFGEN cell can reliably supply a DIFF_REF signal to up to 64 single width pad cells. It is recommended that SSTL2REFGEN be placed in the middle of the 64 cells it is driving, but it is possible to drive from one end.

3.2.2 VREF Reference Bus Guidelines

A SSTL2REFGEN cell can reliably supply a VREF signal to up to 64 single width pad cells.

It is recommended that SSTL2REFGEN be placed in the middle of the 64 cells it is driving, but it is possible to drive from one end.

3.3 HSTL Class I and II I/O Reference Bus Guidelines

The HSTL I/O family requires one analog reference signal bus, VREF, which is used as reference for internal differential amplifiers in the PAD to OUT input receiver path on the HSTLC* pad cell.

The HSTLREFGEN cell provides the VREF signals. Connection is guaranteed via abutment within a Virage 0.13um I/O family pad ring.

3.3.1 VREF Reference Bus Guidelines

A HSTLREFGEN cell can reliably supply a VREF signal to up to 64 single width pad cells.

It is recommended that HSTLREFGEN be placed in the middle of the 64 cells it is driving, but it is possible to drive from one end.

3.4 No Pin I/O Usage

Virage has some cells that have no pins and requires special consideration. This section describes the usage of such cells.

3.4.1 Filler Cell and Corner Cell

Front end kits do not have any notion of a filler or corner cell. However, they exist in backend kits. These cells have no pins, transistors or functions, but they do have power and ground bus connections. Users should not include these cells in their netlist for simulation, but they should be instantiated for the physical layout. Because these cells have no transistors, it is optional to include them for LVS.

3.4.2 I/O Power/Ground Cell

Since these cells are used to supply power and ground to the I/O pad ring, they do not have ppin connections to the core. Since ESD protection is included in these cells, they are required for LVS.

Chapter 4 Power Up Sequence

With Virage I/O library, different voltages are supplied to the core oxide and the second oxide. Because of Virage Logic's ESD structures, there is the equivalent of a parasitic diode from the core power rail to the I/O power rail. Because of this, if the core power is powered on before the I/O power, there will be current flowing through this parasitic diode and may trigger latch-up. To avoid this latch-up problem, Power up the higher voltage first. This will prevent the parasitic diode from turning on. It is important not to power on the higher voltage much earlier than the lower (core) voltage however, as bus conflicting may occur. The time between power supplies coming up should be between 1ms and 500ms ($1\text{ms} < t < 500\text{ms}$), the latter time specified to avoid bus conflicts.

Chapter 5 ESD Protection Methodology

5.1 Power Supply ESD Protection

The ESD protection methodology utilizes the SMI recommended guidelines for VDDC, VSSC, VDDIO and VSSIO protection. This implementation guarantees that all discharge events are directed to VSSPST. For breaking power boundaries on the VDDIO (VD33) power domain diode breakers are provided (See “Power, Ground, Break, and End Cap Cells” on page 5.) There are two general forms that can be implemented. VSSIO only diode breakers or VDDIO and VSSIO diode breakers. The former case breaks the VSSIO power boundary using a cross-connected diodes in the VSSIO (VSSPST) path and forms an open in the VDDIO (VD33) path. Using this type of breaker power domains in the pad ring can be broken and keep a continuous path for ESD discharge events between power domains. The later case allows for the breaking of power boundaries by also placing diodes in the VDDIO (VD33) path. This allows for the diodes to create a short during an ESD event and improve ESD robustness. The later case requires that the power supplies be cycled in during power-on of the chip. The cycling of power should be from lowest supply to highest supply.

Figures Figure 5-1, Figure 5-2 and Figure 5-3 show the VDDC, VSSC, VDDIO, and VSSIO ESD structures and discharge paths for each of the supplies. The VSSIO pad connection discharges into VDDIO supply rail, while the VDDIO pad connection discharges into the VSSIO supply rail, both VDDC and VSSC have discharge paths into either the VSSIO or VDDIO supply rails, with all pad connections having an ultimate discharge path of VSSIO (VSSPST).

Figure 5-1 Power Supply Domain with VSSIO broken only

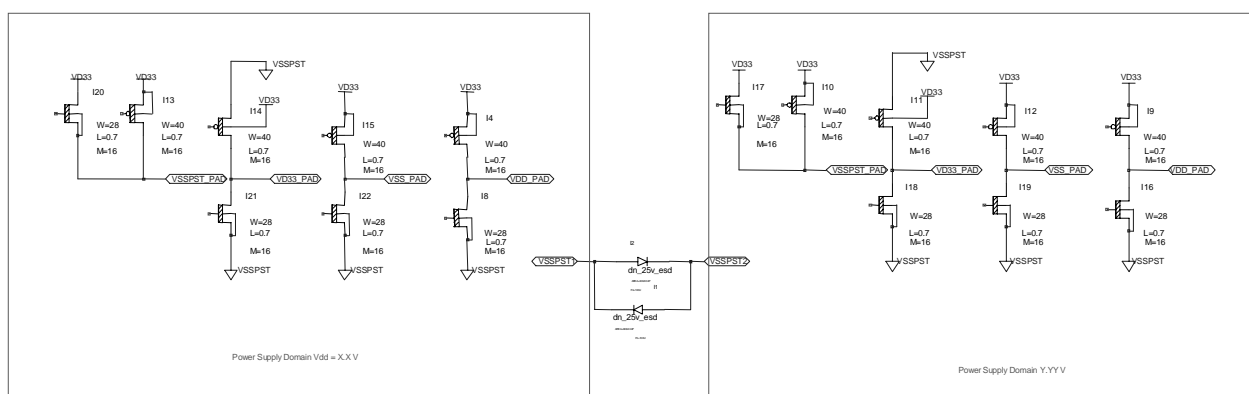
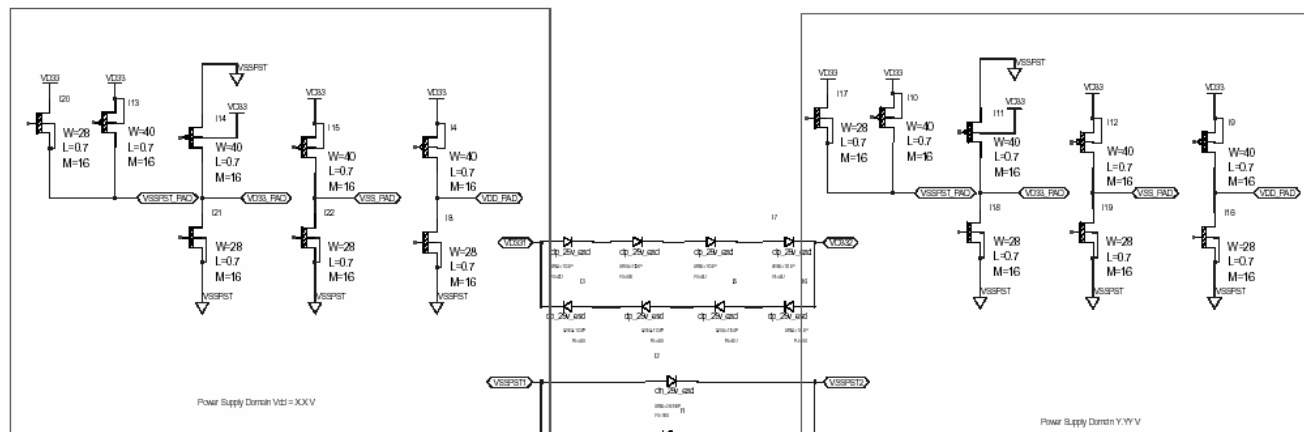


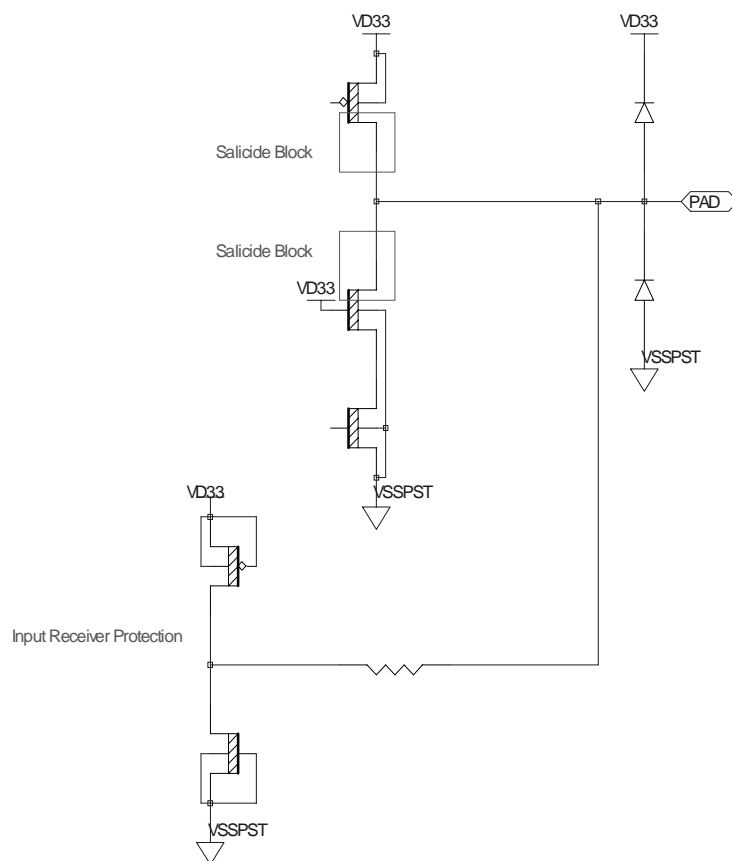
Figure 5-2 Power Supply Domain with VSSIO and VDDIO broken



5.2 I/O Pad ESD Protection

The I/O pad protection uses recommended structures from SMIC and additional structures to improve the ESD robustness of the I/O. The method on how the output driver derives its primary ESD protection is by using a combination of stacked N channel devices, non-minimum channel length devices for both P and N channel output stack transistors and salicide block (RPO) on the source side of the pad connected devices. Additional protection for the device is derived by salicide block N-diffusion resistors in series with the pad connection of the N and P channel Output drive transistors. A typical breakdown of output resistance is 20/80 to 40/60, where 20% to 40% of the output series resistance is in the N or P channel device, and the remaining 80% to 60% of the output resistance is in explicit N-diffusion resistance. The pad side of the resistor is protected by ESD diodes connected to VSSIO and VDDIO (VSSPST, VD33). Both of these devices provide a discharge path for the ESD event into the I/O power rails during and ESD event.

The input is protected by a 200 ohm poly resistor with bleed devices which will discharge the charge built up on the gate of the input receiver during an ESD event

Figure 5-3 I/O ESD Protection

5.3 I/O ESD PAD Ring Assembly

Each power domain within a pad ring must have a VDDC, VSSC, VDDIO and VSSIO cell to ensure protection of power rails during an ESD event. The associate I/O cells with that power boundary must be contiguous with to these power cells (i.e. abutted) by using a combination of additional power cells, spacers or corners to join the power rings in the power boundary formed to create an I/O interface. Diode Breakers should be limited in use only to break power domains. No other opens in the I/O pad ring is allowed with the exception of the use of an ENDCAP at the end of a ring that is being opened to insert special cells that do not share the Virage I/O powering structure or ESD methodology.

Chapter 6 IDDQ Mode

Each Virage I/O has the ability to be placed into IDDQ mode. This is a test mode where all static current paths are turned off. This test mode is enabled by setting the 'pon' pin for the I/O to a '0'. The transmitters in this mode transmit at full swing (except for the LVDS drivers), and the receivers operate in an LVC MOS mode. This mode is low performance and it is suggested that the outputs of I/O cells are tristated while in this mode. Please refer to the datasheets of the I/O for the schematic drawings of the I/Os.

Chapter 7 Flip Chip Guidelines

The following guidelines are only intended as a reference. The actual placement of the flip chip bumps in any IC design is guided by package, chip and electromechanical trade-offs. The pad ring structure provided in the Virage pad ring is designed to support 225um flip chip ball pitch.

All power and ground cells in the pad ring have been designed for double connections of flip chip pads to the power rings in the I/O ring. The I/O cell pitch for this library is 45um. By using the following starting point for flip chip ball placement and trace escape a 6 deep configuration is illustrated. In Figure 7-1, the blue balls represent signal positions in the peripheral placed ball array, the red balls represent power or ground connections into the pad ring (or if power or ground connections are not required, to meet SSO or electromigration limits of the power rail, it could be reassigned to an I/O location), and the green balls are optional balls which if populated and connected could be used as second power connections onto a power supply cell to double the current delivered into the power ring. The balls illustrated are on a 225um pad pitch. It is preferred to have the power balls on the outermost rows to reduce resistance in the power path to the pad ring for ESD considerations. Inner balls should be reserved for I/O signals. Ball assignment for a differential I/O should be done by assigning two adjacent balls the true and complement signals from the I/O cell (which are 90um wide) to ensure good chip level signal integrity balance. All redistribution from the I/O to the flip chip ball should be done in top metal and be routed at maximum width to ensure minimum resistance in the signal path.

Figure 7-1 Example Flip-Chip Route