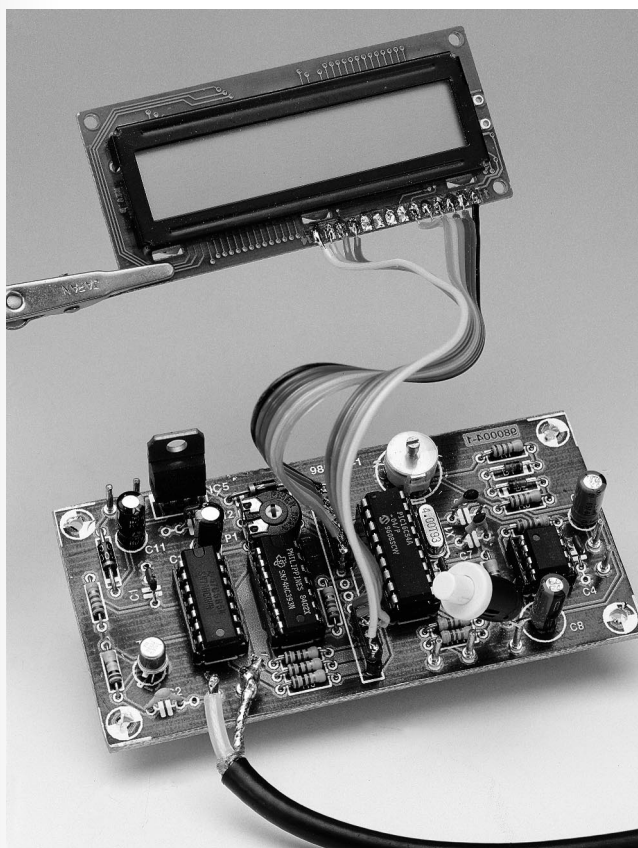# Frequency display and VFO stabilizer

eliminates frequency drift in home-brew and 'surplus' HF receivers

One of the most frequent topics for discussion among the many 'Home Brewers' on the amateur bands is the difficulty of building a VFO that is stable enough to be used on all of the HF bands. The relatively simple circuit described here will stabilize the frequency of an HF VFO, and provide a digital frequency display. The display will allow for the different frequency offsets required for USB and LSB, and the fact that the VFO frequency may be above the signal frequency on some bands, and below it on others.

By Eamon Skelton, EI9GQ

The circuit uses a microcontroller to count the frequency of an HF VFO (variable frequency oscillator), add or subtract the IF (intermediate frequency) offset, and display the signal frequency on a standard Hitachi intelligent LCD display module. The VFO frequency is stabilized by sending a correcting voltage to a varicap diode in the VFO. The circuit is based on a 'Huff & Puff' stabilizer that I have been using for several years.

The circuit design philosophy was to keep the hardware as simple as possible, and to use inexpensive and readily available components. This was made possible by using a microcontroller chip which was programmed to take care of most of the complex functions like counting, arithmetic, and driving the LCD display module. Two versions of the unit were built, one using the 8031 microcontroller, and this version using the PIC 16C54. I have tested the circuit at various frequencies between 8 MHz and 80 MHz.

CIRCUIT DESCRIPTION

The circuit diagram of the VFO stabilizer is shown in **Figure 1**. The circuit is basically a Frequency Locked Loop (FLL). As many of you will be aware, the PIC16C54 microcontroller is a complete computer on a chip with 512×12 bits of ROM, 32 bytes of RAM, a clock circuit, 12 I/O pins, a real time clock/counter, and several other useful features. For a full description of the PIC16C54 and its instruction set, see the Microchip data book or Microchip data sheet DS300151.

The RF signal picked up from the VFO is amplified and digitized by T1, then buffered by IC1b. The BSX20 is a fast switching transistor for use up to 200 MHz. The amplified signal is gated by IC1c and IC1d. A 100-ms gate pulse is generated by a software delay loop in the PIC. The square wave pulses from IC1d are counted by IC2 which is configured as an 8-bit counter.

The output of IC2b is connected to the RTCC input of the PIC through a 1.2kΩ resistor (R6). The PIC has a real-time clock/counter (RTCC) which can count pulses applied to the RTCC input (pin 3). The RTCC register is only eight bits wide giving a maximum count of 255. If the PIC's internal prescaler is set to divide by 256 the
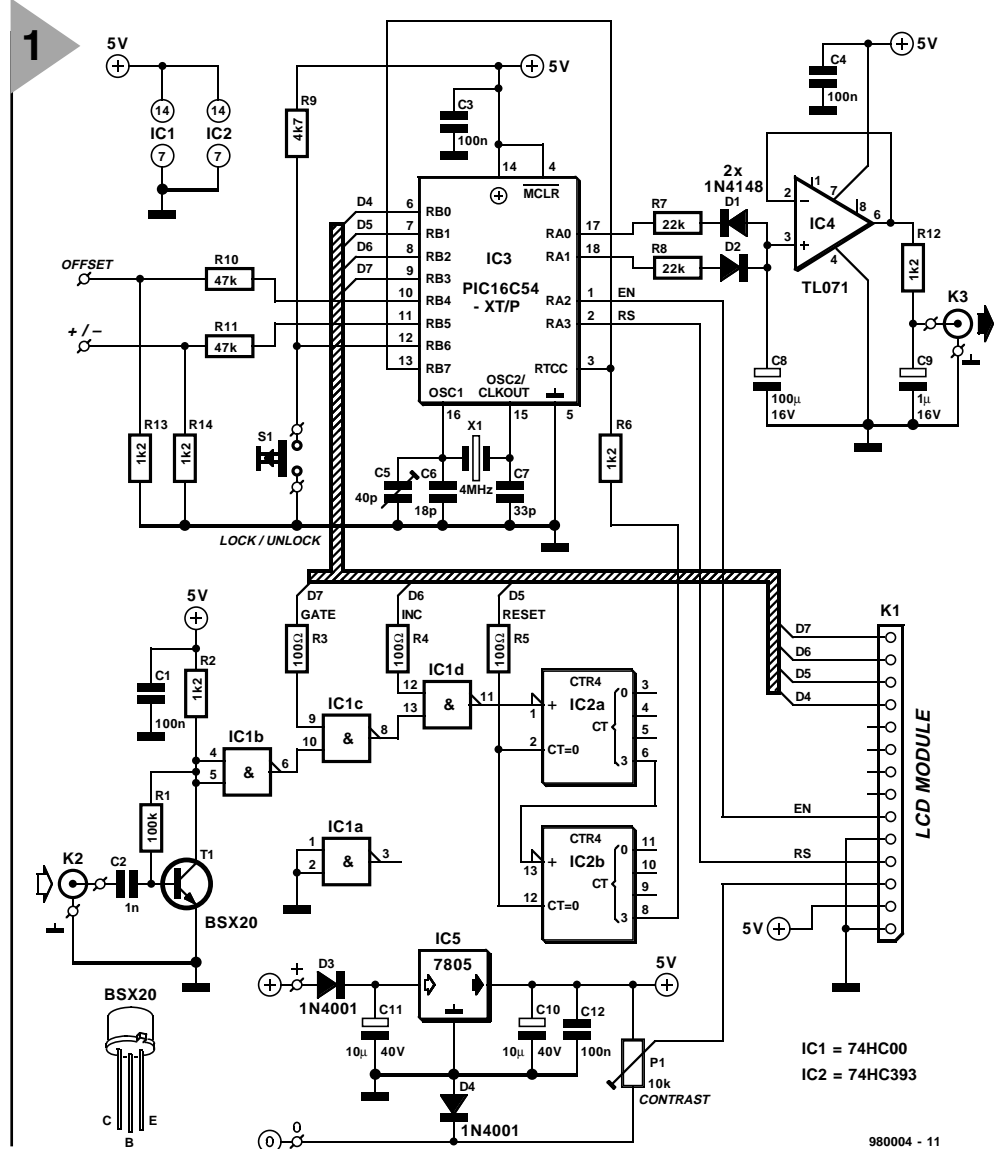
maximum count is 65,535, effectively making a 16-bit counter. With a 1-ms gate time this would allow the counter to count up to 65.535 MHz but the resolution would be 1 kHz which is not good enough for our purposes.

The 74HC393 counter chip increases the count to 24 bits, or 16,777,215. With a 100-ms gate time this will allow a maximum count frequency of 167.77721 MHz and a resolution of 10 Hz, that is, if you can find logic chips that are fast enough. One problem with this arrangement is that it is not possible to read the least significant 8 bits directly from the 393 counter.

This problem is overcome by sending pulses to the counter input through gate IC1d. By counting the number of pulses it takes to make the counter overflow it is a simple matter to calculate the value in the '393 at the time the gate was closed. As the PIC internal prescaler can not be read directly, a similar method is used to calculate the value in the internal prescaler. Pulses are applied to the prescaler input by pin 13 of the PIC (RB7) until the prescaler overflows. The most significant 8 bits can be read directly from the RTCC register. This may seem like a strange way of reading the count but it is quite easy to implement in software and makes the circuit hardware very simple.

Now that we have the count result stored in the PIC, the IF offset must be added or subtracted; the result is the signal frequency in binary. This number is converted first to BCD, then to ASCII and finally sent to the LCD display module. A new count takes place about 9 times every second, the display is updated every second count, or just over 4 times a second. Updating the display more often than this causes the last digit to flicker, updating less often makes the display 'sluggish' when you tune quickly across the band. Before the first digit of the frequency is displayed a test is done to find out if it is a zero. If it is then a blank space is displayed instead, giving automatic leading zero suppression. Whether the IF offset is to be added or subtracted is determined by the state of the ADD/SUBTRACT ($+/-$) input, which is linked to an input pin on the PIC. Whether the offset is for USB (upper sideband) or LSB (lower sideband) is determined by the state of the OFFSET input pin. Suggested circuits for controlling the ADD/SUBTRACT ($+/-$) and OFFSET inputs are shown in **Figures 2 and 3** respectively. Mind you, these are just examples, the exact configuration of the switches depends on the requirements of your HF receiver.

So far the circuit is just acting as a frequency counter and display. At the

end of each count/display cycle, the counters are reset and the cycle is repeated again. No attempt is made to control the frequency of the VFO. The control voltage at the output of the integrator is set at about 2.5 volts and remains there until the LOCK/UNLOCK button, S1, is pressed.

HOW THE VFO IS CONTROLLED

When you find a frequency that you want to stay on, press the LOCK/UNLOCK button. After the button is pressed there is a 100 ms delay, then the result of the most recent count is stored in three registers in the PIC. The result of all subsequent counts are compared with this value. If the current count is less than the stored value, the VFO has apparently drifted lower in frequency; a positive pulse is sent to the integrator (IC4) to correct the error. If the current count is greater than the stored value then a negative correction pulse is generated.

The width of the correction pulse depends on the degree of VFO drift. If the error is less than 10 Hz then a very short pulse of about 2 ms duration is generated. Greater frequency errors result in longer correcting pulses: 20 Hz = 4 ms, 30 Hz = 6 ms, 40 Hz = 8 ms and so on. This results in much tighter control of the VFO than can be achieved with a conventional 'Huff and Puff' circuit.

When the circuit is in locked mode, the LCD display readout changes: 'MHz' disappears from the display and is replaced by the 10-Hz digit. To the right of this is the error level display which is shown as E0 to E9. E0 means that the error is less than 10 Hz, E1 is an error level of 20 Hz, E9 is an error level of 100 Hz. If the error level is greater than 9, a '9' is still displayed. The last character on the display is the correction direction indicator: '>' indicates a positive pulse, '<' indicates a negative pulse. A low error level indication of 0 or 1 and a continuous rapidly alternat-

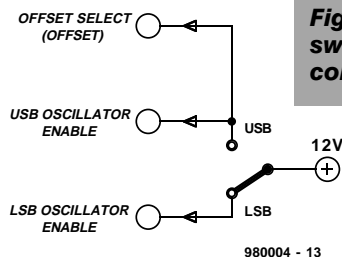**Figure 1. Circuit diagram of the Frequency Display and VFO Stabilizer.**

OFFSET SELECT
(OFFSET)

USB OSCILLATOR
ENABLE

USB

12V
(+)

LSB OSCILLATOR
ENABLE

LSB

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Figure 2. Suggested method of switching the ADD/SUBTRACT (+/−) control input on the board.

ing up/down indication means that all is well, and the VFO frequency is within the control loop bandwidth of the system.

The varicap diode control of the VFO should be arranged so that the maximum frequency change is approximately ±3 kHz. This should be sufficient range to keep a moderately stable VFO locked for hours or even days!

When you need to change frequency, press the LOCK/UNLOCK button again. This puts the device in unlocked mode, the integrator output is set at 2.5 volts and the display changes back to 6 digits followed by

'MHz'. To lock to a new frequency simply press the LOCK/UNLOCK button again.

THE PROGRAM
Various interesting options are available as regards the control software which resides in the PIC microcontroller. To enable you to make your choice, we first tell you what's available for this project, and then make an important statement.

The items available for this project are (1) a **ready-programmed PIC** (for 10.7 MHz IF), (2) a **ready-made PCB** and (3) a **diskette** containing the **source code files** for the PIC control program. For prices, order numbers and other relevant information, please refer to the Readers Services pages elsewhere in this issue.

And now, a serious note. Although this frequency display/VFO stabilizer

is fairly easy to build, you should realize that *considerable experience may be required to establish the link with the VFO in your receiver.* Before building this project, you should, therefore be positive about the following points

1. The receiver is a heterodyne (mixer) design. The VFO frequency is between 8 and about 80 MHz.
2. The VFO has varicap control allowing a tuning range of ±3 kHz to be produced by a control voltage swing of 5 V (2.5 V = centre tuning).
3. The VFO signal can be 'tapped' in a safe way (preferably by inductive coupling) and has a level of at least 100 mV$_{pp}$.

Most experienced radio amateurs (and not only those who actually transmit!) will be able to come to terms with these conditions, if necessary with the help of a fellow ham.

Back to your options! Here's what you can do.

1. I have a receiver with an IF of 10.7 MHz.
Simply order the PCB, the ready-programmed PIC and the source disk supplied through our Readers Services.
2. I have a receiver with an IF other than 10.7 MHz.
Order the PCB (**980004-1**) and the source code disk (**986006-1**) as separate items. Purchase a PIC16C54, and get hold of a an assembler and a PIC programmer. Edit the source code as explained in the README file, and then program your own PIC.
3. I have a receiver with an IF of 455 kHz or 7.8 MHz.
Do the same as under 2. The necessary files are on the disk.
4. I can make my own PCBs and program my own PICs.
Order the diskette only (**986006-1**). Make your own PCB using the artwork shown in this article. Burn your own PIC for the IF you require. Tell your friends about it.
A PIC programmer can be built from one of the many published designs, or a commercially made unit can be purchased from one of several companies advertising in this magazine. The source code file on disk may be edited using any ASCII word processor. Details on modifying the IF offset are also available. Examples are available for 10.7 MHz, 455 kHz and 7.8 MHz.
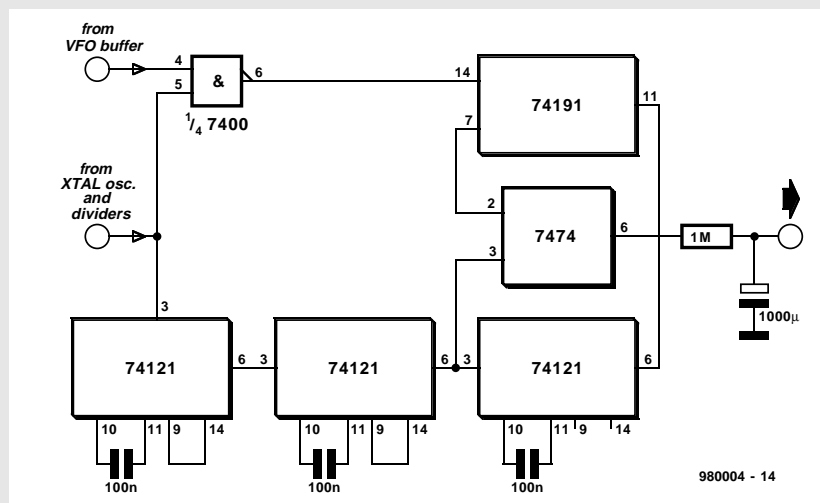
CONSTRUCTION
If you use the PCB layout shown in **Figure 4** and a ready-made board, construction of the circuit is fairly easy. Check the orientation of all polarized components (electrolytic capacitors, diodes, ICs, transistor T1). Use sockets
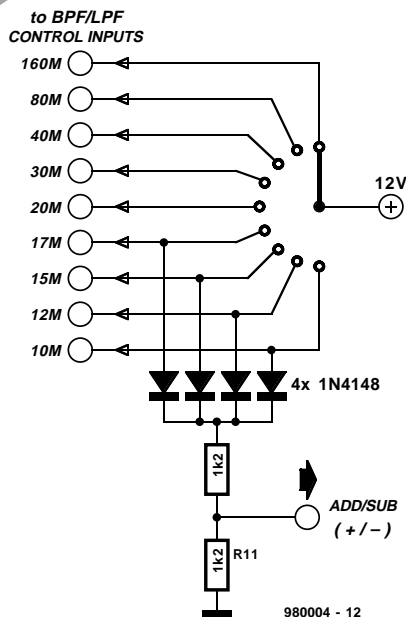
Huff and Puff

Although this circuit is generally referred to as the 'huff and puff' stabilizer among English-speaking hams, it should really be called the PA0KSB VFO stabilizer after its inventor, the Dutch radio amateur Klaas Spaargaren, PA0KSB. The circuit can act as an outboard enhancement with any reasonable VFO, keeping the output frequency stable within a couple of hertz without adding parasitics and other whistles to the VFO output.

A crystal oscillator, whose output frequency need not be a round value, is followed by a divider cascade which open a gate for, say, 1 second. Next, a binary counter counts the VFO cycles within this gate period. On closing the gate, the last counter digit is compared to '8'. If it is smaller, the 2^3 output of the counter is reset to 0. If it is greater, the output is made logic 1. The counter output is applied to a D-bistable. If the gate signal drops to 0, the first one-shot is triggered. Next, the second one-shot clocks the 1 or the 0 into the D-bistable. Finally, counter is reset by the third one-shot. If the counter signal was a 0, the $\overline{Q}$ output of the bistable goes high, charging the capacitor and so causing the VFO frequency to go up. By contrast, a counter signal of 1 causes the frequency to go down. In this way, the VFO frequency 'puffs' at a rate of a few hertz around the stabilization point at which the counter detects an '8' as the last digit. Over the years, the basic design by PA0KSB was enhanced and followed by several variants using a raster of about 40 Hz, allowing virtually continuous tuning.

from
VFO buffer

4
5

&

6

$\frac{1}{4}$ 7400

from
XTAL osc.
and
dividers

14

74191

11

7

2

7474

6

1M

3

1000μ

3

74121

6 3

74121

6 3

74121

6

10 11 9 14

10 11 9 14

10 11 9 14

100n

100n

100n

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3

to BPF/LPF
CONTROL INPUTS

160M
80M
40M
30M
20M
17M
15M
12M
10M

12V
+

4x 1N4148

1k2

ADD/SUB
(+/−)

1k2 R11

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for the ICs if you want to experiment with different logic IC families, LS, ALS, HC etc. If you use 74HC or 74ALS series chips for IC1 and IC2 it will not be necessary to have a heat sink on the 5-V regulator. The circuit was tested with HC ICs, and worked reliably up to about 50 MHz. Higher input frequencies should be possible if you use 'ALS ICs.

The type of opamp used for IC4 is quite critical, the ADOP07CN gave very good results. If you do not have an ADOP07CN available, the TLO71CN also works quite well.

THE DISPLAY

Any general-purpose 1-line 16-character display that uses the Hitachi HD44780 chip should be suitable (the author used a type 16166 LCD display module). Some of these displays have LED or electroluminescent backlighting built in. Do not spend large sums of money on these displays, they are often advertised for less than £5.00.

TESTING

When the unit is first powered up, adjust preset P1 for best contrast on the LCD display. Connect your VFO to the input (C2), set the ADD/SUB input high to add the IF offset, or low to subtract the IF offset. Set the OFFSET switch for USB (high) or LSB (low). The display should show the approximate frequency of the VFO plus or minus the IF offset.

The best way to calibrate the counter accurately is to tune your receiver to a frequency standard signal or a station of known frequency accuracy, then adjust C5 until the displayed frequency is correct. The capacitor val-

ues shown in the circuit diagram worked fine with several 4-MHz crystals from the author's junkbox. If the crystal you are using requires different capacitor values it may be necessary to change the value of C6.

In the author's HF transceiver, the circuit was put in a small box made from copper clad glass fibre board, this box was mounted on top of the VFO. The RF input and control output connections were made with miniature (RG174 or similar) coaxial cable. A short length of ribbon cable is used to connect the LCD module to the PCB. The OFFSET select input may be connected to the USB/LSB switch on the front panel of the rig. The ADD/SUBTRACT (+/−) input may be connected to the band switch of the rig using four diodes (see Figure 2). If you only need to subtract the IF offset, you can connect the add/subtract (+/−) input to ground.

(980004-1)

Components list

Resistors:
R1 = 100 kΩ
R2,R6,R12,R13,R14 = 1kΩ2
R3,R4,R5 = 100Ω
R7,R8 = 22kΩ
R9 = 4kΩ7
R10,R11 = 47kΩ
P1 = 10kΩ preset H

Capacitors:
C1,C3,C4,C12 = 100nF
C2 = 1nF
C5 = 40pF trimmer
C6 = 18pF ceramic
C7 = 33pF ceramic
C8 = 100µF 16V radial
C9 = 1µF 16V radial
C10,C11 = 10µF 40V radial

Semiconductors:
D1,D2 = 1N4148
D3,D4 = 1N4001
T1 = BSX20
IC1 = 74HC00 (see text)
IC2 = 74HC393 (see text)
IC3 = PIC16C54-XT/P (order code 986502-1)
IC4 = TL071CP
IC5 = 7805

Miscellaneous:
X1 = 4 MHz quartz crystal
S1 = push-button, 1 make contact
K1 = 14-way SIL header
LCD module 1×16 characters
PCB only, order code 980004-1
Disk only, order code 986006-1
PIC only, order code 986502-1

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