

***PWWAA***

***LC Marseille***

# **LA-6842P REV 0.2 Schematic**

**Intel Processor (ARD) /PCH (HM55)**

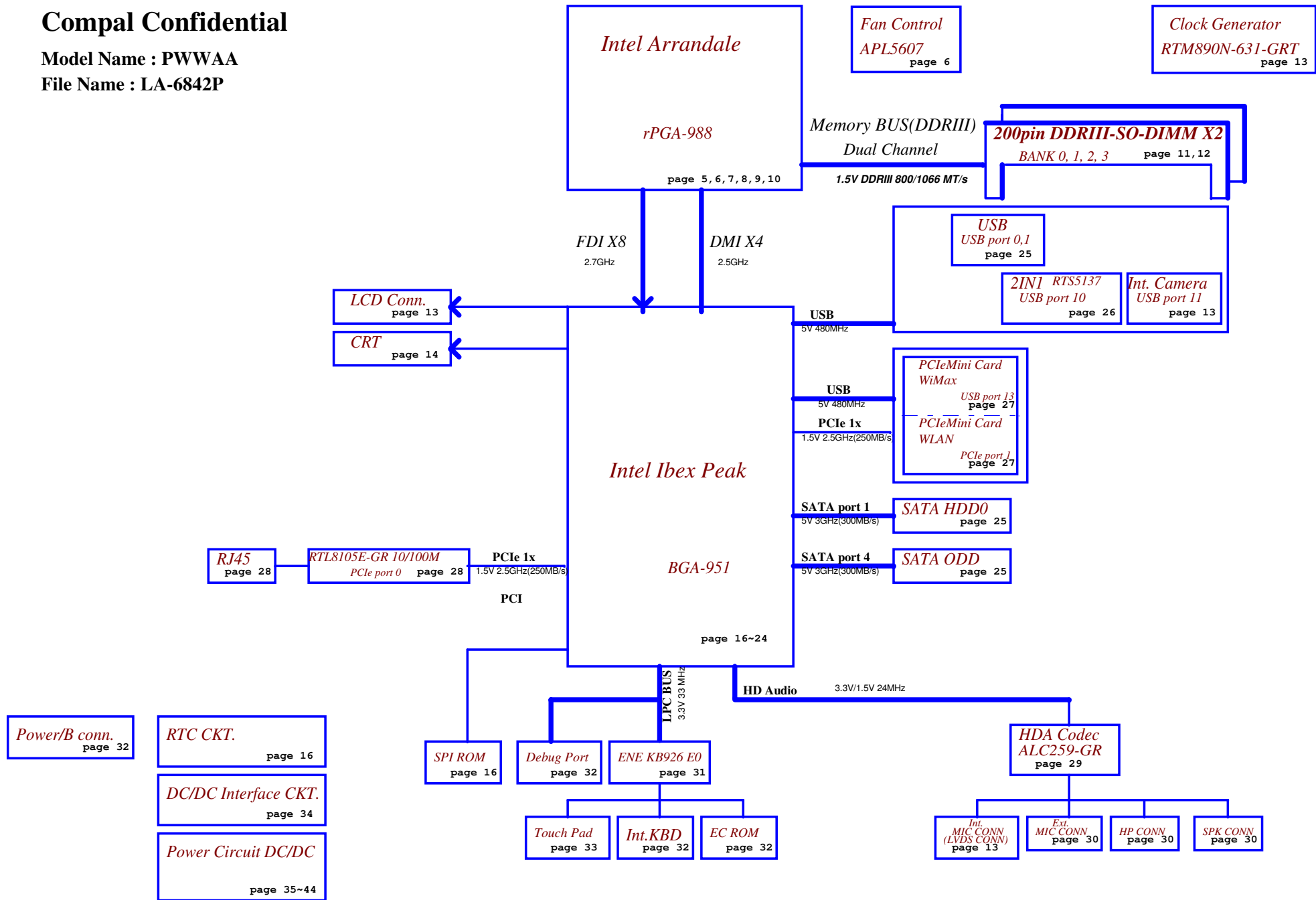
**2010-07-22 Rev 0.2**

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				Date: Wednesday, July 28, 2010	Rev 0.2
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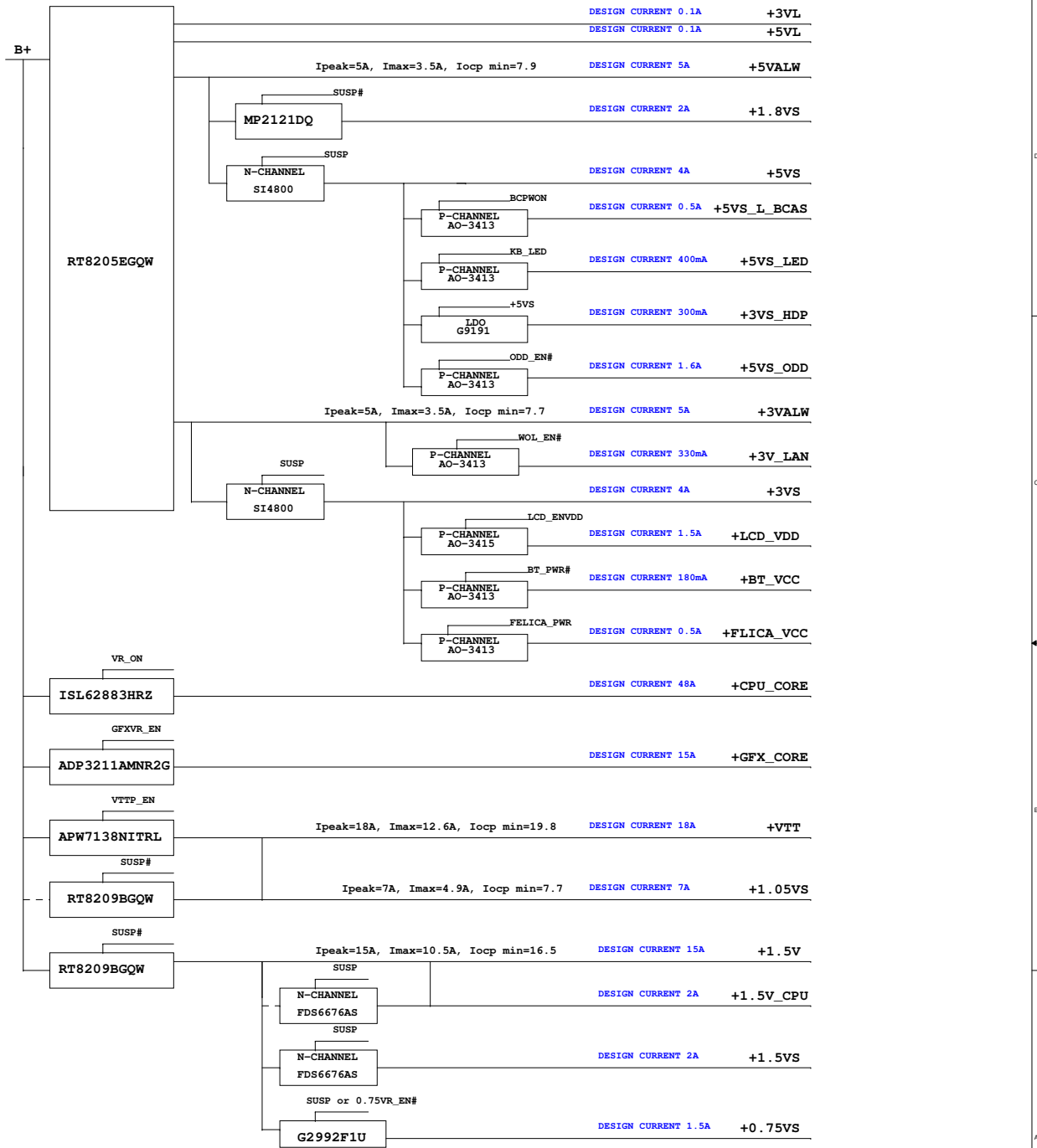
# Compal Confidential

Model Name : PWWAA

File Name : LA-6842P



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Voltage Rails ( O MEANS ON X MEANS OFF )

<div>power plane</div> <div>State</div>	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

BTO Option Table

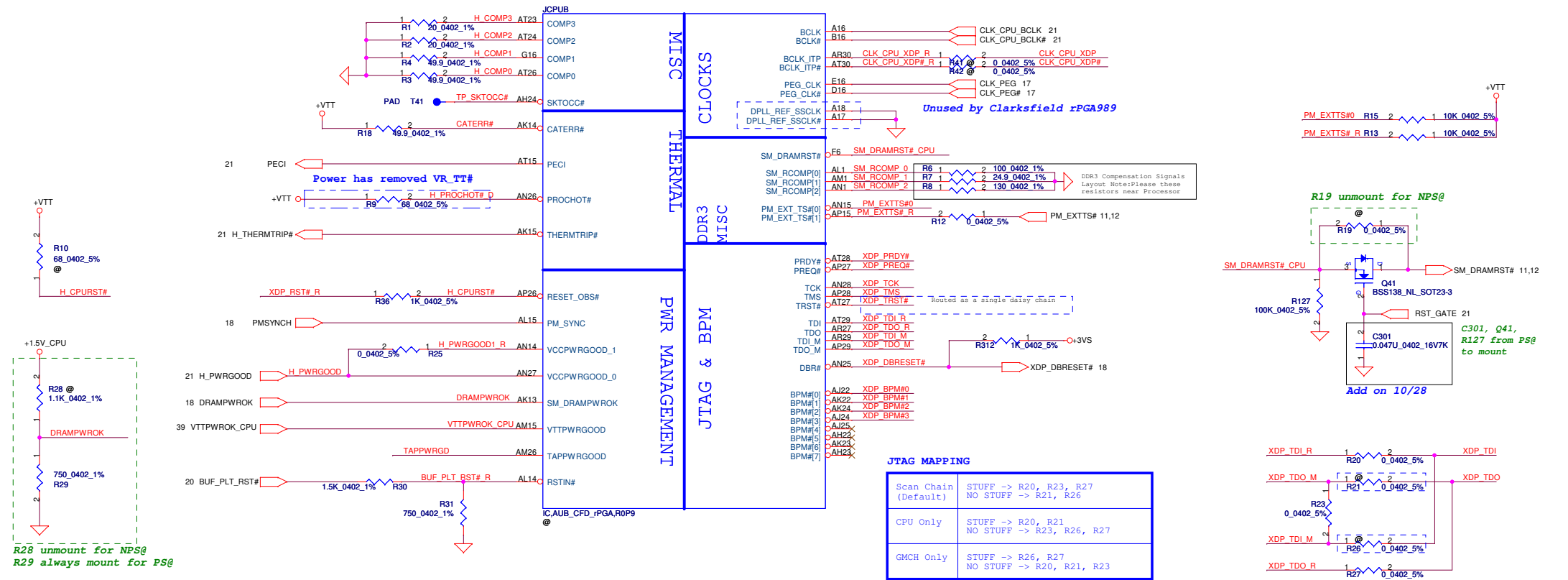
Function	MINI PCI-E SLOT		LAN					
description			SLOT1	LAN				
explain			WLAN/BT	10/100M				
BTO								

Function				Camera & Mic			
description				Camera & Mic			
explain				Camera & Mic			
BTO				CAM@			

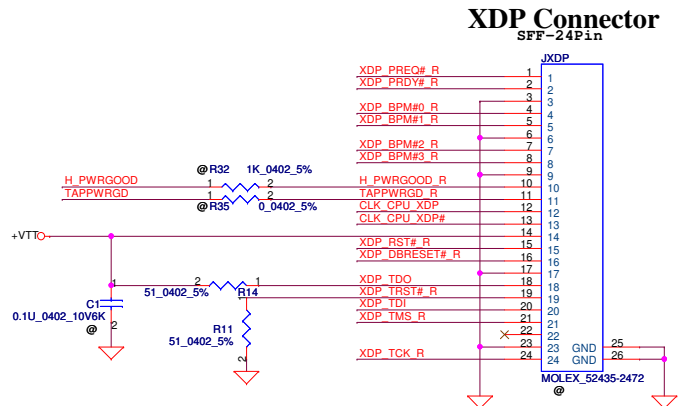
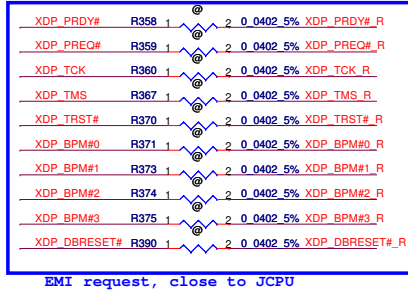
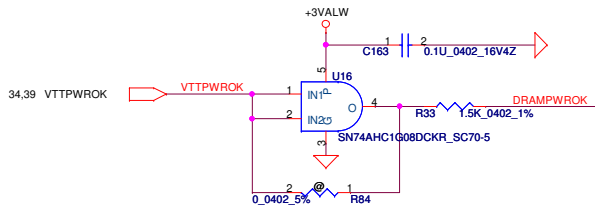
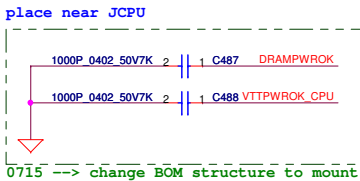
Function	S3 Power Saving	
description	S3 Power Saving	
explain		Power Saving
BTO		

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

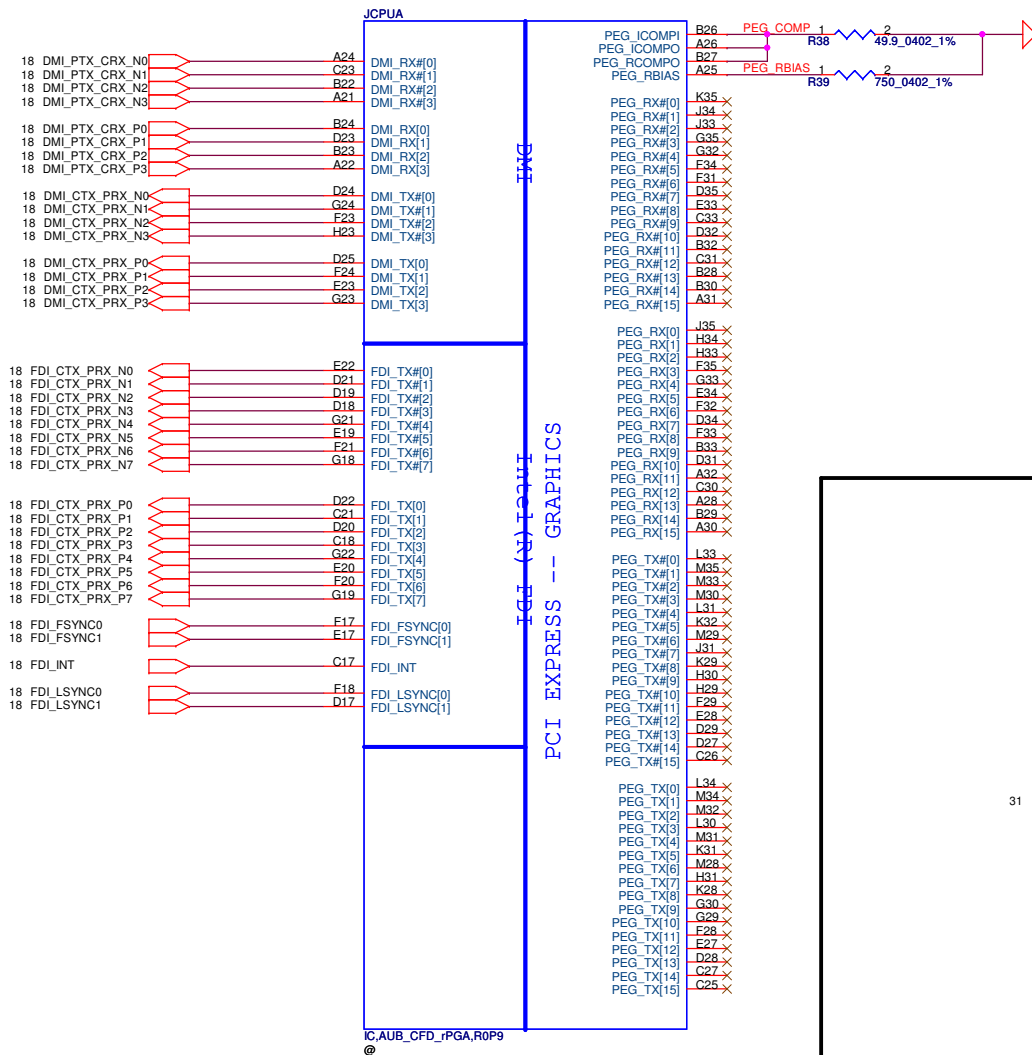
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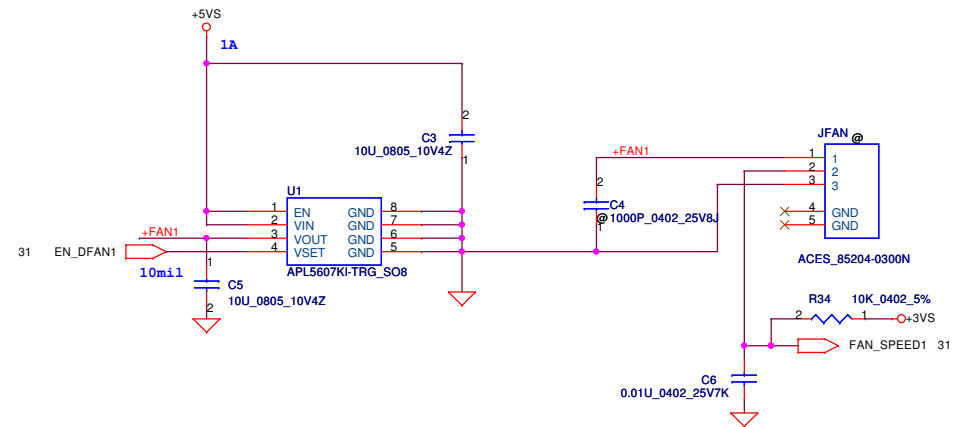
## For S3 CPU Power Saving



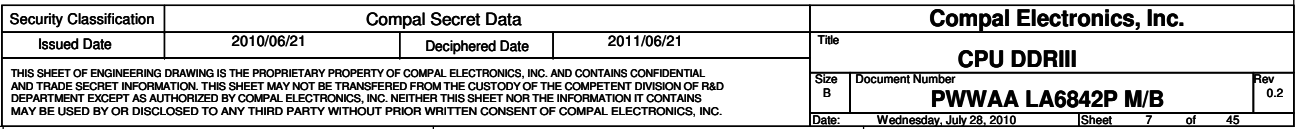
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						Size		Document Number		Rev	
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## FAN Control Circuit



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The diagram shows a 4-core system with a central component labeled 47P\_0402\_50V8J. The component is connected to a +GFX\_CORE supply and a ground symbol. The component is connected to four pads, each labeled 47P\_0402\_50V8J. The pads are connected to four capacitors: C97, C118, C119, and C93. The capacitors are connected to a common ground plane.

A schematic diagram showing a capacitor labeled "330U\_D2\_2VM\_R6M" with a value of "496" and a polarity symbol. The capacitor is connected between a red circle terminal labeled "+GFX\_CORE" (pin 1) and a red triangle terminal (pin 2).

```
0714 --> C271 mount,
        C496 unmount
```



AT21	VAXG1
AT19	VAXG2
AT18	VAXG3
AT16	VAXG4
AR21	VAXG5
AR19	VAXG6
AR16	VAXG7
AP21	VAXG8
AP19	VAXG9
AP18	VAXG1
AP16	VAXG1
AN21	VAXG1
AN19	VAXG1
AN18	VAXG1
AM21	VAXG1
AM19	VAXG1
AM16	VAXG1
AL21	VAXG2
AL19	VAXG2
AL18	VAXG2
AK21	VAXG2
AK19	VAXG2
AK18	VAXG2
AJ21	VAXG2
AJ19	VAXG3
AJ18	VAXG3
AJ16	VAXG3
AH21	VAXG3
AH19	VAXG3
AH18	VAXG3
AH16	VAXG3

100

PEG & DMI

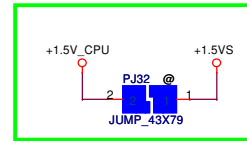
IC,AUB\_CFD\_rPGA,R0P9  
@

Diagram illustrating the connection of SENSE LINES and S VIDS signals:

- SENSE LINES** are connected to **VAXG\_SENSE** and **VSSAXG\_SENSE**.
- S VIDS** signals are connected to **GFX\_VID[0]** through **GFX\_VID[6]**.

POWER

DDR3 - 1.5V RAILS

1.1V

1.8V

VCCPLL  
VCCPLL  
VCCPLL

**Clarksfield: 0.6A**  
**Auburndale:1.35A**

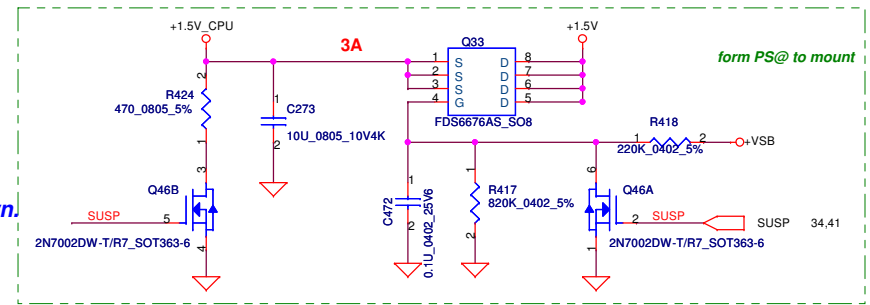


Diagram illustrating the connection of SENSE LINES and S VIDS signals:

- SENSE LINES** are connected to **VAXG\_SENSE** and **VSSAXG\_SENSE**.
- S VIDS** signals are connected to **GFX\_VID[0]** through **GFX\_VID[6]**.

GFXVR_VID_0	43
GFXVR_VID_1	43
GFXVR_VID_2	43
GFXVR_VID_3	43
GFXVR_VID_4	43
GFXVR_VID_5	43
GFXVR_VID_6	43

GFXVR\_EN 43  
T8 PAD  
GFXVR\_IMON 43

PJ31  
JUMP\_43X79

2 1

PJ31 need to open for S3 CPU Power Saving

PJ31 need to open for  
S3 CPU Power Saving

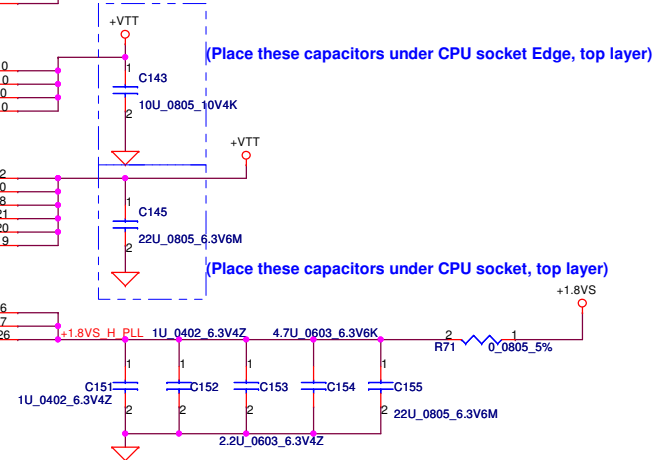


1.1V

1.8V

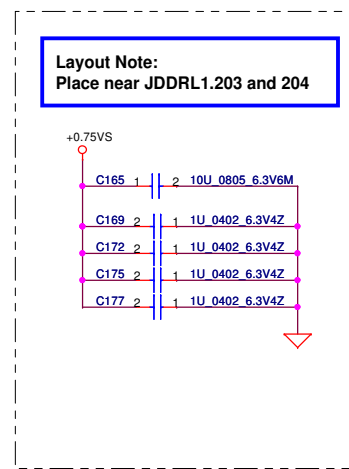
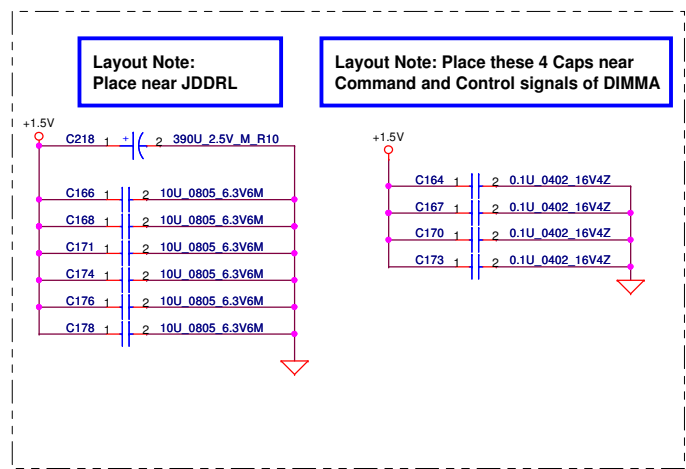
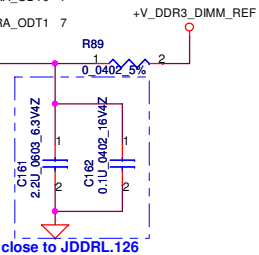
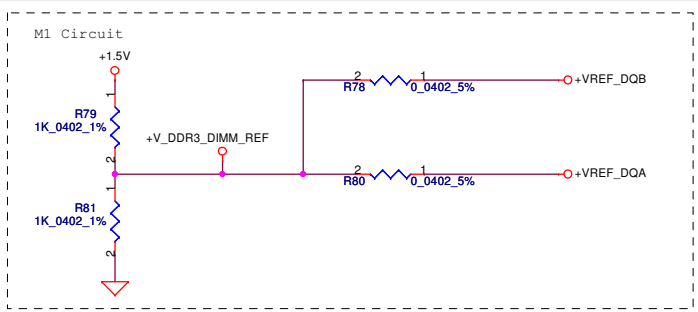
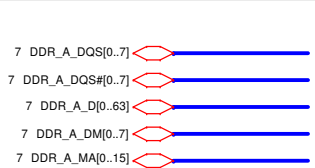
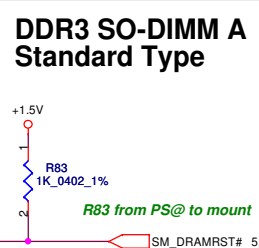
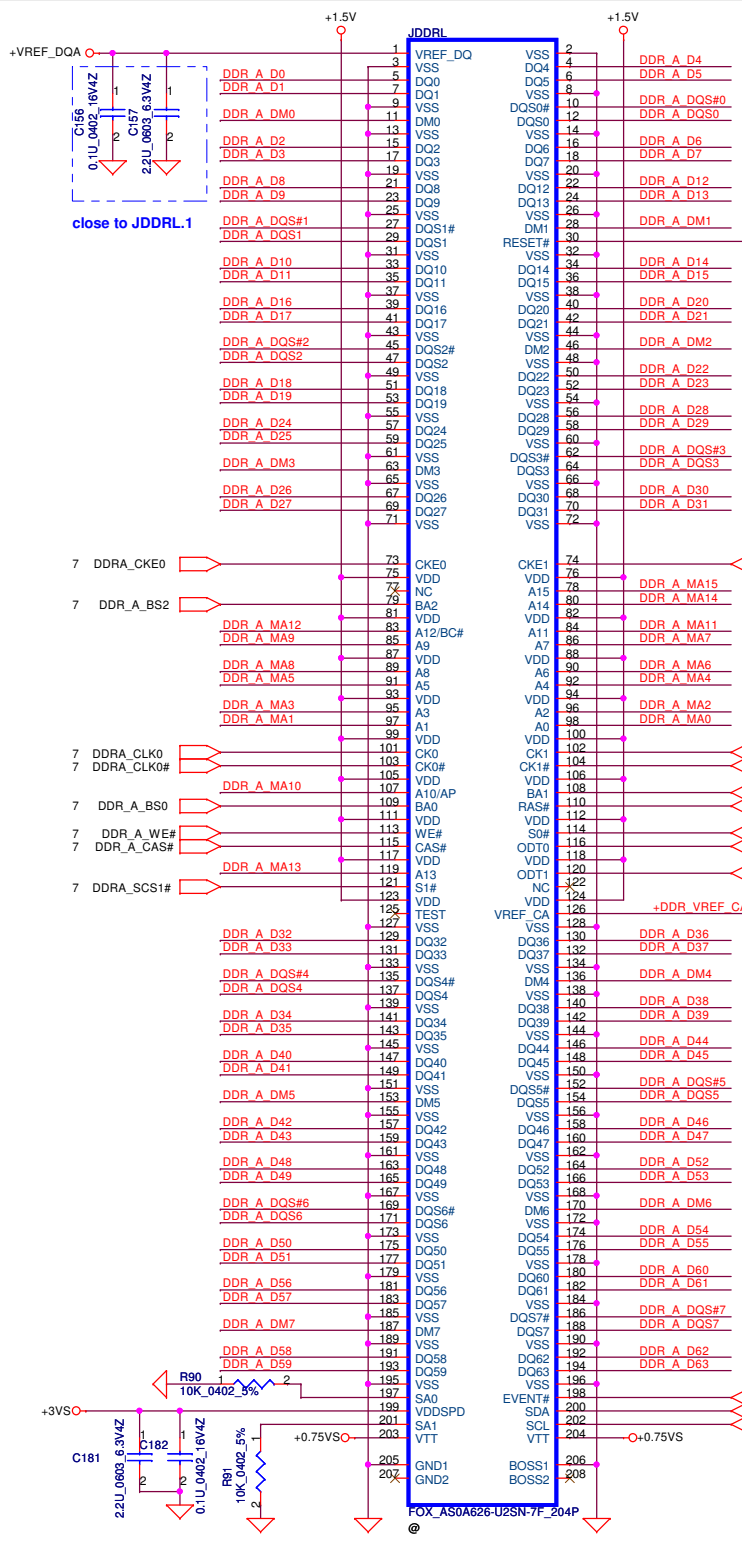
VCCPLL  
VCCPLL  
VCCPLL

Clarksfield: 0.6A  
Auburndale: 1.35A



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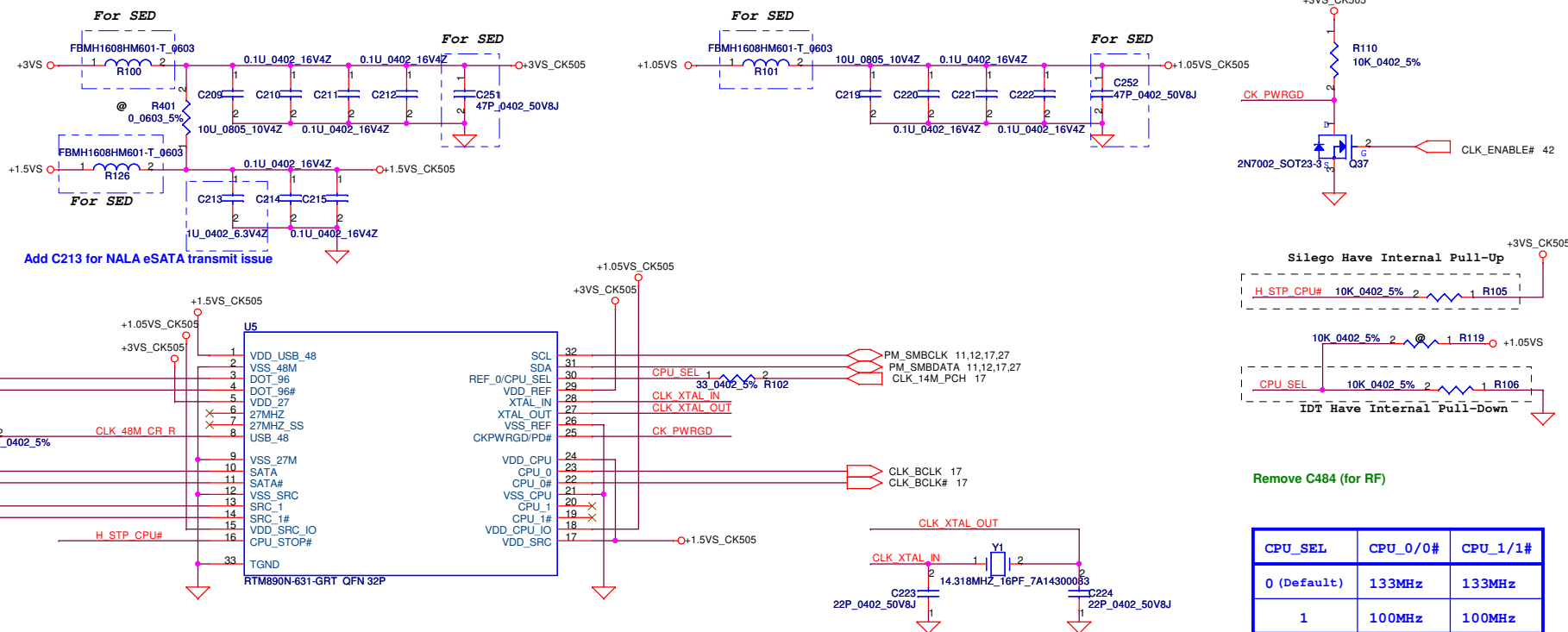
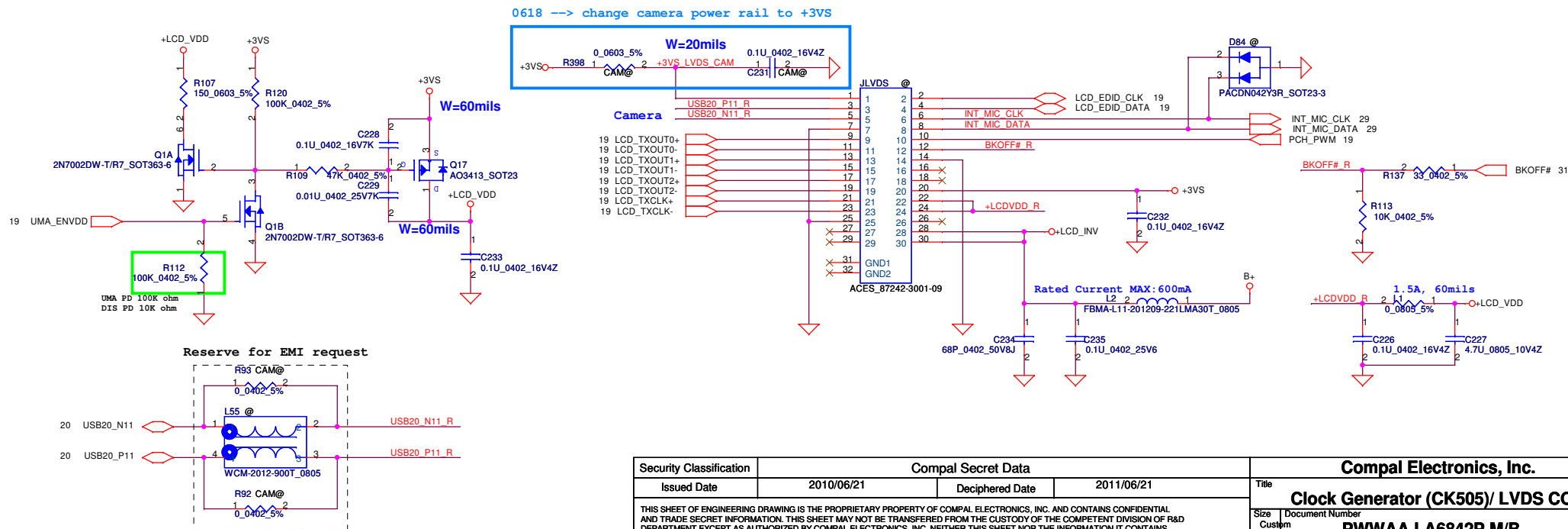




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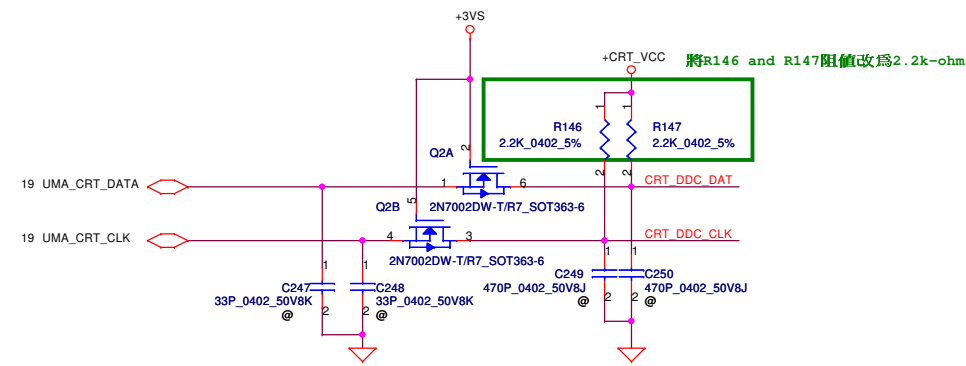
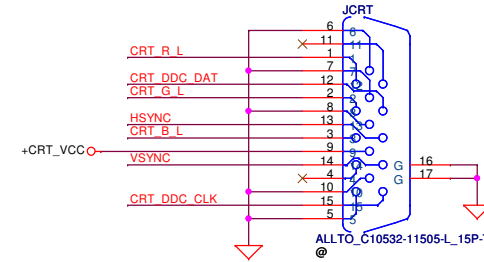
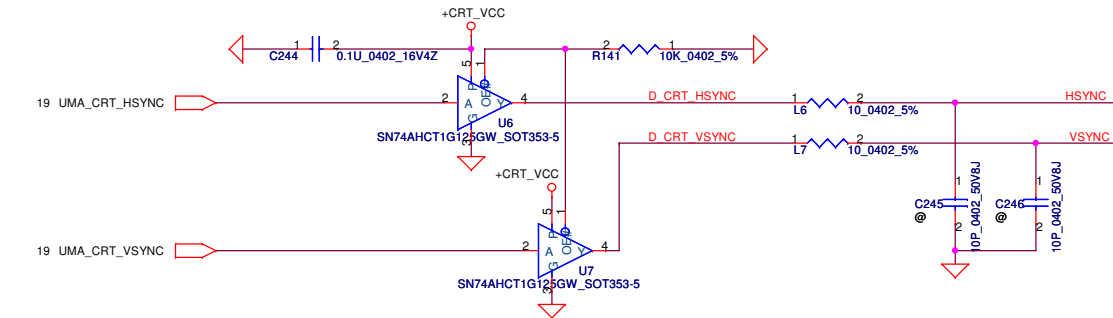
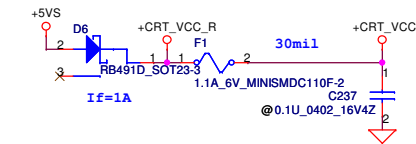
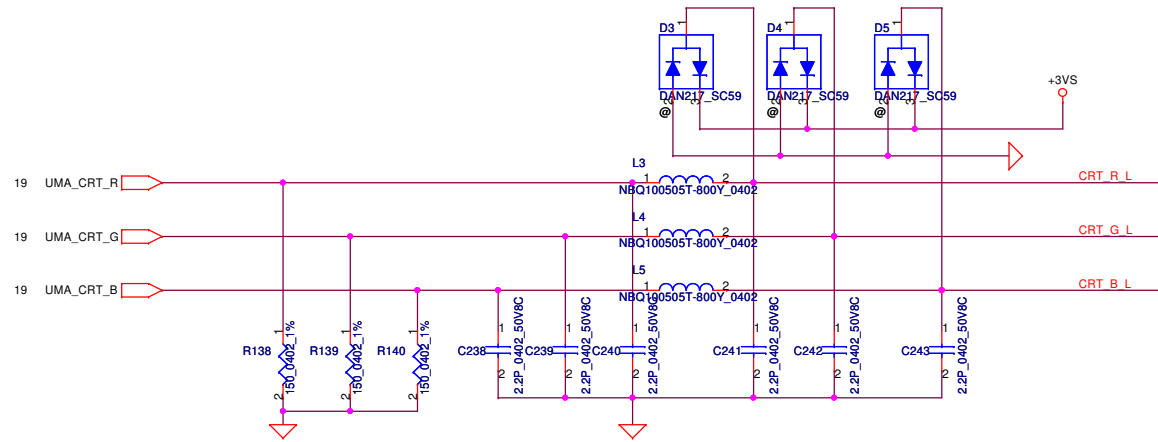


## Clock Generator

**LVDS / Int.Camera / Int.MIC Conn**

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# CRT CONNECTOR

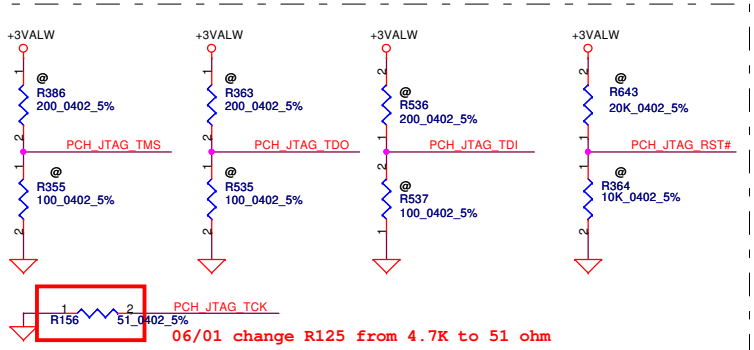
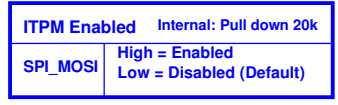
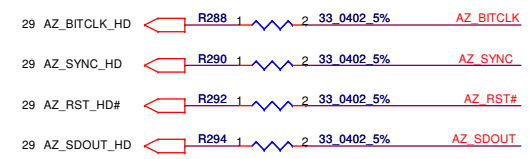
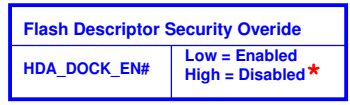
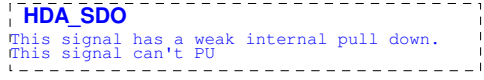
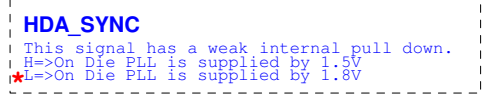
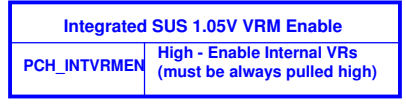
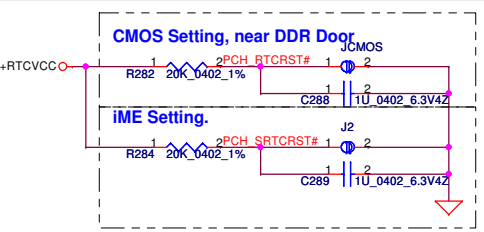


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0624 --> Remove BIOS ROM Debug Circuit

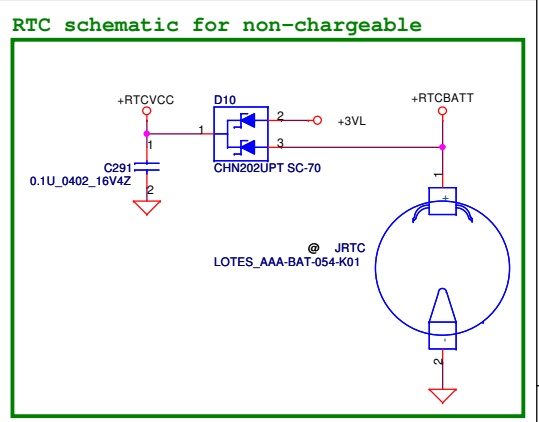
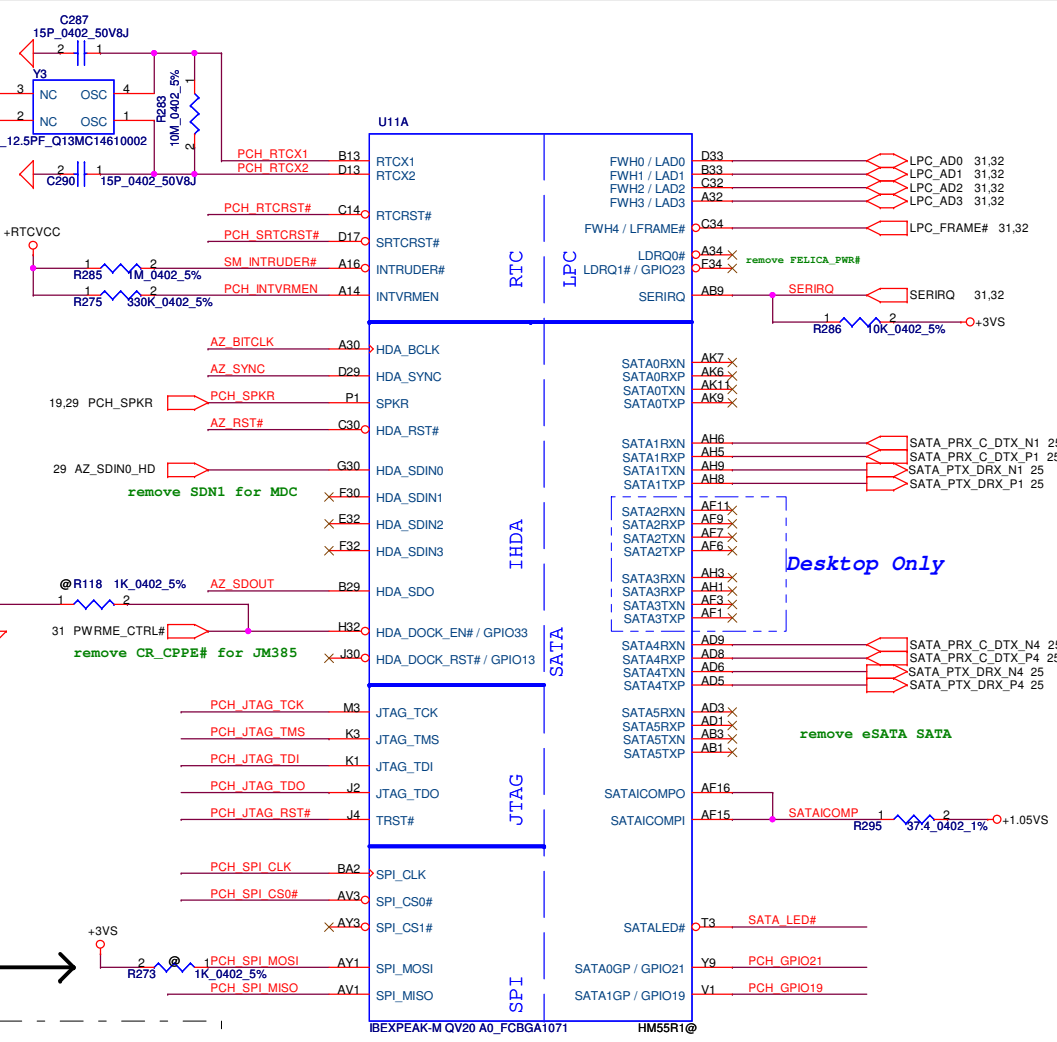
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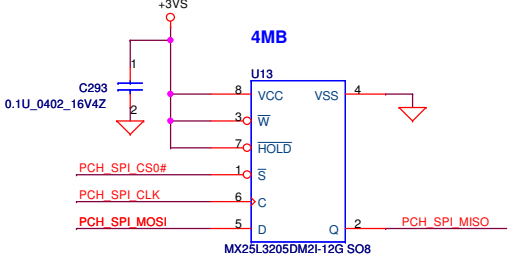
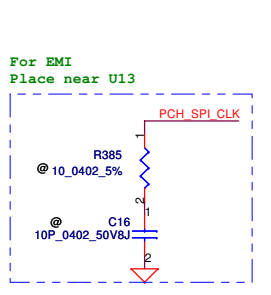
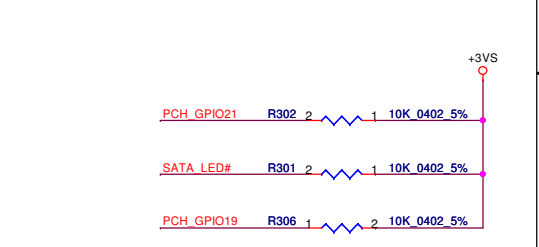


06/01 change R125 from 4.7K to 51 ohm

PCH_Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	No Install	No Install
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install



1ST HDD

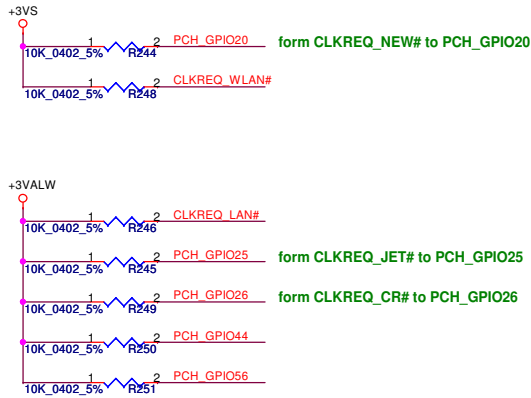




For LAN

For WLAN

LAN  
WLAN



remove NewCard PCIE

remove JET PCIE

remove CardReader PCIE

NC

U11B

PCI-E\*

Controller Link

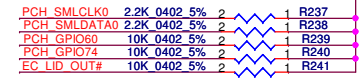
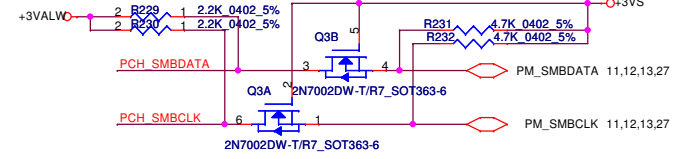
PEG

From CLK BUFFER

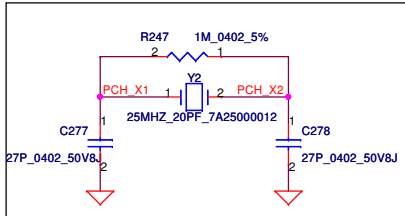
Clock Flex

PERN1  
PERP1  
PETN1  
PETP1  
PERN2  
PERP2  
PETN2  
PETP2  
PERN3  
PERP3  
PETN3  
PETP3  
PERN4  
PERP4  
PETN4  
PETP4  
PERN5  
PERP5  
PETN5  
PETP5  
PERN6  
PERP6  
PETN6  
PETP6  
PERN7  
PERP7  
PETN7  
PETP7  
PERN8  
PERP8  
PETN8  
PETP8  
AK48  
AK47  
PCIECLKRQ0# / GPIO73  
PCIECLKRQ1# / GPIO18  
PCIECLKRQ2# / GPIO20  
PCIECLKRQ3# / GPIO25  
PCIECLKRQ4# / GPIO26  
PCIECLKRQ5# / GPIO44  
CLKOUT\_PEG\_B\_N  
CLKOUT\_PEG\_B\_P  
PEG\_B\_CLKRQ# / GPIO56  
BEXPEAK-M QV20 A0\_FCBGA1071

SMBALERT# / GPIO11  
SMBCLK  
SMBDATA  
SML0ALERT# / GPIO60  
SML0CLK  
SML0DATA  
SML1ALERT# / GPIO74  
SML1CLK / GPIO58  
SML1DATA / GPIO75  
CL\_CLK1  
CL\_DATA1  
CL\_RST1#  
PEG\_A\_CLKRQ# / GPIO47  
CLKOUT\_PEG\_A\_N  
CLKOUT\_PEG\_A\_P  
CLKOUT\_DMI\_N  
CLKOUT\_DMI\_P  
CLKOUT\_DP\_N / CLKOUT\_BCLK1\_N  
CLKOUT\_DP\_P / CLKOUT\_BCLK1\_P  
CLKIN\_DMI\_N  
CLKIN\_DMI\_P  
CLKIN\_BCLK\_N  
CLKIN\_BCLK\_P  
CLKIN\_DOT\_96N  
CLKIN\_DOT\_96P  
CLKIN\_SATA\_N / CKSSCD\_N  
CLKIN\_SATA\_P / CKSSCD\_P  
REFCLK14IN  
CLKIN\_PCIELOOPBACK  
XTAL25\_IN  
XTAL25\_OUT  
XCLK\_RCOMP  
CLKOUTFLEX0 / GPIO64  
CLKOUTFLEX1 / GPIO65  
CLKOUTFLEX2 / GPIO66  
CLKOUTFLEX3 / GPIO67  
HM55R1@

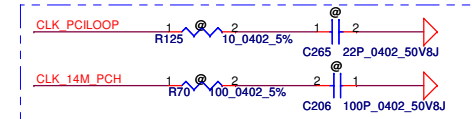


FROM CLK GEN FOR: 133/100/96/14.318 MHZ

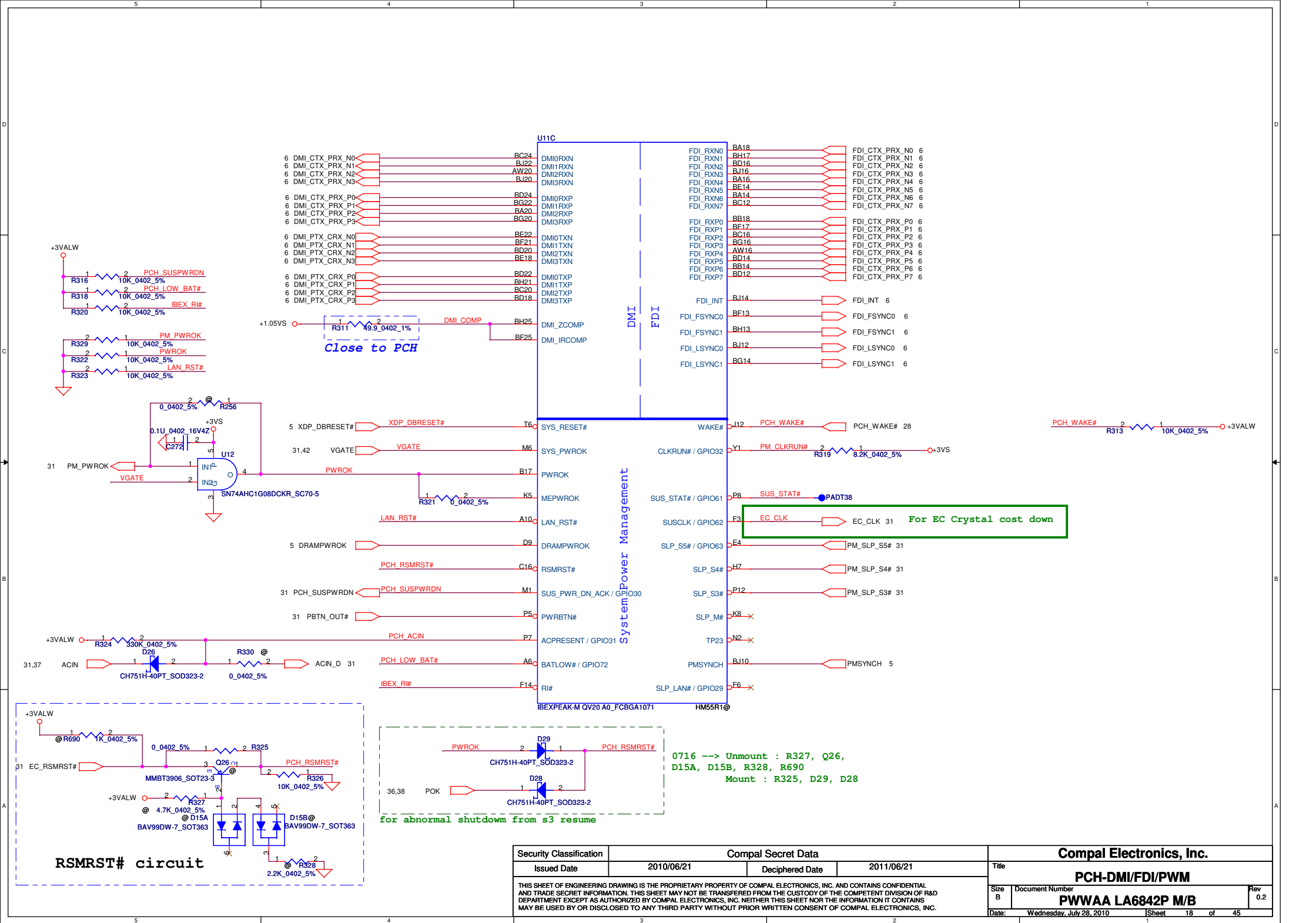


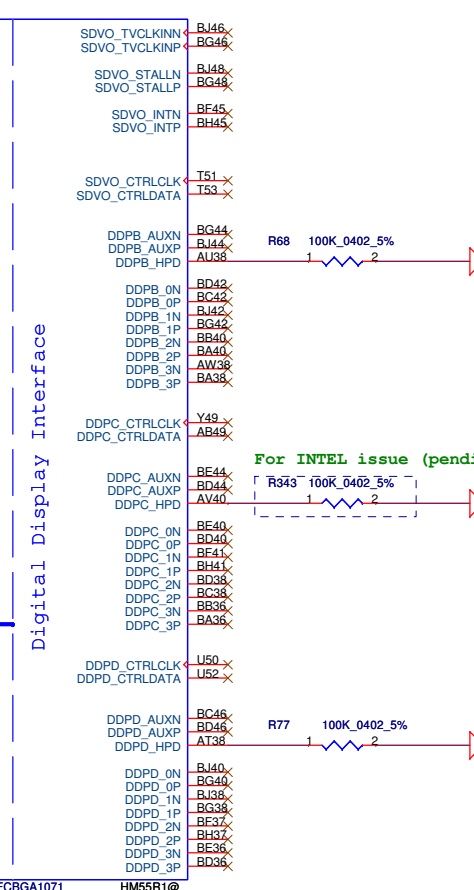
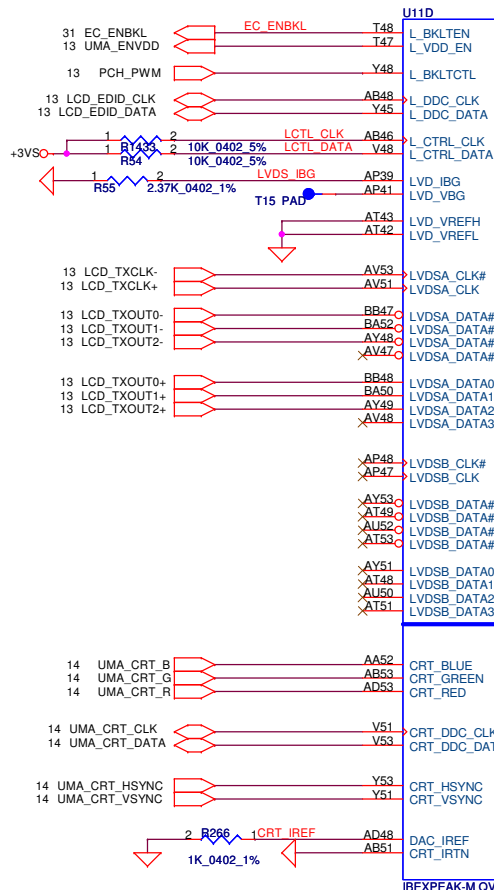
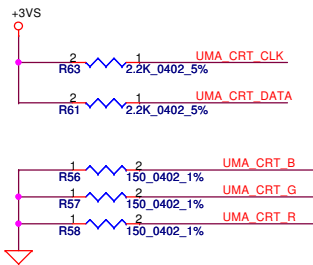
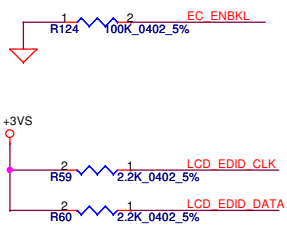
Note: Stuff 0 ohm if 25MHz crystal un-stuff

for EMI request



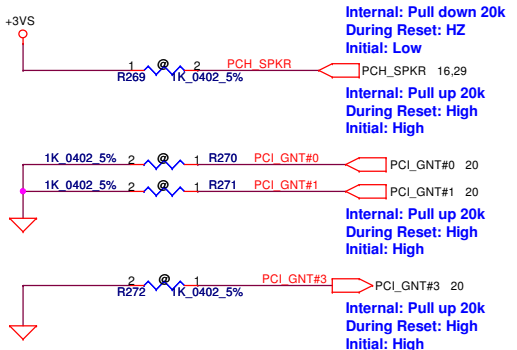
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				Date	Wednesday, July 28, 2010
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For INTEL issue (pending interrupts from the PCH for unused HDMI ports)

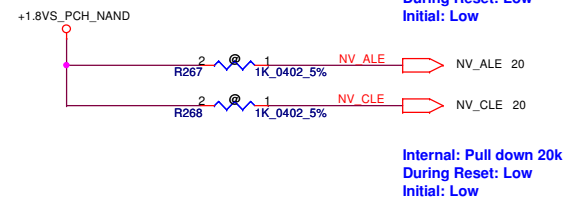
# PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

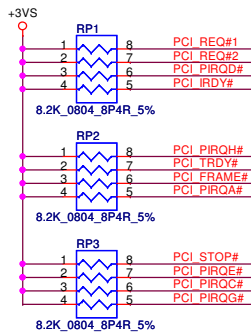
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



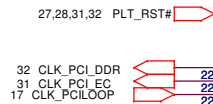
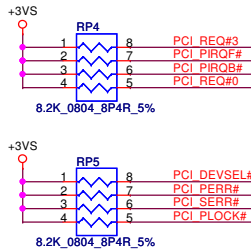
Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

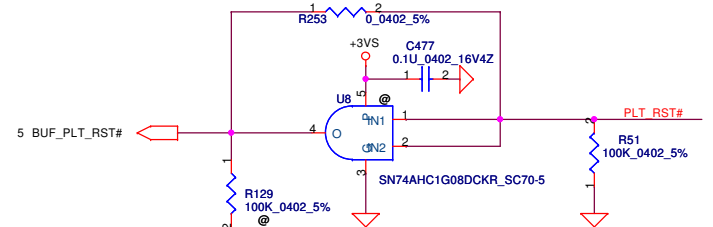
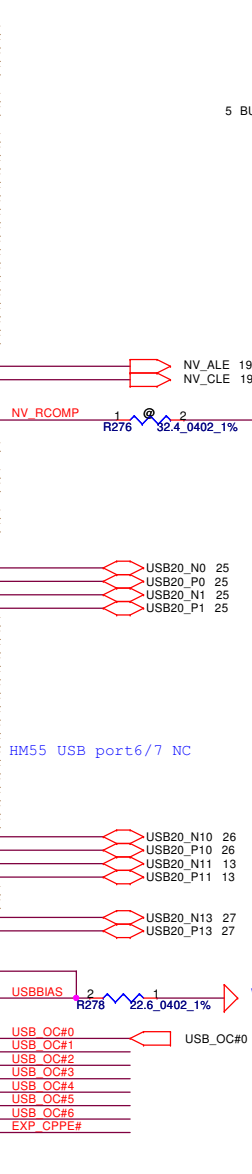
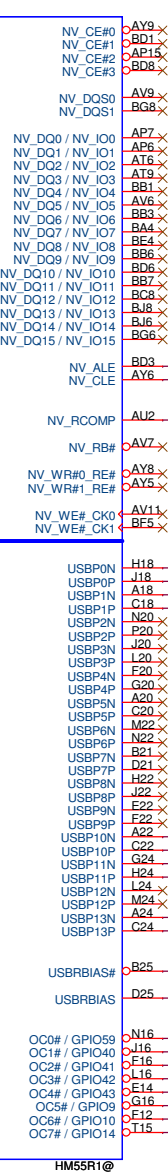
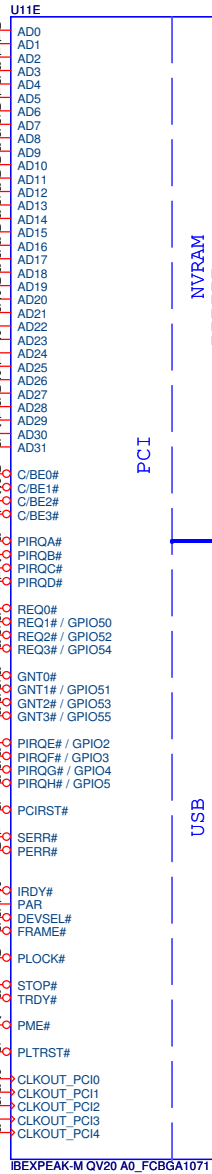
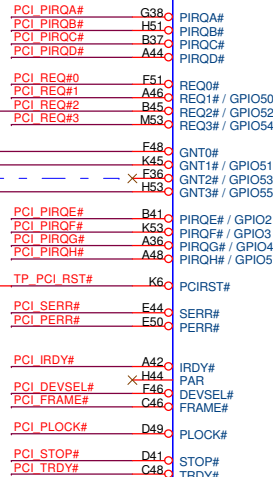


add PCI\_REQ#2 for non-ODD\_EN#

GNT2#: Not pull low, internal pull up 20K



T37 PAD



USB-LIGHT1  
USB-LIGHT2

USB-Left1

remove eSATA

remove NewCard

remove BT

remove FingerPr

remove FELICA

Card reader(2 in 1)

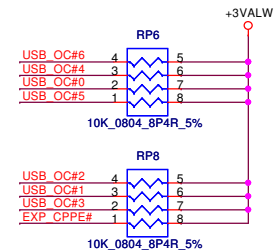
Int. Camera

remove 3G/TV#1

WiMax(WLAN)

Within 500 mils

(USB-Right)



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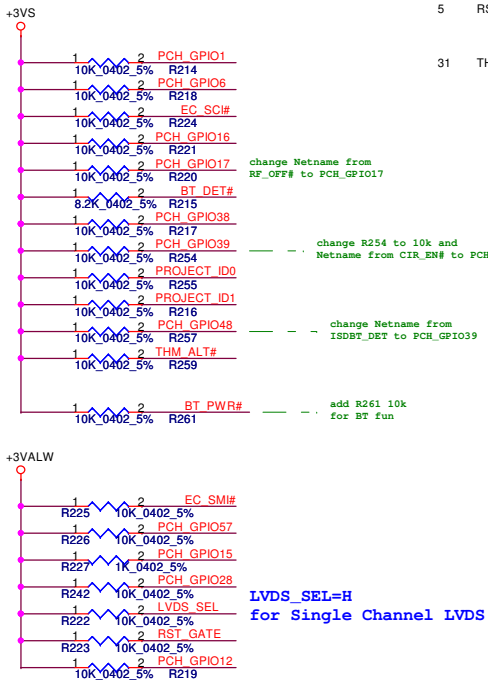
GPIO8  
Not pull down  
Internal: Pull up 20k  
During Reset: High  
Initial: High

GPIO15  
a Strong pull up may be needed  
for GPIO Functionality  
Internal: Pull down 20k  
During Reset: Low  
Initial: Low

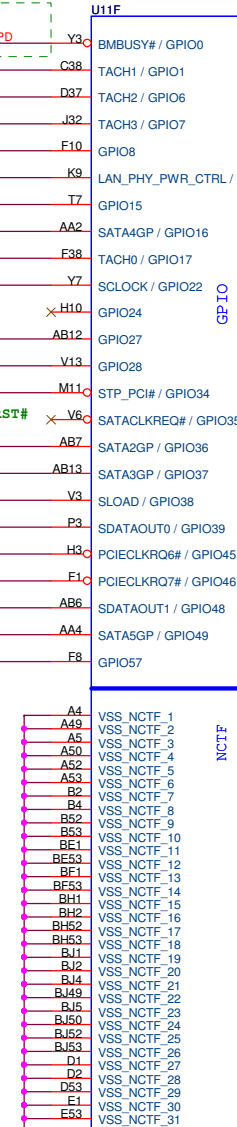
#### On-Die PLL VR

PCH\_GPIO27 High = Enabled (Default)  
Low = Disabled

PROJECT_ID		
Name	ID0	ID1
NBQAA 11.6/13.3"	L	L
NBQAA 14"	L	H
*NBQAA 16"	H	L
NALAA 17.3"	H	H

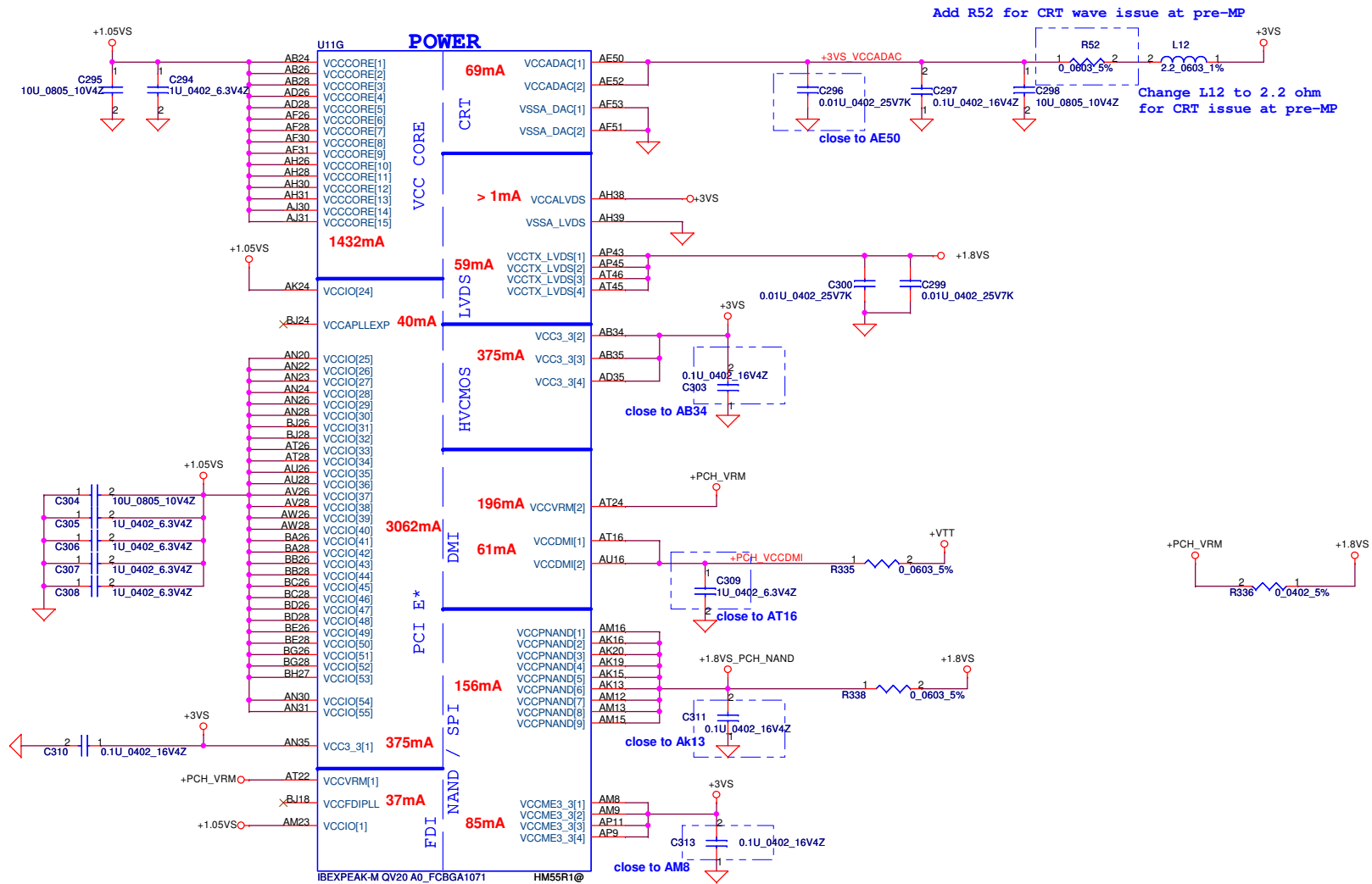


LVDS\_SEL=H  
for Single Channel LVDS



Not pull low  
internal pull up  
Internal: Pull up 20k  
During Reset: High  
Initial: High

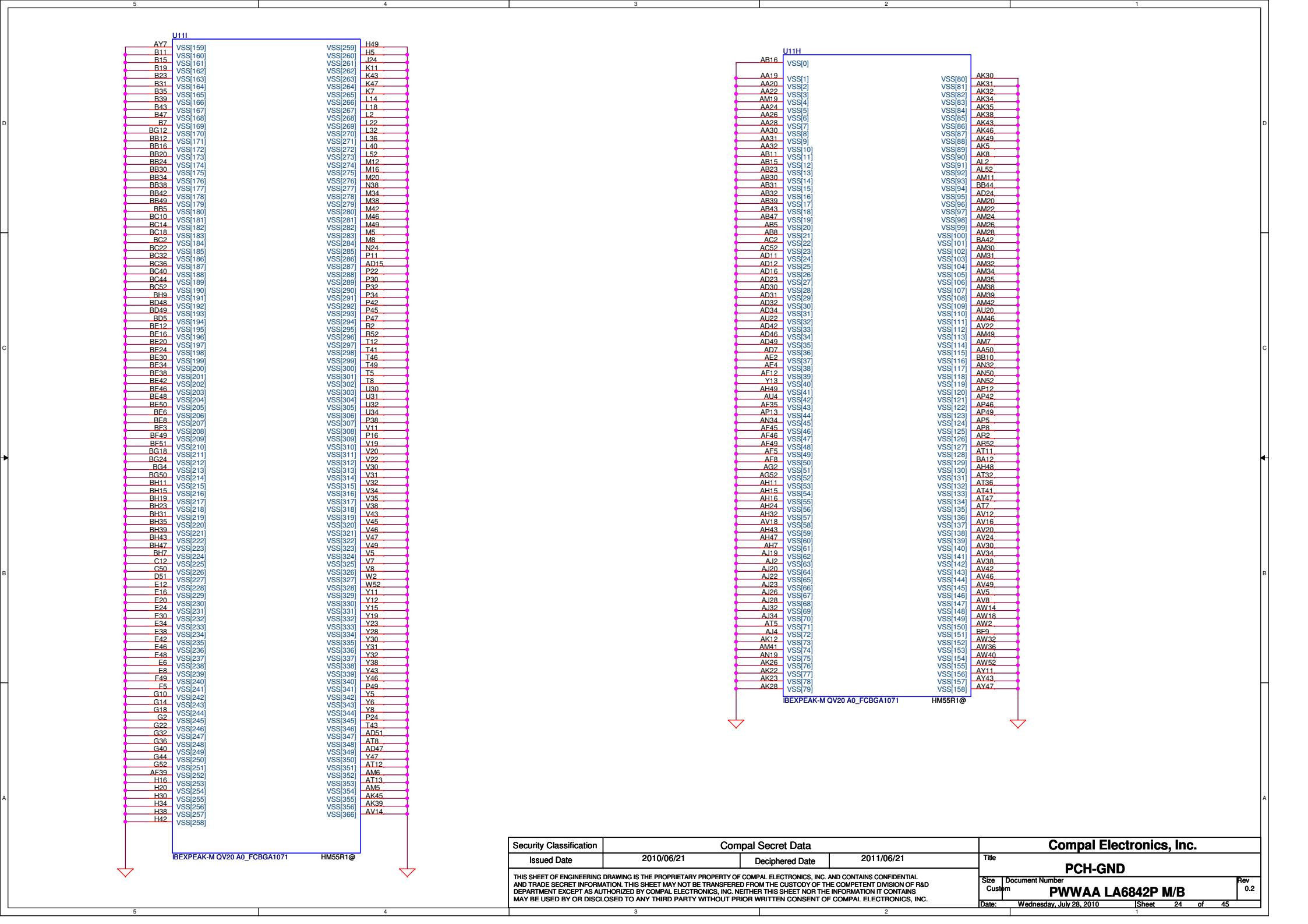
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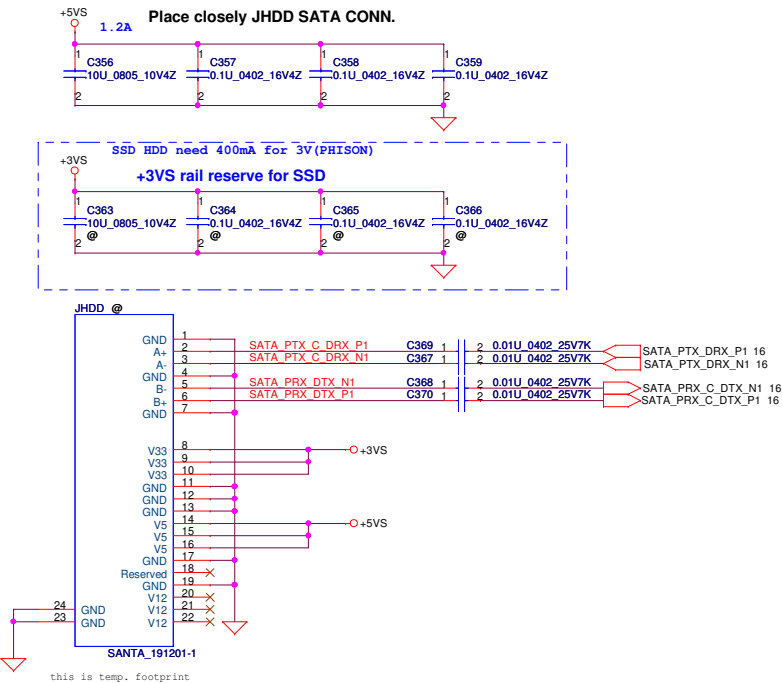




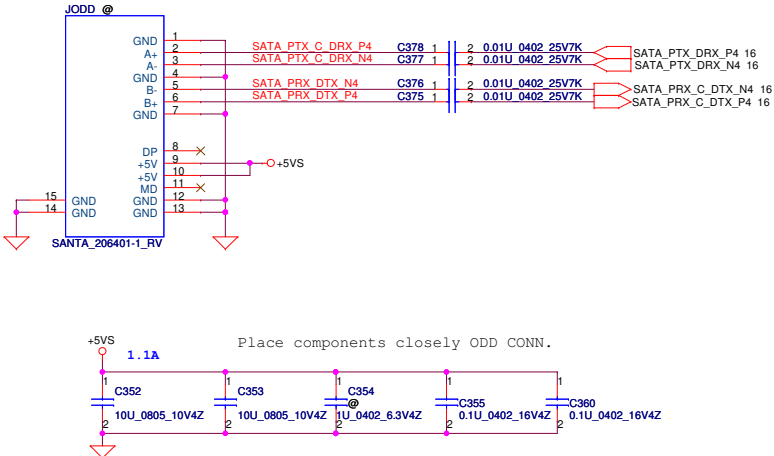
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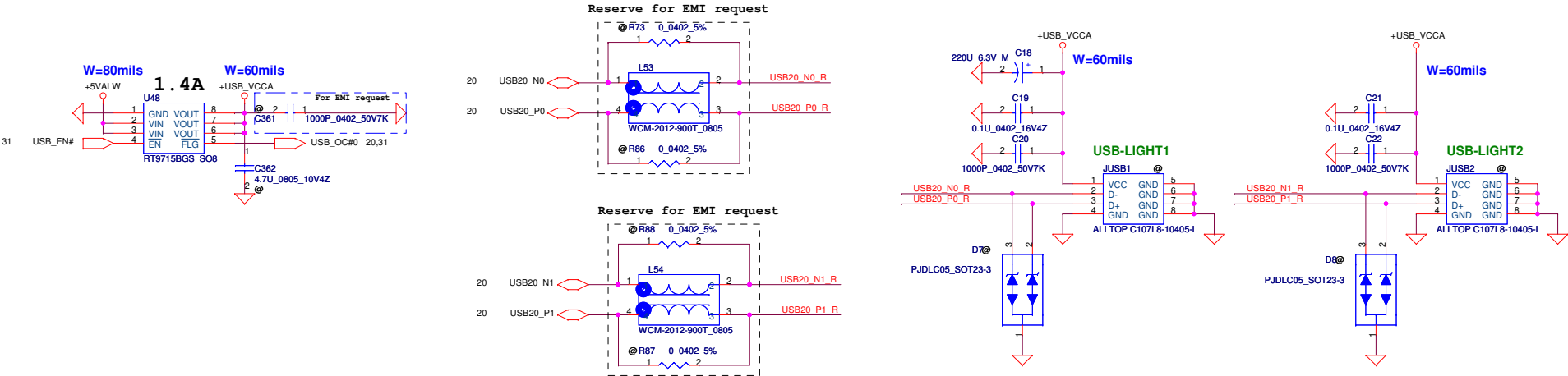
SATA HDD Conn.



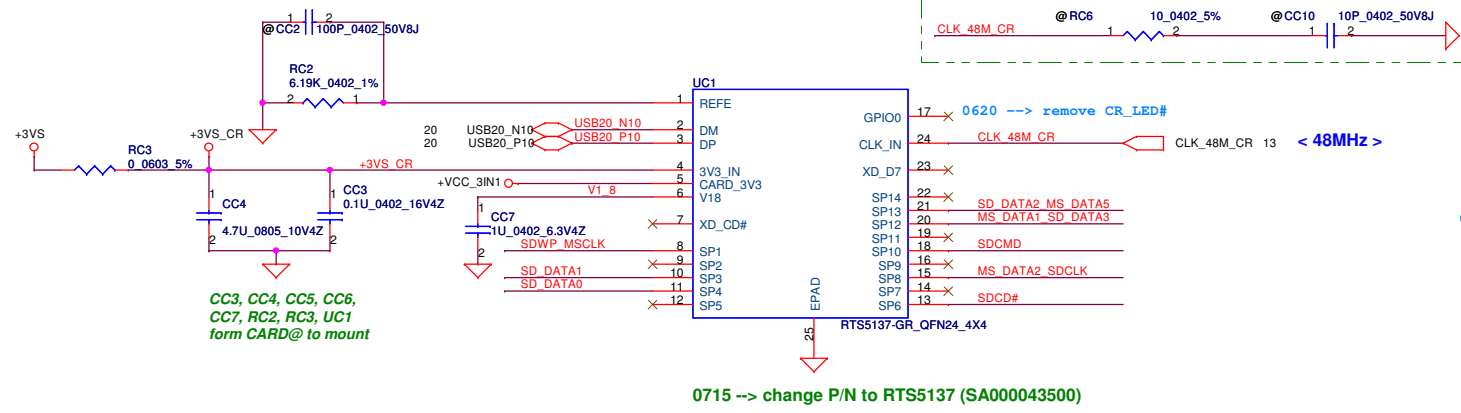
SATA ODD Conn



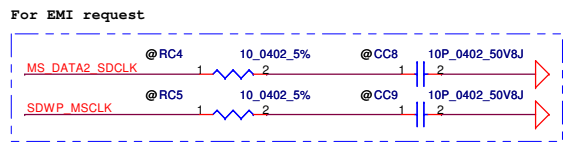
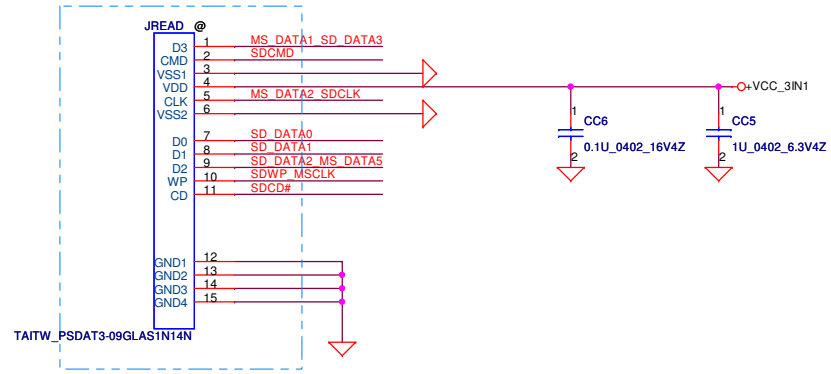
USB Conn. (2 Port)



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< 2 in 1 Card Reader >  
0624 --> change CARDREADER conn.



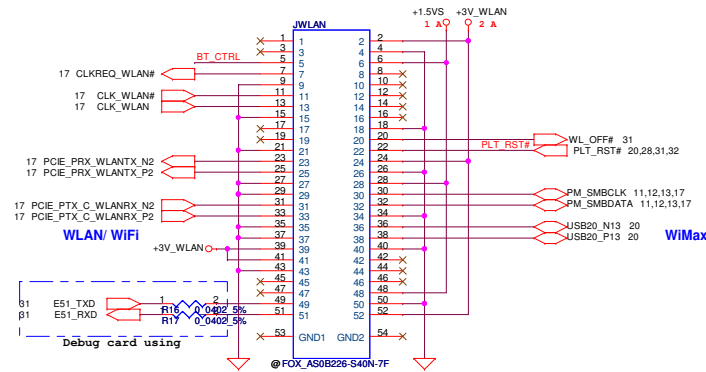
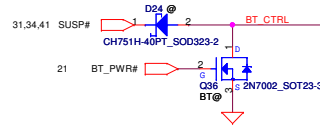
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# PCle Mini Card-WLAN/WiMax

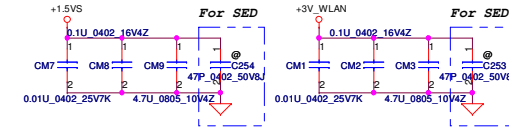
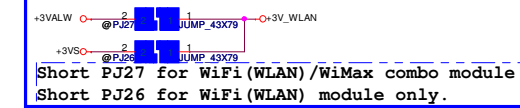
## WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

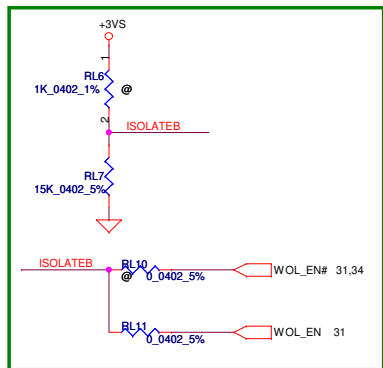
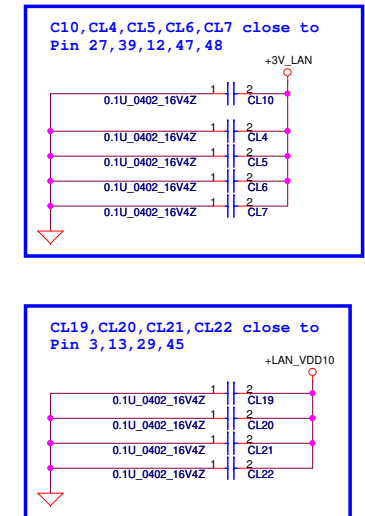
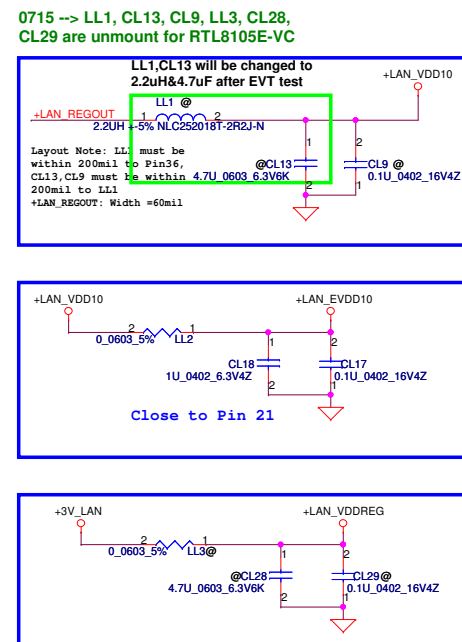
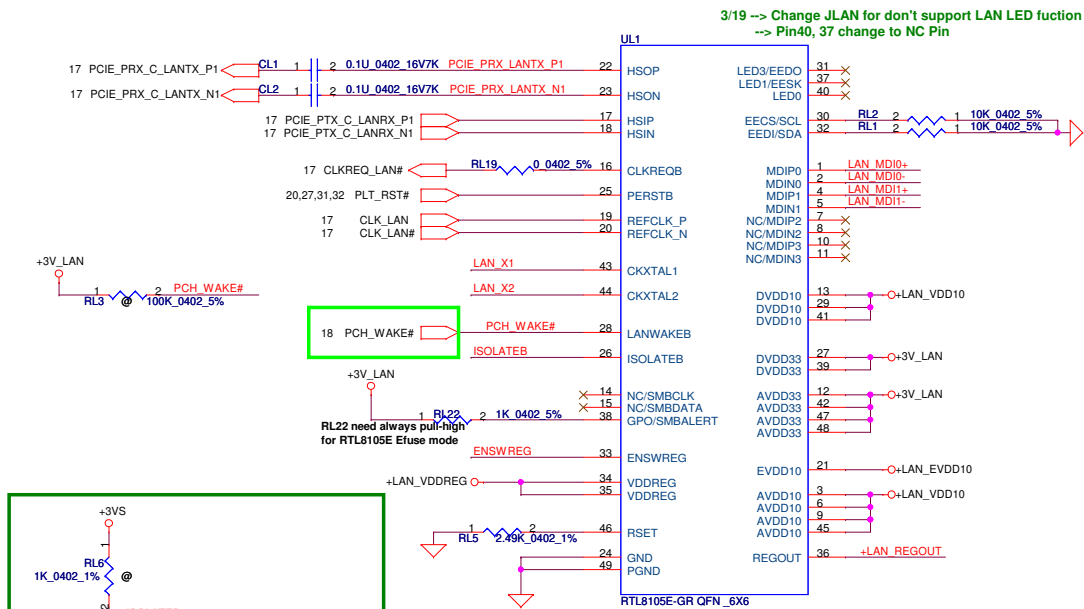
\*\*If +3V\_WLAN is +3VS, please remove D24.



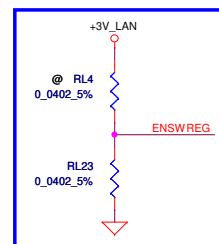
## Slot#1 Half PCIe Mini Card-WLAN/WiMax



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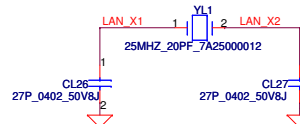


Add RL10 for +3V\_LAN power enable signal  
Add RL11 for wake on LAN function enable signal

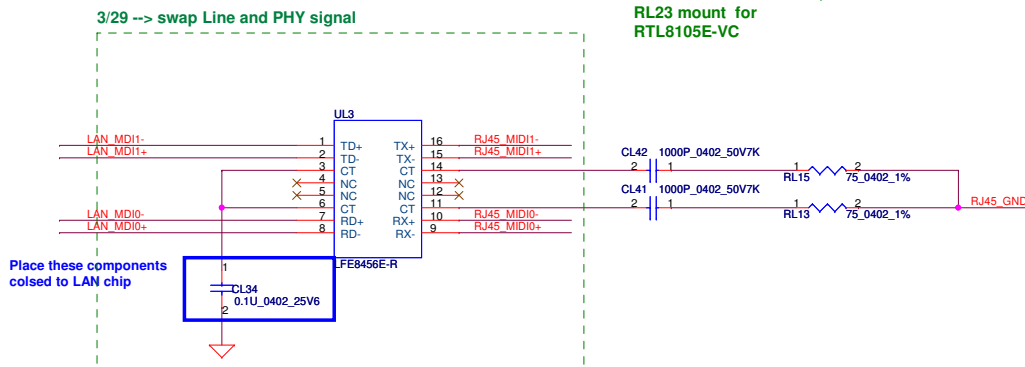
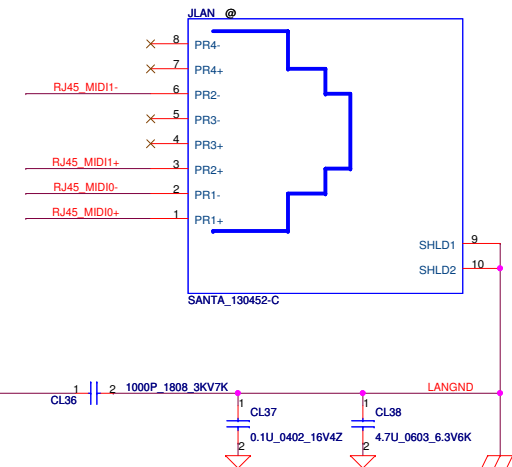


0715 --> RL4 is unmount,  
RL23 mount for  
RTL8105E-VC

4/2-->remove RL8, RL9, CL11

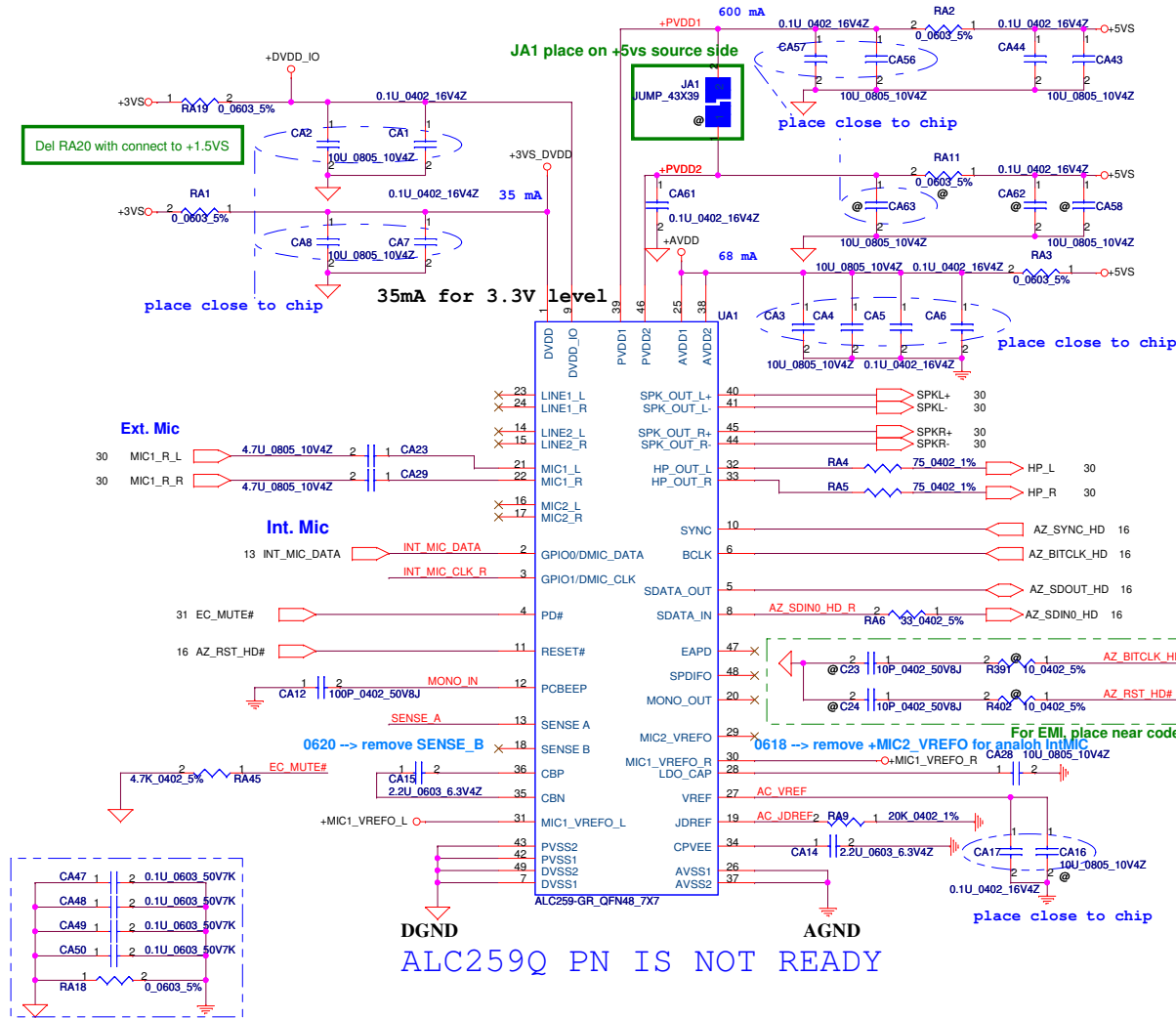


## LAN Conn.



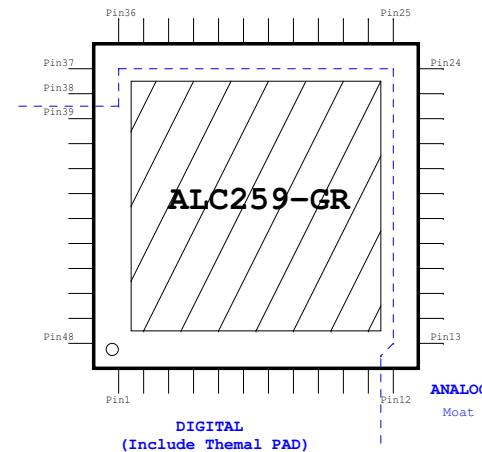
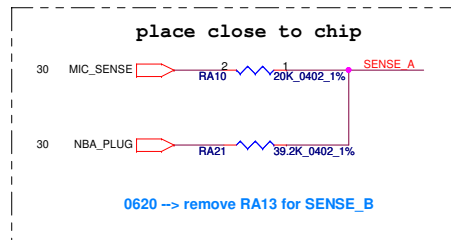
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# Codec

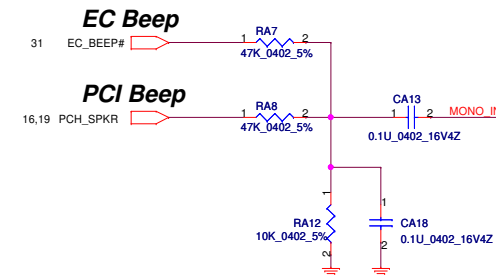


ALC259Q PN IS NOT READY

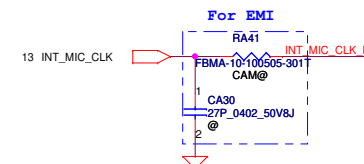
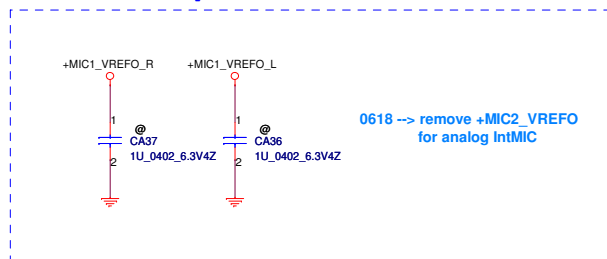
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	



## Beep sound

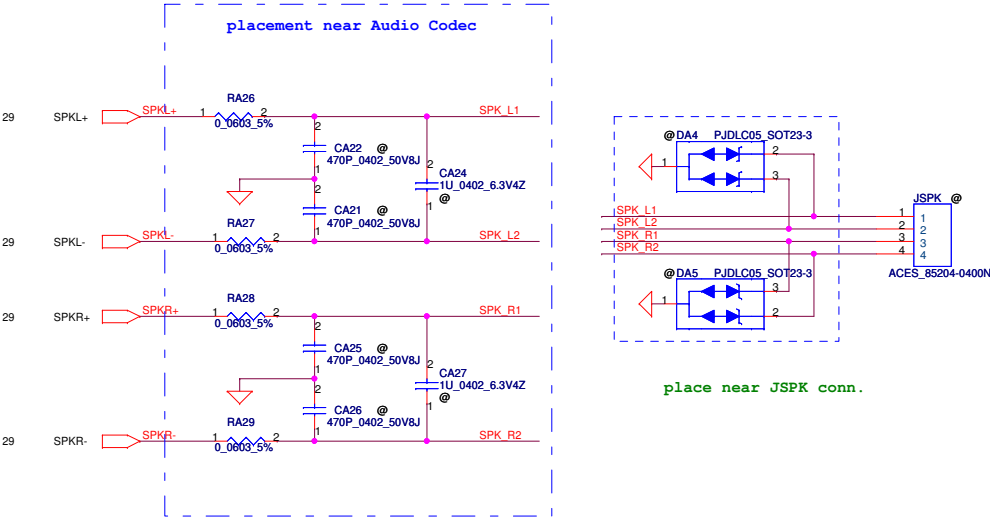


Place close to chip

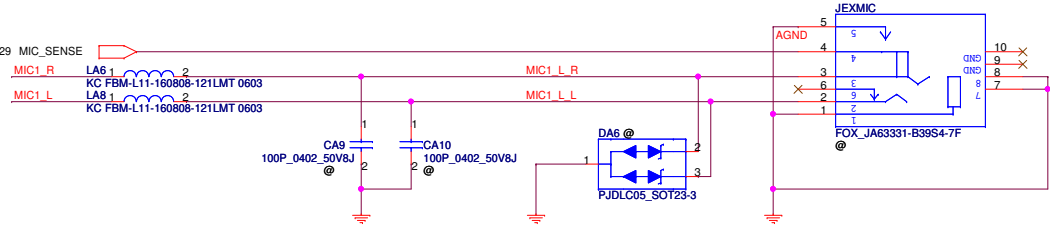


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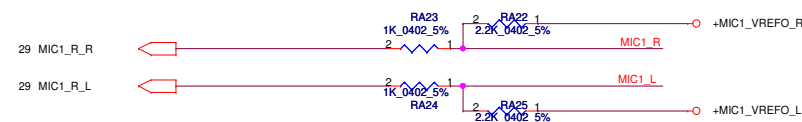
Speaker Connector



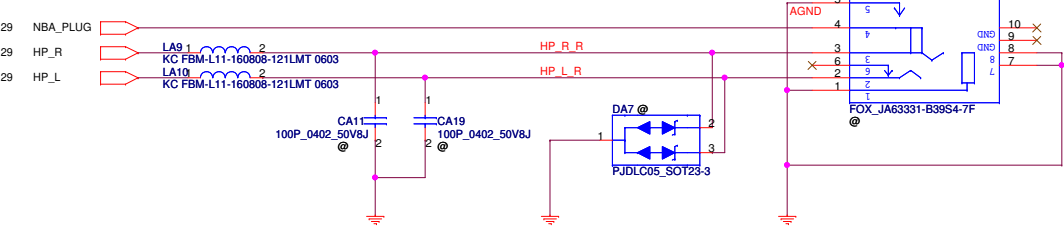
Ex.MIC JACK



Ext.MIC/LINE IN



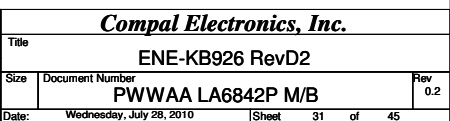
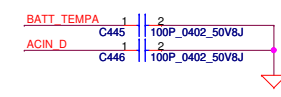
Head Phone JACK



Int. Mic

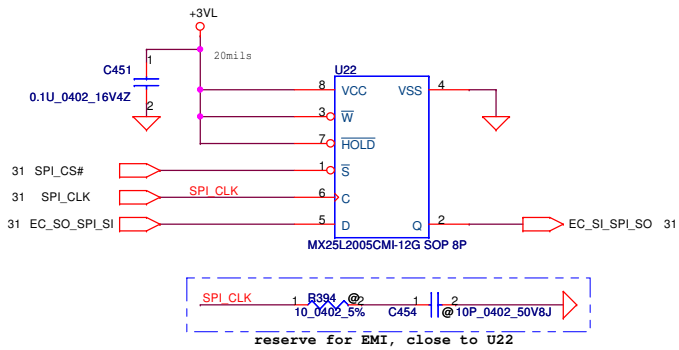
0618 --> remove Analog IntMIC, and change to DIGITAL MIC

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				Date	Wednesday, July 28, 2010
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				Rev	0.2

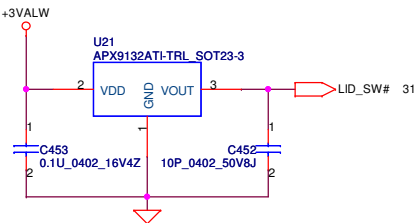


EC SEL	EC Version
High	KB926D3
Low	KB926E0

SPI Flash (256KB)

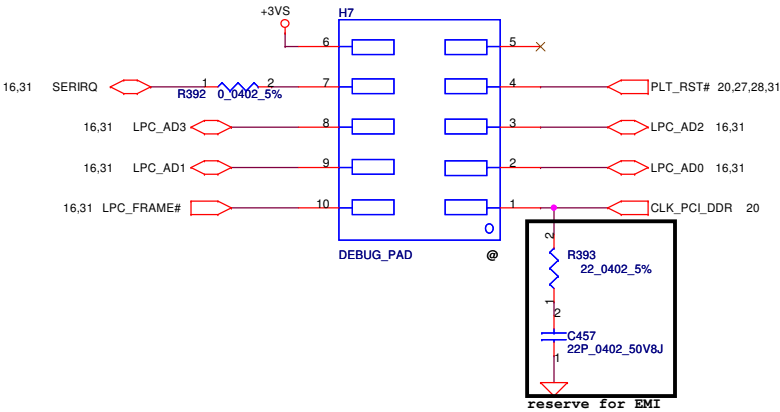


Lid SW



LPC Debug Port

Please place the PAD under DDR DIMM.



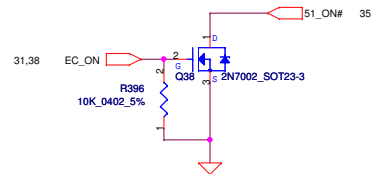
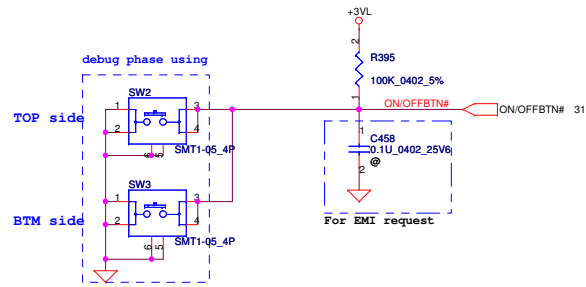
KEYBOARD CONN.



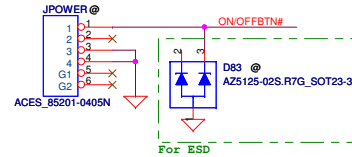
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Issued Date		Deciphered Date		Title	
2010/06/21		2011/06/21		SPI ROM/TP/KB/Debug	
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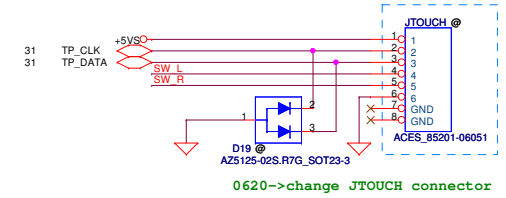
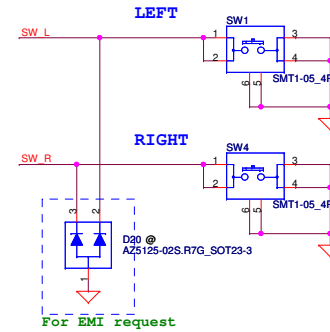
## Power Button



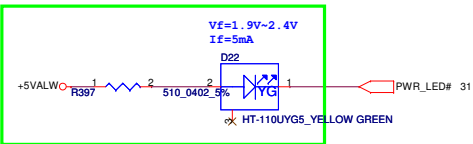
## PWR/B to MB Conn.



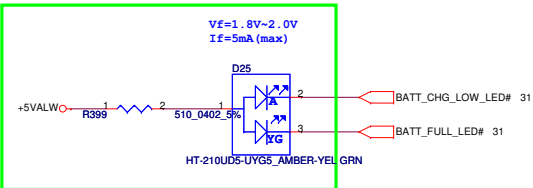
## TP Button/Conn.



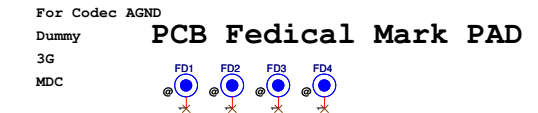
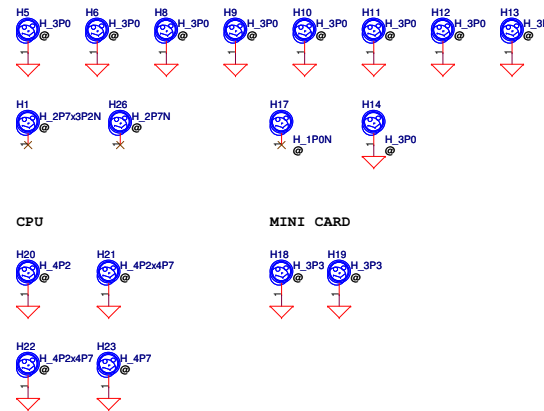
## POWER/SUSPEND LED



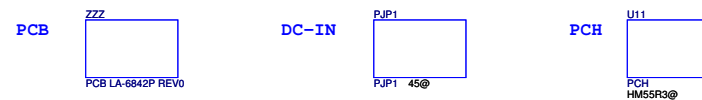
## BATT CHARGE/FULL LED



## Screw Hole



## ISPD



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				Rev	0.2

[illegible]

0715 ---> Q31 change to SB548000310 the same as +5VS

[illegible]

5.39 VTTPWROK

R169 100K\_0402\_5%

Q48A 2N7002DW-T/R/SOT363-6

SUSP

Q48B 2N7002DW-T/R/SOT363-6

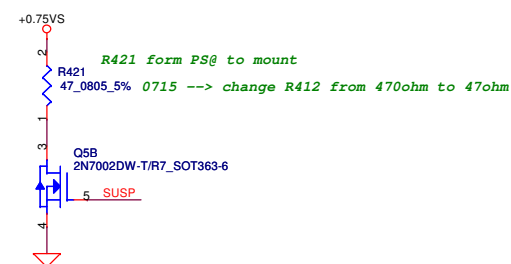
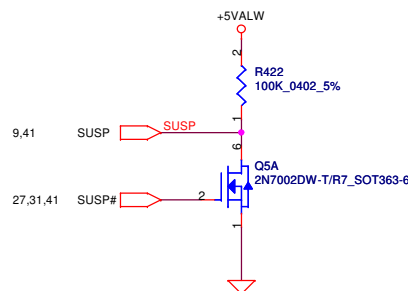
0.75VR\_EN

+3VALW

R425 100K\_0402\_5%

0.75VR\_EN# 41

Q48A,B  
R169, R425 form PS@ to mount

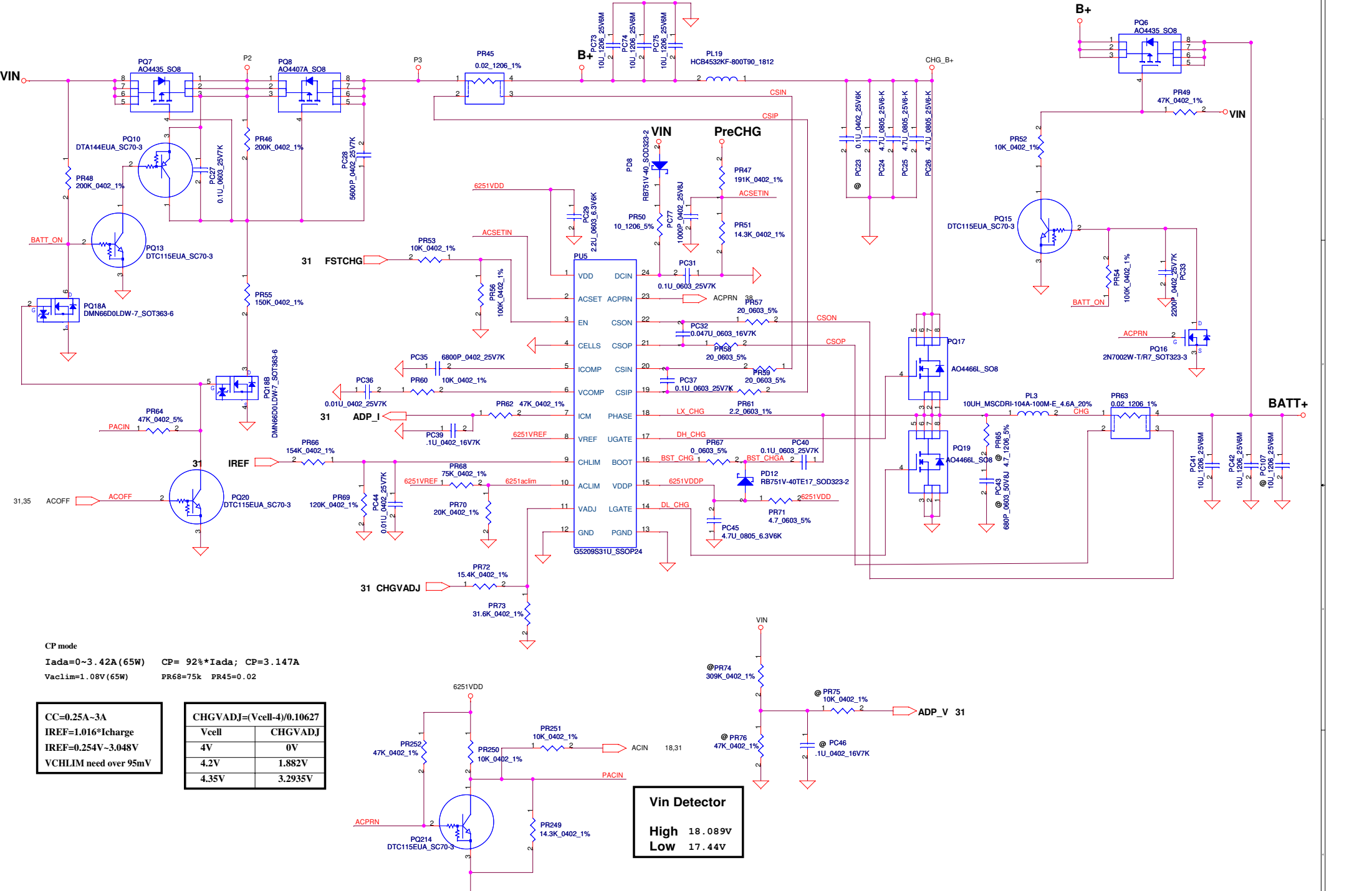


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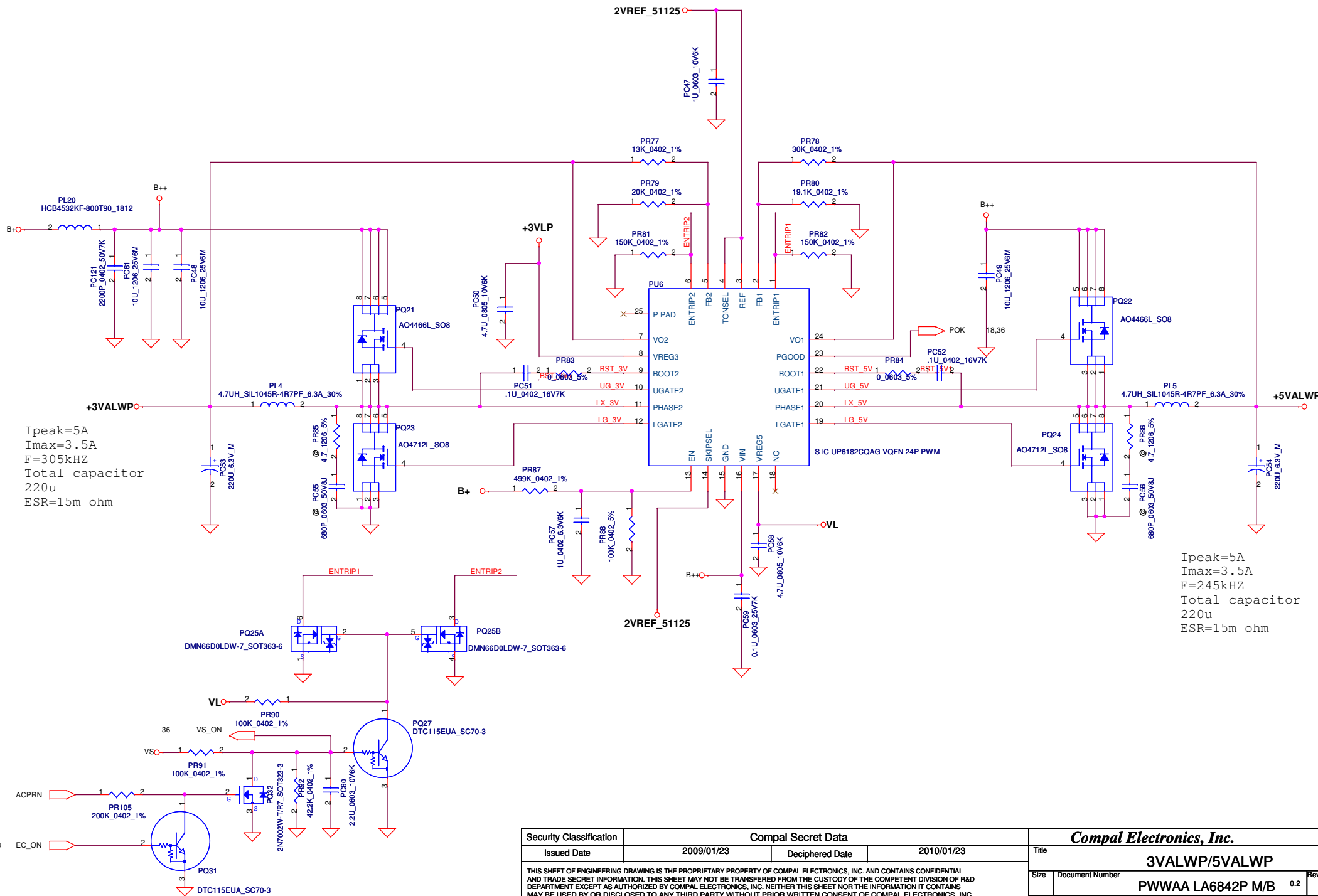


CP mode  
I<sub>ada</sub>=0~3.42A (65W) CP= 92%\*I<sub>ada</sub>; CP=3.147A  
V<sub>acLim</sub>=1.08V (65W) PR68=75k PR45=0.02

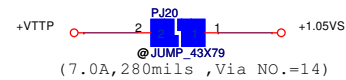
CC=0.25A~3A  
I<sub>REF</sub>=1.016\*I<sub>charge</sub>  
I<sub>REF</sub>=0.254V~3.048V  
V<sub>CHLIM</sub> need over 95mV

CHGVADJ=(V <sub>cell</sub> -4)/0.10627	
V <sub>cell</sub>	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

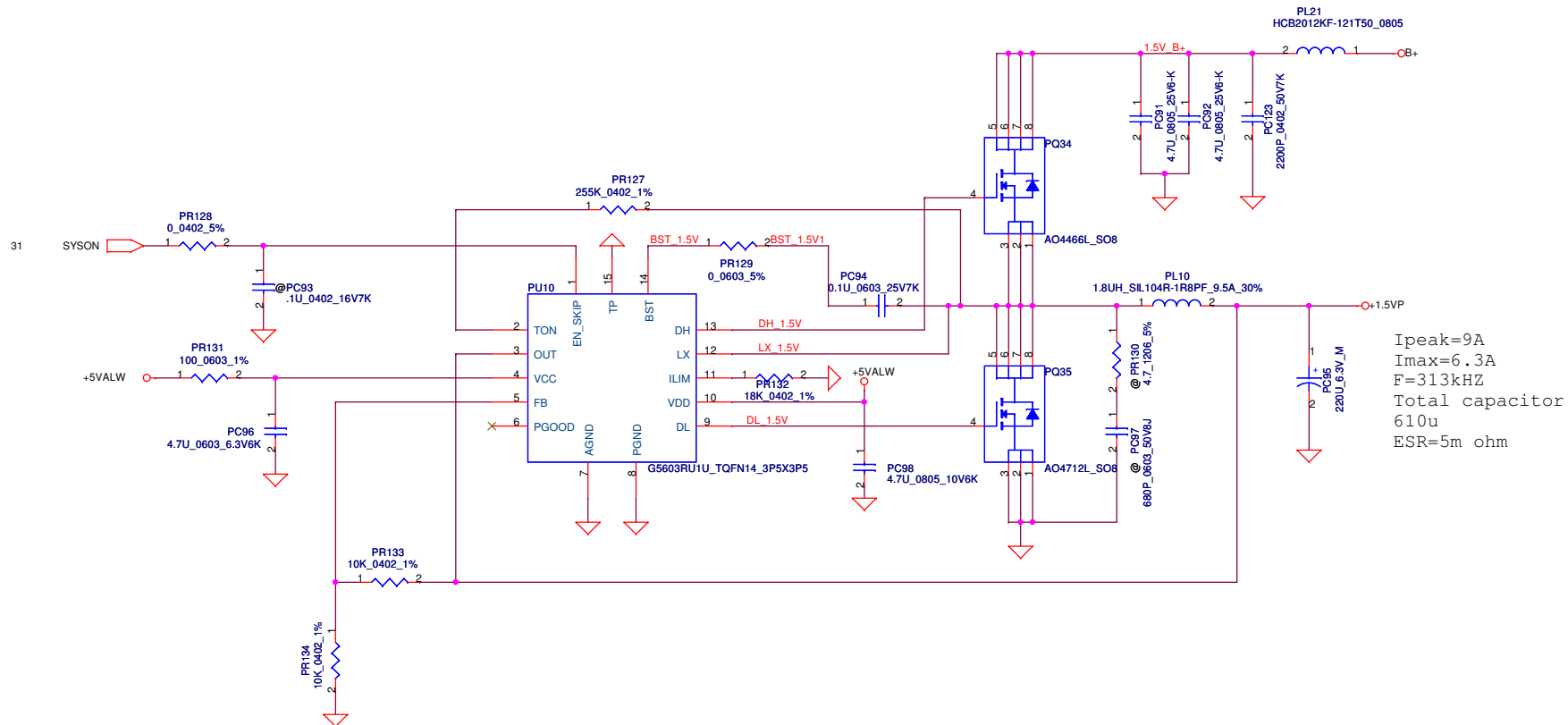
**Vin Detector**  
High 18.089V  
Low 17.44V



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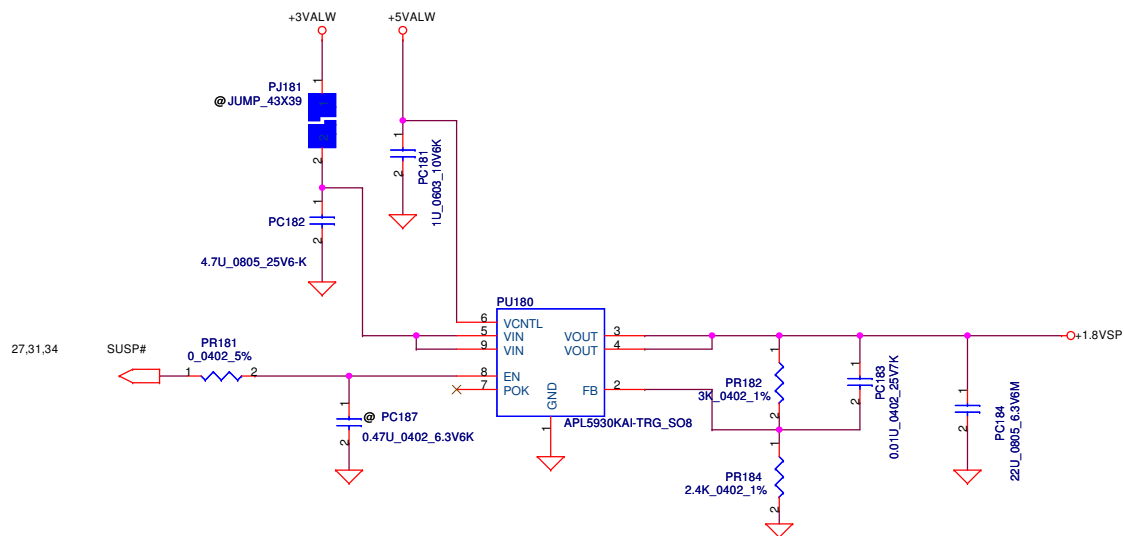
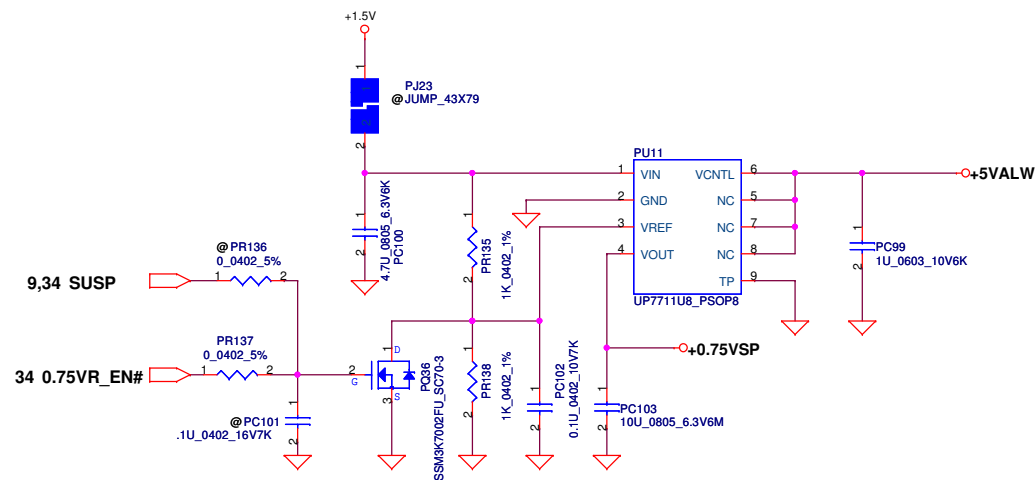


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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title <b>+VTTP</b>		
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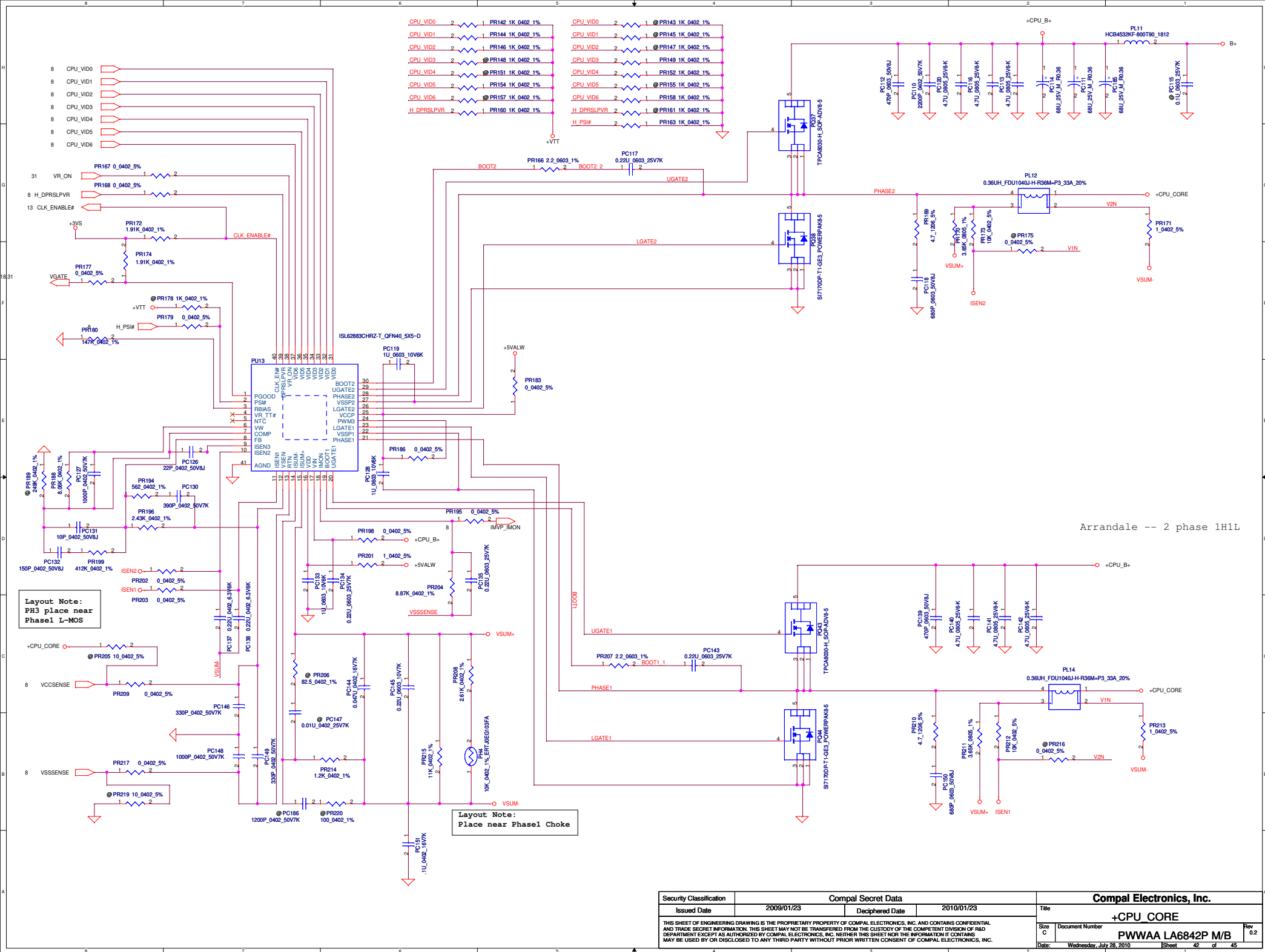
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										0.75VSP/+1.8VSP	
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										Sheet 41 of 45	

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/07/13	42		Change PL12,PL14 to SH00000IN00	BOM modify
2010/07/13	43		Change PL16 to SH00000IN00	BOM modify
2010/07/23	36		Change PC19 to SE070104Z80	BOM modify
2010/07/26	36		Add PD6,PD7	EMI request
2010/07/26	37		Add PC73,PC74,PC75(10U_1206)	EMI request
2010/07/26	38		Add PC121(2200P_0402),PC61(10U_1206)	EMI request
2010/07/26	39		Add PC122(2200P_0402),PC62(10U_1206)	EMI request
2010/07/26	40		Add PC123(2200P_0402)	EMI request

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				Size	Rev
		Document Number			0.2
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PIR (Product Improve Record)

PWWAA LA-6842P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.1 TO 0.2  
GERBER-OUT DATE: 2010/07/31  
NO    DATE    PAGE    MODIFICATION LIST

PURPOSE

1. 20100714 / Page13 --> add 10u Cap to +1.5VS\_CK505    For eSATA transmit issue    ---> not add 10u Cap into schematic yet

NWQAA LA-6061P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 1.0 TO 2.0  
GERBER-OUT DATE: 2010/03/19  
NO    DATE    PAGE    MODIFICATION LIST

PURPOSE

1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue

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		Size	Document Number		Rev
		Custom	PWWAA LA6842P M/B		0.2
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