

COMPAL CONFIDENTIAL

MODEL NAME : *Sapporo XA*

COMPAL P/N : *DFL10*

PCB NO : *LA-2051*

Revision : *0.1A*

Sapporo XA Schematics Document

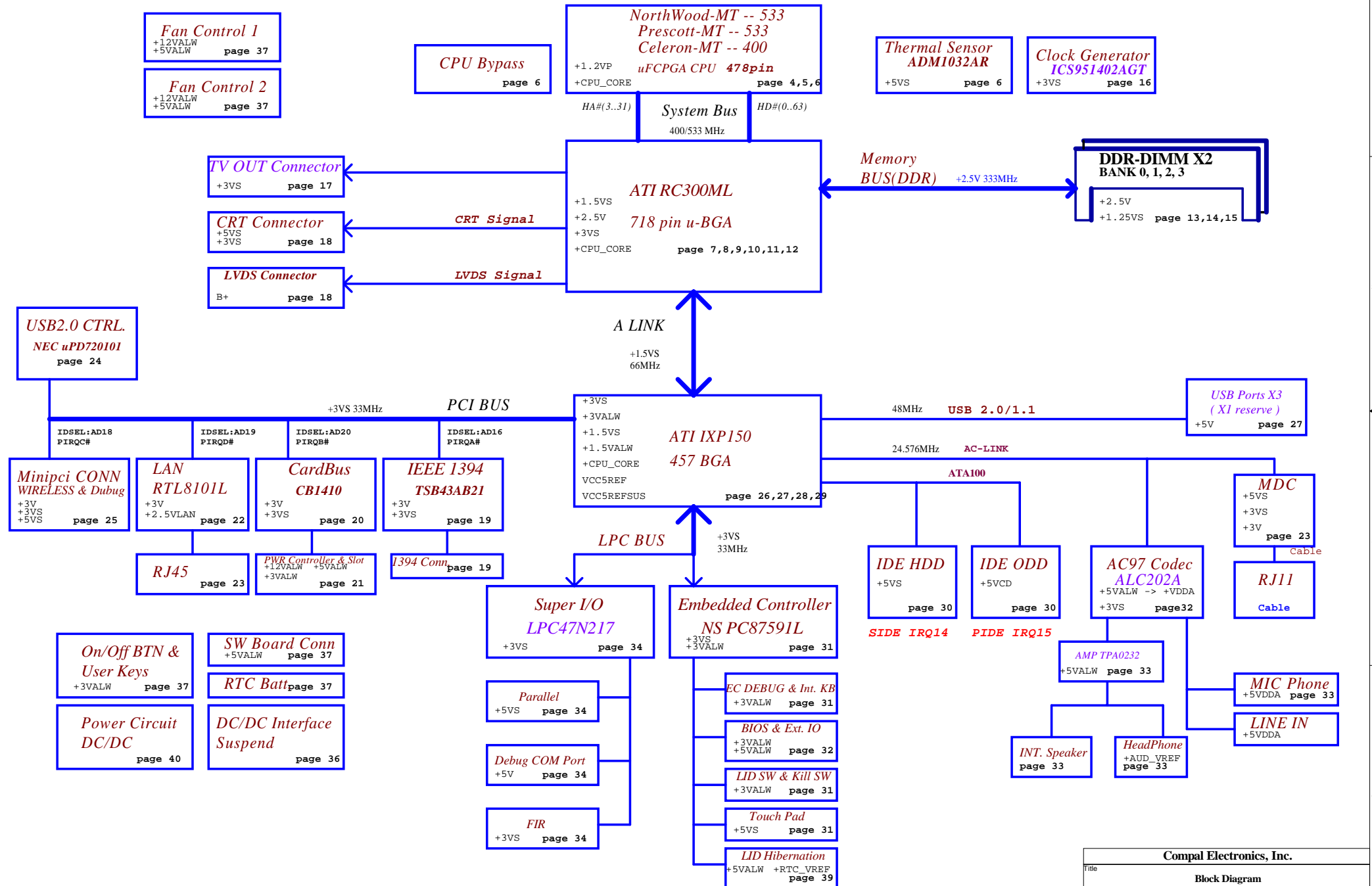
uFCBGA/uFCPGA NorthWood MT

2003 8 27 v0.1A

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Cover Sheet			
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Block Diagram



Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	The voltage for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.5VS	1.5V I/O power rail for ATI-RS300M/RC300M NB AGP.	ON	OFF	OFF
+1.8VS	1.8V switched power rail for ATI-RS300M/RC300M NB.	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V system power rail for SB,LAN,CardReader and HUB.	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V system power rail .	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD31 (INT.)	N/A	N/A
USB	AD30 (INT.)	N/A	D
AC97	AD31 (INT.)	N/A	B
ATA 100	AD31 (INT.)	N/A	A
ETHERNET	AD24(INT.)	N/A	C
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A
Wireless LAN(MINI PCI) AD18		3	C

EXT USB AD23(EXT.) 4 A,C,D

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16)	1010 000X b		

EC SM Bus2 address

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

Power Managment table

Signal	+3VALW	+5V	+2.5VS
	+5VALW	+3V	+1.8VS
State	+12VALW	+2.5V	+5VS
			+3VS
			+1.5VS
			+CPU_CORE
			+1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

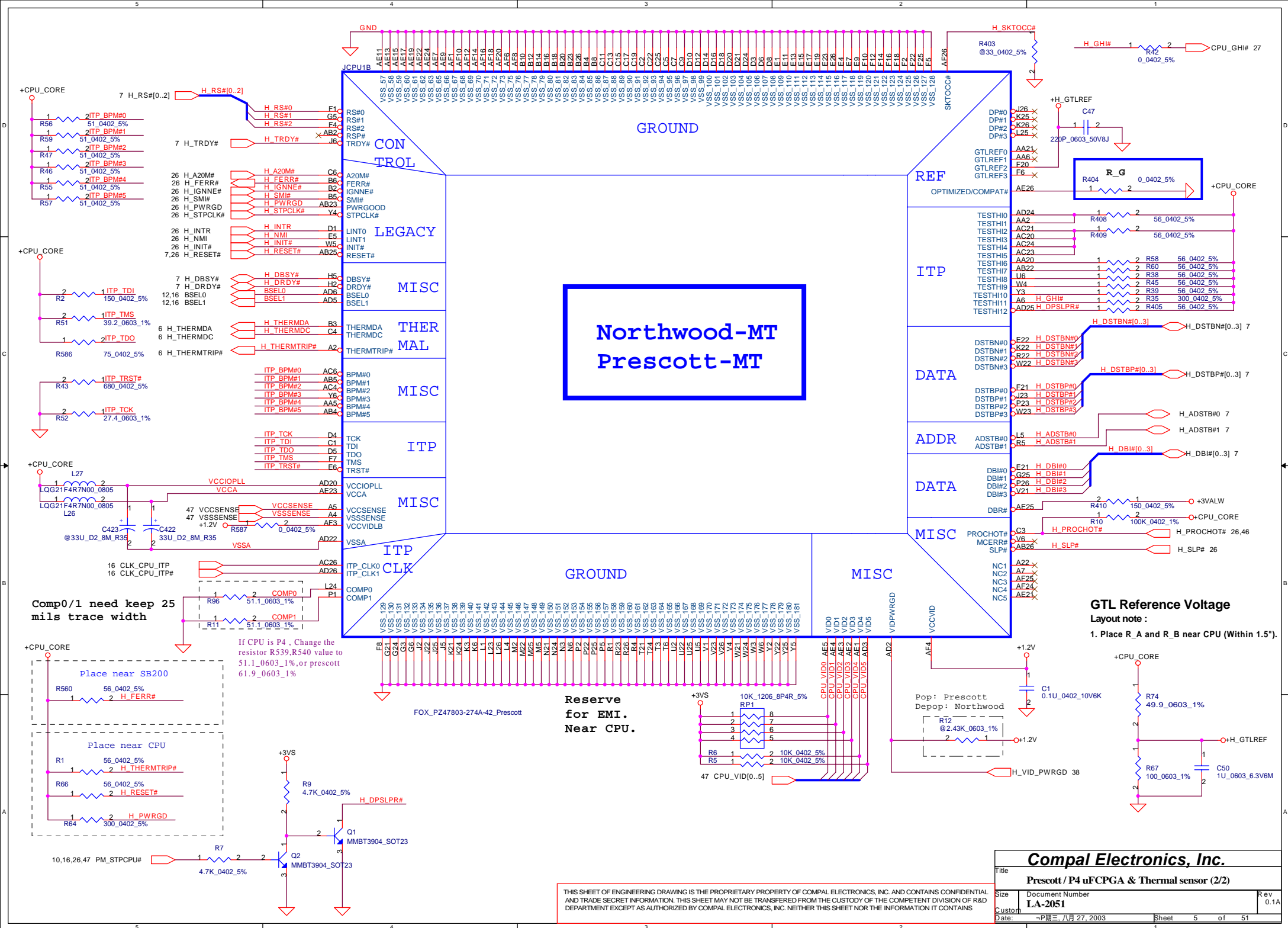
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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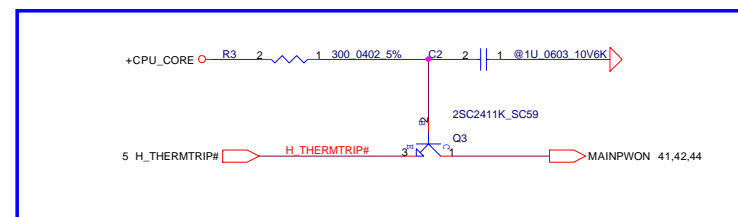
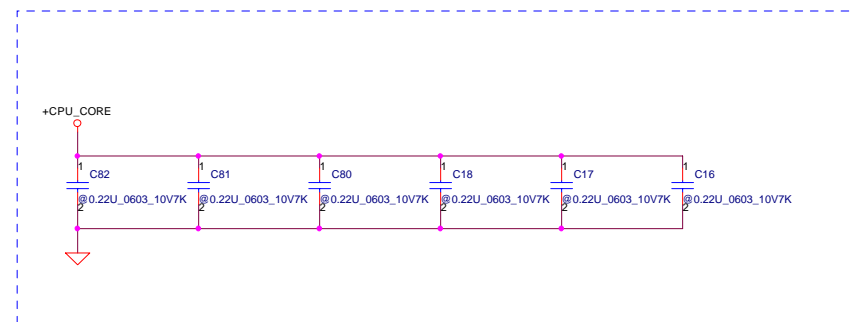
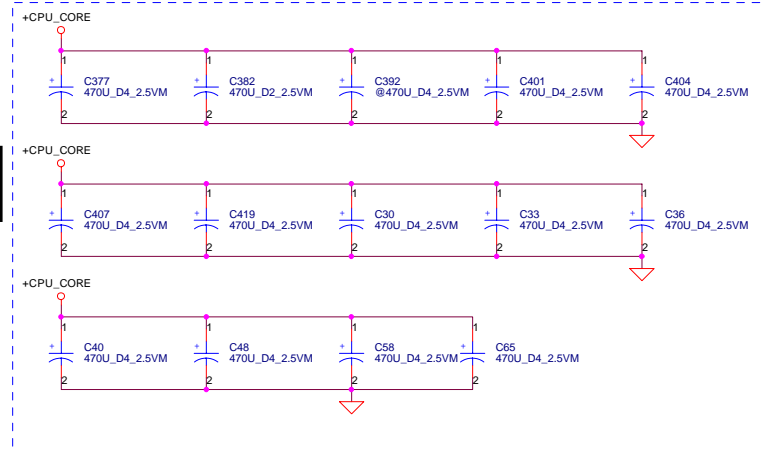
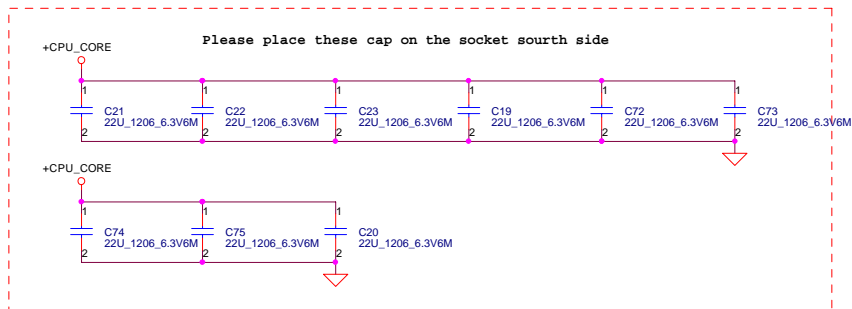
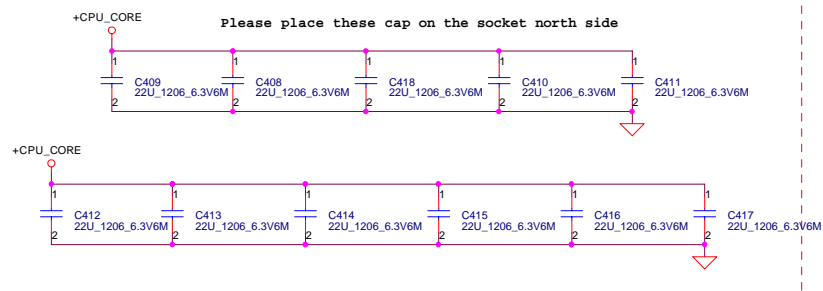
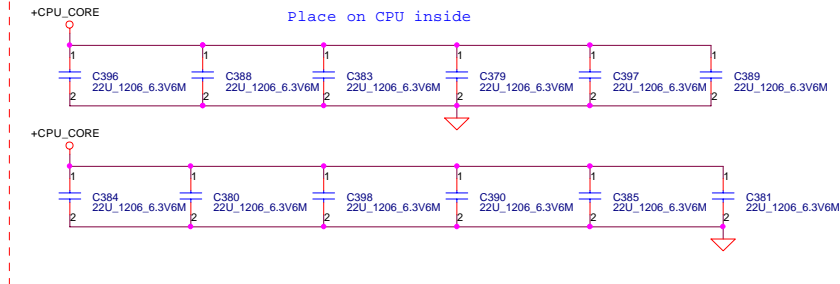
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Note & Revision			
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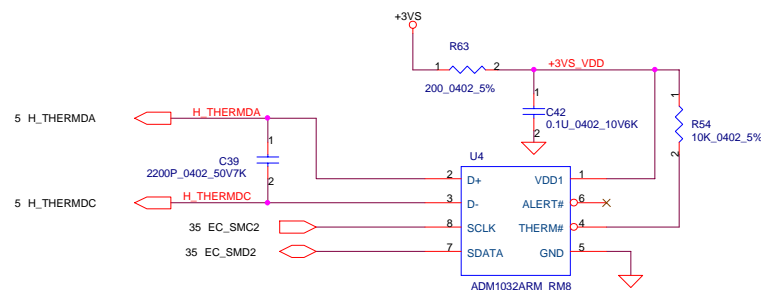
Layout note :
Place close to CPU. Use 2-3 vias per PAD.
Place 22uF caps x31 pcs, populated 14pcs.

Layout note :
Place close to CPU power and
ground pin as possible
(<1inch)

For Desktop's CPU:
470uF x 15/12mOhm H=1.8 each
Total 0.923m ohm

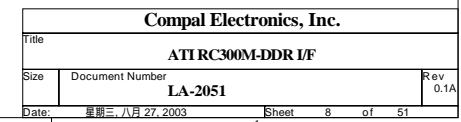
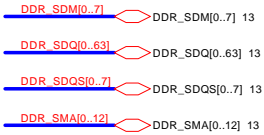


CPU Temperature Sensor



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Title CPU Decoupling CAP.			
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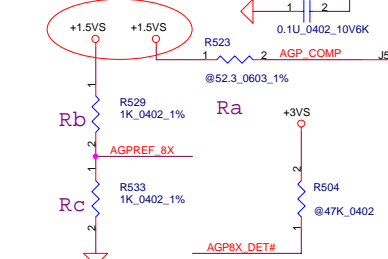
12,26 A_AD[0..31] A_AD[0..31]
12,26 A_CBE#[0..3] A_CBE#[0..3]

A_AD0 AK5
A_AD1 AJ5
A_AD2 AH5
A_AD3 AH4
A_AD4 AJ3
A_AD5 AJ2
A_AD6 AH2
A_AD7 AH1
A_AD8 AG2
A_AD9 AG1
A_AD10 AG1
A_AD11 AE3
A_AD12 AF1
A_AD13 AF2
A_AD14 AF4
A_AD15 AE3
A_AD16 AE4
A_AD17 AE5
A_AD18 AE6
A_AD19 AC2
A_AD20 AC4
A_AD21 AB3
A_AD22 AB5
A_AD23 AB5
A_AD24 AB6
A_AD25 AA2
A_AD26 AA4
A_AD27 AA5
A_AD28 AA6
A_AD29 Y3
A_AD30 Y6
A_AD31 Y8
ALINK_AD0
ALINK_AD1
ALINK_AD2
ALINK_AD3
ALINK_AD4
ALINK_AD5
ALINK_AD6
ALINK_AD7
ALINK_AD8
ALINK_AD9
ALINK_AD10
ALINK_AD11
ALINK_AD12
ALINK_AD13
ALINK_AD14
ALINK_AD15
ALINK_AD16
ALINK_AD17
ALINK_AD18
ALINK_AD19
ALINK_AD20
ALINK_AD21
ALINK_AD22
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ALINK_AD27
ALINK_AD28
ALINK_AD29
ALINK_AD30
ALINK_AD31

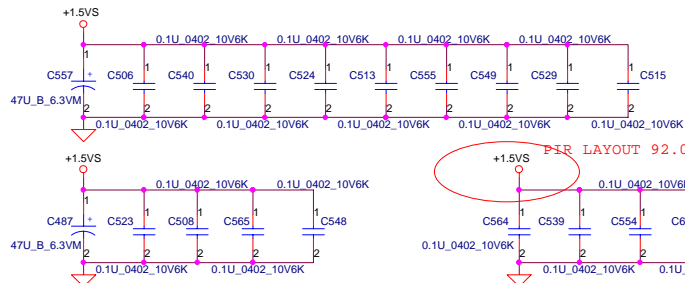
A_CBE#0 AG5
A_CBE#1 AE2
A_CBE#2 AC3
A_CBE#3 AC3
ALINK_CBE#0
ALINK_CBE#1
ALINK_CBE#2
ALINK_CBE#3

12,26 A_PAR AC6
26 A_STROBE# AC6
26 A_ACAT# AC5
26 A_END# AD2
19,20,24,26 PCI_PIRQA# W4
26 A_DEVSEL# 2 0_0402_5% W4
26 A_OFF# AD3
26 A_SBRREQ# W5
26 A_SBGNT# W6
PCI_PAR/ALINK_NC
PCI_STROBE#/ALINK_STROBE#
PCI_ACAT#/ALINK_ACAT#
PCI_END#/ALINK_END#
PCI_DEVSEL#/ALINK_DEVSEL#
PCI_OFF#/ALINK_OFF#
PCI_STOP#/ALINK_STOP#
ALINK_SBRREQ#
ALINK_SBGNT#
PCI_REQ#/ALINK_NC
PCI_GNT#/ALINK_NC

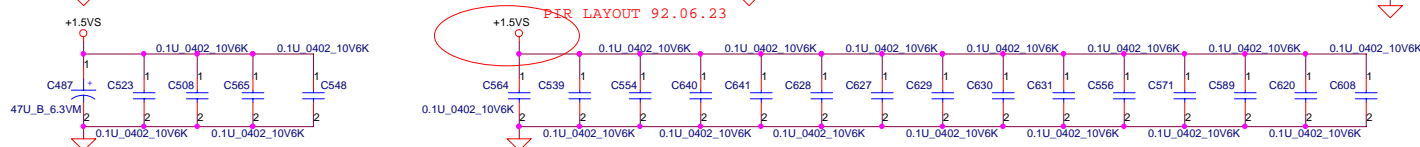
AGP8X_DET# M5
AGPREF_8X J6
AGP_COMP J5
AGP_COMP



8X(M9+M10@)	4X(NAGP@)
Ra 169_0402_1%	52_1_0402_1%
Rb 324_0402_1%	1k_0402_1%
Rc 100_0402_1%	1k_0402_1%



PIR LAYOUT 92.06.23



Note: PLACE CLOSE TO U27 (NB RC300M)

PART3CF6

PCI Bus 0 / A-Link I/F
PCI BUS 1 / AGP Bus (GPIO, TMD5, TMD5, ZVPort)

AGP_AD0/TMD2_HSYNC W2
AGP_AD1/TMD2_VSYNC W3
AGP_AD2/TMD2_D1 W2
AGP_AD3/TMD2_D0 W3
AGP_AD4/TMD2_D3 W2
AGP_AD5/TMD2_D2 W1
AGP_AD6/TMD2_D5 W3
AGP_AD7/TMD2_D4 W3
AGP_AD8/TMD2_D6 W2
AGP_AD9/TMD2_D9 W2
AGP_AD10/TMD2_D8 W1
AGP_AD11/TMD2_D1 W3
AGP_AD12/TMD2_D10 W3
AGP_AD13 W3
AGP_AD14 W2
AGP_AD15 W2
AGP_AD16/TMD1_VSYNC W2
AGP_AD17/TMD1_HSYNC W2
AGP_AD18/TMD1_DE W2
AGP_AD19/TMD1_D0 W2
AGP_AD20/TMD1_D1 W2
AGP_AD21/TMD1_D2 W2
AGP_AD22/TMD1_D3 W1
AGP_AD23/TMD1_D4 W1
AGP_AD24/TMD1_D1 W3
AGP_AD25/TMD1_D6 W2
AGP_AD26/TMD1_D9 W2
AGP_AD27/TMD1_D8 W2
AGP_AD28/TMD1_D11 W2
AGP_AD29/TMD1_D10 W2
AGP_AD30/TMD5_HPD W2
ALINK_AD31 W1

AGP2_SBSTB/AGP3_SBSTB/NC/LVDS_BLOK
AGP2_SBSTB/AGP3_SBSTB/NC/ENA_BL
AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK#
AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK#
AGP2_ADSTB1/AGP3_ADSTB1/TMD1_CLK#
AGP2_ADSTB1/AGP3_ADSTB1/TMD1_CLK#

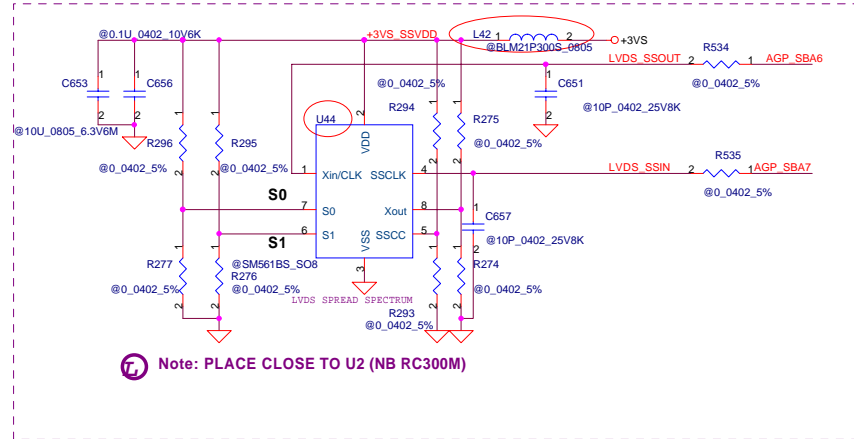
AGP2_CBE#0/AGP3_CBE0/TMD2_D7
AGP2_CBE#1/AGP3_CBE1/TMD2_DE
AGP2_CBE#2/AGP3_CBE2
AGP2_CBE#3/AGP3_CBE3/TMD1_D5

AGP2_IRDY#/AGP3_IRDY#/GPIO8/I2C_CLK
AGP2_TRDY#/AGP3_TRDY#/TMD5_DVI_CLK
AGP2_STOP#/AGP3_STOP#/GPIO10/DVC_DATA
AGP2_FRAME#/AGP3_FRAME#/TMD5_DVI_DATA
AGP2_DEVSEL#/AGP3_DEVSEL#/GPIO9/I2C_DATA
AGP2_PIPE#/AGP3_PIPE#/DBI_HI
AGP2_NC#/AGP3_NC#/DBI_LO
AGP2_WB#/AGP3_WB#

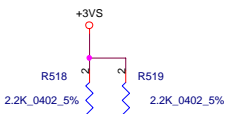
AGP2_SBA0/AGP3_SBA0/GPIO0/VDDC_CNTL0
AGP2_SBA1/AGP3_SBA1/GPIO1/VDDC_CNTL1
AGP2_SBA2/AGP3_SBA2/GPIO2/LVDS_BLOK#
AGP2_SBA3/AGP3_SBA3/GPIO3/LVDS_BLOK#
AGP2_SBA4/AGP3_SBA4/GPIO4/STP_AGP#
AGP2_SBA5/AGP3_SBA5/GPIO5/AGP_BUSY#
AGP2_SBA6/AGP3_SBA6/GPIO6/LVDS_SSOUT
AGP2_SBA7/AGP3_SBA7/GPIO7/LVDS_SSIN

AGP_ST0
AGP_ST1
AGP_ST2

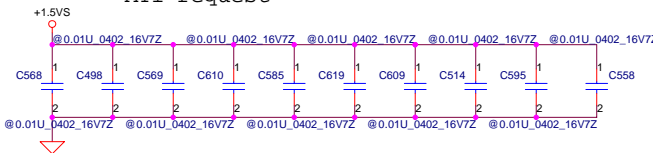
DDC_CLK C3
DDC_DAT C2
AGP_SBA2 C4
AGP_SBA3 C4
AGP_SBA4 C4
AGP_SBA5 C4
AGP_SBA6 C4
AGP_SBA7 C4



Note: PLACE CLOSE TO U2 (NB RC300M)



ATI request

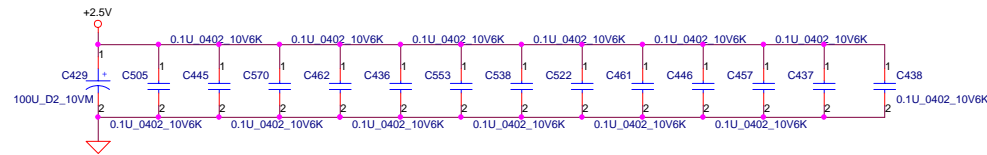
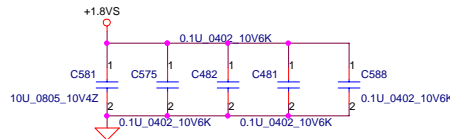
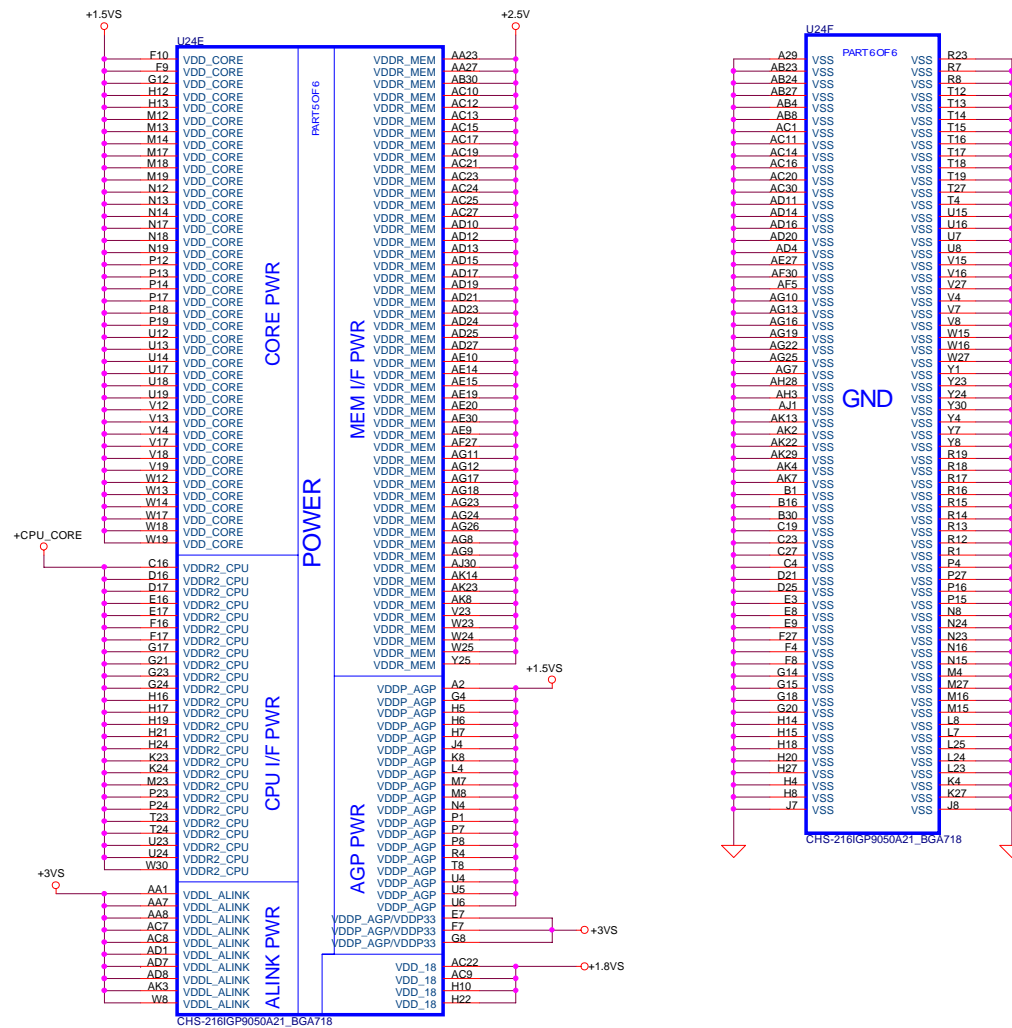


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ATIRC300M-AGP, ALINK BUS

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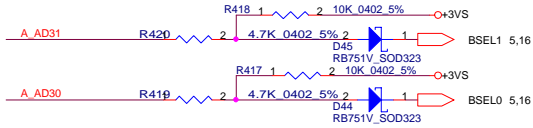
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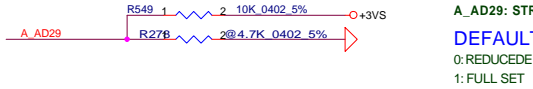
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ATI RC300M-POWER			
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9,26 A_AD[0..31] A_AD[0..31]
9,26 A_CBE#[0..3] A_CBE#[0..3]



A_AD[31..30] : FSB CLK SPEED
DEFAULT: 01
00: 100 MHz
01: 133 MHz
10: 200MHz
11:166 MHz



A_AD29: STRAP CONFIGURATION
DEFAULT: 1
0: REDUCEDE SET
1: FULL SET



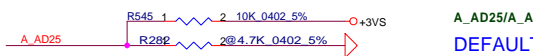
A_AD28: SPREAD SPECTRUM ENABLE
DEFAULT: 0
0: DISABLE
1: ENABLE



A_AD27: FrcShortReset#
DEFAULT: 1
0: TEST MODE
1: NORMAL MODE



A_AD26 : ENABLE IOQ
DEFAULT: 1
0: IOQ=1
1: IOQ=12



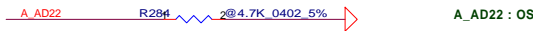
A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 10
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V
AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17--DON'T CARE



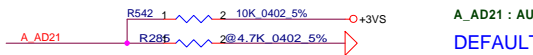
A_AD24 : MOBILE CPU SELECT
DEFAULT: 1
0: BANIAS CPU
1: OTHER CPU



A_AD23 : CLOCK BYPASS DISABLE
DEFAULT: 1
0: TEST MODE
1: NORMAL



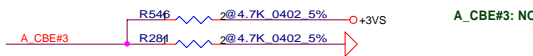
A_AD22 : OSC PAD OUTPUT PCICLK
DEFAULT : 1
0:PCICLK OUT
1: OSC CLK OUT



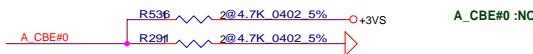
A_AD21 : AUTO_CAL ENABLE
DEFAULT : 1
0: DISABLE
1: ENABLE



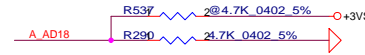
A_AD20 : INTERNAL CLK GEN ENABLE
DEFAULT : 0
0: DISABLE
1: ENABLE



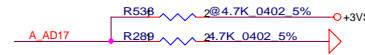
A_CBE#3: NOT USED



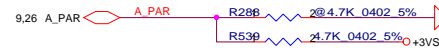
A_CBE#0 :NO USED



A_AD18 : ENABLE PHASE CALIBRATION
DEFAULT: 0
0: DISABLE
1:ENABLE



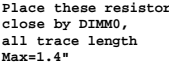
A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 0
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V

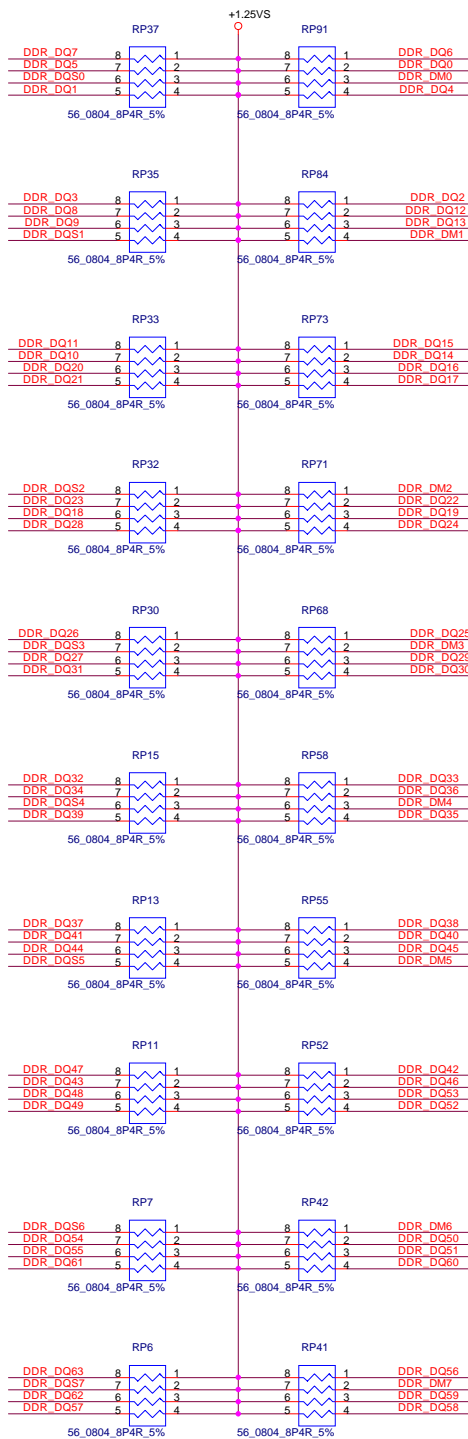


PAR: EXTENDED DEBUG MODE
DEFAULT : 1
0: DEBUG MODE
1: NORMAL

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ATIRC300M-SYSTEM STRAP			
Size	Document Number	Rev	
	LA-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	12 of 51

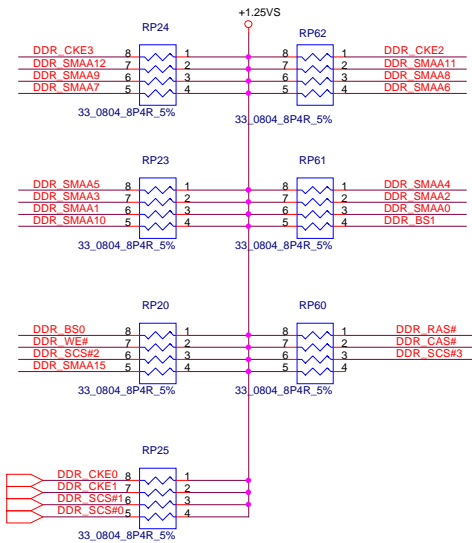
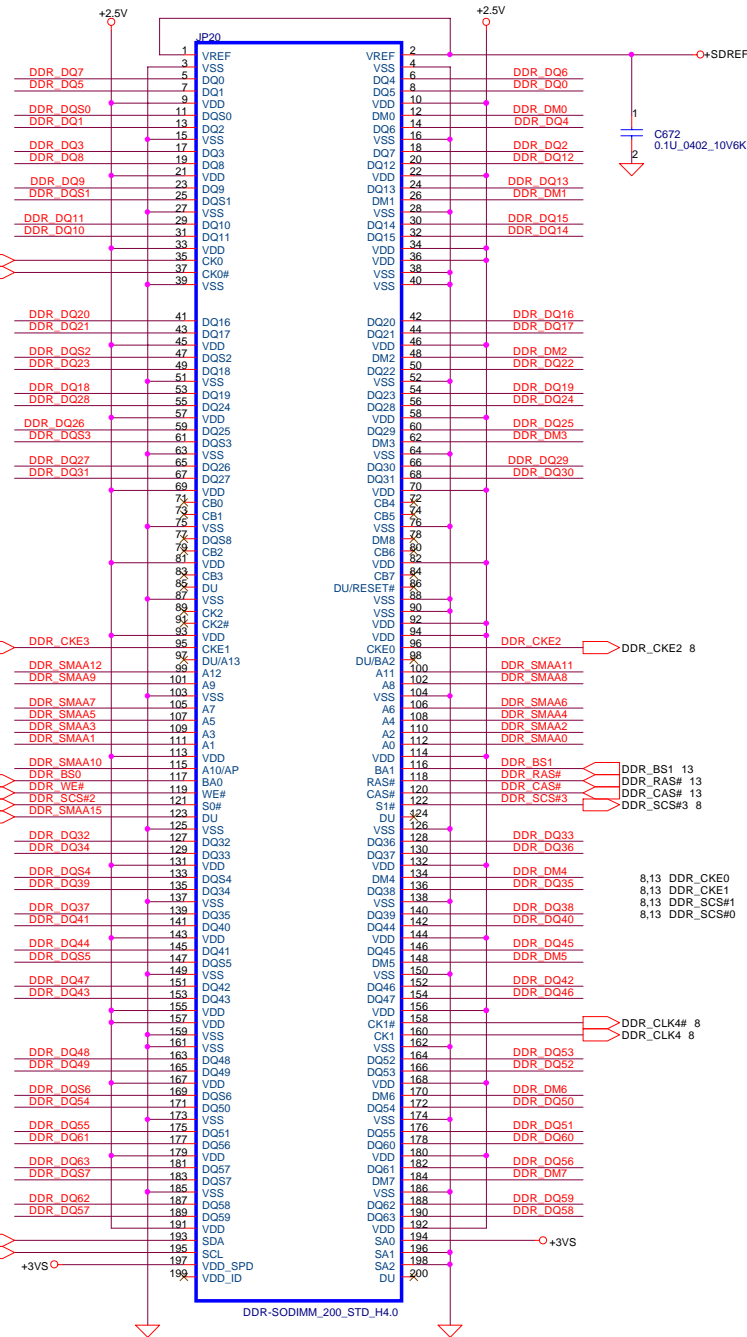




Layout note
Place these resistor
closely DIMM1,
all trace
length<800mil

13,16,27 SMATA
13,16,27 SMCLK

DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#



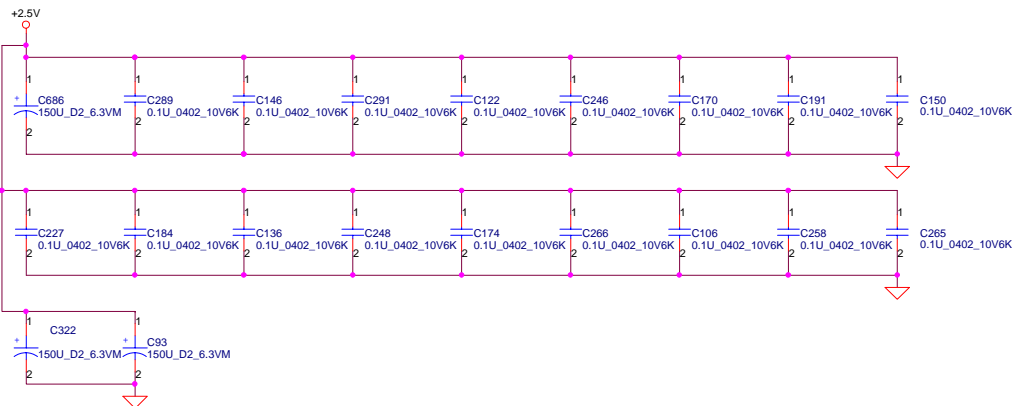
DDR_DQ50[.7] DDR_DQ50[.7] 13
DDR_DQ0[.63] DDR_DQ0[.63] 13
DDR_DM0[.7] DDR_DM0[.7] 13
DDR_SMAA[0..12] DDR_SMAA[0..12] 13

Layout note
Place these resistor
close by DIMM1,
all trace length
Max=0.8"

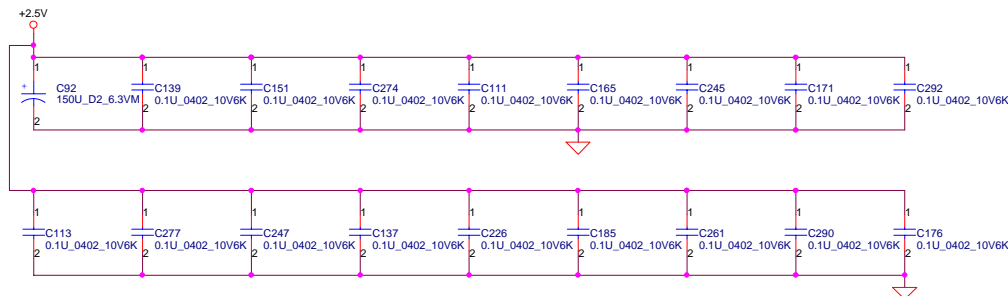
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Compale Electronics, Inc.			
Title			
DDR-SODIMM SLOT1			
Size	Document Number	Rev	
	LA-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	14 of 51

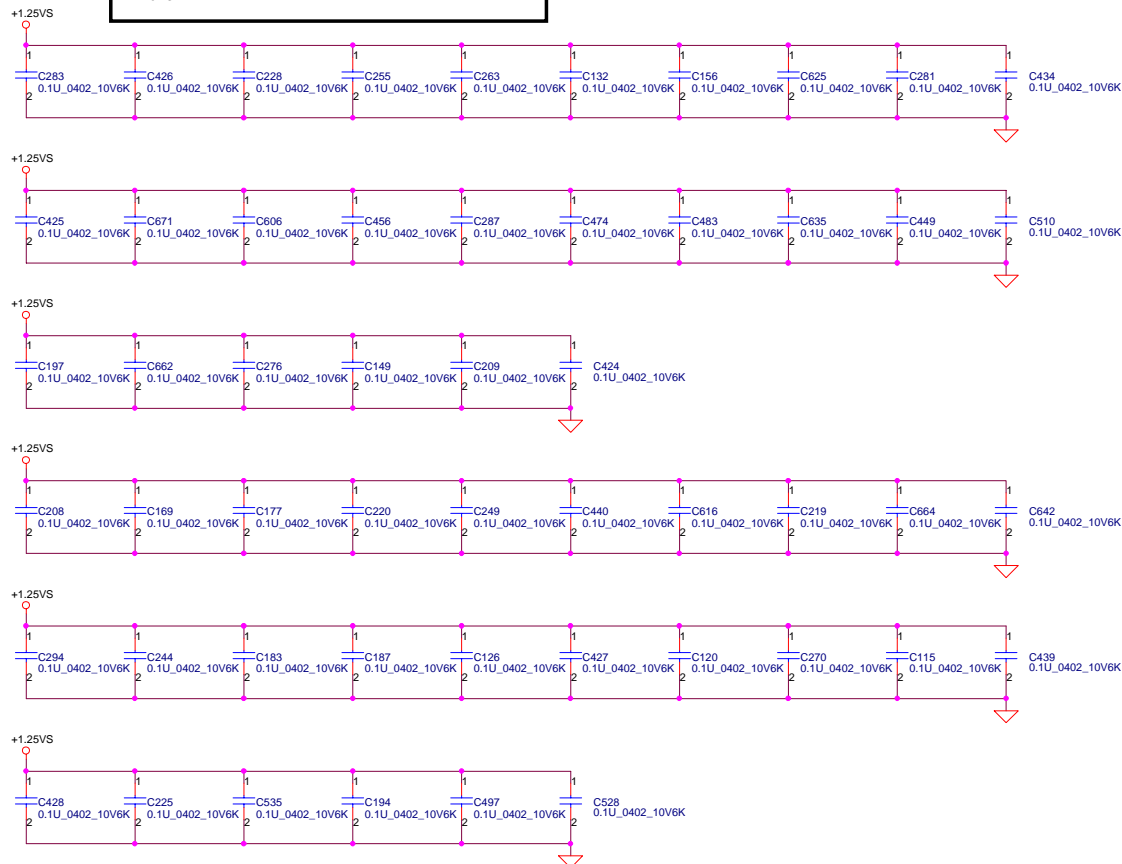
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



Layout note :
Distribute as close as possible
to DDR-SODIMM1.

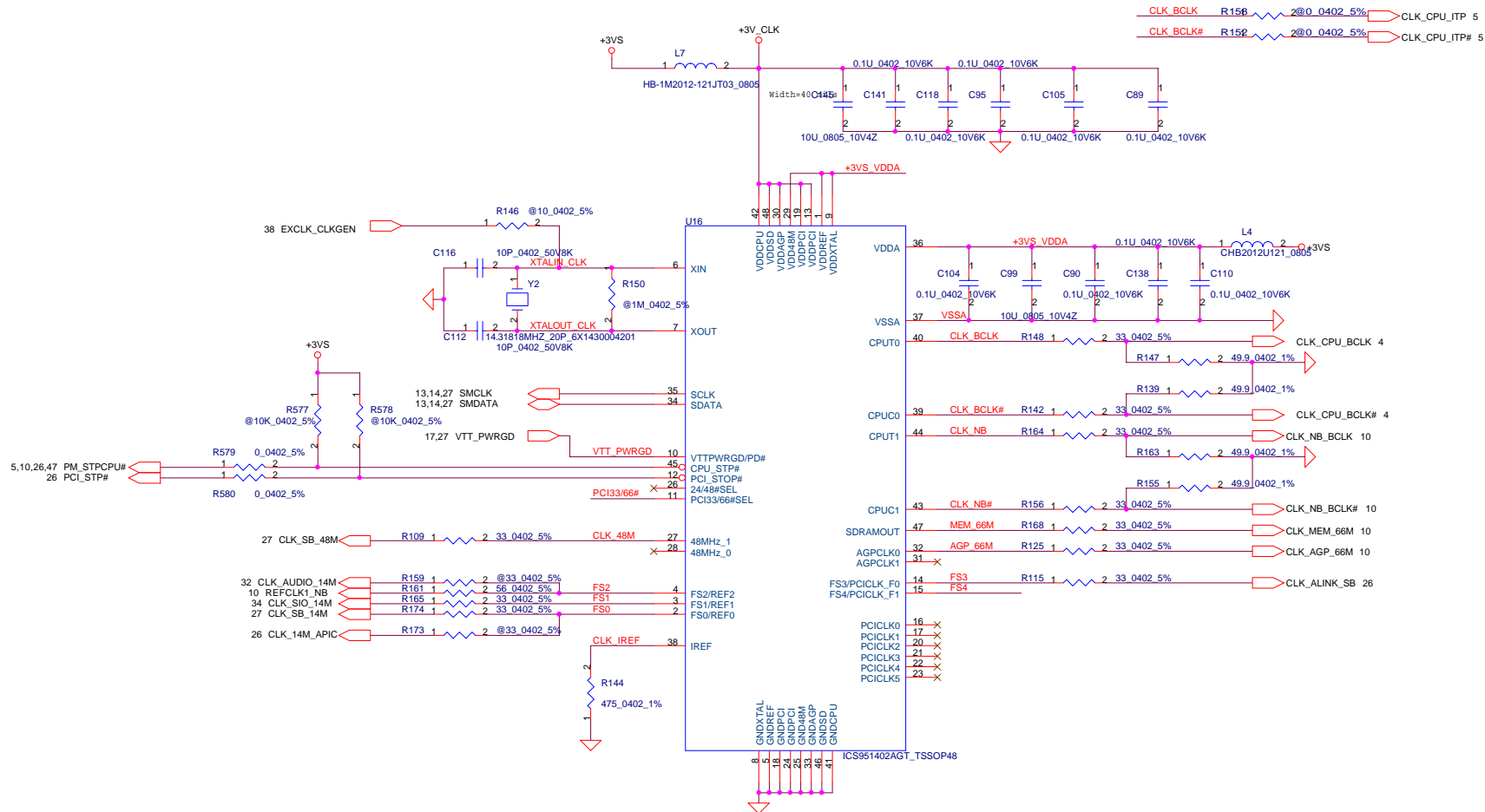


Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS



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Compal Electronics, Inc.			
Title			
DDR SODIMM Decoupling			
Size	Document Number	Rev	
	L/A-2051	0.1A	
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CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	Spread OFF OR Center spread +/-0.3%
0	0	0	0	1	133	133	
0	0	0	0	0	100	100	

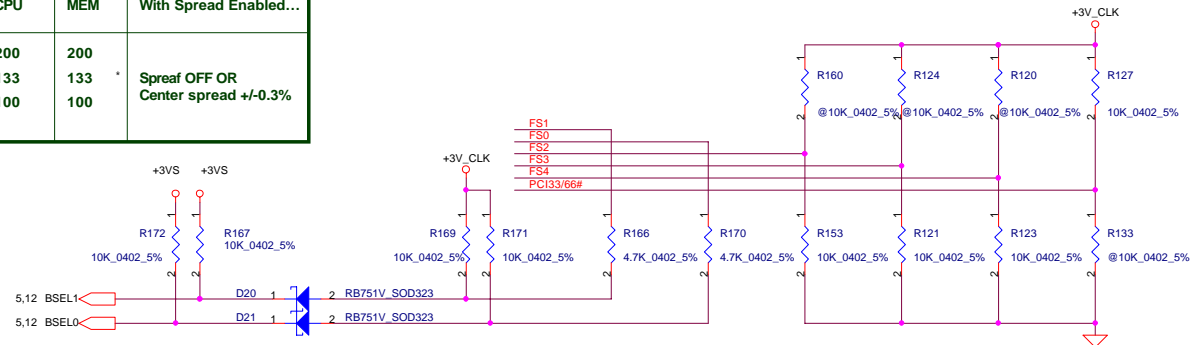
★ ★

Note: 0 = PULL LOW
1 = PULL HIGH

A-LINK FREQ

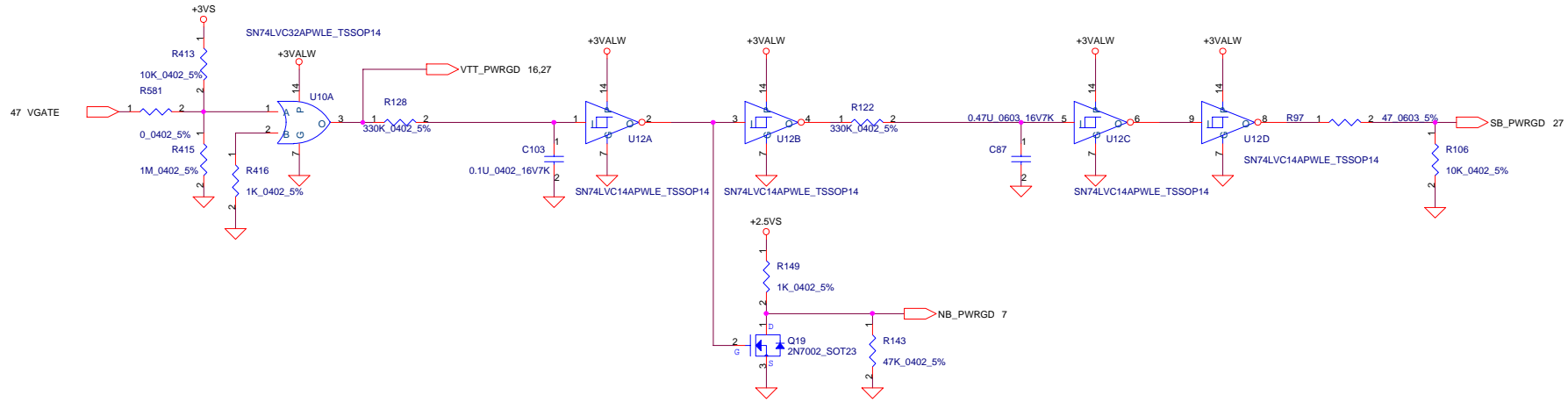
★ ★

PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

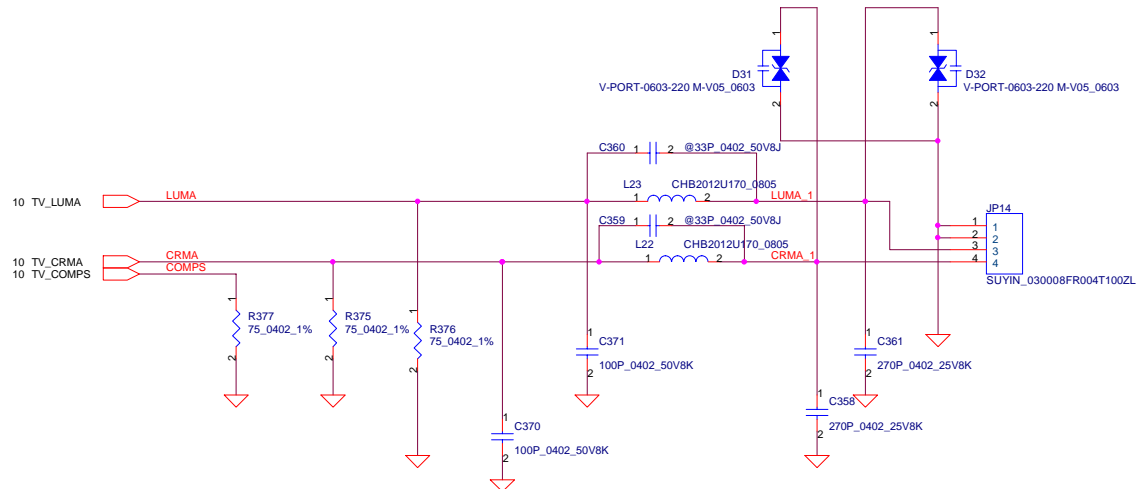


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Compal Electronics, Inc.		
Clock Generator		
Title	Document Number LA-2051	Rev 0.1A
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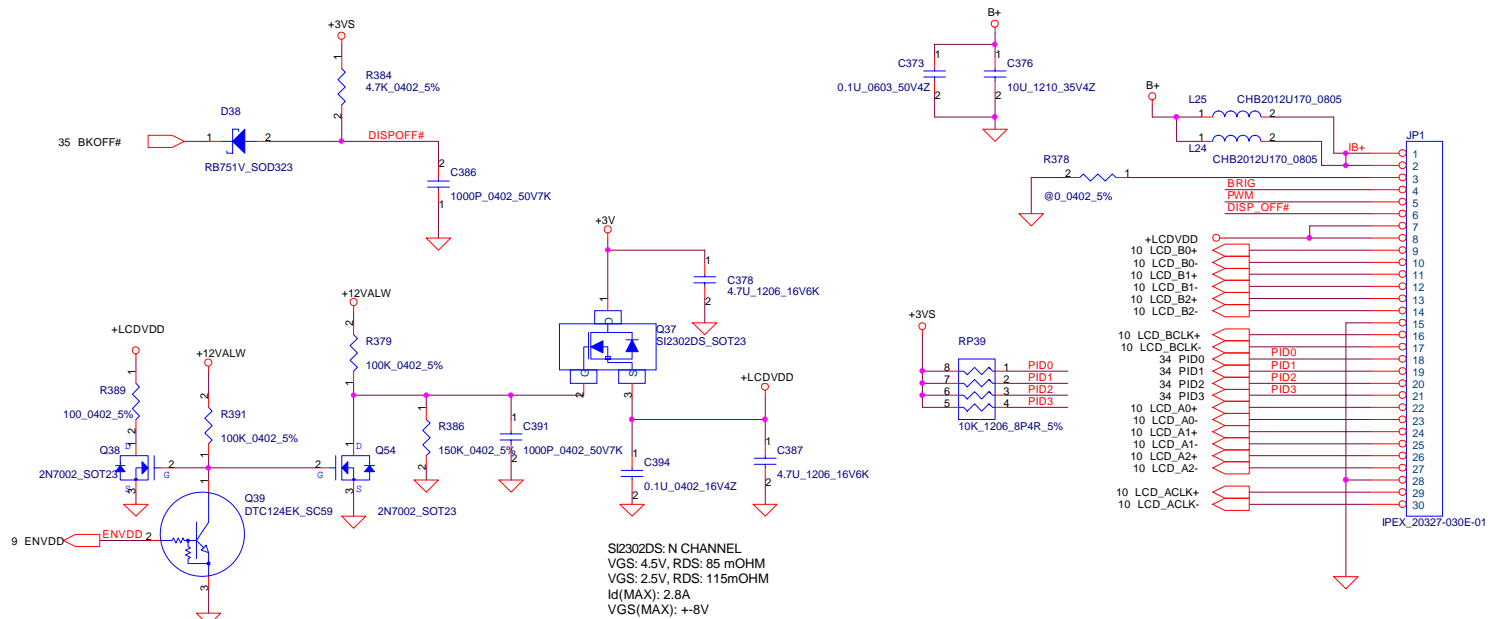
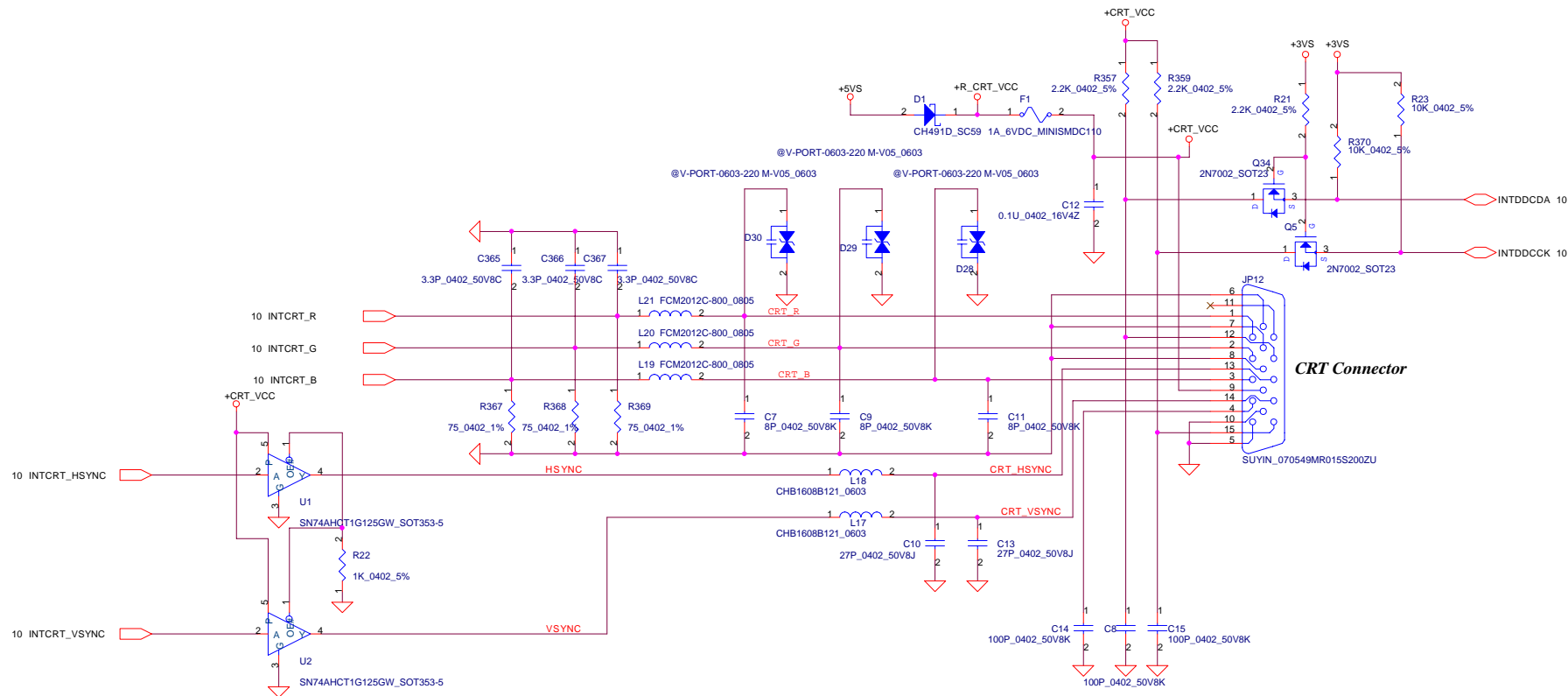


TV-OUT CONN.

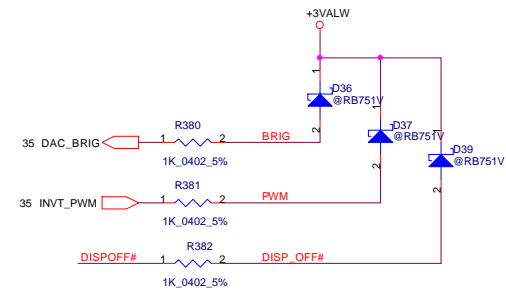


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Compal Electronics, Ltd.			
CH-7011& TV-CONN.			
Title	Document Number	Rev	
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Protect for EC

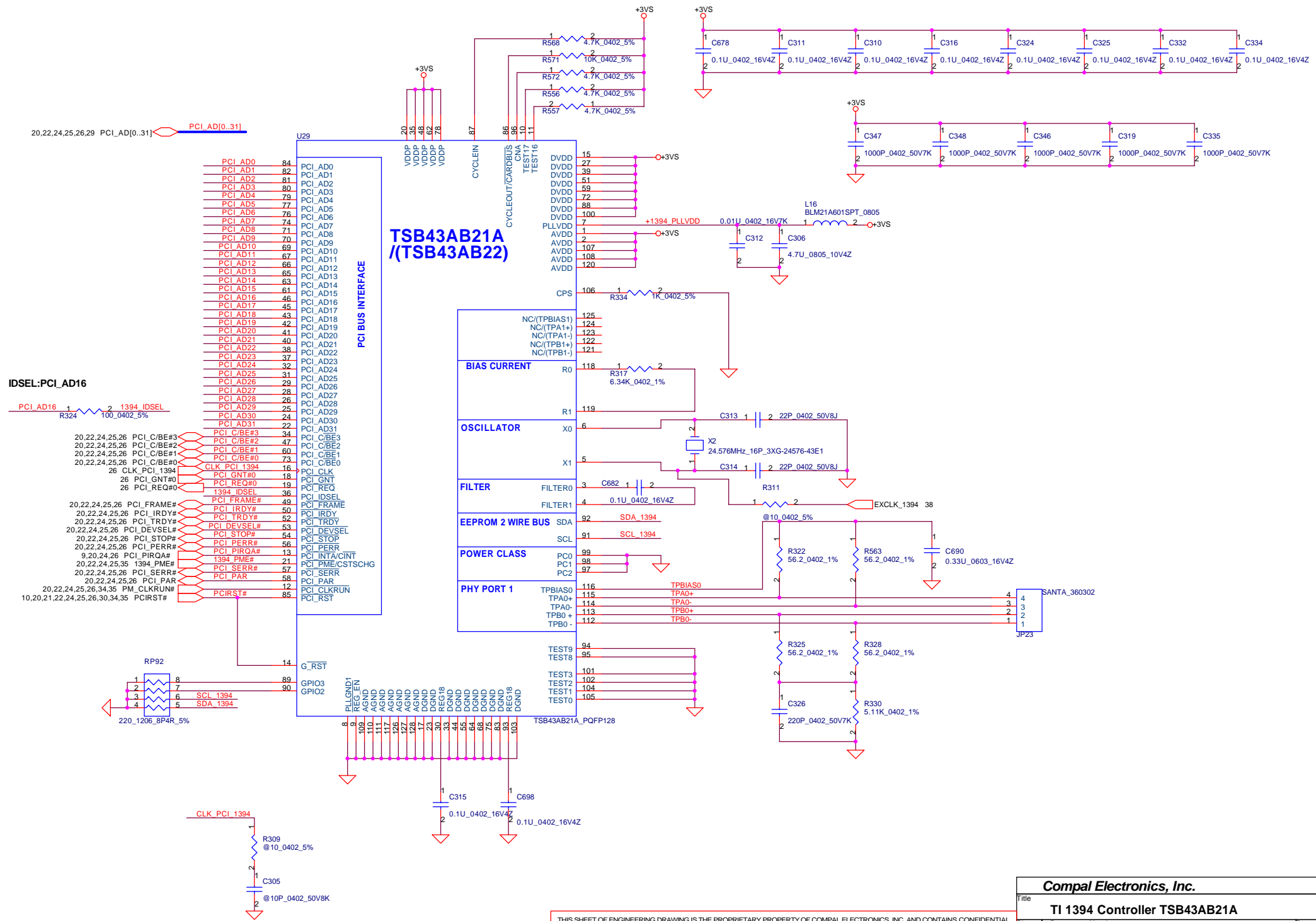


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Compal Electronics, Ltd.			
CRT & LVDS CONN.			
Title	Document Number	Rev	
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TSB43AB21A (TSB43AB22)

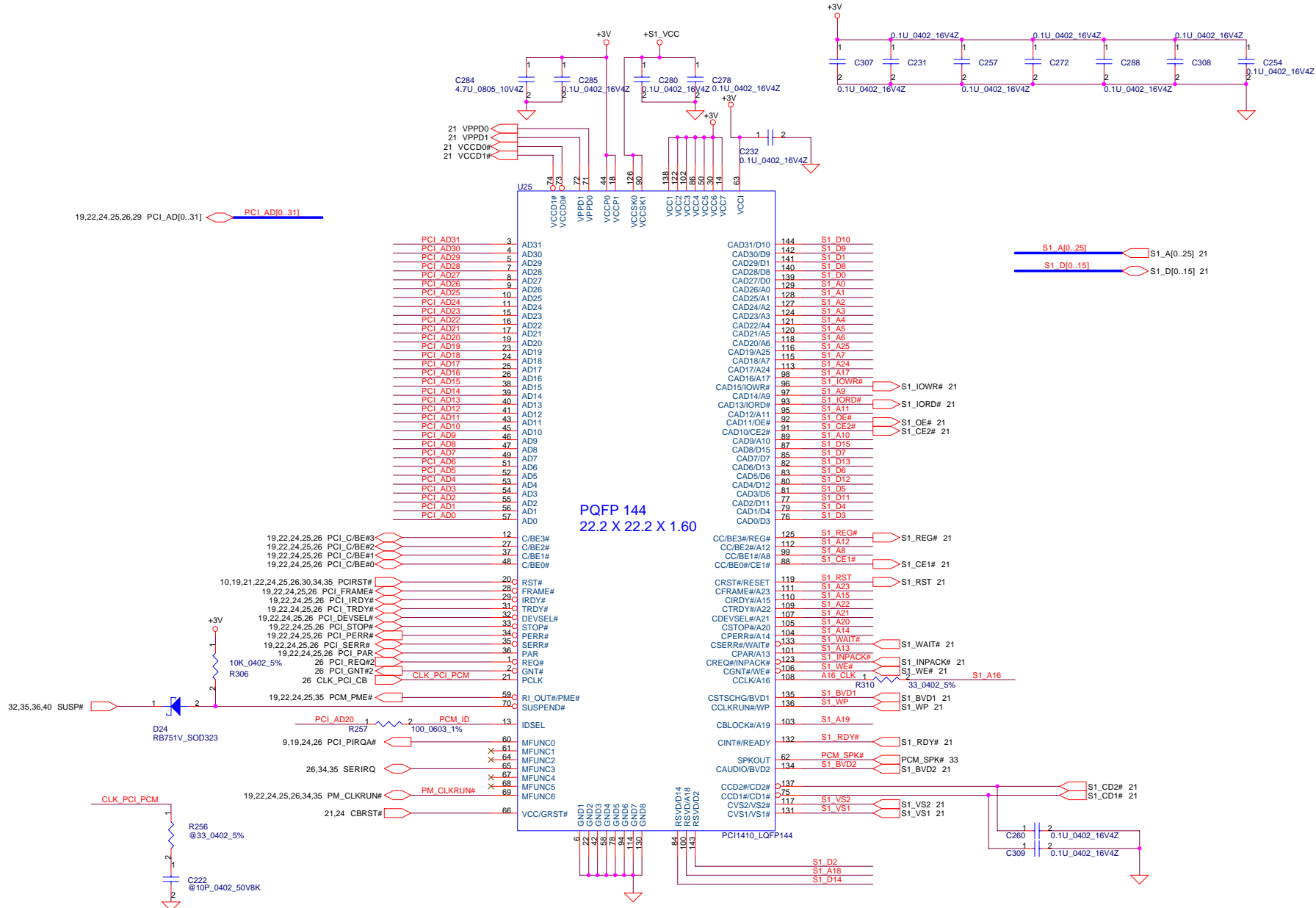
PCI BUS INTERFACE



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Compal Electronics, Inc.			
Title			
TI 1394 Controller TSB43AB21A			
Size	Document Number	Rev	
Custom	LA-2051	0.1A	
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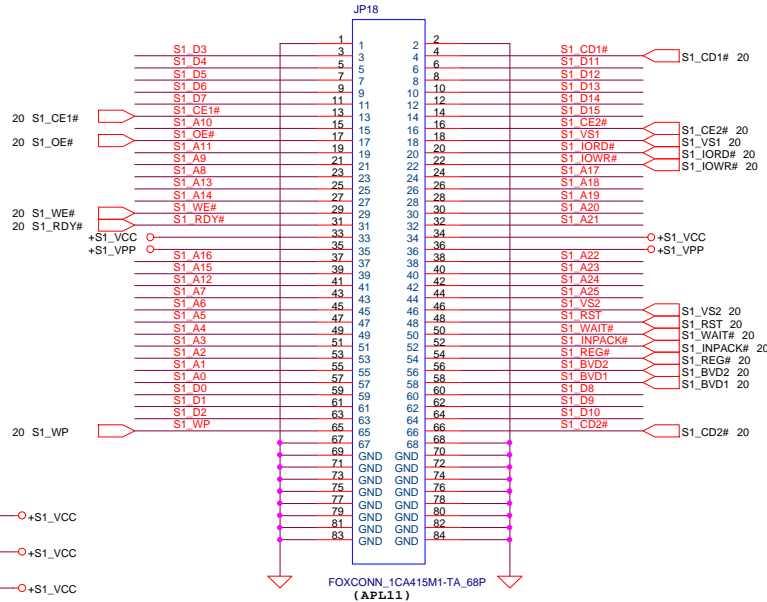
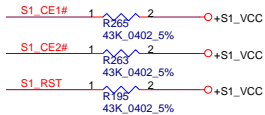
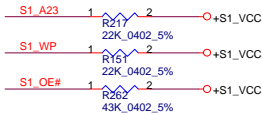
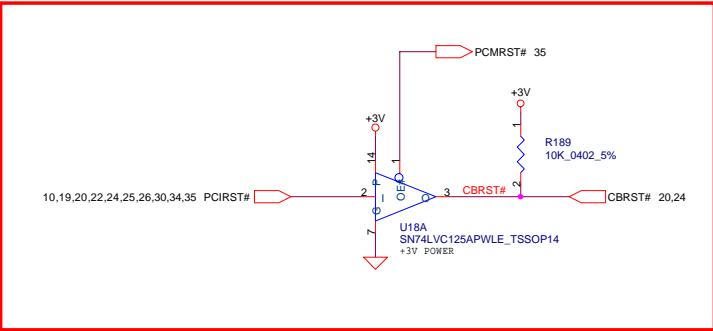
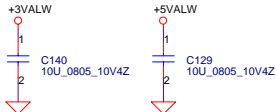
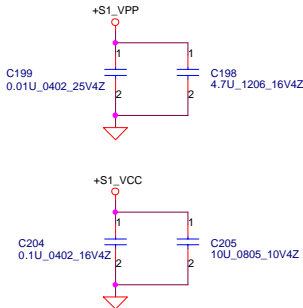
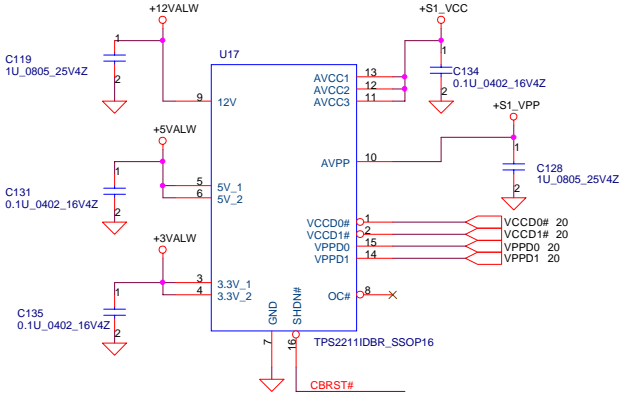
CARD BUS AD20 REQ#2/GNT#2 PCI_PIRQA#



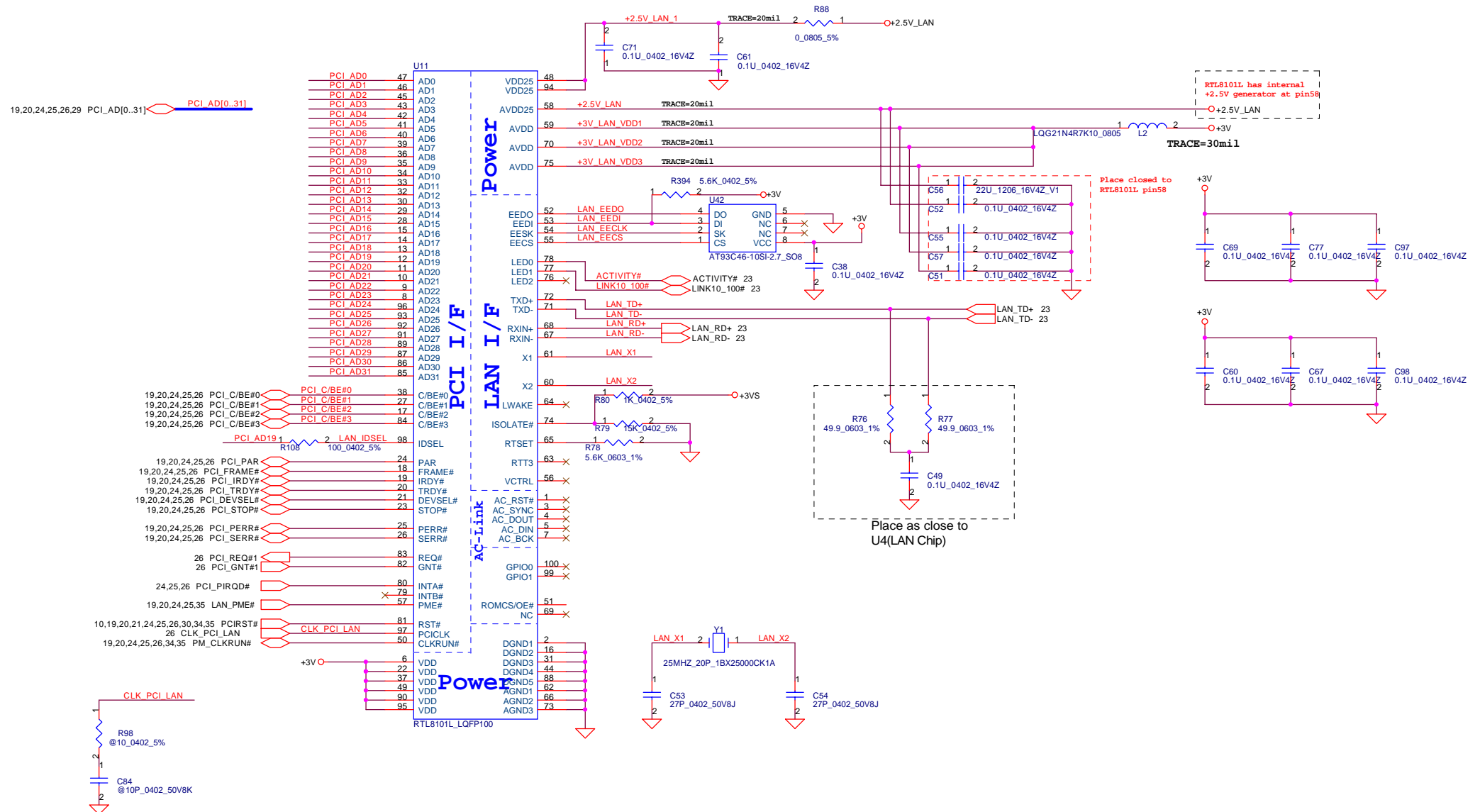
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Compal Electronics, Ltd.			
Title CardBus Controller<TI PCI1410>			
Size Custom	Document Number LA-2051	Rev 0.1A	
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PCMCIA Power Controller



LAN AD19 REQ#1/GNT#1 PCI_PIRQD#



Compal Electronics, Inc.

Title	LAN REALTEK RTL8101L
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Size	Document Number LA-2051
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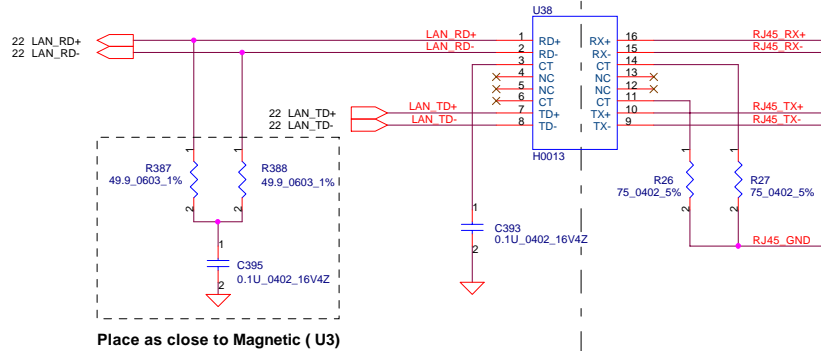
Rev	
0.1A	

Date: 星期三, 八月 27, 2003 Sheet 22 of 51

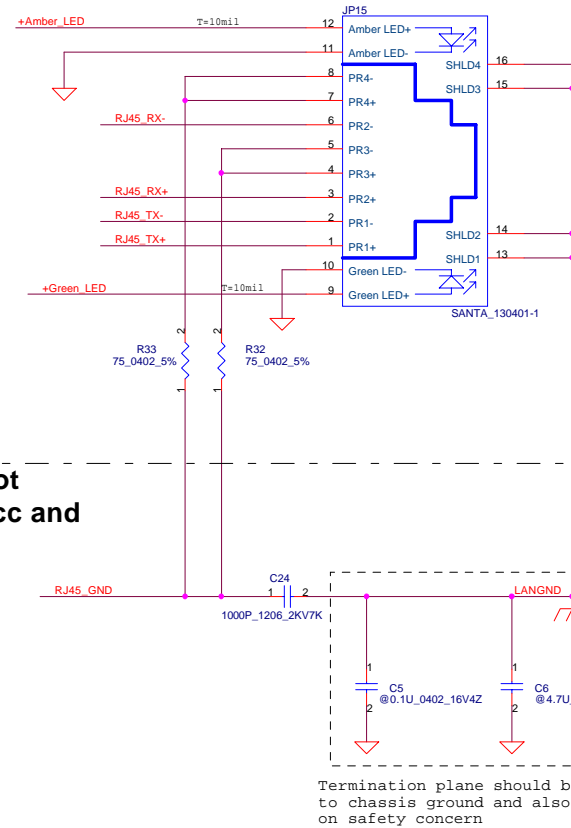
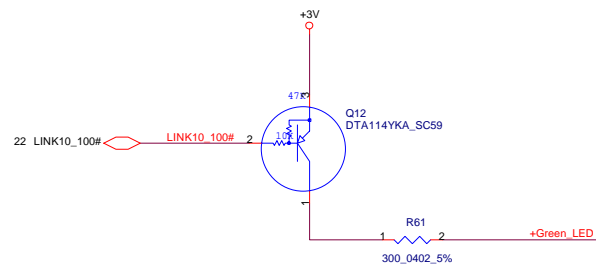
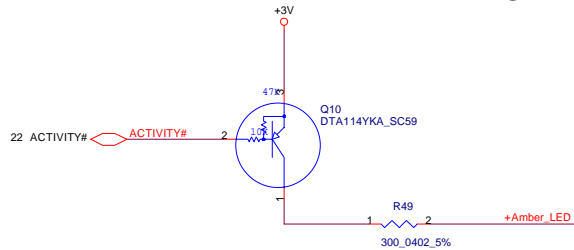
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Keep Out 40mil

Layout Note
H0013 pls close to
conn.



LAYOUT NOTICE: This area do not
connect to power plan include Vcc and
GND in any layer

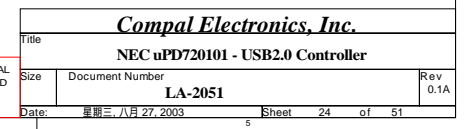


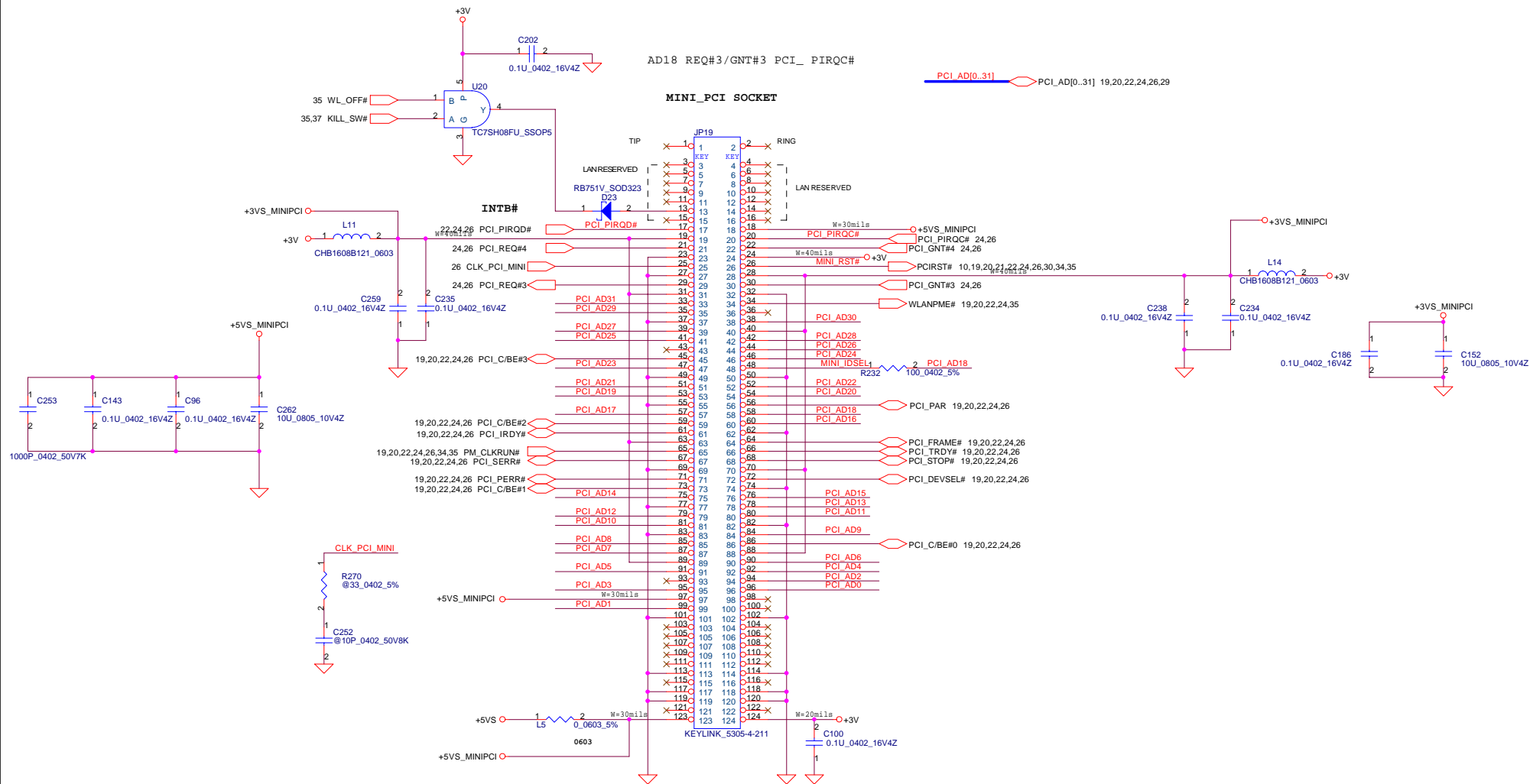
Compal Electronics, Ltd.

RJ11/RJ45 Connector

Title	Document Number	Rev
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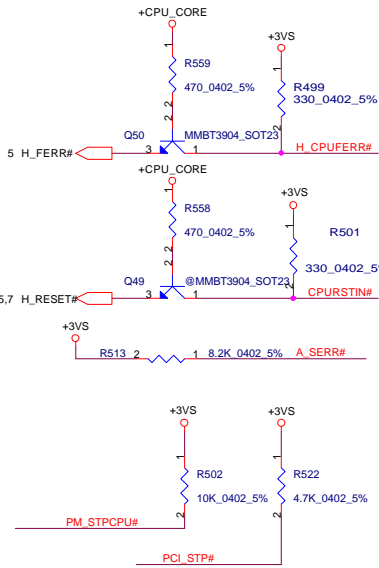




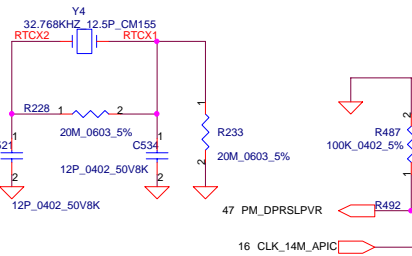
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Compal Electronics, Ltd.			
Title			
Mini PCI Slot			
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9,12 A_AD[0..31] A_AD[0..31]
9,12 A_CBE[0..3] A_CBE[0..3]



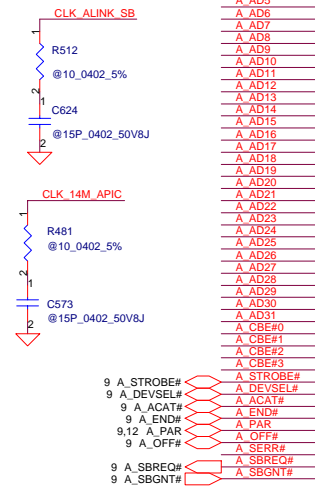
H_INIT# R486 2 200_0402_5%
H_A20M# R402 2 200_0402_5%
H_SLP# R395 2 200_0402_5%
H_INTR# R396 2 200_0402_5%
H_NMI# R400 2 200_0402_5%
H_SMI# R397 2 200_0402_5%
H_STPCLK# R398 2 200_0402_5%
H_IGNNE# R399 2 200_0402_5%



H_SLP# C707 2 1 180P_0603_50V8J
H_SMI# C708 2 1 180P_0603_50V8J
H_STPCLK# C709 2 1 180P_0603_50V8J
H_IGNNE# C710 2 1 180P_0603_50V8J
H_A20M# C406 2 1 180P_0603_50V8J
H_INTR# C402 2 1 180P_0603_50V8J
H_NMI# C403 2 1 180P_0603_50V8J
H_NMI# C405 2 1 180P_0603_50V8J

PLACE CLOSE TO CPU SOCKET

16 CLK_ALINK_SB CLK_ALINK_SB
R508 2 2K_0402_5% NBRST#
PULL DOWN FOR S3



9 A_STROBE# A_STROBE#
9 A_DEVSEL# A_DEVSEL#
9 A_ACAT# A_ACAT#
9 A_END# A_END#
9 A_PAR# A_PAR#
9 A_OFF# A_OFF#
9 A_SERR# A_SERR#
9 A_SBGNT# A_SBGNT#
5,10,16,47 PM_STPCPU# N200
16 PCI_STP# R233

RTXC1 AC12 X1

RTXC2 AC11 X2

CPURSTIN# B18C

CPU_PWRGD B17

INTR/LINT0 B16

INTR/LINT1 C17

SMI# C16

SLP# E19

H_A20M# D18C

H_IGNNE# D17C

H_A20M# E19C

H_CPUPERR# F18C

H_STPCLK# E17C

GPIO0 E17C

SSMUXSEL/GPIO0 E18

DPRSLPVR C19

APIC_D0 C19

APIC_D1 C18

APIC_CLK B19

APIC_CLK B19

APIC_CLK B19

APIC_CLK B19

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APIC_CLK B19

APIC_CLK B19

U23A

SB200 SB

Part 1 of 3

PCI CLK#

PCI CLK#

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Layout note:

Trace length of PCI_CLK_R + PCI_CLK_FB should be less than 200 mils.

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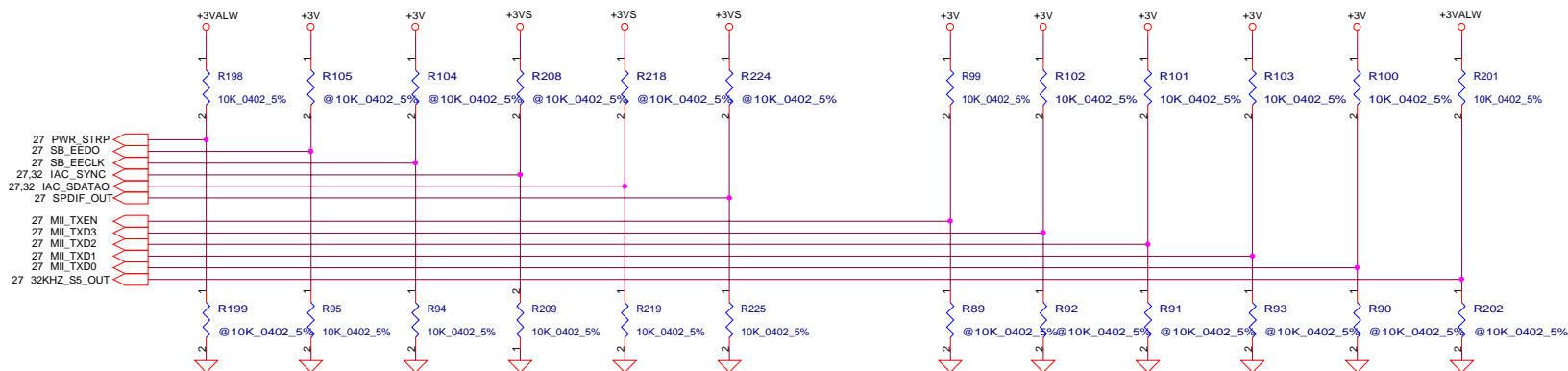
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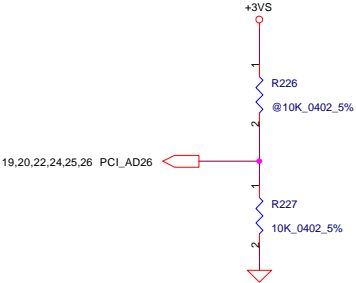
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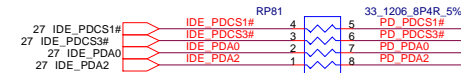
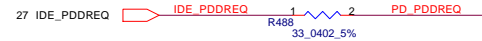
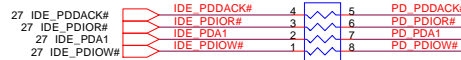
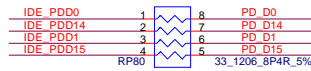
REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)

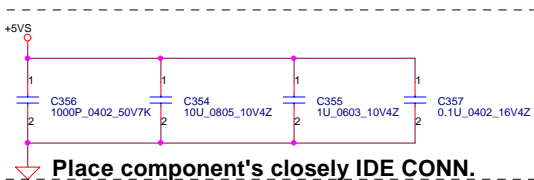
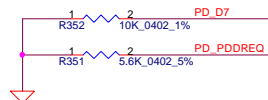
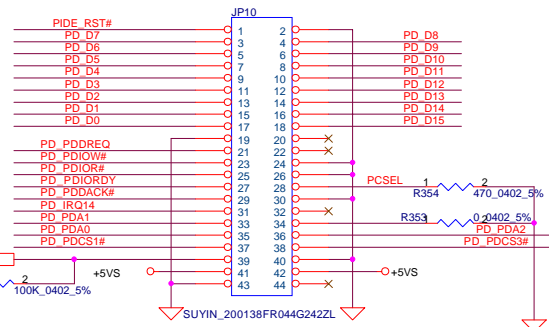


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27 IDE_PDD[0..15] IDE_PDD[0..15]

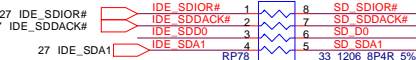
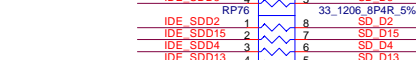
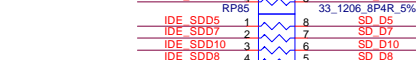
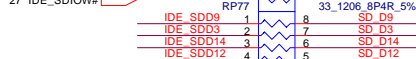
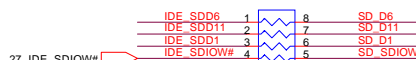
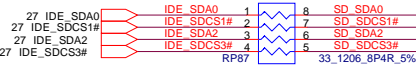


IDE Module CONN.

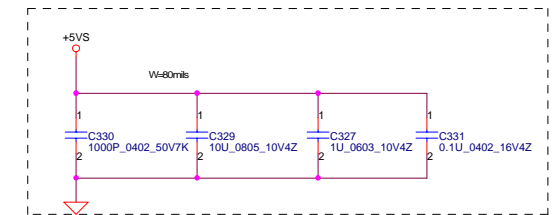
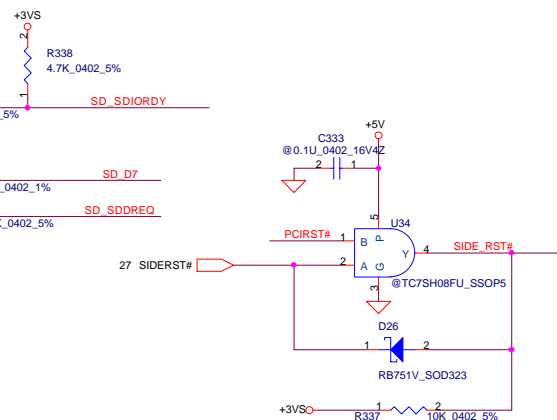
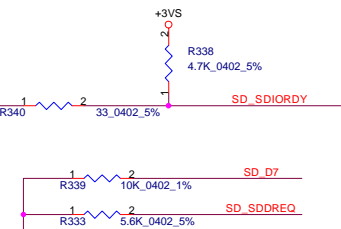
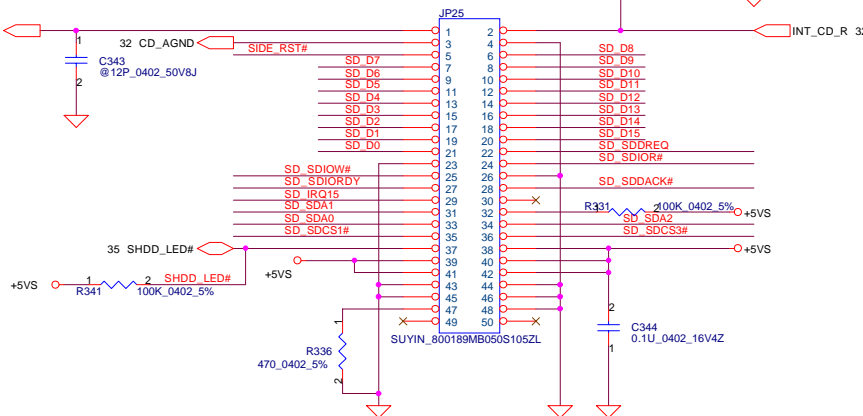


Place component's closely IDE CONN.

27 IDE_SDD[0..15] IDE_SDD[0..15]



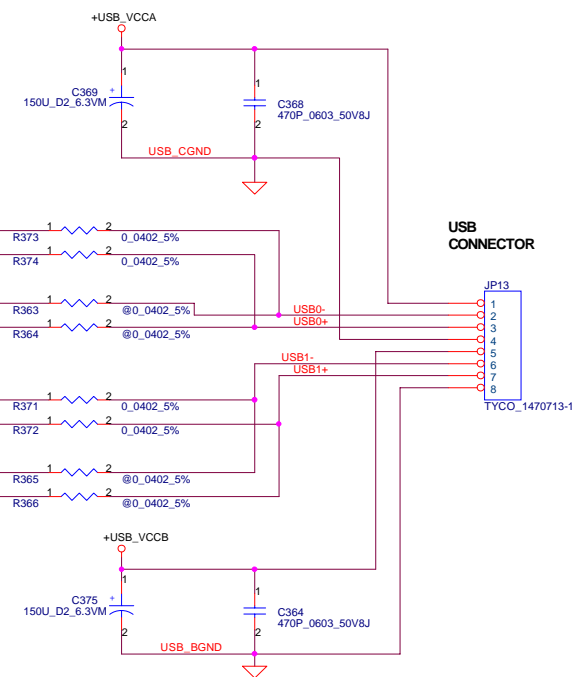
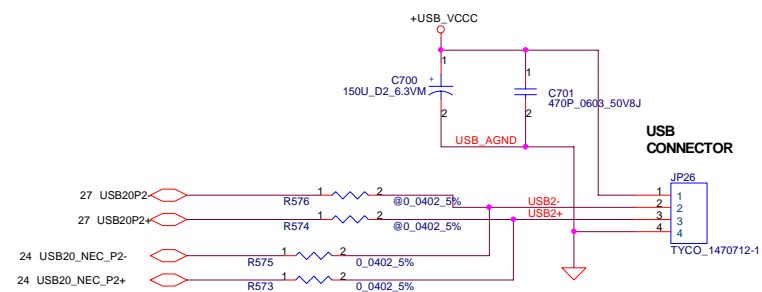
CD-ROM Module CONN.



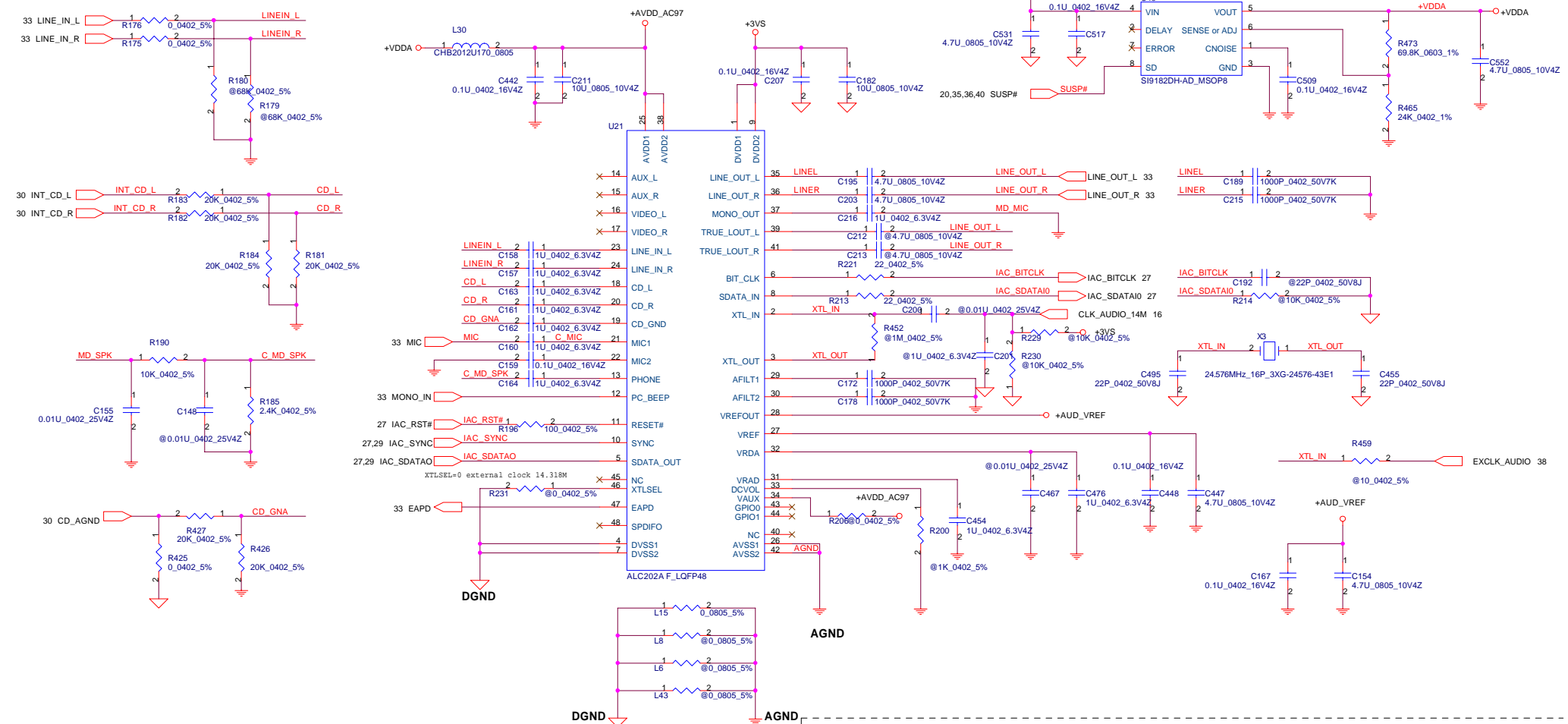
Place component's closely CD-ROM CONN.

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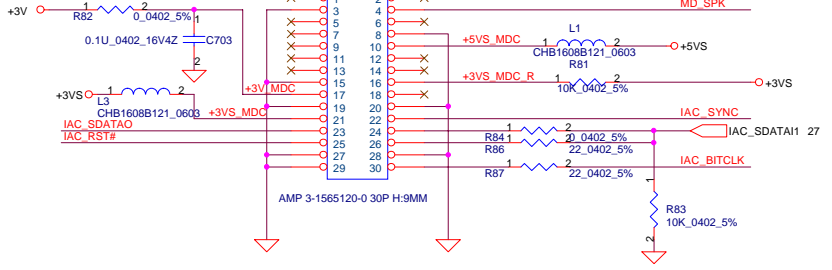
Compal Electronics, Ltd.			
Title			
IDE & CD-ROM Connector			
Size	Document Number	Rev	
Customer	LA-2051	0.1A	
Date	星期三, 八月 27, 2003	Sheet	30 of 51

[illegible]

AC97 Codec



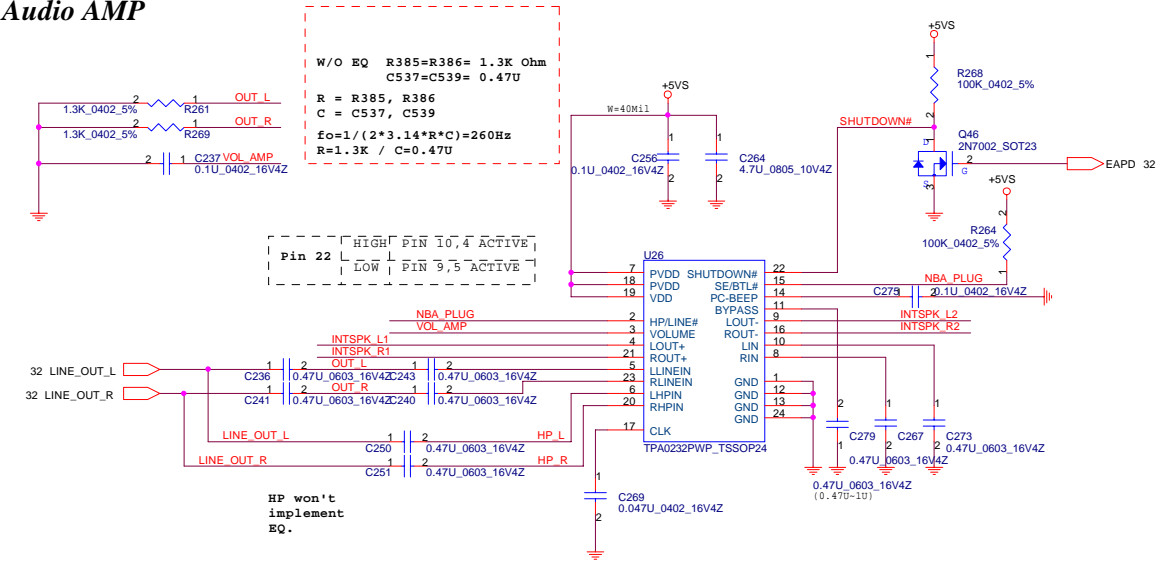
MDC Connector



Compal Electronics, Ltd.			
AC97 Codec ALC202			
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Size	LA-2051	0.1A	
Date	星期三, 八月 27, 2003	Sheet	32 of 51

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Audio AMP

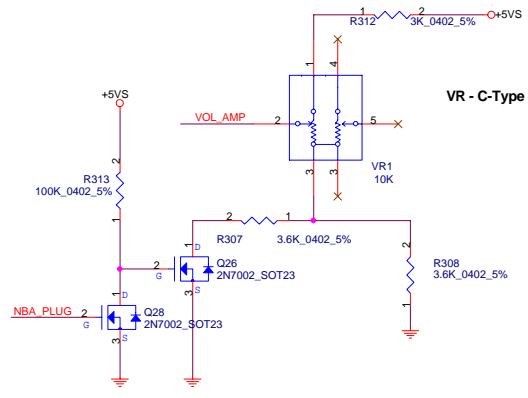


W/O EQ R385=R386= 1.3K Ohm
C537=C539= 0.47U
R = R385, R386
C = C537, C539
 $f_o = 1 / (2 * 3.14 * R * C) = 260\text{Hz}$
R=1.3K / C=0.47U

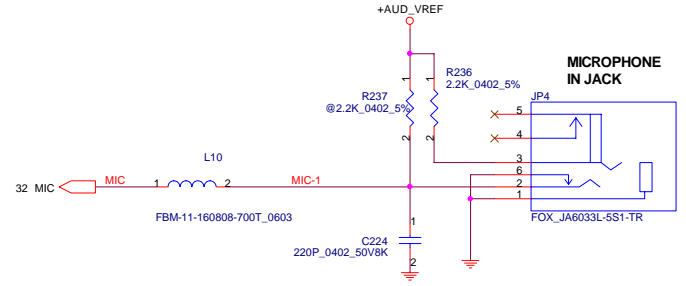
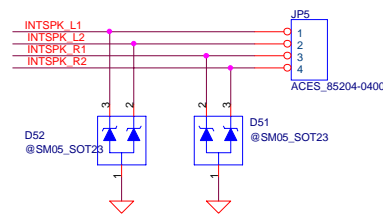
Pin 22 HIGH PIN 10,4 ACTIVE
Pin 22 LOW PIN 9,5 ACTIVE

HP won't implement EQ.

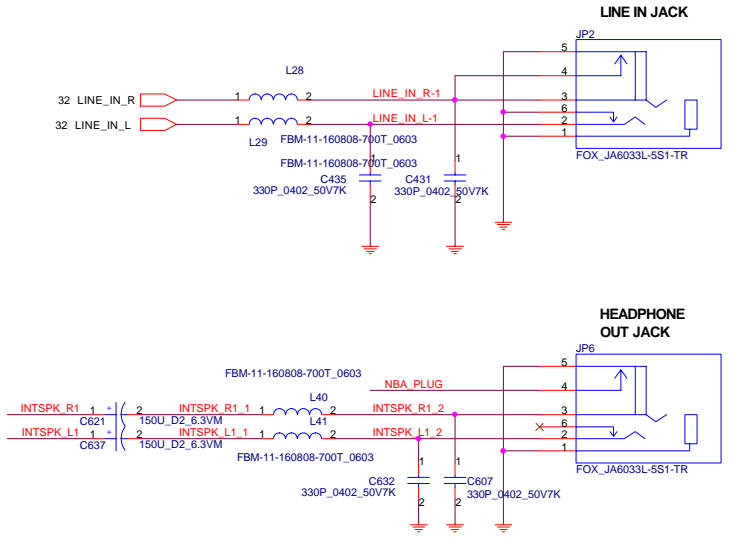
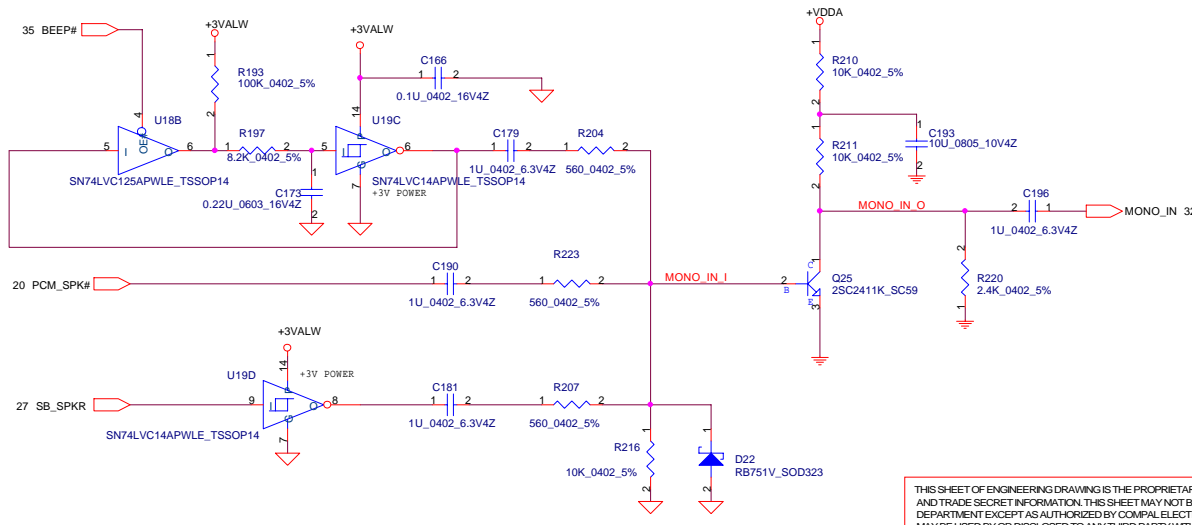
	W/O EQ	
R513	3K	
R307	3.6K	
R308	3.6K	
Bias (Gain)	SPK 0.608 V 12 dB HP 1.216V 0dB	



Speaker Connector



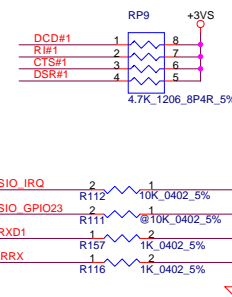
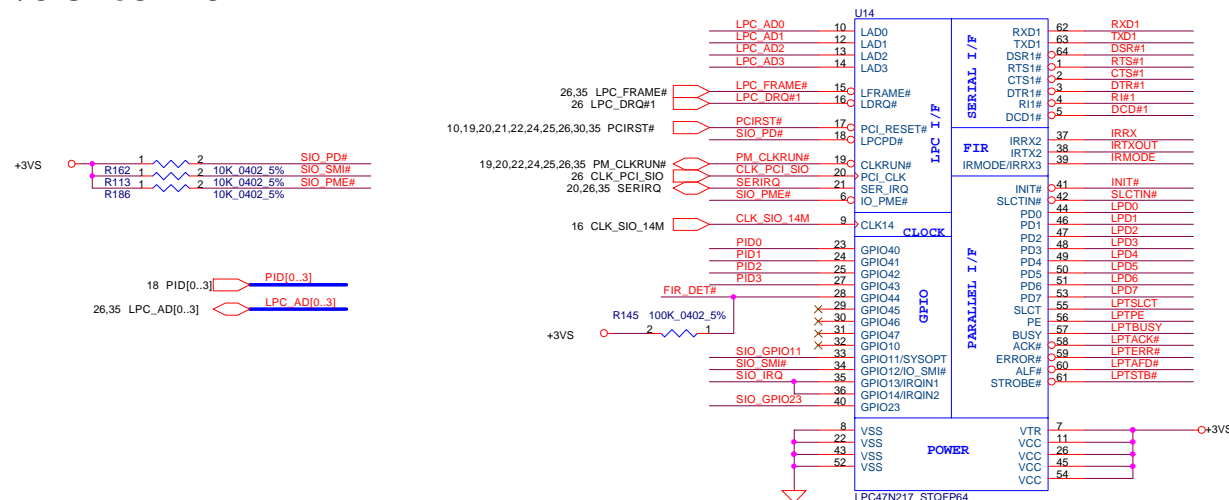
System Sound



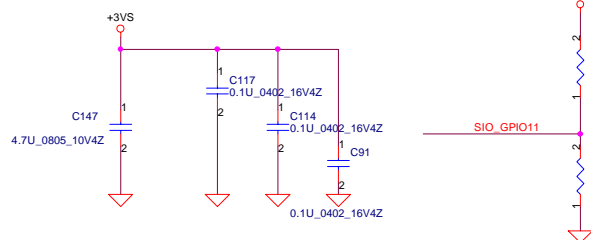
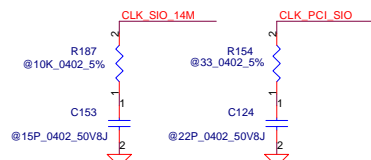
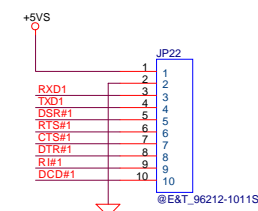
Compal Electronics, Ltd.			
Title Audio AMP & JACK			
Size	Document Number	Rev	
Custom	LA-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	33 of 51

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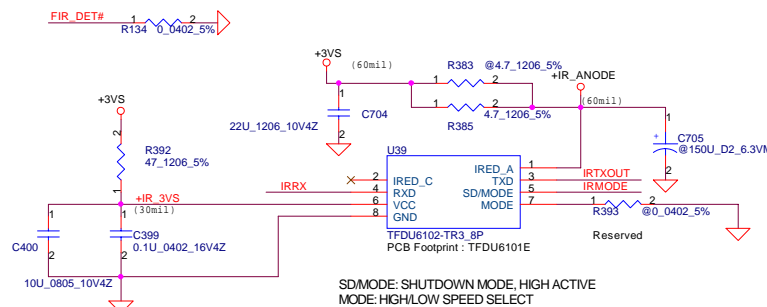
SUPER I/O SMsC LPC47N217



Serial Port for Debug



FIR Module



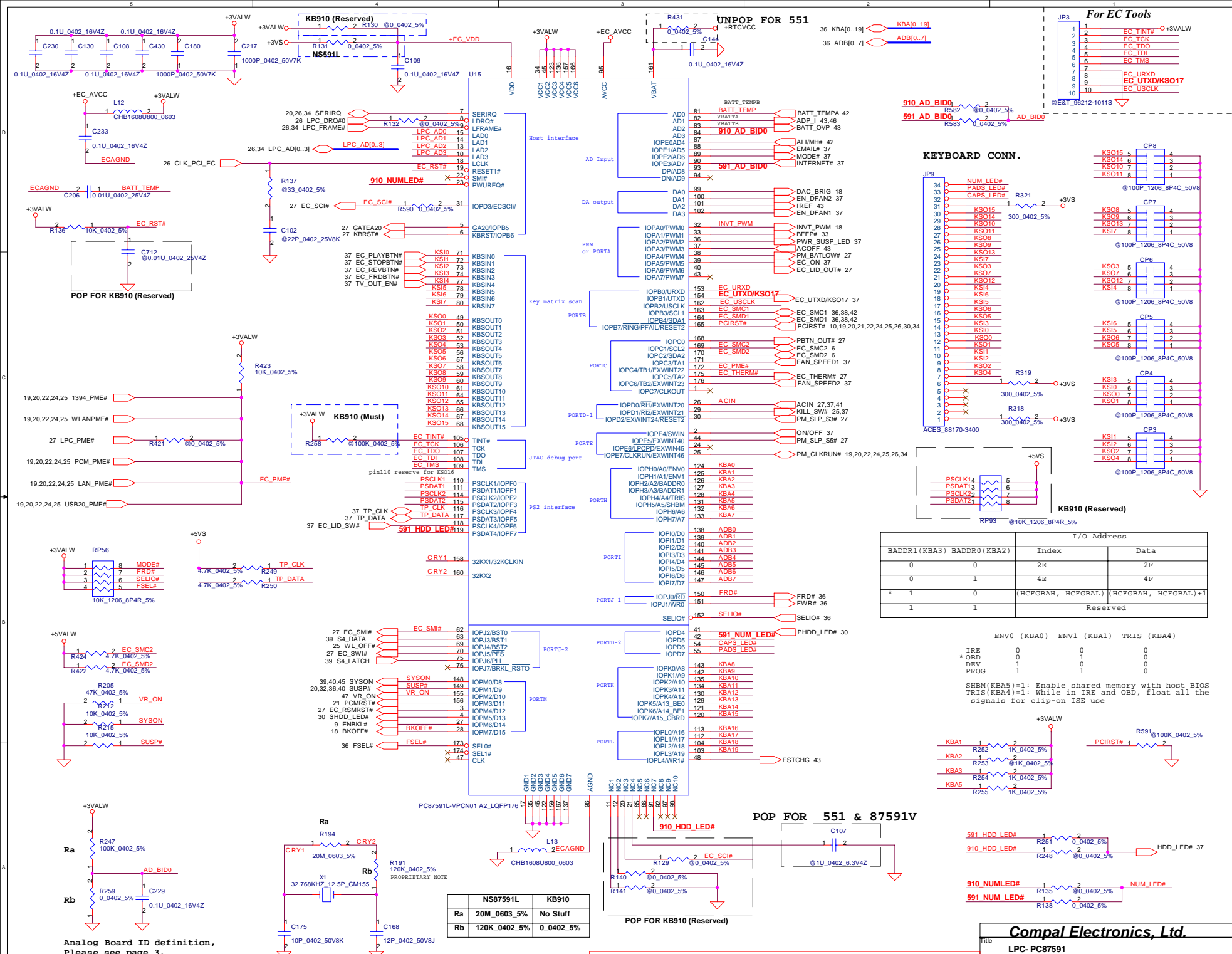
Compal Electronics, Ltd.

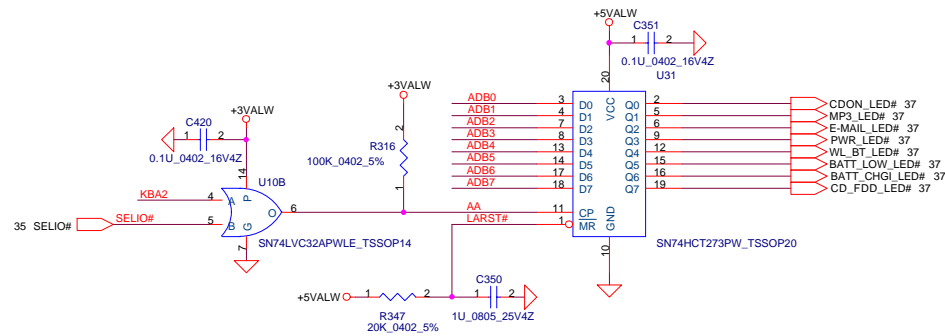
LPC-Super I/O

Size	Document Number	Rev
Custom	A-2051	0.1A

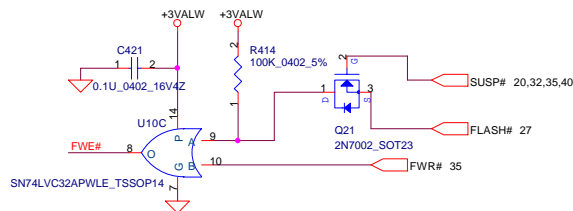
Date: 星期四, 八月 28, 2003 Sheet 34 of 51

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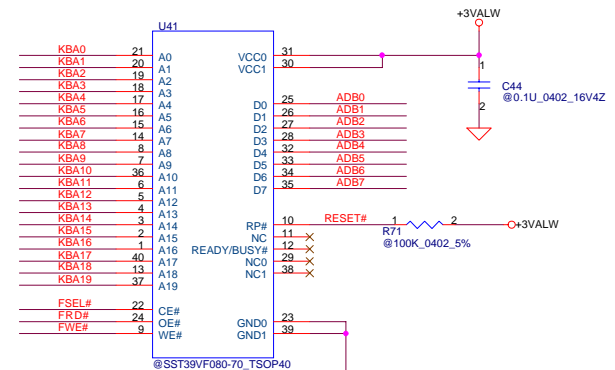
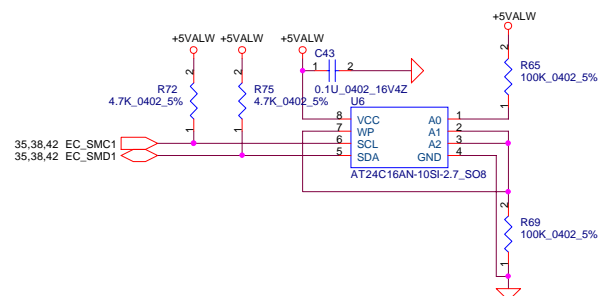
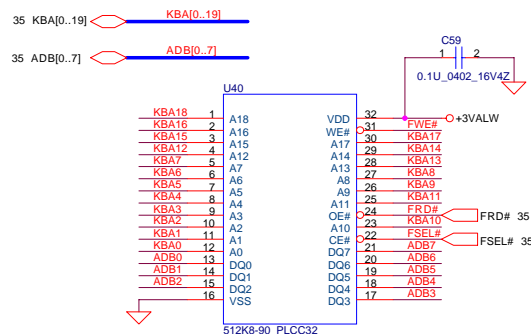




System BIOS



SMBus EEPROM

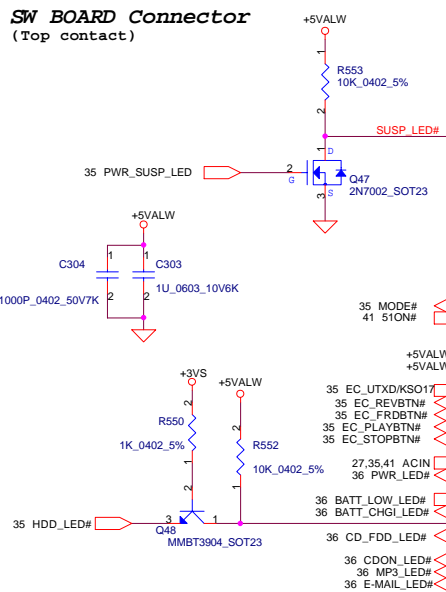


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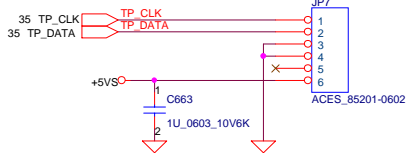
Compal Electronics, Ltd.

Title		
BIOS & Ext.I/O		
Size	Document Number	Rev
Cusor	LA-2051	0.1A
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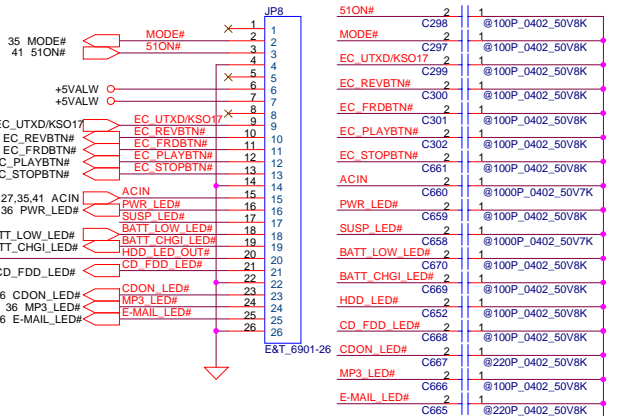
SW BOARD Connector (Top contact)



Touch Pad Connector



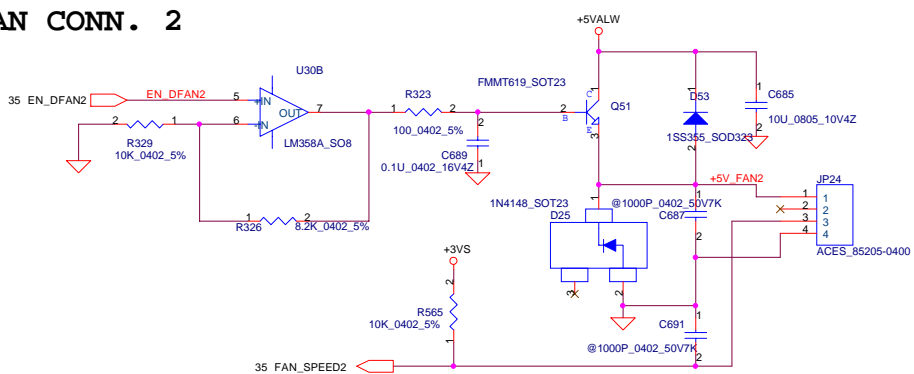
PLACE CLOSE TO JP8



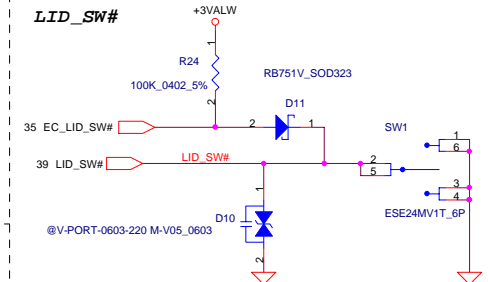
For EMI

FAN CONN. 1

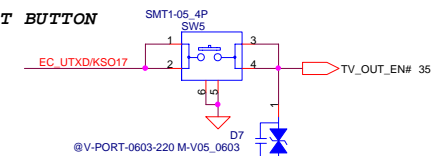
FAN CONN. 2



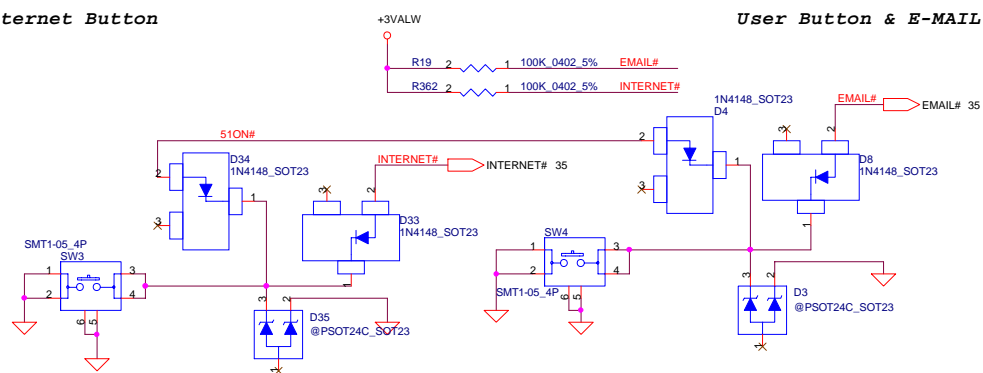
LID_SW#



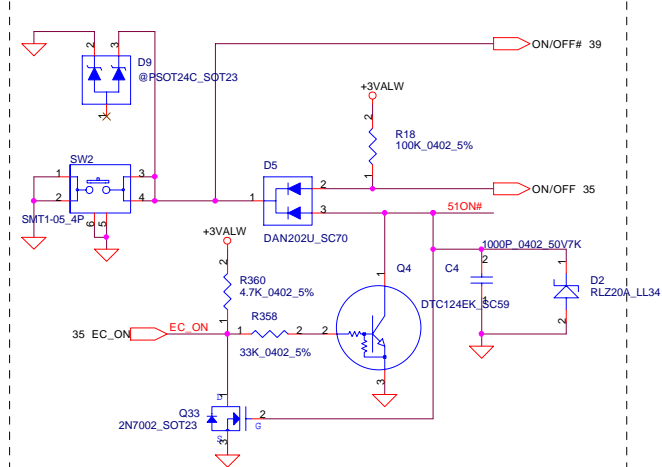
TV-OUT BUTTON



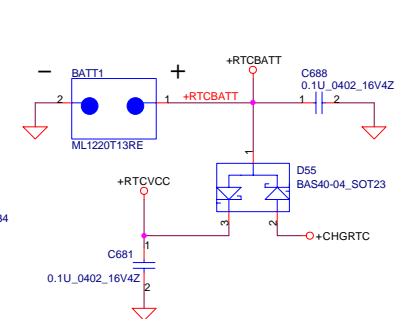
Internet Button



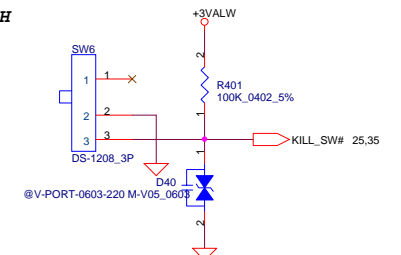
Power Button



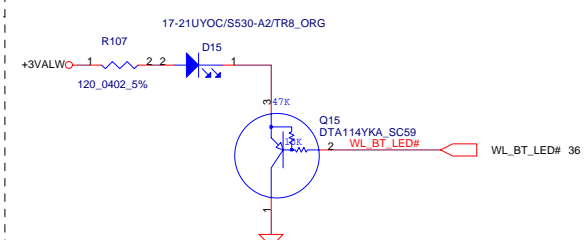
RTC BATT



Kill SWITCH



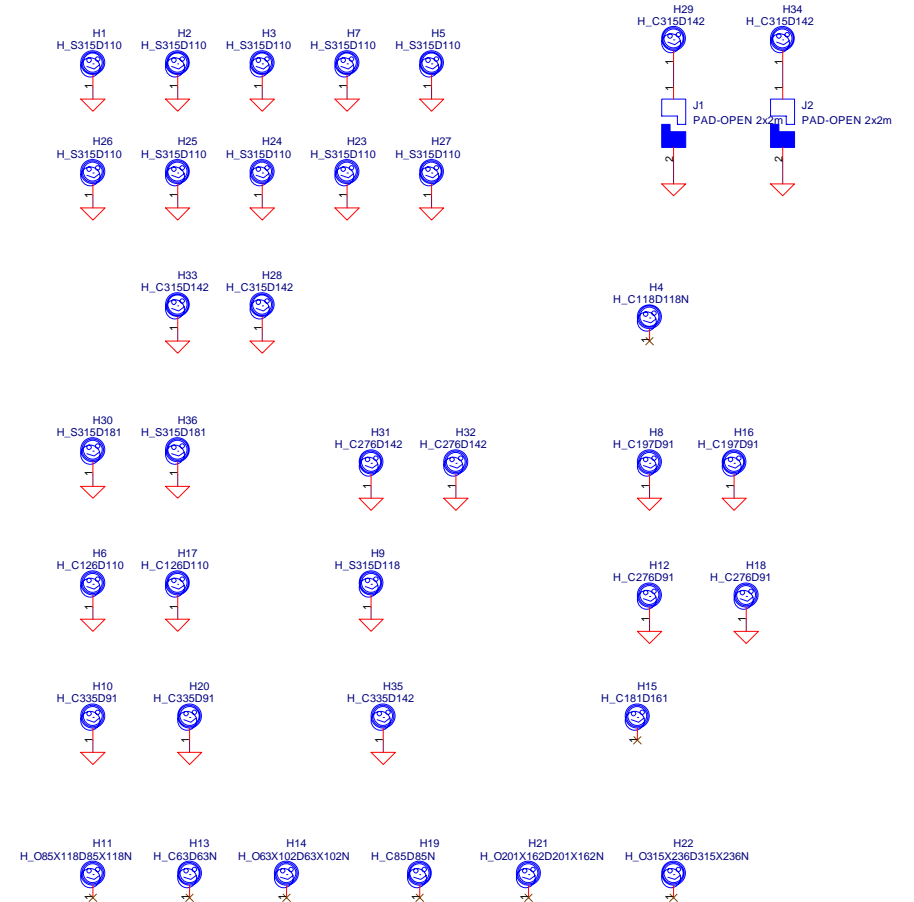
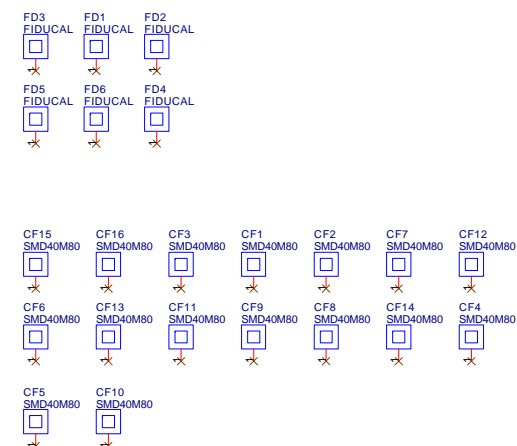
WIRELESS ACTIVE AMB LED

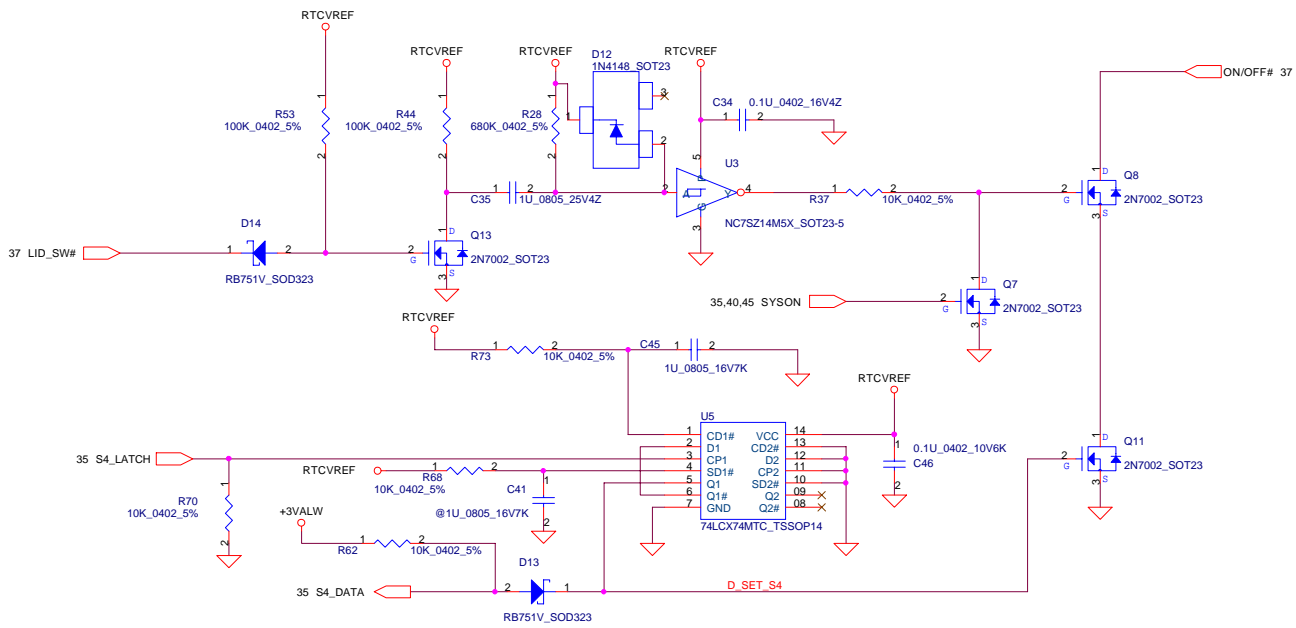


User Button & E-MAIL SW

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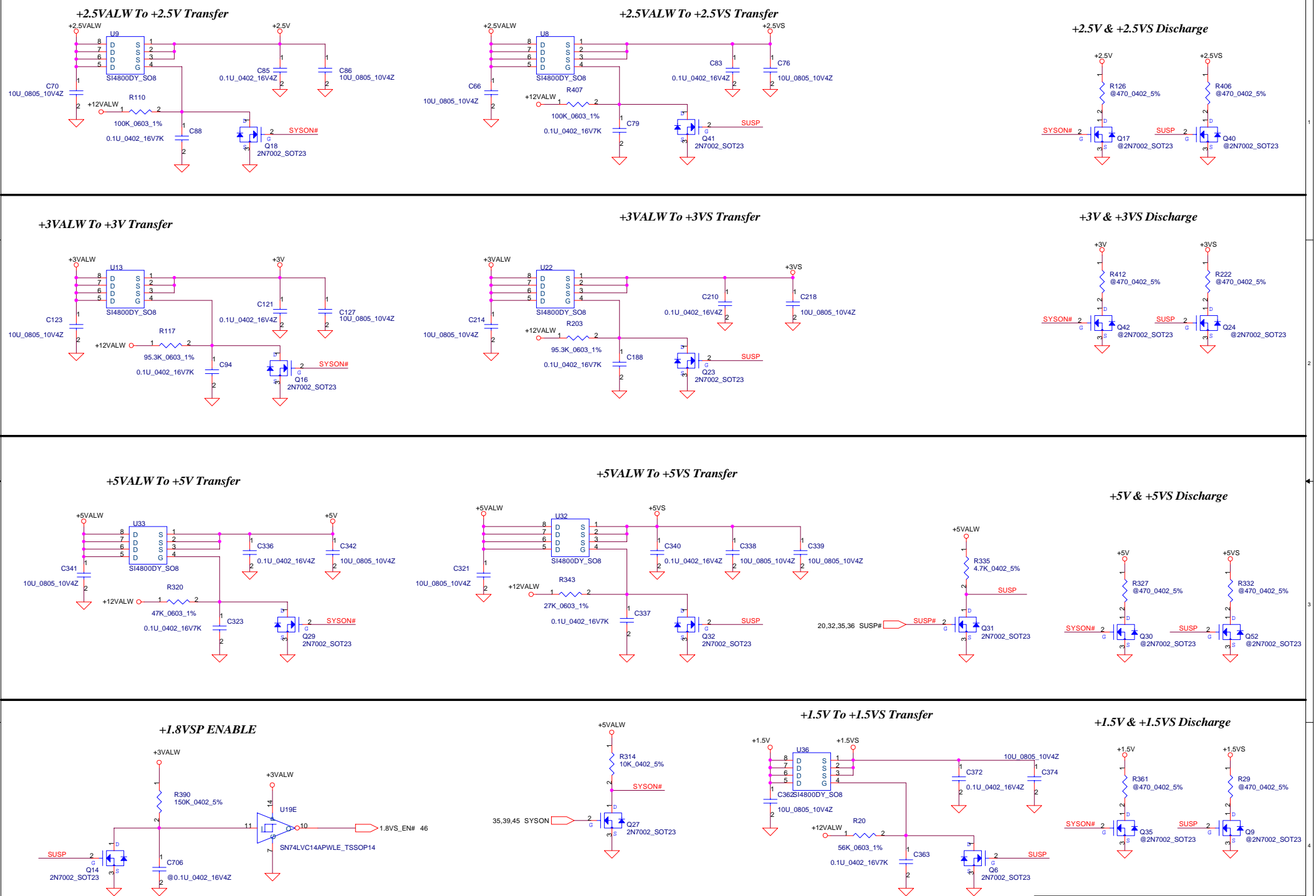
Compalelectronics, Ltd.			
System Connectors			
Title	Document Number	Rev	
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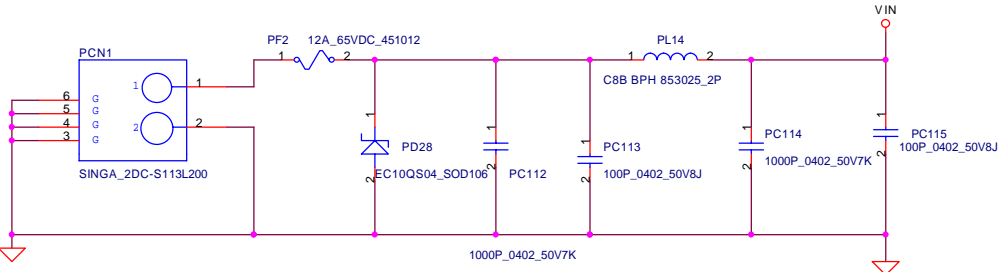
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Title			
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Size	Document Number		Rev
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Date:	星期三, 八月 27, 2003		Sheet 39 of 51

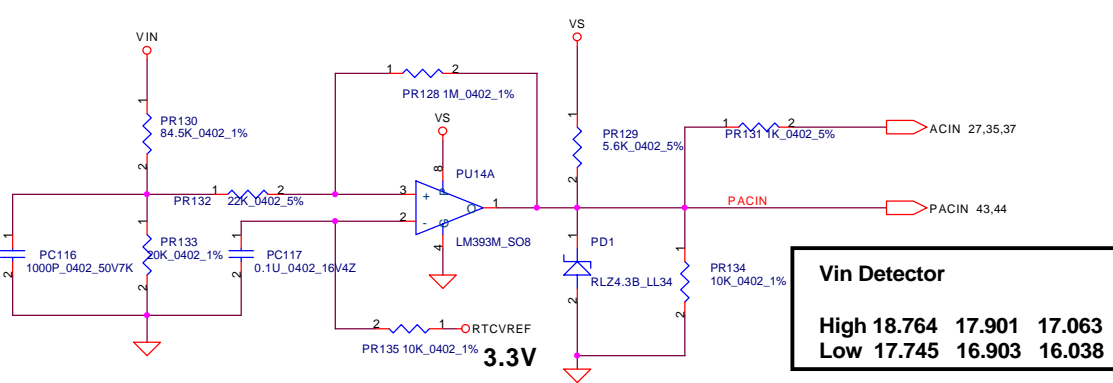


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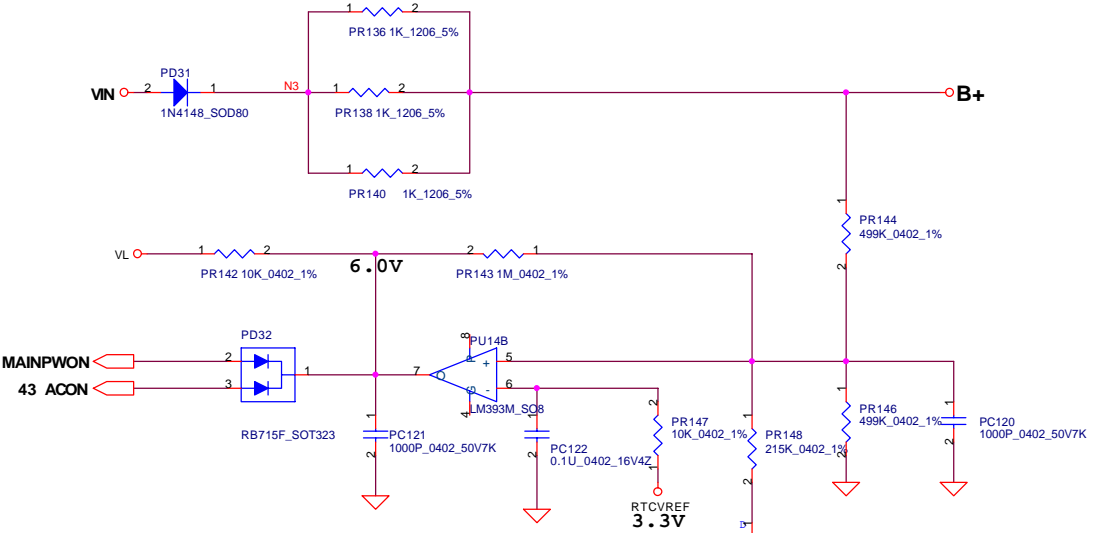
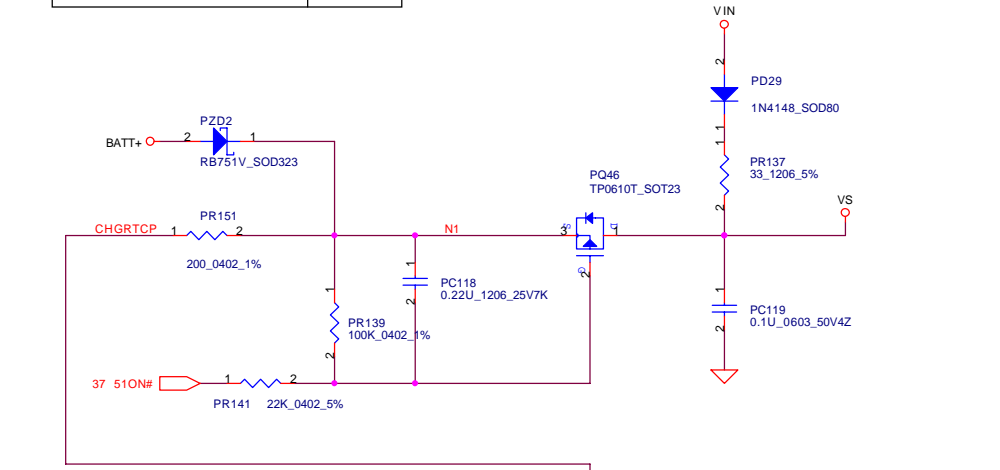
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DC/DC Interface			
Size	Document Number	Rev	
Custom	LA-2051	0.1A	
Date:	星期三, 八月 27, 2003	Sheet	40 of 51



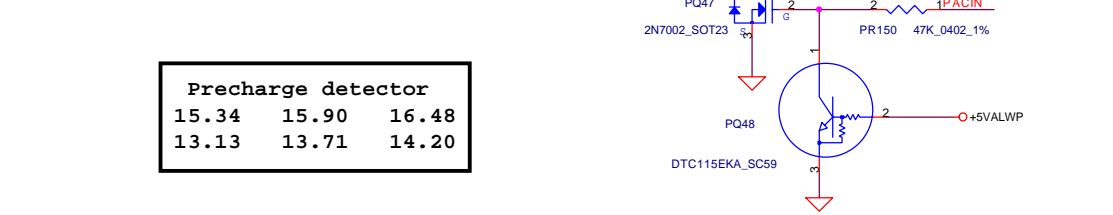
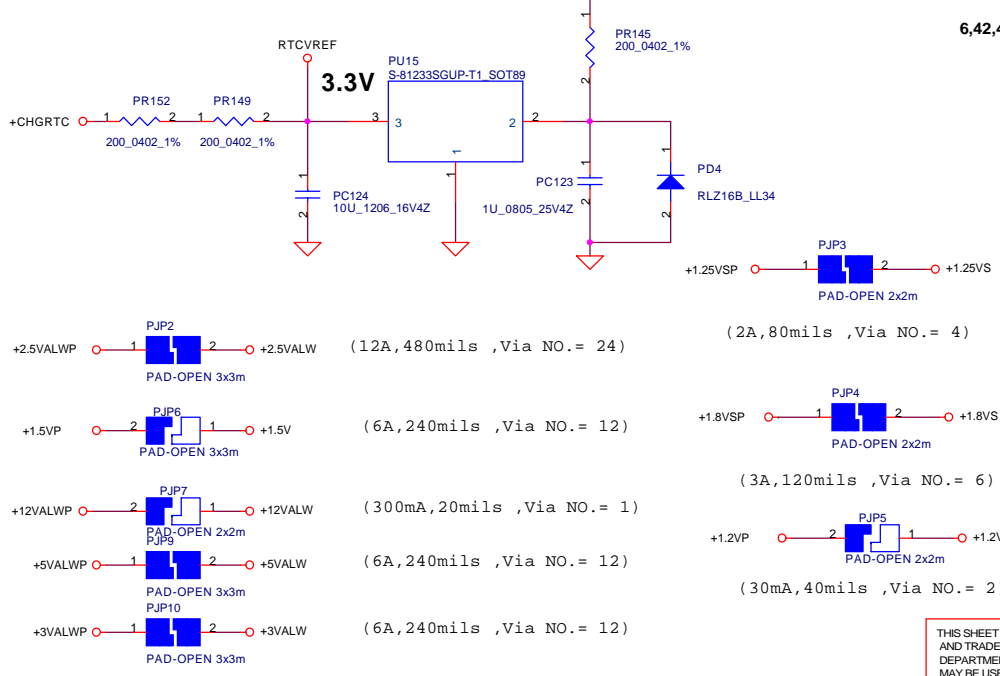
SINGA_2DC-S133L200	120W
SINGA_2DC-S726B201	90W



Vin Detector			
High	18.764	17.901	17.063
Low	17.745	16.903	16.038

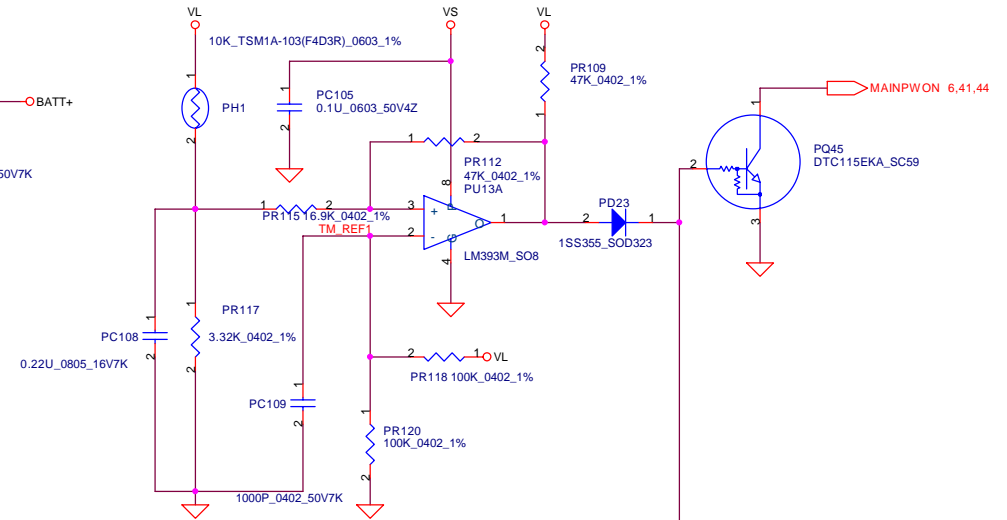


Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20

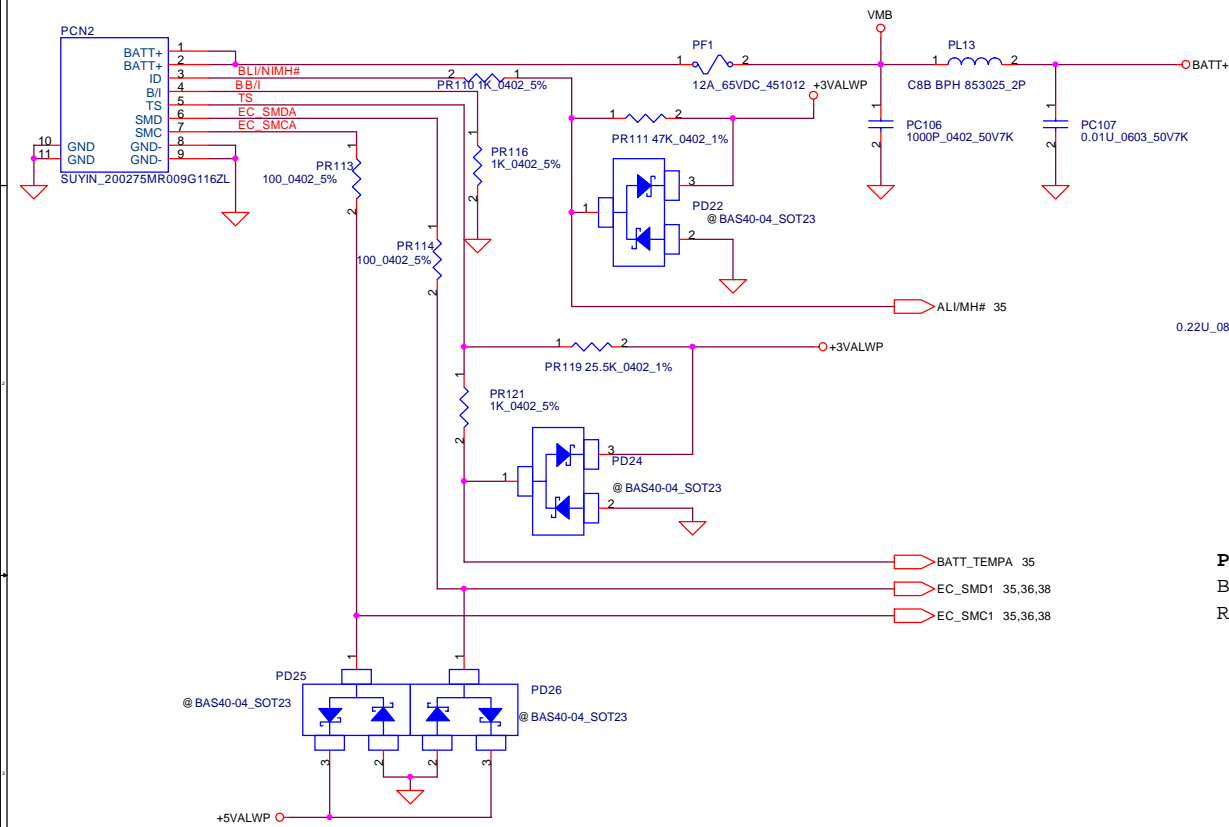
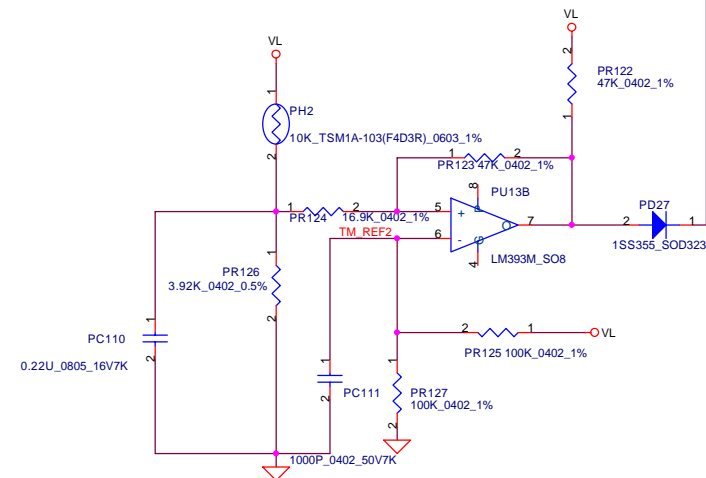


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PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 44(45) degree C



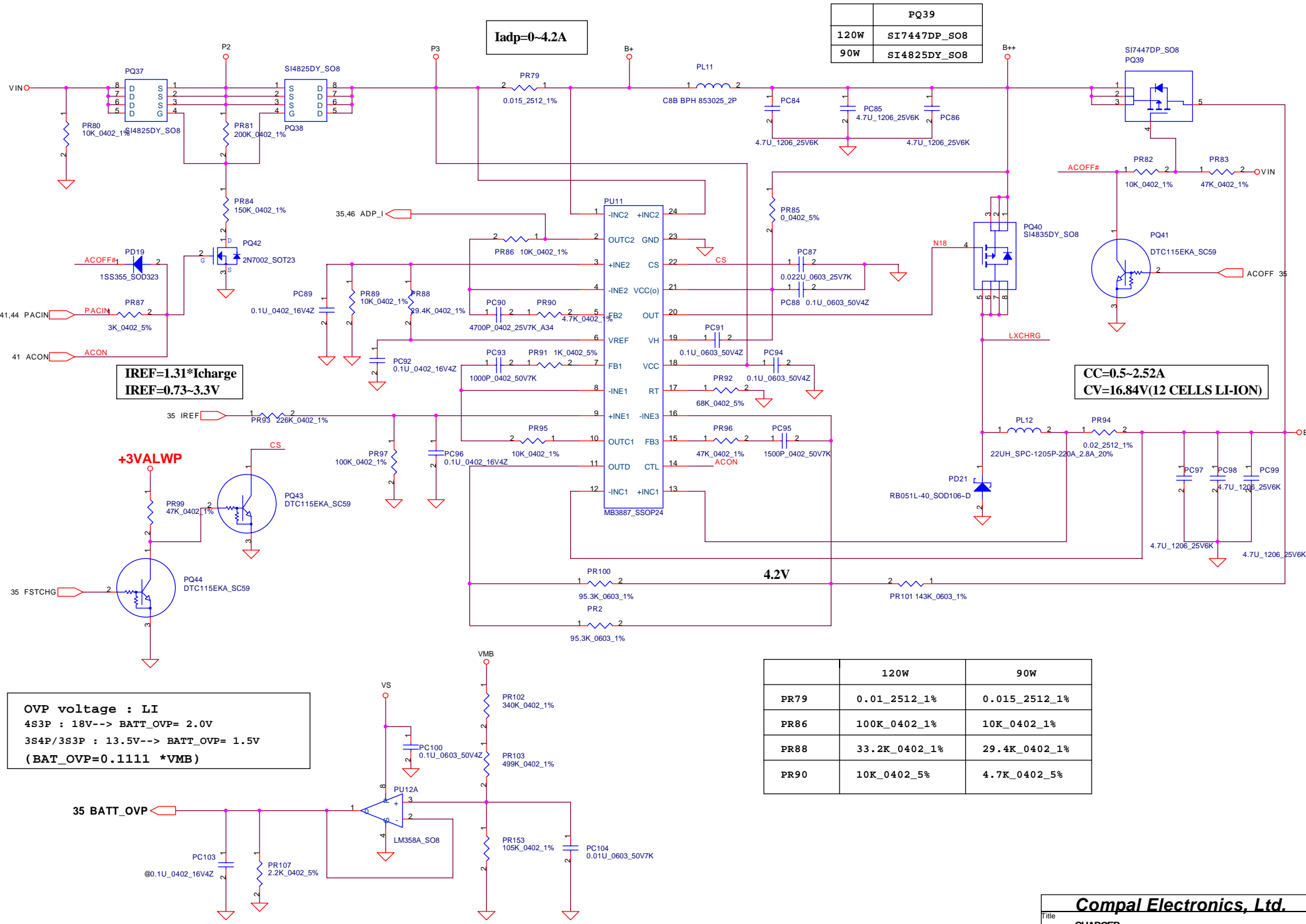
PH2 near main Battery CONN :
 BAT. thermal protection at 78 degree C
 Recovery at 39(40) degree C



Compal Electronics, Ltd.

Title		BATTERY CONN / OTP	
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Iadp=0-4.2A

	PQ39
120W	SI7447DP_SO8
90W	SI4825DY_SO8

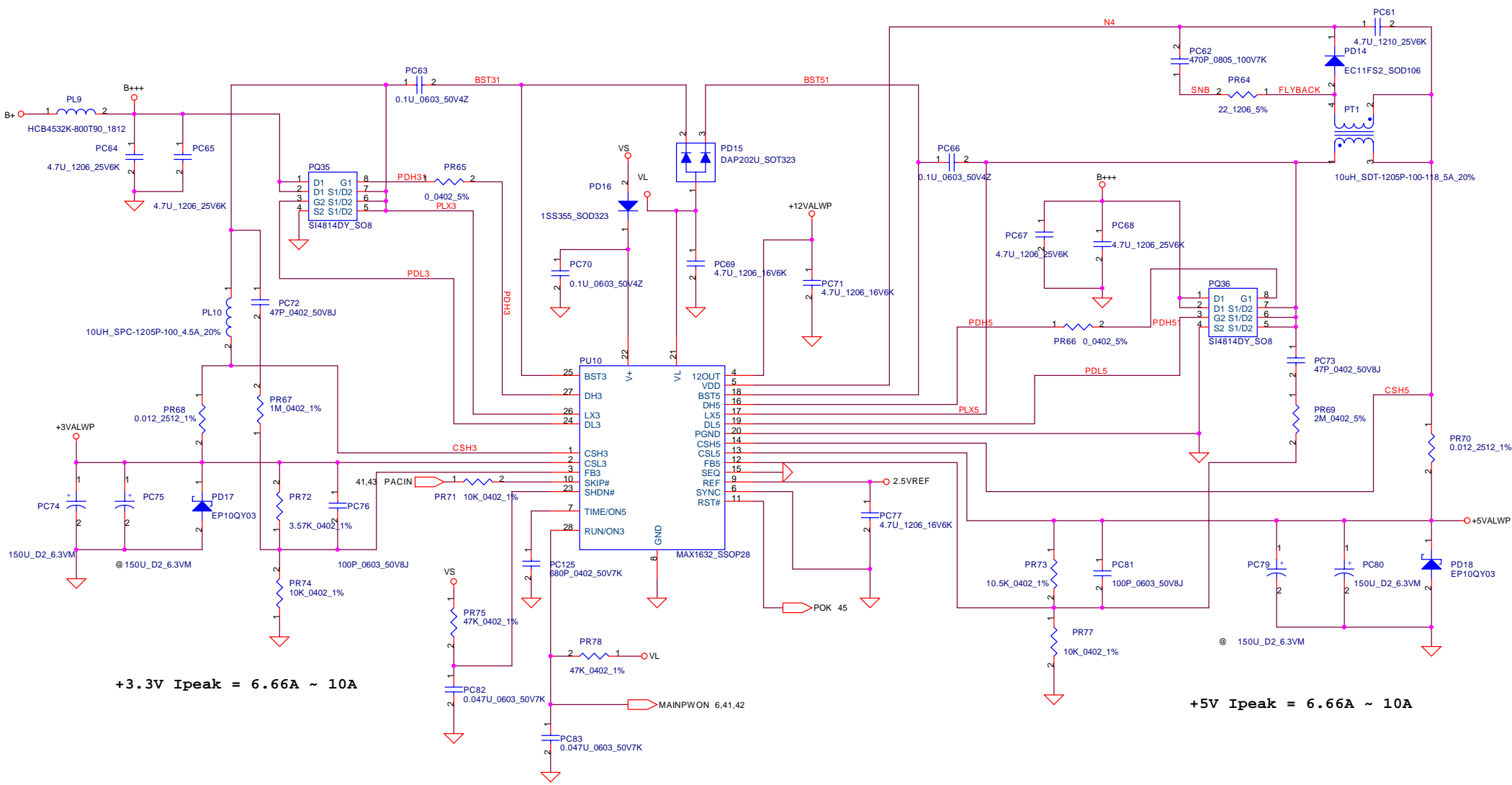
CC=0.5-2.52A
CV=16.84V(12 CELLS LI-ION)

IREF=1.31*Icharge
IREF=0.73~3.3V

OVP voltage : LI
4S3P : 18V--> BATT_OVP= 2.0V
3S4P/3S3P : 13.5V--> BATT_OVP= 1.5V
(BATT_OVP=0.1111 *VMB)

	120W	90W
PR79	0.01_2512_1%	0.015_2512_1%
PR86	100K_0402_1%	10K_0402_1%
PR88	33.2K_0402_1%	29.4K_0402_1%
PR90	10K_0402_5%	4.7K_0402_5%

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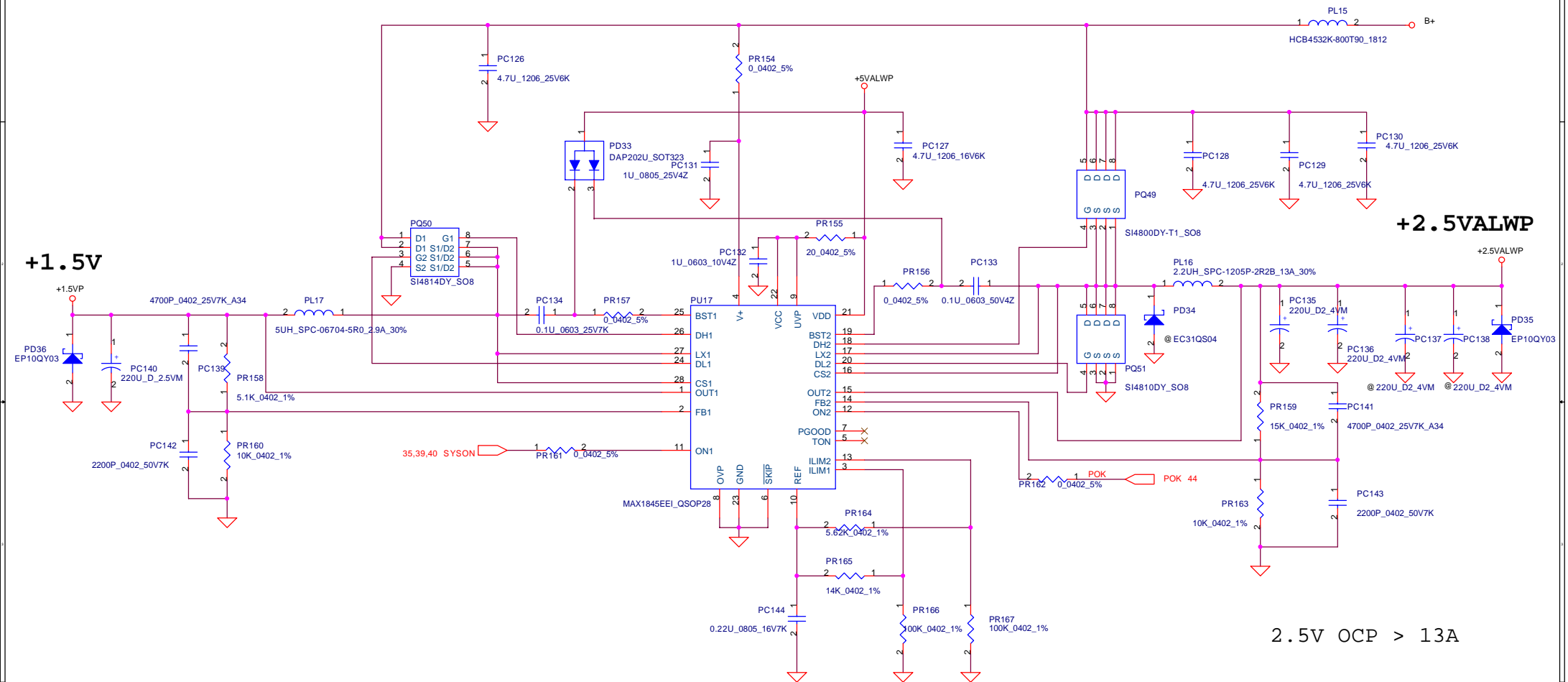
+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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5V/3V/12V			
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+2.5VALWP/+1.5VP



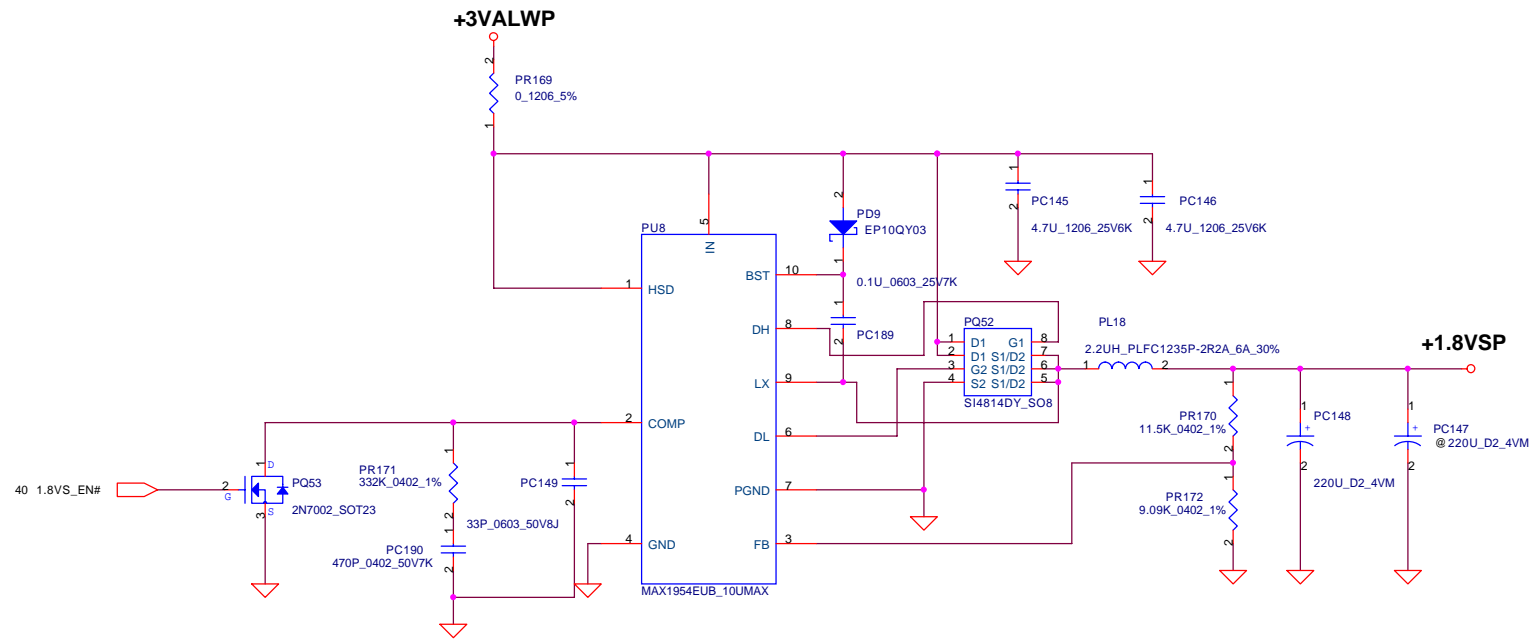
2.5V OCP > 13A

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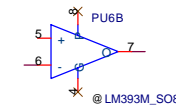
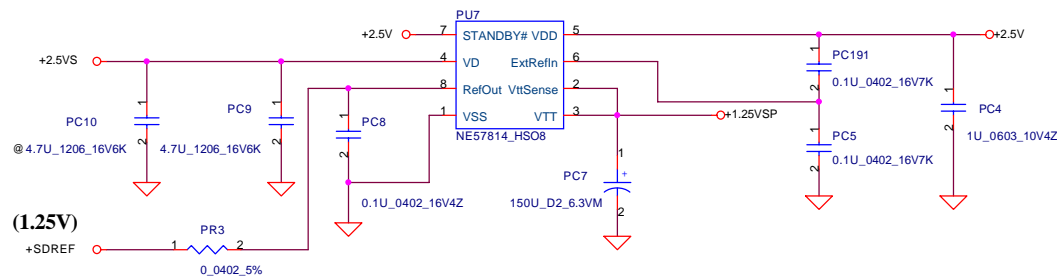
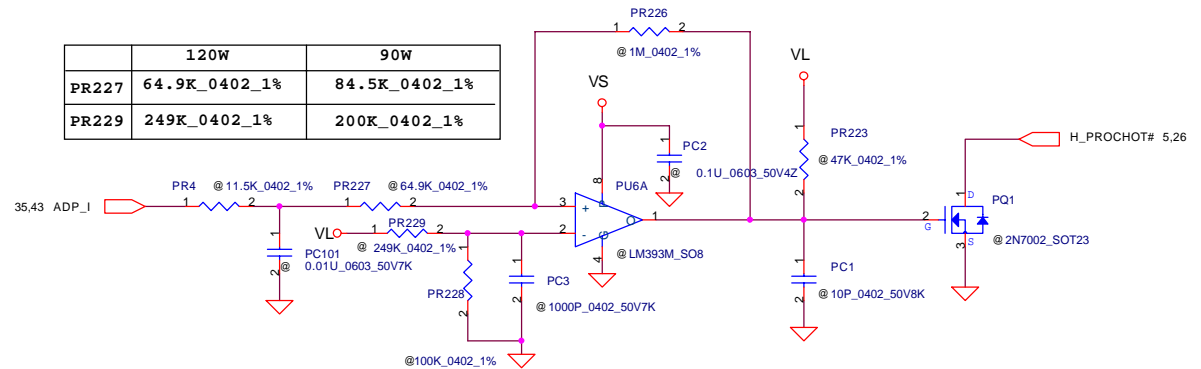
+2.5VALWP/1.5VP

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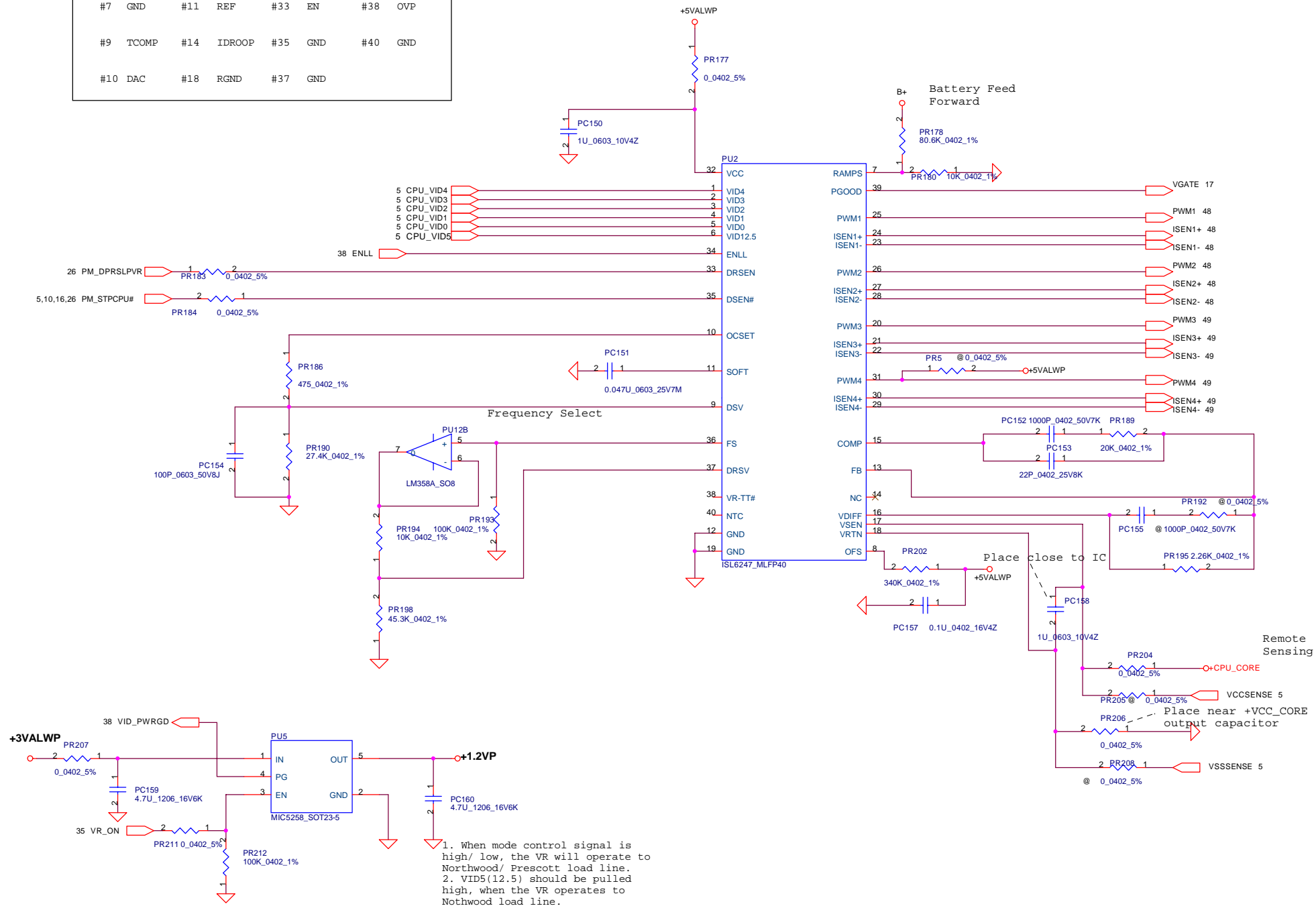
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	120W	90W
PR227	64.9K_0402_1%	84.5K_0402_1%
PR229	249K_0402_1%	200K_0402_1%



#7	GND	#11	REF	#33	EN	#38	OVP
#9	TCOMP	#14	IDROOP	#35	GND	#40	GND
#10	DAC	#18	RGND	#37	GND		



BOOTSELECT=1 PRESCOTT

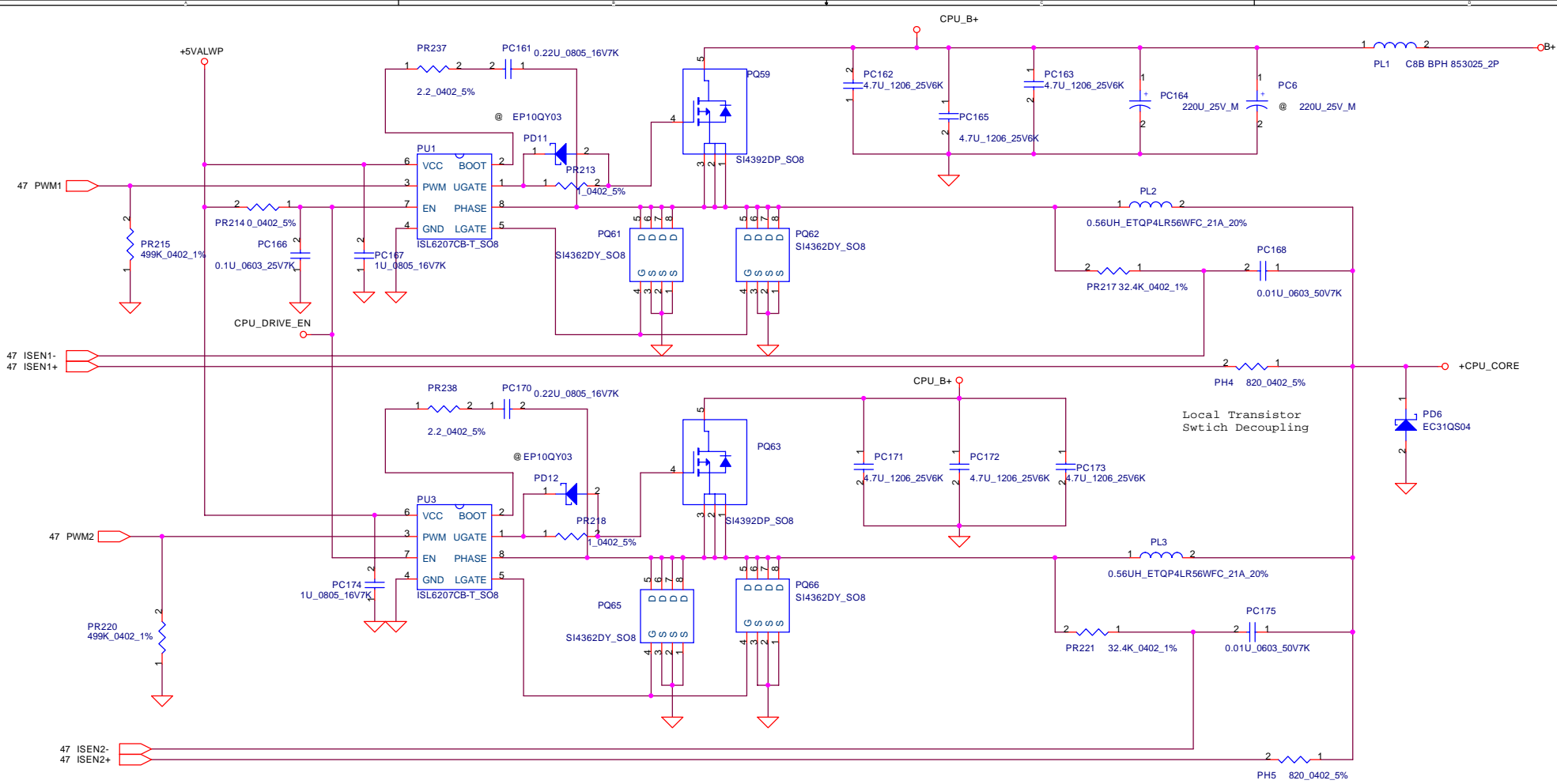
BOOTSELECT=0 NORTHWOOD

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CPU_CORE_ControllerSize
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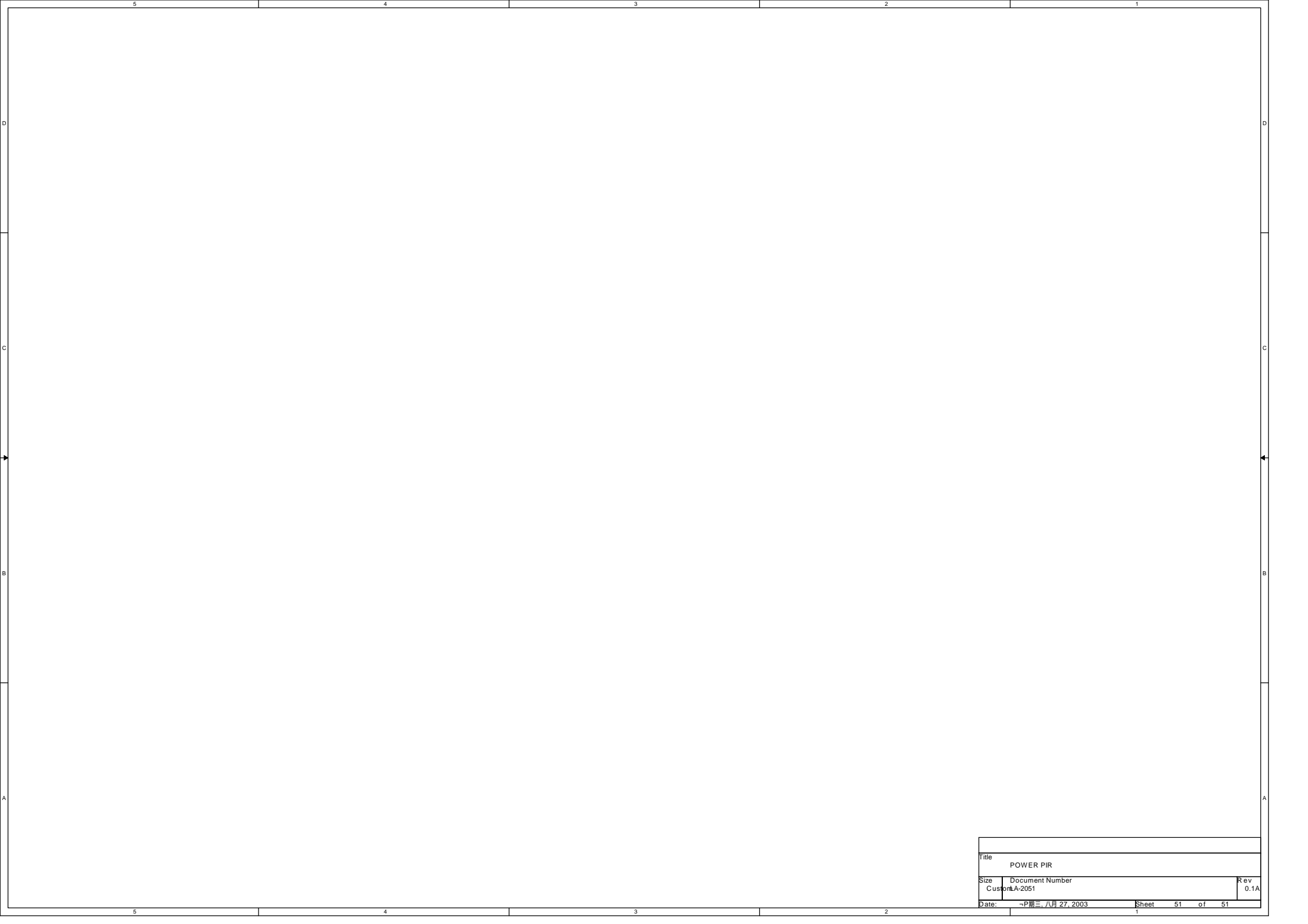
CPU_CORE Power stage

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