ENGIN112: Introduction to Electrical and Computer Engineering
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Understanding Sequential Circuit Timing

Perhaps the two most distinguishing characteristics of a computer are its processor clock speed and the size of its main memory. While it is relatively easy to understand the concept of main memory size (the number of storage bits in the computer), the concept of processor clock speed is a little more difficult to grasp. In this document we will explain what is meant by sequential circuit clock speed, and more importantly, how to calculate it using the timing parameters of combinational and sequential circuit components.

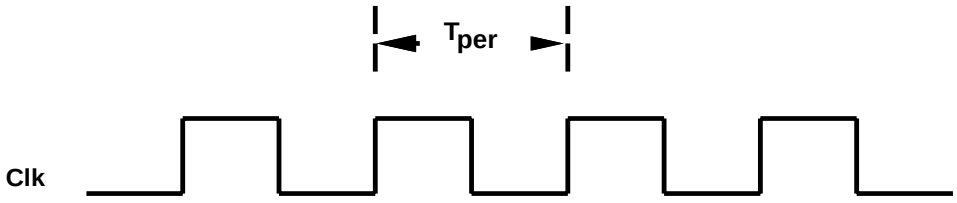

Figure 1: Periodic Clock Signal

As we have discussed this term, edge-trigged flip flops, such as the D flip flop, are controlled by a clock signal, such as the signal labeled Clk in Figure 1. A clock signal is a periodic square wave which alternates between logic high (1) and logic low (0) values at predictable times. The amount of time between rising clock edges is called the **clock period**, T_{per}, of the clock. In modern computers the clock period is usually under 10 nanoseconds (10 ns). The inverse of the clock period ($\frac{1}{T_{per}}$) is the **clock frequency**, f. Since the clock is used as the control input to edge-triggered flip flops, the clock frequency measures how often the data is transfered, or *clocked*, into edge-triggered flip flops. A bigger clock frequency indicates that data is being stored more quickly, and the sequential circuit is generating results at a faster rate. Typical clock frequencies for modern computer systems range from 1 megaHertz (MHz) to around 5 gigaHertz (GHz).

1 Timing Parameters for Combinational Logic

When implemented physically, combinational circuits, such as AND and OR gates, exhibit certain timing characteristics. When a binary value (0 or 1) is applied at the input to a combinational circuit, the change at the circuit output is not instantaneous due to electrical constraints. Circuit input-to-output delay in combinational circuits can be expressed with two parameters, t_{pd} and t_{cd}, defined as follows:

- **Propagation delay (t_{pd})** - This value indicates the amount of time needed for a change in a logic input to result in a **permanent** change at an output. Combinational logic is guaranteed not to show any further output changes in response to an input change **after** t_{pd} time units have passed.

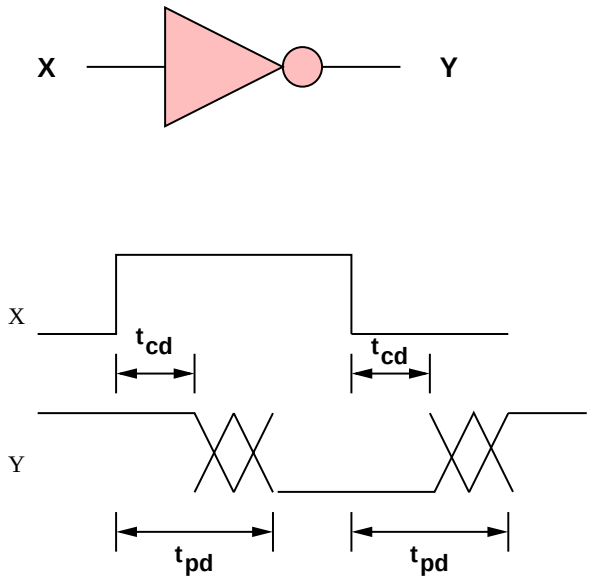

Figure 2: Combinational Propagation and Contamination Delay

- **Contamination delay (t_{cd}) -** This value indicates the amount of time needed for a change in a logic input to result in an **initial** change at an output [1]. Combinational logic is guaranteed not to show any output change in response to an input change **before** t_{cd} time units have passed.

An example of combinational propagation and contamination delay appears in Figure 2. When input X changes, the change in Y is not instantaneous. The inverter output maintains its initial value until time t_{cd} has passed. After this time, the Y output of the inverter may be at an intermediate value for a while (indicated by the cross-hatched area) before the final output value is created. After the propagation delay, t_{pd}, the inverter output is stable and is guaranteed not to change again until another input change.

Combinational propagation delays are additive. It is possible to determine the propagation delay of a larger combinational circuit by adding the propagation delays of the circuit components **along the longest path**. For example, the propagation delay of the **combined circuit** in Figure 3 is 5 ns, since the **longest** delay from a circuit input (w, x, y) to the output z is the sum of the component propagation delays through gates A and B, 3 ns + 2 ns = 5 ns. The 4 ns propagation delay path through gates C and B can be ignored in determining the overall propagation delay of the circuit since it is shorter than 5 ns. In contrast, the determination of the contamination delay of the combined circuit requires identifying the **shortest** path of contamination delays from input to output. In Figure 3, the contamination delay of the combined circuit is 2 ns, since the shortest sum of contamination delays from an input (y) to an output (z), is t_{cd}(C) + t_{cd}(B) = 1 ns + 1 ns = 2ns. Note that this value is smaller than the contamination delay path through gates A and B (2 ns + 1ns = 3 ns).

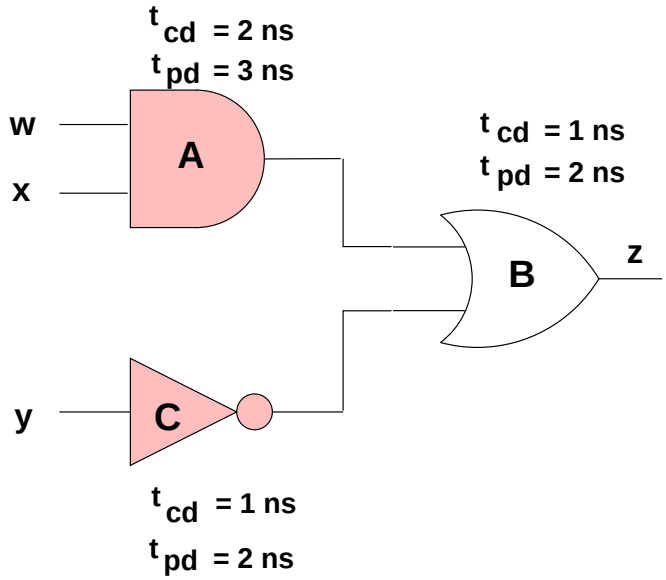

Figure 3: Combined Combinational Circuit Dealy

2 Timing Parameters for Sequential Logic

Like combinational circuits, when sequential circuits, such as edge-triggered flip-flops, are physically implemented, they exhibit certain timing characteristics. Unlike combinational circuits, these characteristics are specified in relation to the **clock input**. Since flip-flops only change value in response to a change in the clock value, timing parameters can be specified in relation to the rising (for positive edge-triggered) or falling (for negative-edge triggered) clock edge. The following parameters specify sequential circuit behavior. Unless otherwise specified, the following descriptions pertain to positive edge-triggered circuits. Similar definitions can be made for negative edge-triggered circuits.

- **Propagation delay (t_{Clk-Q})** - This value indicates the amount of time needed for a change in the flip flop-clock input (e.g. rising edge) to result in a **permanent** change at the flip-flop output (Q). When the clock edge arrives, the D input value is transfered to output Q. Note from Figure 4, that the output of the flip-flop may be at an intermediate value for a while (indicated by the cross-hatched area) before the final output value is created. After t_{Clk-Q}, the output is guaranteed not to change value again until another clock edge trigger (e.g. rising edge) arrives.
- **Contamination delay (t_{cd})** - This value indicates the amount of time needed for a change in the flip-flop clock input to result in the **initial** change at the flip-flop output (Q). Note from Figure 4, that the output of the flip-flop maintains its initial value until time t_{cd} has passed. The flip-flop is guaranteed not to show any output change in response to an input change until after t_{cd} has passed.
- **Setup time (t_s)** - This value indicates the amount of time **before** the clock edge that data input D **must** be stable. As shown in Figure 4, D is stable t_s time units before the rising

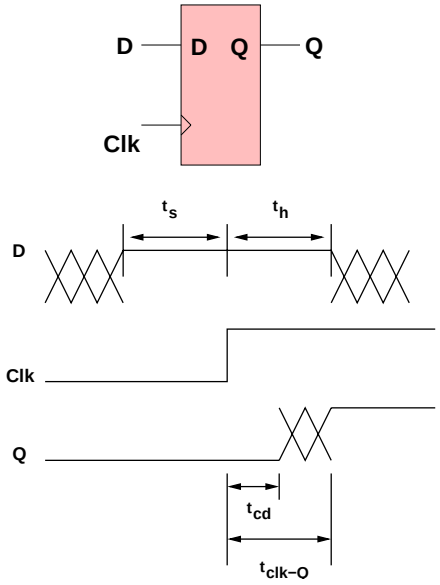

Figure 4: Setup and Hold Time for Sequential Circuits

clock edge.

- **Hold time (t_h)** - This value indicates the amount of time **after** the clock edge that data input D **must** be held stable. As shown in Figure 4, the hold time is always measured from the rising clock edge (for positive edge-triggered) to a point after the edge.

Setup and hold times are *restrictions* that a flip-flop places on combinational or sequential circuitry that drives a flip-flop D input. The circuit must be designed so that the D flip flop input signal arrives at least t_s time units **before** the clock edge and does not change until at least t_h time units **after** the clock edge. If either of these restrictions are violated for any of the flip-flops in the circuit, the circuit will not operate correctly. These restrictions limit the maximum clock frequency at which the circuit can operate. If the rising clock edges in Figure 1 are too close together, data will not have enough time to propagate through the circuit to the flip-flop input and arrive t_s time units before the rising clock edge.

3 Determining the Max. Clock Frequency for a Sequential Circuit

Most digital circuits contain both combinational components (gates, muxes, adders, etc.) and sequential components (flip-flops). These components can be combined to form sequential circuits that perform computation and store results. By using combinational and sequential component parameters, it is possible to determine the maximum clock frequency at which a circuit will operate and generate correct results. This analysis can best be examined through use of an example. A sample sequential cicuit is shown in Figure 5.

Before starting timing analysis, consider the flow of data in this circuit in response to a rising clock

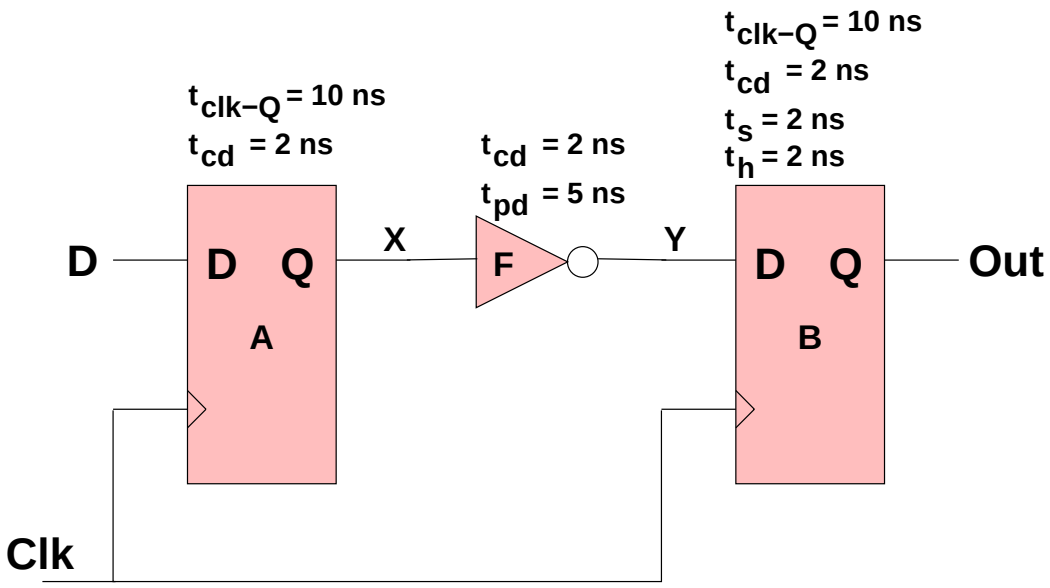

Figure 5: An Example Sequential Circuit

edge, starting at flip-flop A.

1. Following the rising clock edge on Clk, a valid output appears on signal X after t_{Clk-Q} = 10 ns.
2. A valid output Y appears at the output of inverter F, t_{pd} = 5 ns after a valid X arrives at the gate.
3. Signal Y is clocked into flip-flop B on the next rising clock edge. This signal must arrive at least t_s = 2ns before the rising clock edge.

As a result, the *minimum clock period*, T_{min} of the circuit is:

$$T_{min} = t_{Clk-Q}(A) + t_{pd}(F) + t_s(B) = 10ns + 5ns + 2ns = 17ns \quad (1)$$

and the **maximum clock frequency** of the circuit is $\frac{1}{T_{min}}$ = $\frac{1}{17ns}$ = 58.8 MHz. Waveforms that show the determination of the minimum clock period are show in Figure 6.

Since the Clk input is attached to both flip-flops, both will change value at the same time. On each clock edge, the same three steps starting from flip flop A are repeated. On the next edge, a new value is clocked into flip-flop B that is a result of the **previous** clock edge on flip-flop A.

In a typical sequential circuit design there are often millions of flip-flop to flip-flop paths that need to be considered in calculating the maximum clock frequency. This frequency must be determined by locating the **longest** path among all the flip-flop paths in the circuit. For example, consider the circuit shown in Figure 7. In this example, there are three flip-flop to flip-flop paths (flop A to flop

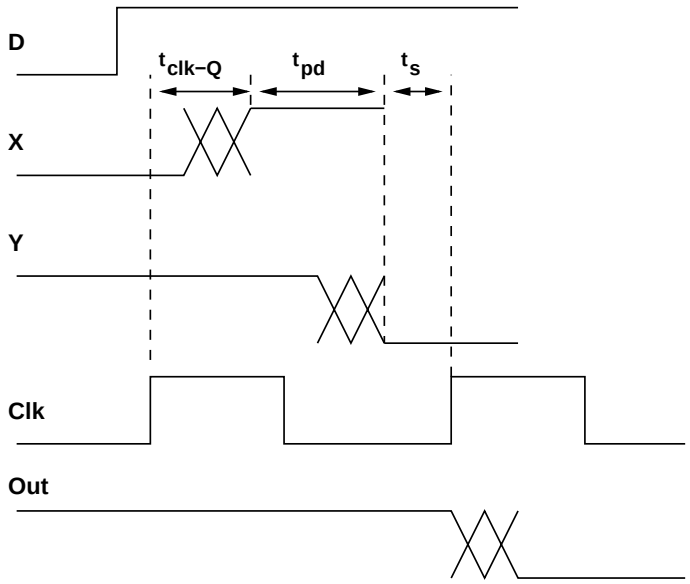

Figure 6: Timing Waveforms for the Circuit in Fig. 5

B, flop A to flop C, flop B to flop C). Using an approach similar to Equation 1, the delay along all three paths are:

- T_{AB} = $t_{Clk-Q}(A)$ + $t_s(B)$ = 9 ns + 2 ns = 11 ns
- T_{AC} = $t_{Clk-Q}(A)$ + $t_{pd}(Z)$ + $t_s(C)$ = 9 ns + 4 ns + 2 ns = 15 ns
- T_{BC} = $t_{Clk-Q}(B)$ + $t_{pd}(Z)$ + $t_s(C)$ = 10 ns + 4 ns + 2 ns = 16 ns

Since the T_{BC} is the **largest** of the path delays, the minimum clock period for the circuit is T_{min} = 16 ns and the maximum clock frequency is $\frac{1}{T_{min}}$ = 62.5 MHz.

4 Validating Flip-Flop Hold Time

Unfortunately, simply designing a circuit for a specific maximum clock frequency is not enough to ensure that the circuit will work properly. As mentioned earlier, the hold time, t_h must be satisfied for each flip-flop input, indicating that each D input cannot change until t_h time units after the clock edge. Fortunately, the **contamination delays** of combinational circuitry and flip-flops help prevent flip-flop inputs from changing instantaneously. This observation can be illustrated by re-examining Figure 5.

The hold time requirement on flip-flop B indicates that the Y input to flip-flop B **should not change** until at least 2 ns after the rising clock edge of Clk. By examining the circuit, it can be seen that the *earliest* the signal can start to change is equal to the sum of the contamination delays of flip-flop A and inverter X. Therefore, if

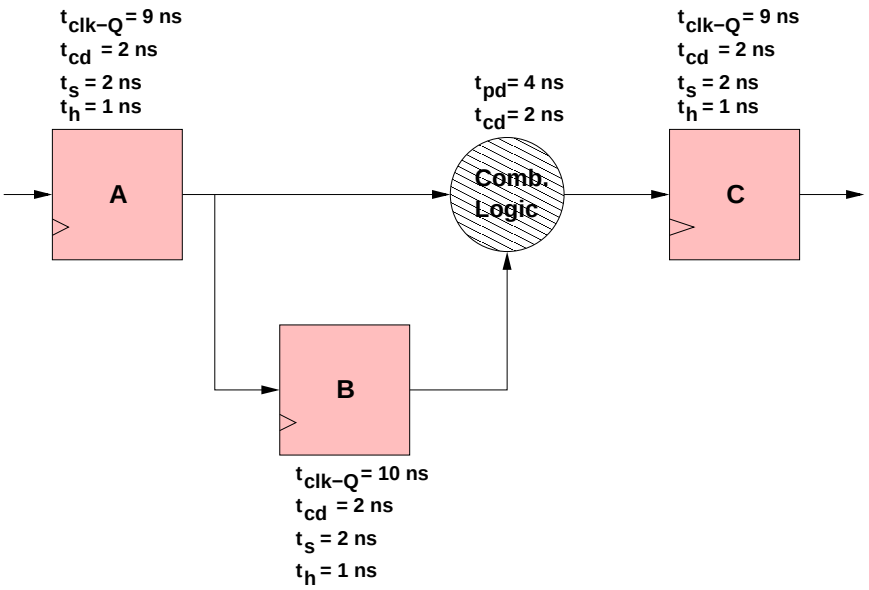

Figure 7: Multi-path Sequential Circuit

$$t_h(B) \leq t_{cd}(A) + t_{cd}(X) \tag{2}$$

the circuit is guaranteed to work correctly. Since t_h, 2 ns, is less than $t_{cd}(A) + t_{cd}(B)$, 4 ns, the hold time is satisifed and the circuit will work correctly. A similar analysis can be performed along each flip-flop to flip-flop path in Figure 7. These three paths lead to the following relationships for the A to B, A to C, and B to C paths, respectively:

$$t_h(B) \leq t_{cd}(A) \;\; [A\ to\ B\ path] \tag{3}$$
$$t_h(C) \leq t_{cd}(A) + t_{cd}(Z) \;\; [A\ to\ C\ path] \tag{4}$$
$$t_h(C) \leq t_{cd}(B) + t_{cd}(Z) \;\; [B\ to\ C\ path] \tag{5}$$

plugging in the values from Figure 7 gives:

$$1ns \leq 2ns \;\; [A\ to\ B\ path] \tag{6}$$
$$1ns \leq 2ns + 2ns \;\; [A\ to\ C\ path] \tag{7}$$
$$1ns \leq 2ns + 2ns \;\; [B\ to\ C\ path] \tag{8}$$

It is apparent that even the fastest flip-flop to flip-flop path (2 ns) is slower that the required hold time (1 ns). None of the flip flop input values will change until at least 2 ns following the clock edge due to the contamination delays along the paths. For each circuit in the path, the contamination delay guarantees that a change in the circuit input will not be shown at the circuit output until t_{cd} time units.

5 Conclusion

Sequential circuits rely on a clock signal to control the movement of system data. Given a set of combinational and sequential components and their associated timing parameters, it is possible to determine the maximum clock frequency that can be used with the circuit. This analysis includes the examination of every flip-flop to flip-flop path in the circuit. The examination includes both the propagation delays along the paths and the data setup time at the destination flip-flop. Following the calculation of the maximum clock frequency, each flip-flop to flip-flop path can be examined to ensure that flip-flop hold times are satisfied. If the contamination delays along each path are greater than or equal to the destination flip flop hold time, the circuit will operate as designed.

References

[1] S. Ward and R. Halstead. *Computation Structures*. McGraw-Hill, Boston, Ma, 1991.