Simple Audio Loopback Using CC251X

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Keywords

- *ADC*
- *DAC*
- *µLaw*
- *CC2510*
- *CC2511*

1 Introduction

The above mentioned SoCs contains an ADC, a DAC and an I2S interface making it suitable for voice quality audio applications without using an external codec. The following design note shows how a simple mono loopback code can be implemented with µlaw encoding / decoding.

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2 Abbreviations

ADC	Analog to Digital Converter
DSM	Delta Sigma Modulator
I2S	Inter-IC Sound

3 ADC

The following code sets up the ADC to sample input AIN0.

```
// Enable ADC AIN0 as input
// Set ADC start condition to '11' ADCCON1.ST = 1
// Set ref.voltage (AVDD pin), decimation rate (14 bit resolution)
// Disable extra conversion
void initAdc (void) {
  ADCCFG = 0x01;
  ADCCON1 = 0x33;
  ADCCON2 = 0xB0;
  ADCCON3 = 0x00;
}
```

When single-ended input is used, only positive conversion results are generated, effectively reducing the resolution to 13 bits. Remember also that when reading the ADC data, the two least significant bits of the ADCL register is always read as zero.

4 DSM

The follow code sets up the DSM to 8 kHz sample rate.

```
// Configure IO-pin as output for the DSM
// Suspend timer 1 (T1CTL:MODE = 0)
// Clear timer counter by writing any value to T1CNTL
// Set the sample rate, 8kHz by writing T1CC0H:T1CC0L
// Set Timer 1 channel 0 to compare mode (T1CCTL0.MODE = 1)
// Load first sample as zero
// Enable timer counter to modulo mode (T1CTL.MODE = 2)
// Configure the DSM by setting the MODE and CAP fields in T1CCT1
// Enable interrupt on timer 1 overflow
// Enable DSM mode (T1CCTL1.CMP = 7)
void initDsm (void) {
  P1SEL |= 0x02;
  PERCFG |= 0x40;
  P1DIR |= 0x02;
  T1CTL &= ~0x03;
  T1CNTL = 0x00;
  T1CC0H = 0x0C;
  T1CC0L = 0xB1;
  T1CCTL0 |= 0x04;
  T1CC1L = 0;
  T1CC1H = 0;
  T1CTL |= 0x02;
  T1CCTL1 &= ~0x07;
  TIMER1_ENABLE_OVERFLOW_INT(TRUE);
  INT_ENABLE(INUM_T1, INT_ON);
  T1CCTL1 |= 0x38;
}
```

5 µLaw Compression / Encoding

Compressing the audio will reduce the amount of data needed to be transmitted over radio

The µLaw (ITU standard G.712) has 13-bit or 78dB dynamic range and a compression ratio of up to 2:1. µlaw is based on fine quantization for low-level signals and a coarser quantization for loud levels. This approach exploits the perception of the human auditory system where small variations in loud signals are not detected and the amount of information in the audio signal can be reduced without significantly reducing the quality of the audio experience.

µlaw is also supported in USB Audio Device Class Definition, which could be an option if using the CC2511 USB functionality.

The following two functions utilize the µlaw encoding / compression implemented into the I2S interface without enabling the interface itself.

```
// Enable µlaw compression(I2SCFG0.ULAWE cleared & I2SCFG0.ULAWC set)
// Write uncompressed data to I2SDATH:I2SDATL registers
// The Compression takes one clock cycle to perform
// The result can be read from the I2SDATH register.
BYTE ulawCompression (INT16 sample) {
  I2SCFG0 = 0x10;
  I2SDATL = (BYTE) sample;
  I2SDATH = (BYTE) (sample >> 8);
  return I2SDATH;
}

// Enable µlaw expansion (I2SCFG0.ULAWE set & I2SCFG0.ULAWC cleared)
// Write compressed data to I2SDATH register
// The expansion takes one clock cycle to perform
// The result can be read from the I2SDATH:I2SDATL registers
INT16 ulawExpansion (BYTE ulawcode) {
  INT16 expandedValue;
  I2SCFG0 = 0x20;
  I2SDATH = ulawcode;
  expandedValue = I2SDATL;
  expandedValue |= I2SDATH << 8;
  return expandedValue;
}
```

6 Main Function and Interrupt Service Routine

The following code bundles everything together with the main function initialising the ADC/DSM while the Timer 1 interrupt service routine updates the DSM, read the ADC, start a new ADC conversion and performs the µlaw compression/expansion at a 8 kHz sample rate. In order to keep the DSM output jitter-free, make sure that the DSM output happens at a given interval.

```
void main (void)
{
  // Initialations
  SET_MAIN_CLOCK_SOURCE(CRYSTAL);
  SET_MAIN_CLOCK_SPEED(MHZ_26);
  CLKCON = (CLKCON & 0xC7);
  initAdc();                          // Initialize the ADC
  initDsm();                          // Initialize the DSM
  INT_GLOBAL_ENABLE(TRUE);            // Global interrupt enabled
  while(1);                           // Endless loop
}

/* Since the ADC is set up with single-ended input, only positive
conversion results are generated effectively reducing the resolution
to 13 bit. Shift the result one to the left and you have a 16 bit
result. The two LSB is garbage, but it's not needed to mask these as
we will ulaw compress the data anyway. */
#pragma vector=T1_VECTOR
__interrupt void T1_IRQ(void){
  static INT16 sampleOut=0;
  static UINT16 sampleIn;
  static BYTE muLawCode;

  if(T1CTL & 0x10){
    T1CC1L = (BYTE)sampleOut;         // Update the DSM frequency
    T1CC1H = (BYTE)(sampleOut >> 8);
    sampleIn = (((INT16)ADCH) << 8);// Get MSB ADC result
    sampleIn |= ADCL;                 // Get LSB ADC result
    ADCCON1 |= 0x40;                  // Start new ADC conversion
    If(sampleIn & 0x8000)
      sampleIn = 0;                   // Remove unwanted neg.numb
    sampleIn = sampleIn << 1;         // Convert to 16 bit
    sampleOut = sampleIn-32767;       // Convert to signed int.
    muLawCode = ulawCompression (sampleOut);
    sampleOut = ulawExpansion(muLawCode);
  }
  T1CTL &= ~0x10;
}
```

7 General Information

7.1 Document History

Revision	Date	Description/Changes
SWRA138	2007.04.16	Initial release.

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