Static Random Access Memory

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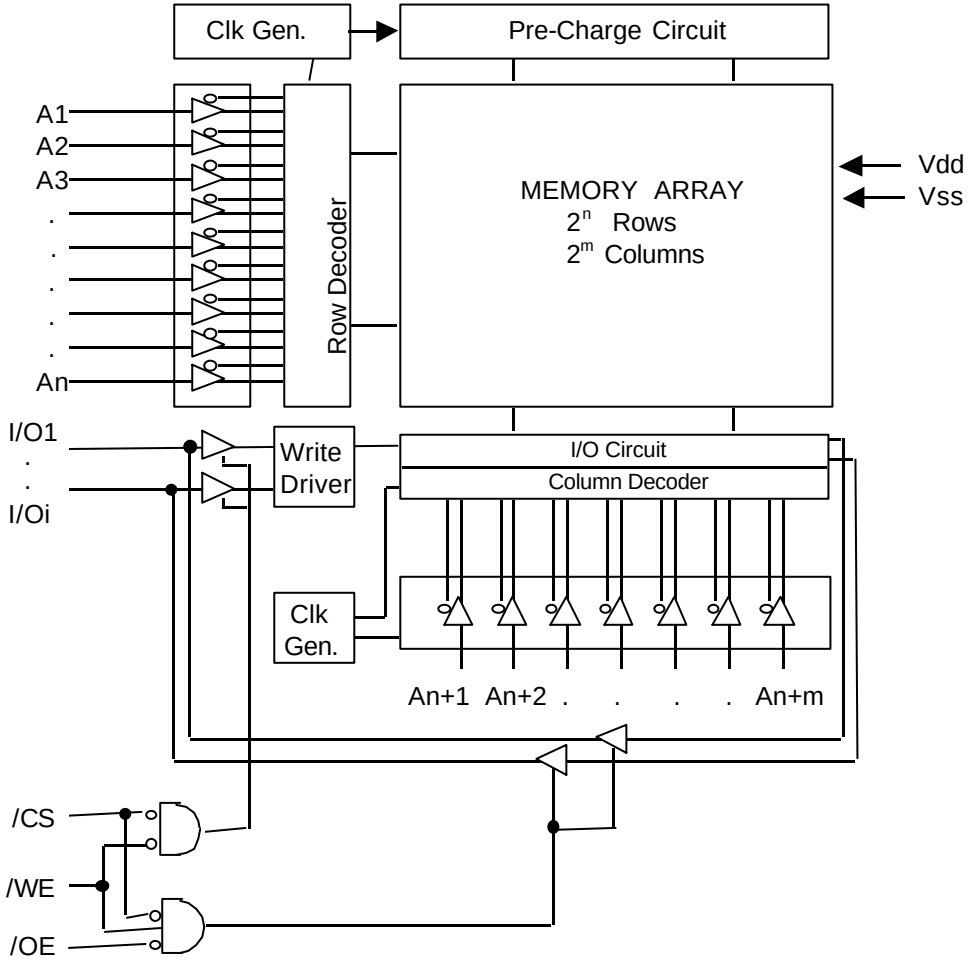
1-1. Basic Architecture and AC/DC Characteristics

1-1-1. Functional Block Diagram of Standard SRAM



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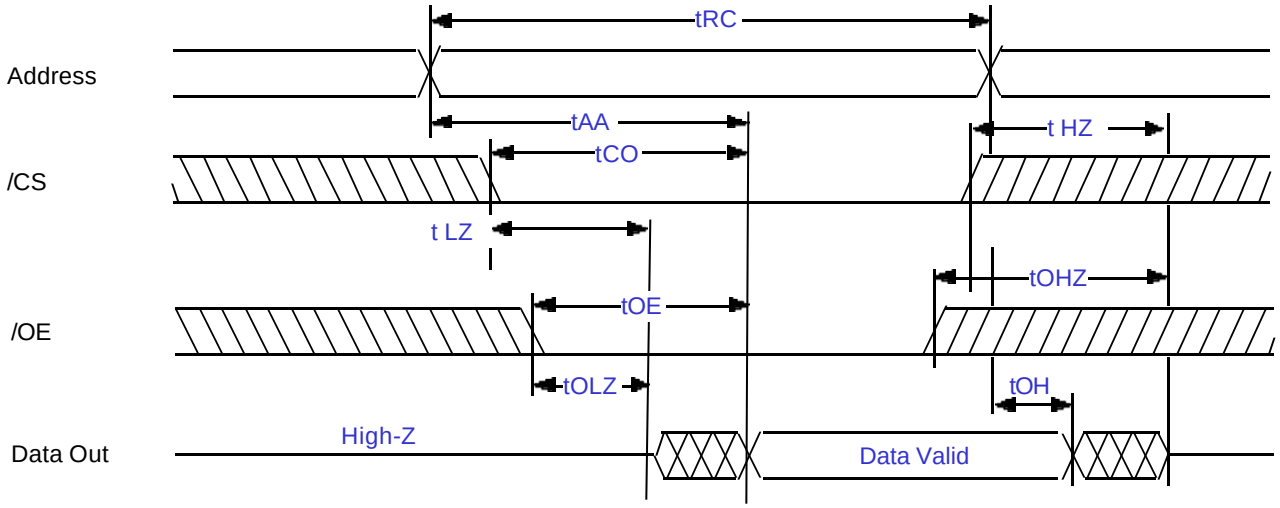
1-1-2. Typical Read Cycle Timing

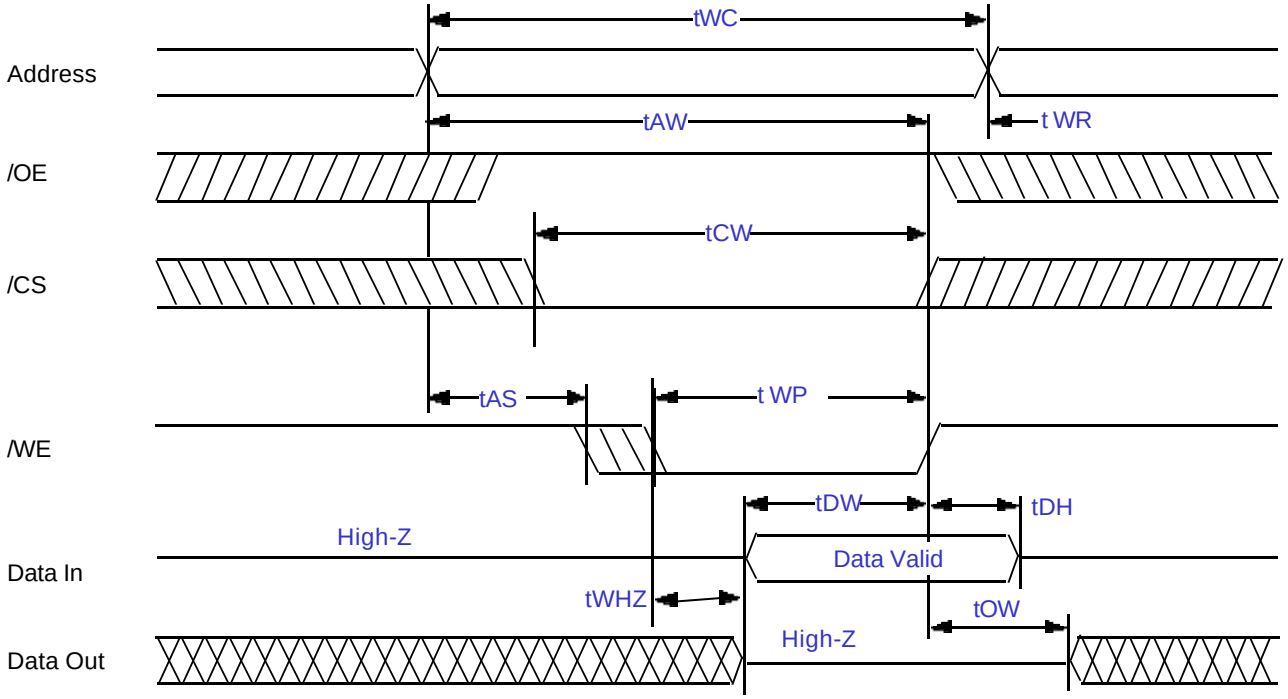


Example of 1Mb SRAM

Parameter	Symbol	KM68V1002-12		KM68V1002-15		KM68V1002-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

(From SAMSUNG SRAM Databook 1996)

1-1-3. Typical Write Cycle Timing



Example of 1Mb SRAM

Parameter	Symbol	KM68V1002-12		KM68V1002-15		KM68V1002-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	12	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

(From SAMSUNG SRAM Databook 1996)

1-1-4. DC and Operating Characteristics

Example of 1Mb SRAM DC Power

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	VIN=Vss to Vcc		-2	2	uA
Output Leakage Current	ILO	/CS=VIH or /OE=VIH or /WE=VIL VOUT=VSS to Vcc		-2	2	uA
Operating Current	ICC	Min. Cycle, 100% Duty /CS=VIL, VIN=VIH or VIL, IOUT=0mA		- - - -	200	mA
Standby Current	ISB	Min. Cycle, /CS=VIH		-	20	mA
	ISB1	f=0MHz, /CS ≥ Vcc -0.2V,	Normal	-	10	mA
		VIN ≥ Vcc -0.2V or VIN ≤ 0.2V	L-ver.	-	0.1	
Output Low Voltage	VOL	IOL=8mA		-	0.4	V
Output High Voltage	VOH	IOH = - 4mA		2.4	-	V

(From SAMSUNG SRAM Databook 1996)

(TA= 0 to 70℃, Vcc=3.3V ± 0.3V)

1-2. SRAM Features

1-2-1. Low Power SRAM

- Low Power Supply Voltage : 5V -> 3V -> 1.8V -> sub 1.0V

  -> Low Power Dissipation for Handheld Application

- Low Standby Power Dissipation : 100uA -> 10uA -> 1uA

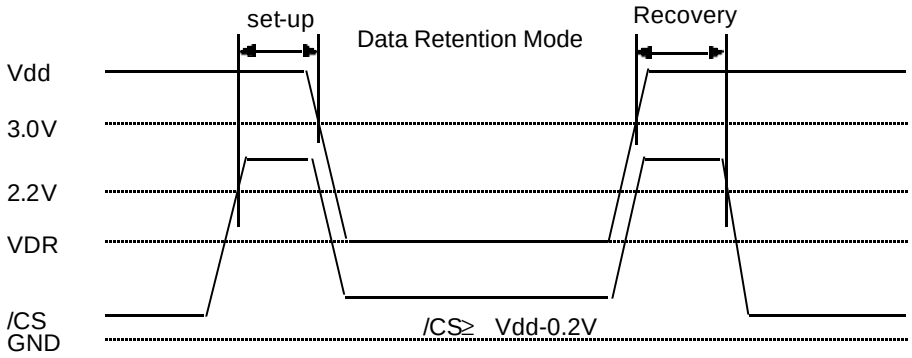
  -> support for Data Retention Application

- Small Size Package : sTSOP, CSP(uBGA, FPBGA), MCP

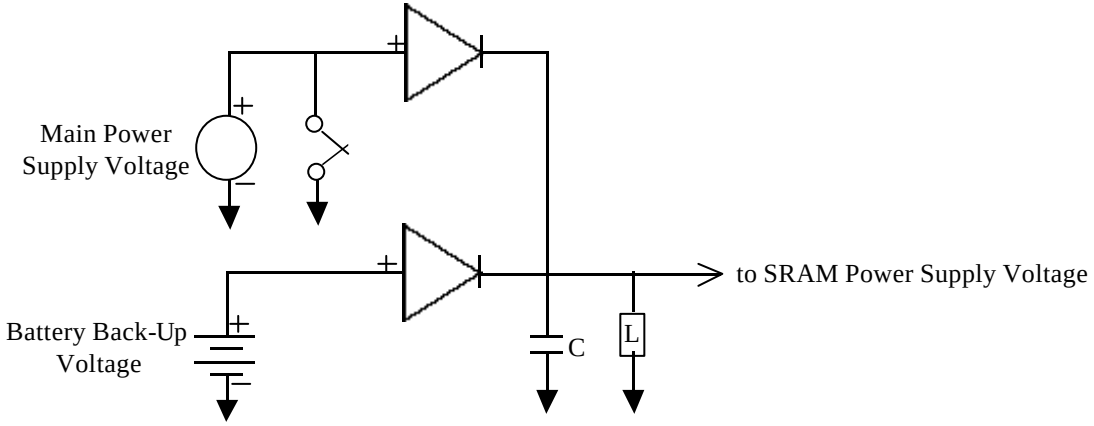
  -> reduce the package area for Handheld Application

Data Retention Mode

Transition Timing to Battery



Battery Back-Up System



1-2-2. FAST SRAM

- Power Supply Voltage : 5V, 3.3V

  -> JEDEC standard power supply voltage

- Low Operating Power Dissipation

  -> Application for large amount of SRAM usage

- FAST Speed requirements : 8ns-20ns

1-2-3. Synchronous SRAM

- Low Power Supply Voltage : 3.3V -> 2.5V -> 1.8V

  -> Small geometry Transistor technology to improve speed

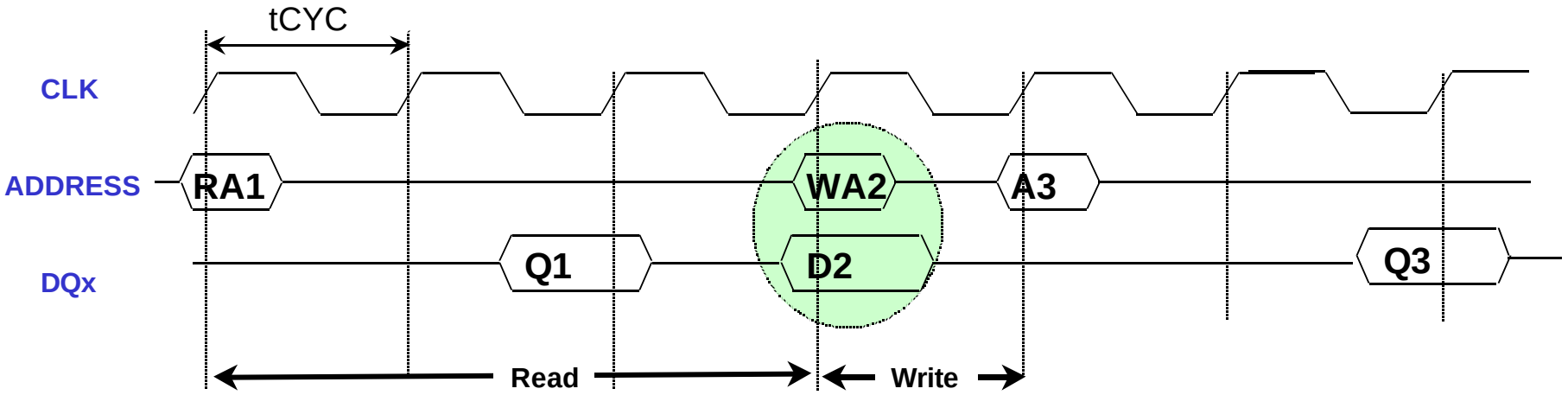
- Various Sync. SRAM Features : LW(Late Write), DLW(Deep Late Write), DDR(Double Data Rate)

  -> Late Write operation to enhance the bus efficiency

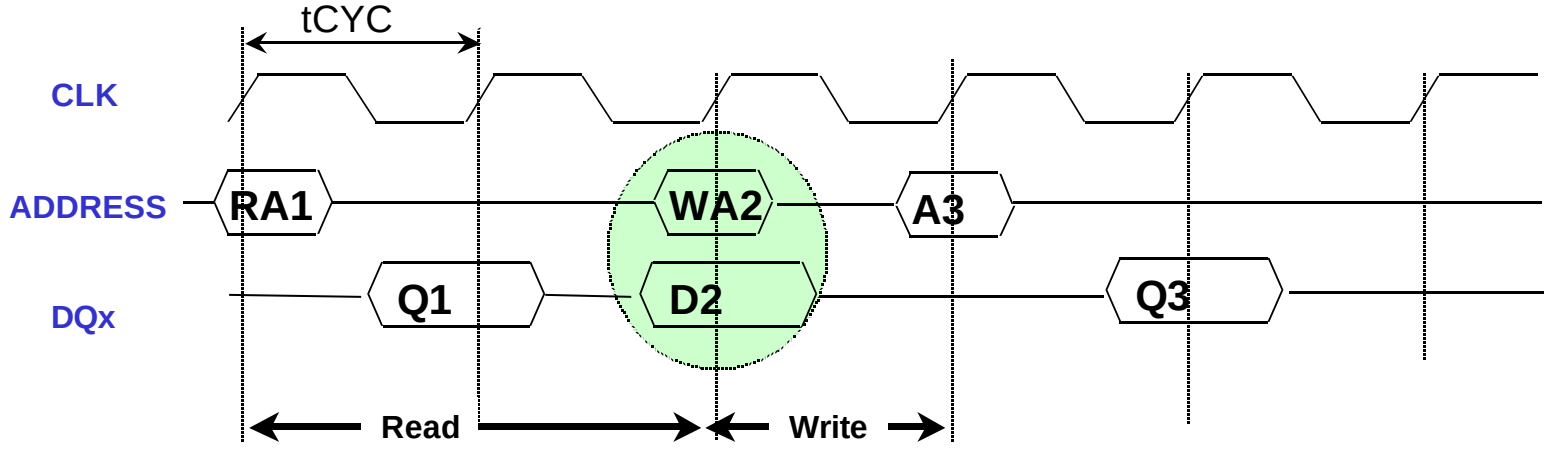
- High Bandwidth Interface : LVTTL -> LVCMOS -> HSTL
- FAST Speed Requirements : 150MHz-over 500MHz(1Gbps)
- High Performance Package Solution : TQFP, BGA, FCBGA

Various Sync. SRAM Features

Standard Write (Register-Register/Pipe Line)



Standard Write (Register-Latch/Flow Through)



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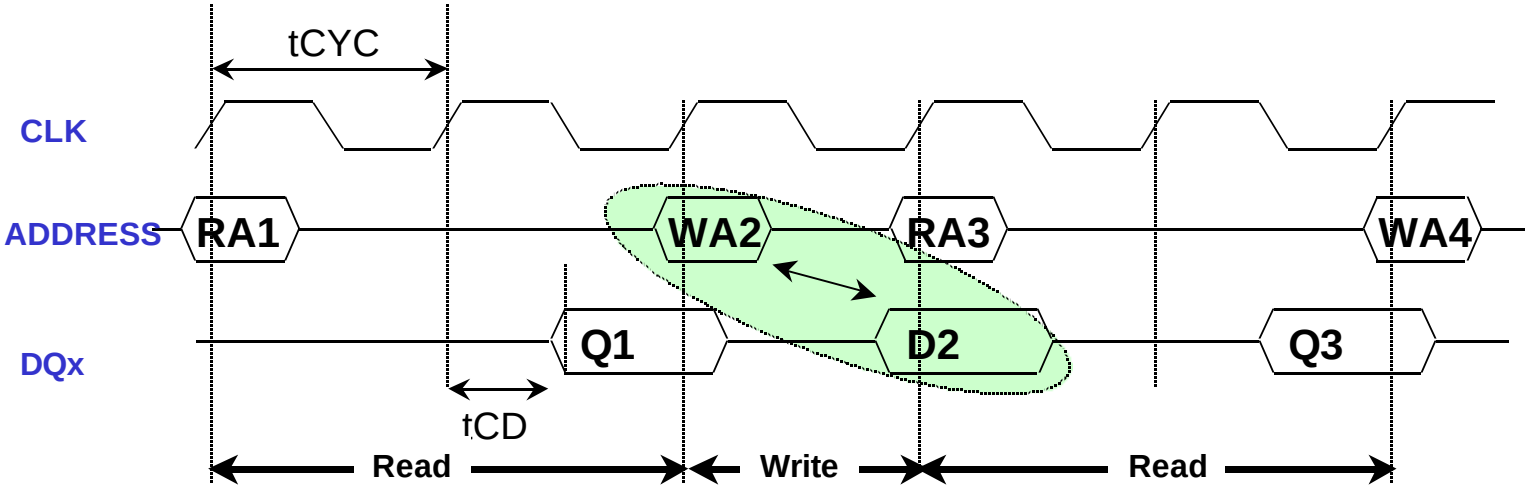
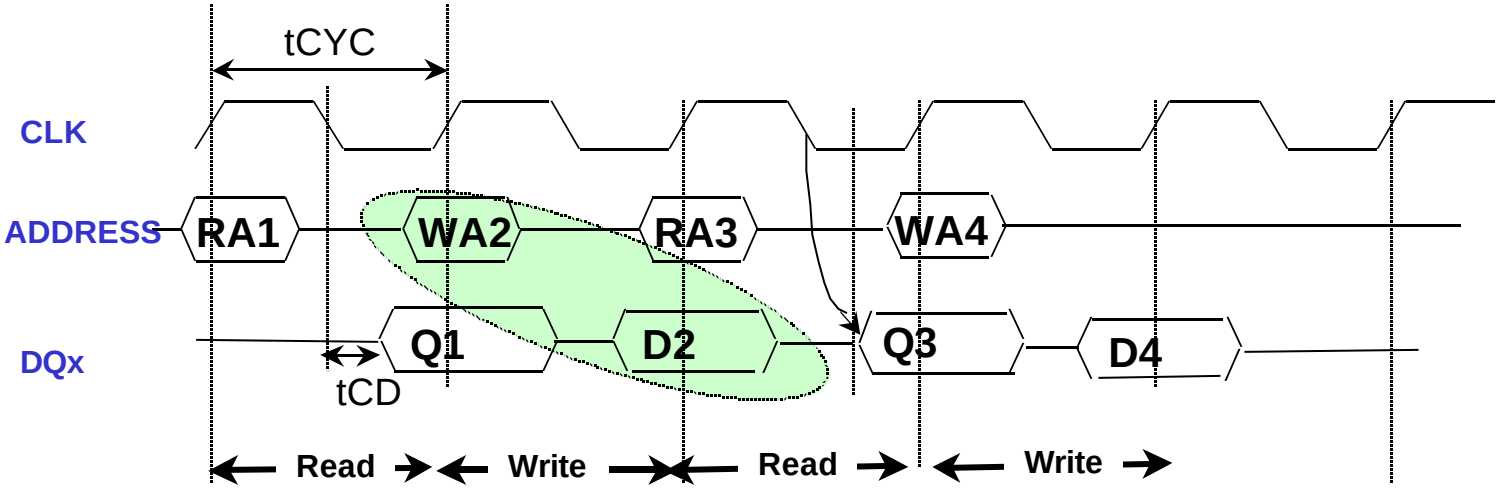
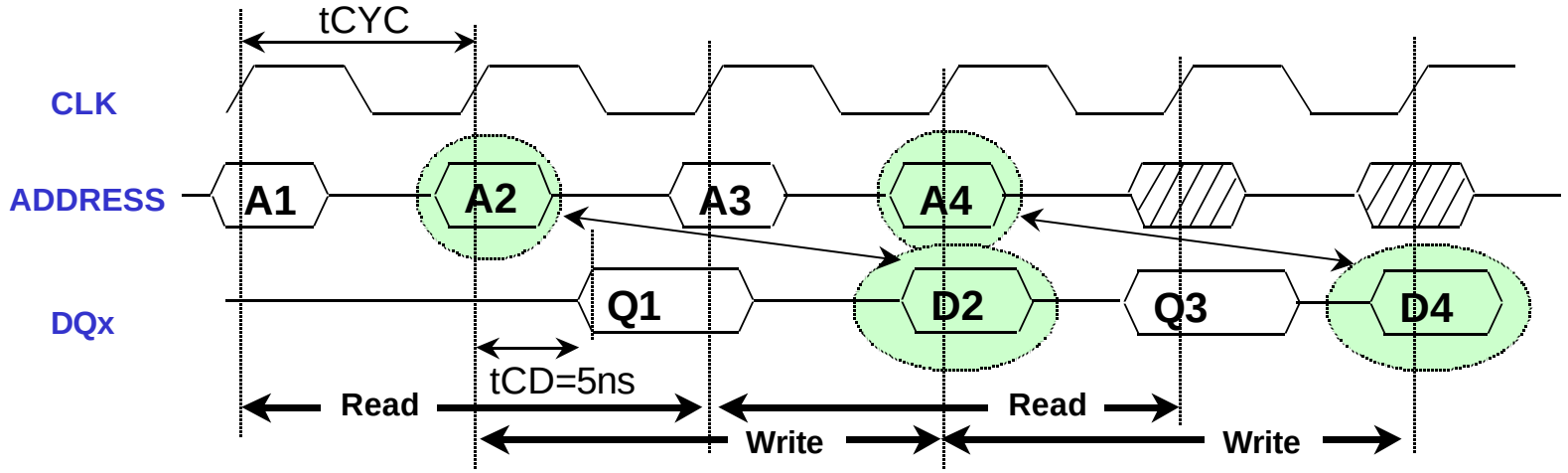
Late Write (Register-Register/Pipe Line)



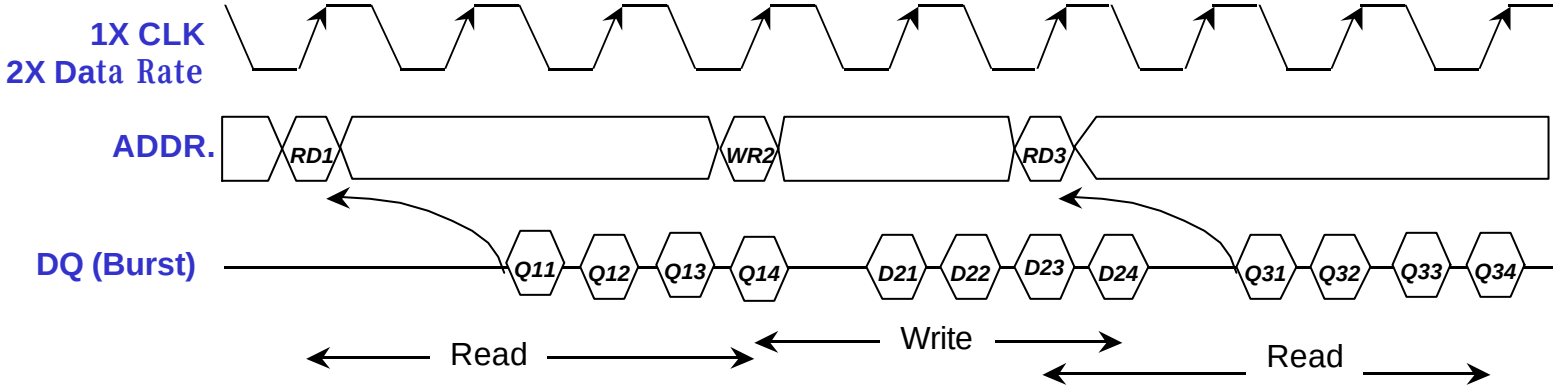
Late Write (Register-Latch/Flow Through)



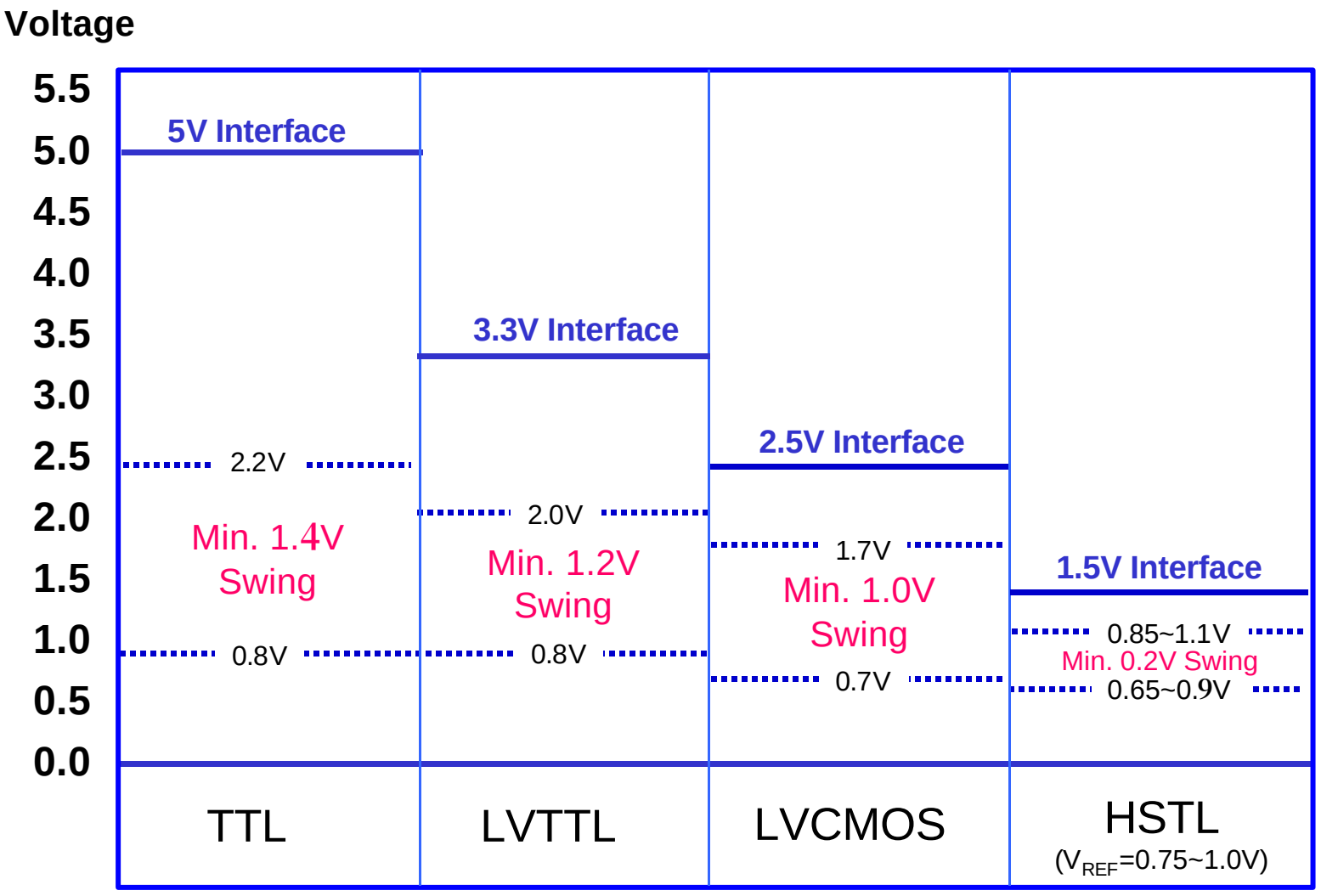
Deep Late Write (Register-Register/Pipe Line)



Double Data Rate (Register-Register/Pipe Line)



High Bandwidth Interface



1-3. SRAM cell Technology

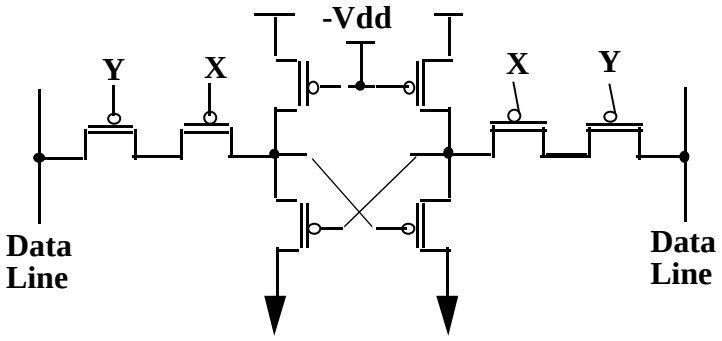
- Low cost, High Density Commodity SRAM for Small Microprocessor controlled system
  . Change from NMOS Cell to Mix-MOS Cell

- Low Standby power for Battery Back-Up and Battery Operated System
  . Change from Mix-MOS Cell to TFT(Thin Film Transistor) or Full CMOS Cell

- FAST speed for Cache SRAM
  . Change from NMOS Cell to Mix-MOS or Full CMOS Cell

PMOS Enhancement Load Cell

- Substituting Bipolar SRAM Cell
  - . High device yield and low cost
  - . Low standby power dissipation as compared with the bipolar SRAM cell
- Use diffusion process to make MOS transistor in mid of 1960s
  - . Limitation of the low power supply voltage due to increase Vtp

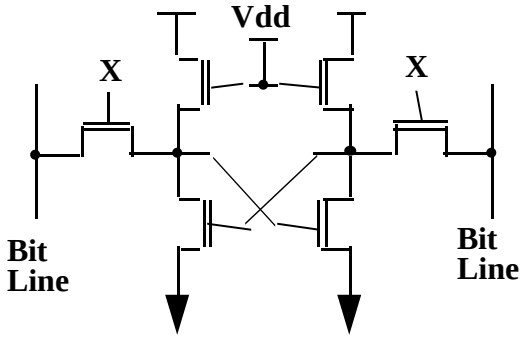


. 64 bit Array
. SiO2 120nm
. Vdd = -18V
. 150 - 200ns

(From Joseph H. Friedrich [1], Fairchild 1968)

NMOS Enhancement Load Cell

- Substituting PMOS Load SRAM Cell
  . Meet sub 100ns speed
- Use high doping substrate or substrate bias in end of 1960s
  . High stand-by power dissipation
  . Limitation of small cell size

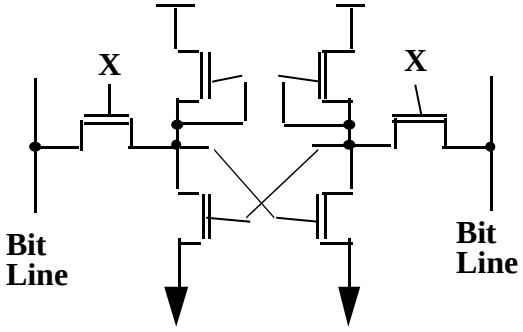


. 144 bit Array
. Vdd = 12V
. 40ns write cycle

(From Yasuo Tarui. et al., [2] NEC 1969)

NMOS Depletion Load Cell

- Substituting NMOS Enhancement Load SRAM Cell
  . Fully static with no dynamic or bootstrapped node
  . Low voltage operation (5V supply voltage) due to the low threshold voltage
- Use ion implantation process
  . High stand-by power dissipation
  . Limitation of small cell size

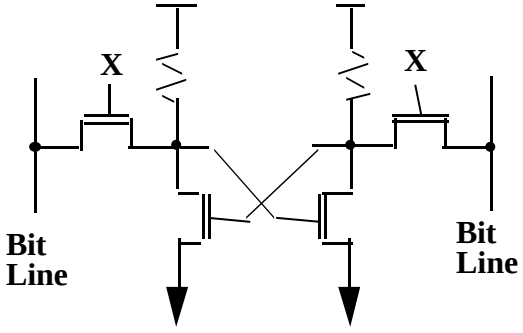


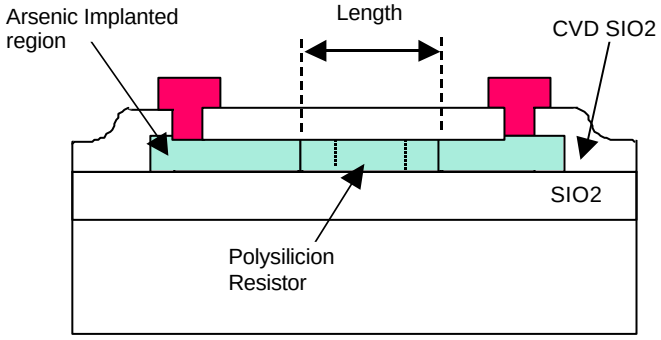
. 1K bit Array
. SiO2 120nm
. Vdd = 5V
. 150ns

(From R.M.Jecmen. et al., [3] Intel 1974)

High-Resistivity Poly Load Cell (Mix-MOS)

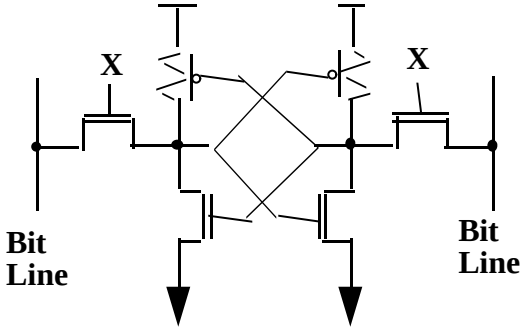
- Substituting NMOS Load SRAM Cell
  - . Cost effective chip size
  - . Low stand-by dissipation
- Negative Temperature Coefficient Resistance: Isb = I_0 exp (-Ea/KT)
  - . Compensate the temperature dependence of the junction leakage current and the subthreshold current
- Have been used 16Kb SARM to 1Mb SRAM since end of 1970s
  - . Limitation of low stand-by power dissipation for high density SRAM
  - . Limitation of low power supply voltage (less 2.5V) operation
- High density limitation [4]
  - . SLOW : 4Mb (with 1uA stand-by current)
  - . FAST : 4Gb (minimum 4mA stand-by current)

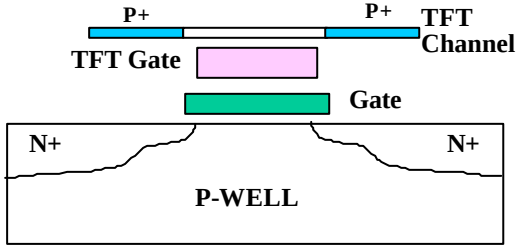




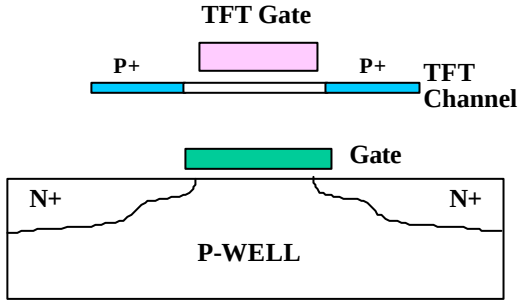
TFT (Thin Film Transistor) Load Cell

- Compatible cell size as compared with poly load cell
- Low stand-by power dissipation with retaining data retention voltage
- Improved SER (Soft Error Rate)
- Using high density SRAM (4Mb SRAM) since end of 1980s
  . Complicated process
  . Limitation of low power supply voltage (less 3.0V) operation





Bottom Gate TFT



Top Gate TFT

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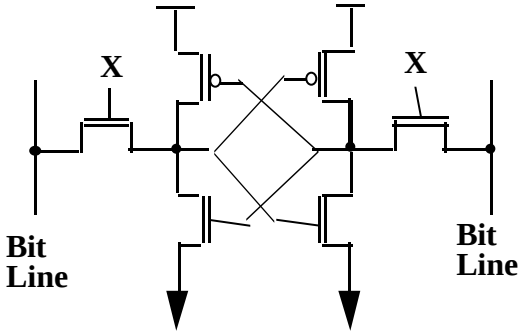
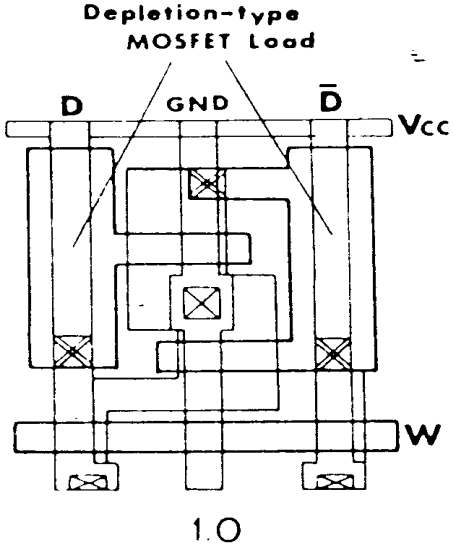
Full CMOS Cell

- Ultra low stand-by power dissipation with good data retention characteristics
- Good stability for wide noise margin
  . Less 2.0V low power supply voltage operation
- Good SER (Soft Error Rate) Characteristics
- Future SRAM Technology for Low Vdd/Ultra High speed product
- Limitation of small cell size
  . Mainly used internal cache of MPU

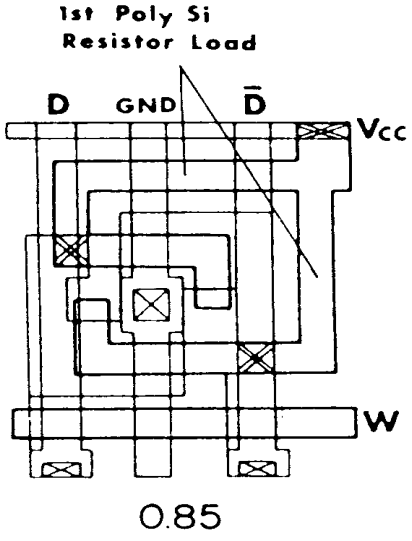


1-3-2. Comparison of layout of load devices in SRAM memory cells

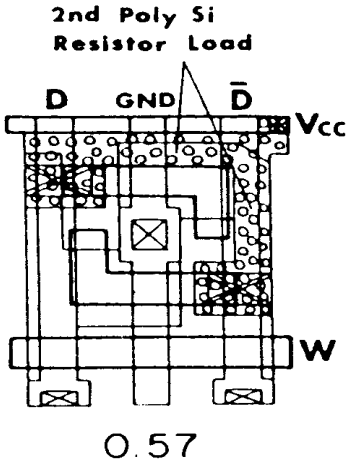
NMOS and Mix-MOS SRAM cell



Depletion mode Load



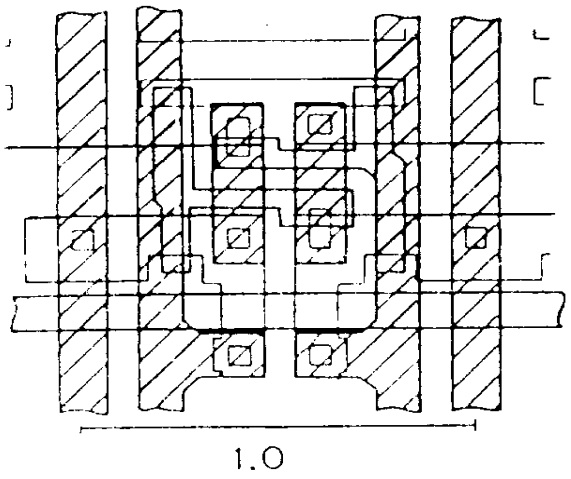
Single polysilicon Cell



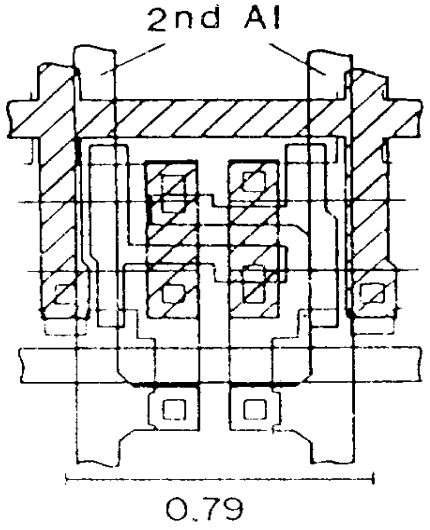
Double polysilicon Cell

- Cell size reduction
  . scaling from 3um CMOS to 2um CMOS
  . adding the second level of polysilicon for the stacked load resistor [5]

Full CMOS SRAM cell



Single aluminum interconnect



Double aluminum interconnect

- Cell size reduction
  . adding the second level of metal for the local interconnection [6]

1-4. SRAM Technology for Peripheral Circuits

- MOS SRAMs are the fastest MOS memories.
- Bipolar SRAMs are the fastest of all memories.

1-4-1. Bipolar

- Application for ultra high speed SRAM
  . Cache and Main Memory in high performance mainframe computers
  . ECL interface
- High cost and High power dissipation

1-4-2. NMOS

- Lower cost than Bipolar
- Limitation of high density and high performance due to complicated circuit design
  . need dynamic circuit and bootstrapped circuit technique
- Limitation of low power dissipation and high speed

1-4-3. CMOS

- Low cost and low power dissipation
- Easy to make high density SRAM

- Limitation of high speed
  . improve the MOS Transistor
  . use Dynamic Gate Logic

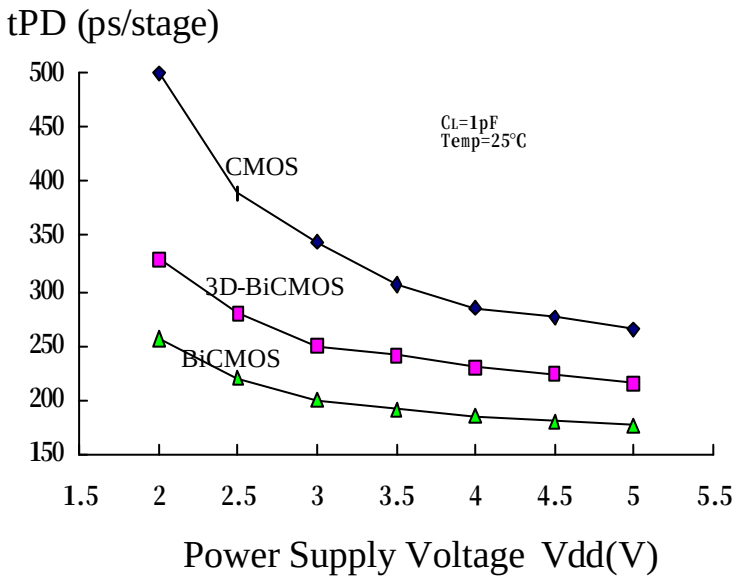
1-4-4. BiCMOS

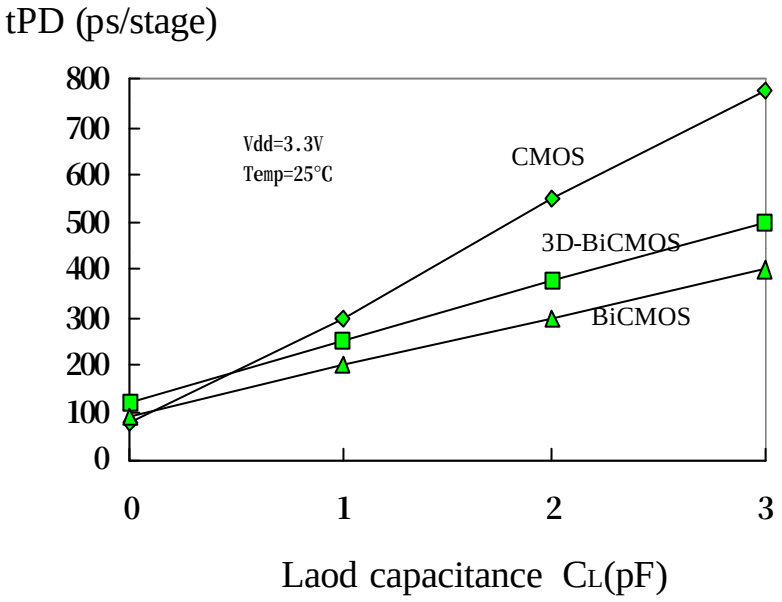
- High speed
  . application for small volume/high performance

- Complicated process [7][8]
  . use triple diffused BiCMOS process

- Limitation of low power supply voltage [9]
  . improve the MOS Transistor (Lower Vth)
  . use BiNMOS or NBiCMOS
  . Base boost technique

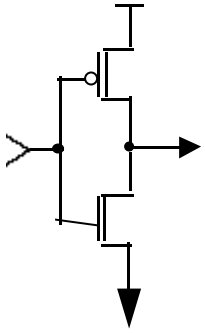
Propagation Delay with Process Technology (From H.G. Byun et al. [10], Samsung 1995)



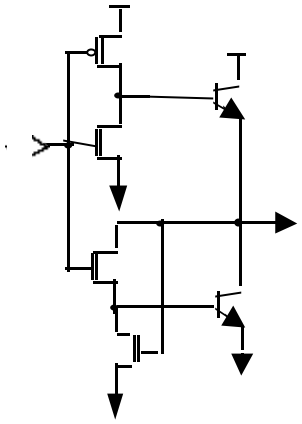


Propagation Delay with Inverter Logic

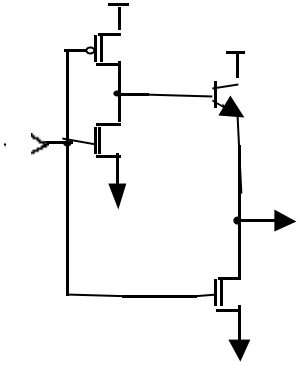
(From H.G. Byun et al. [10], Samsung 1995)



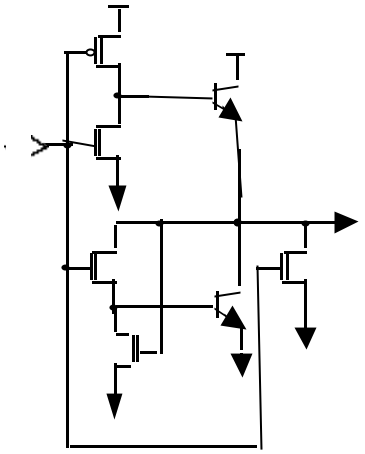
CMOS



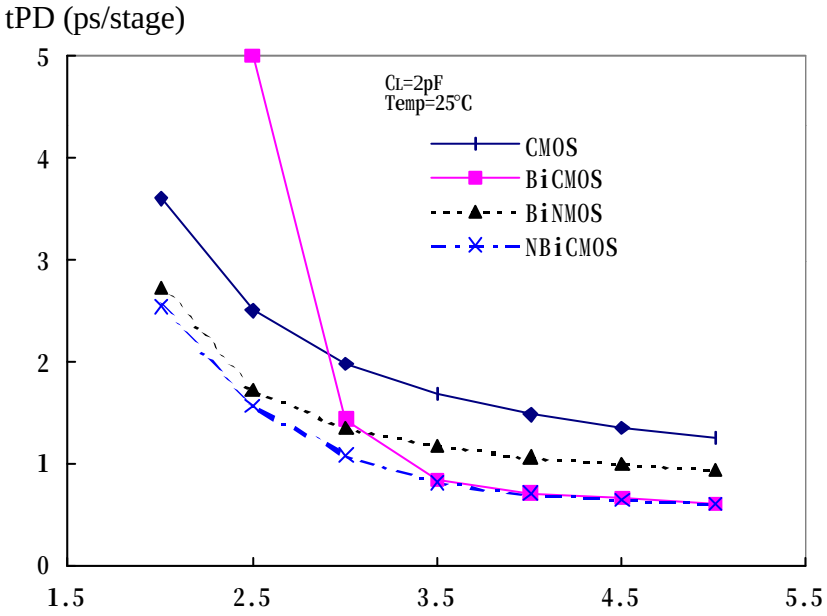
BiCMOS



BiNMOS



NBiCMOS



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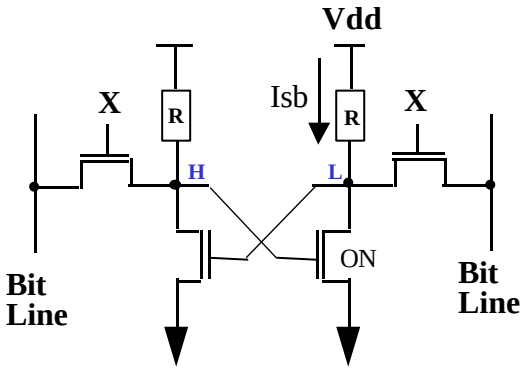
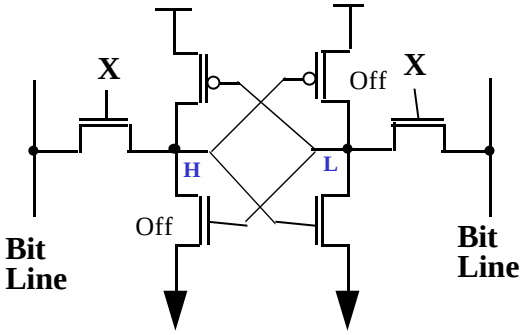
2. SRAM Cell and Basic Core Operation

2-1. SRAM Cell Operation

2-1-1 Chip Power-Down Mode (Stand-By)





- One inverter is always ON for the Poly Laod or NMOS Load cells
  when in the standby mode.
  . Current(Isb) is drawn from Vdd
- In the Full-CMOS cell, one transistor in each of the coupled inverters is OFF.
  . Only junction leakage current is drawn from Vdd

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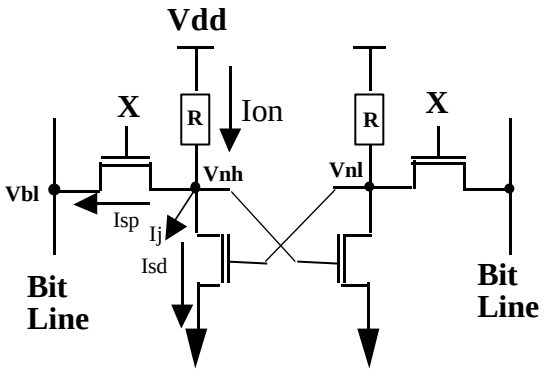
2-1-2. Data Retention

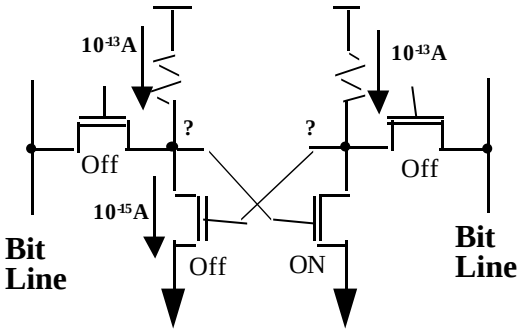


- Data Retention Voltage (Vdr)
  . Min. power supply voltage to retain high node data in the standby mode.
- a prerequisite of Data Retention

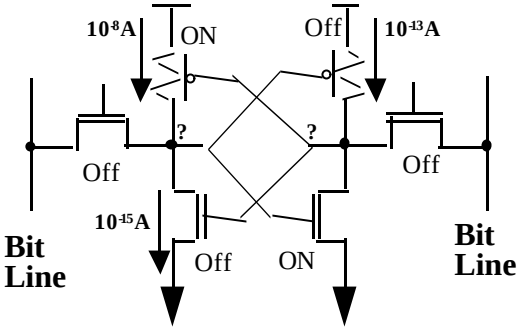
  Ion [= (Vdd - Vnh) / R] ≥ Isp + Isd + Ij

  Where Ion = Charge Current
  Isp = Sbthreshold current of Pass Transistor @ VDS=Vnh-Vbl, Vgs=0V
  Isd = Sbthreshold current of Pull-down Transistor @ VDS=Vnh, Vgs=Vnl
  Ij = Junction leakage for high node @ Vnh

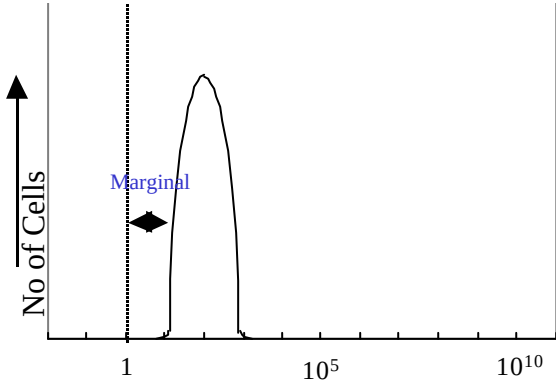
Data Retention Margin

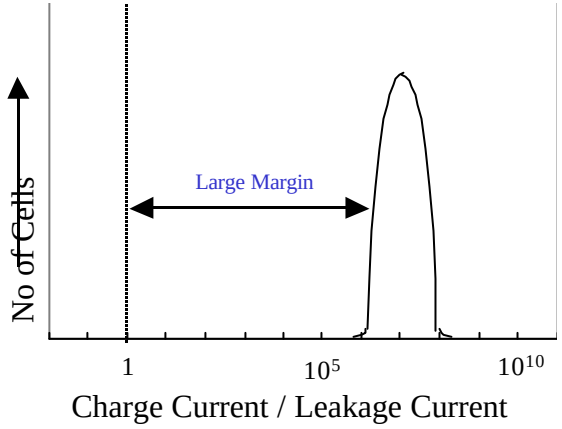


High Resistive Poly Load Cell



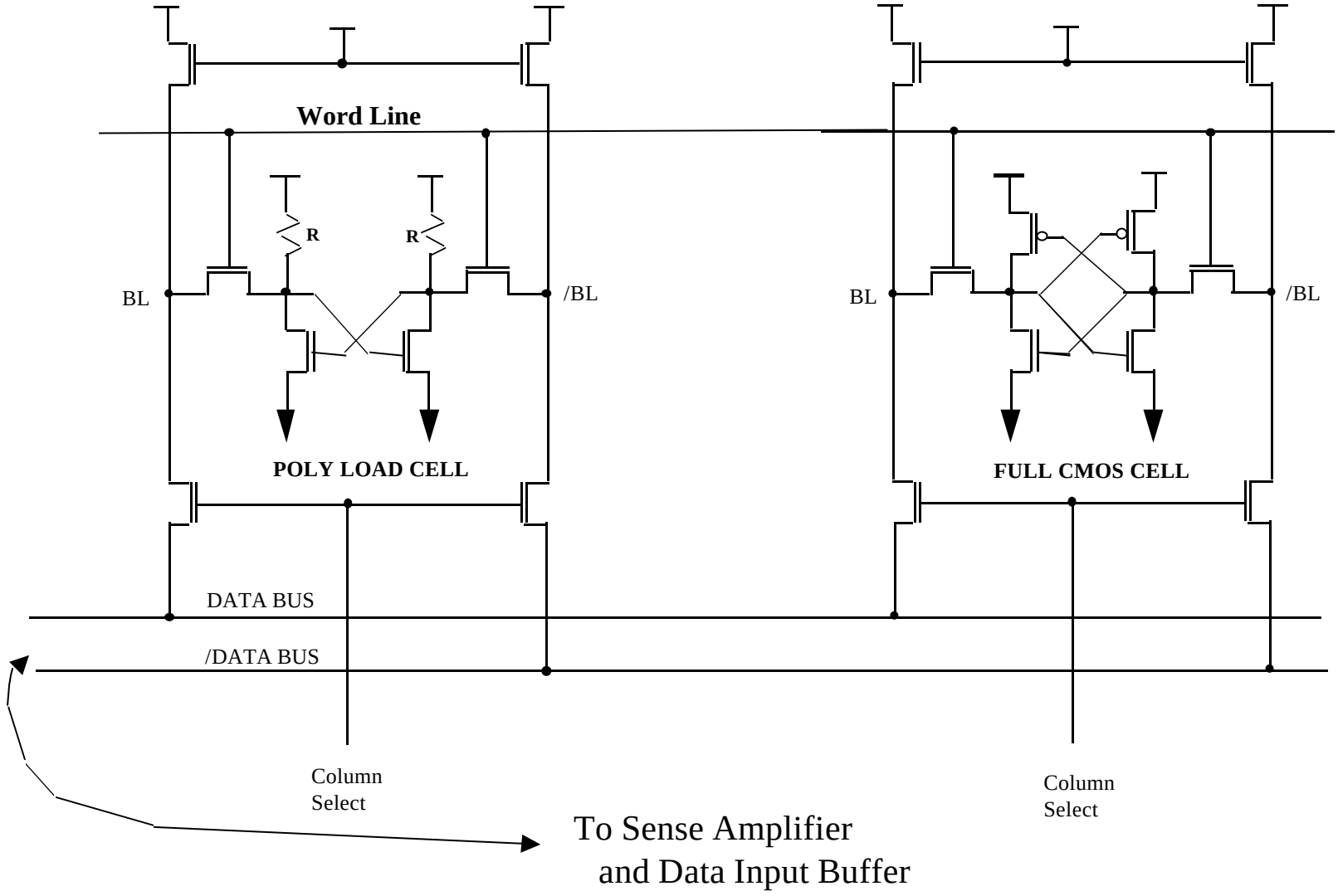
TFT (Thin Film Transistor) Load Cell



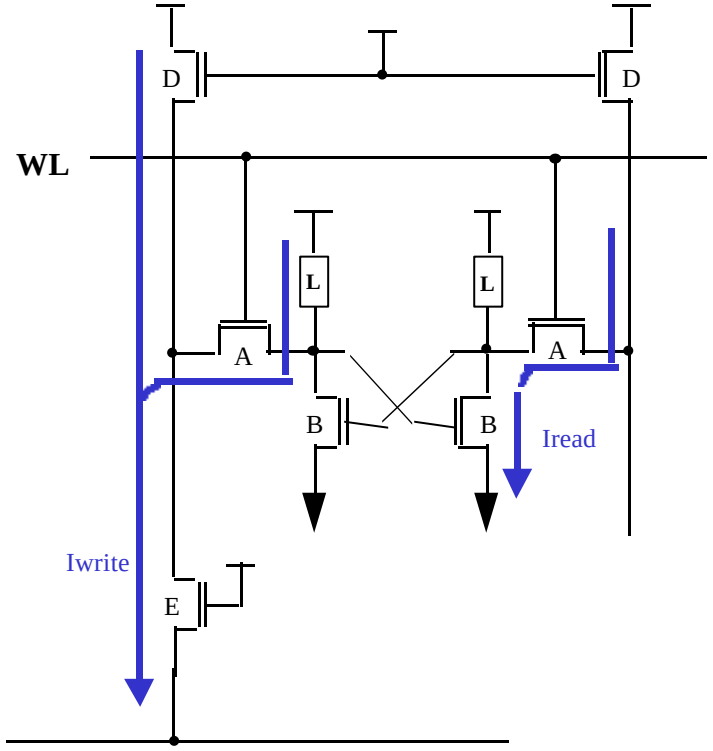


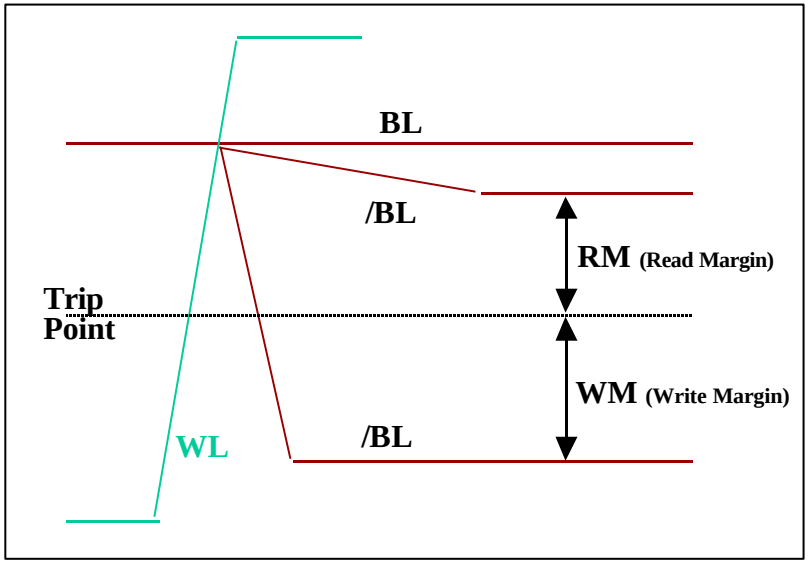
(From T.Y.OOTAMI. et al. [11], Toshiba 1990)

2-2. Read/Write Operation

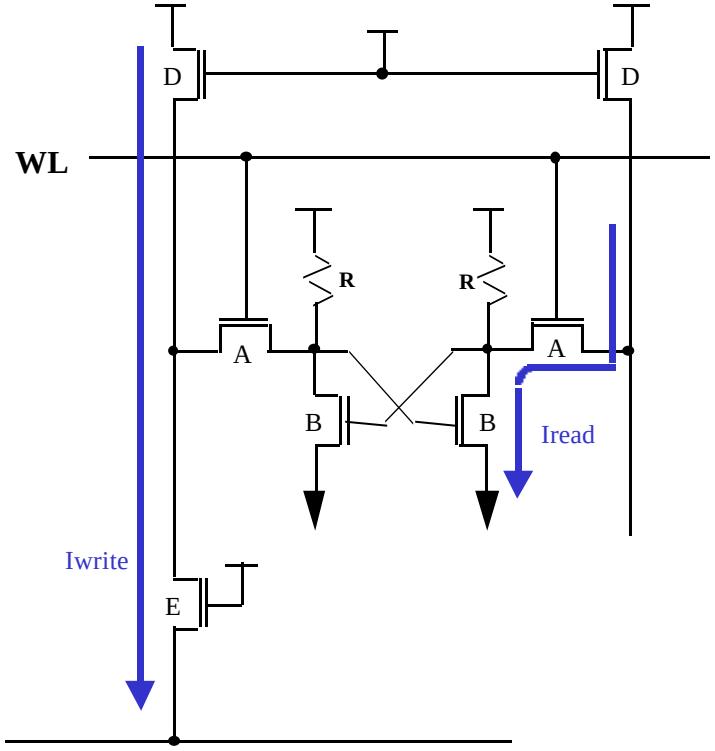


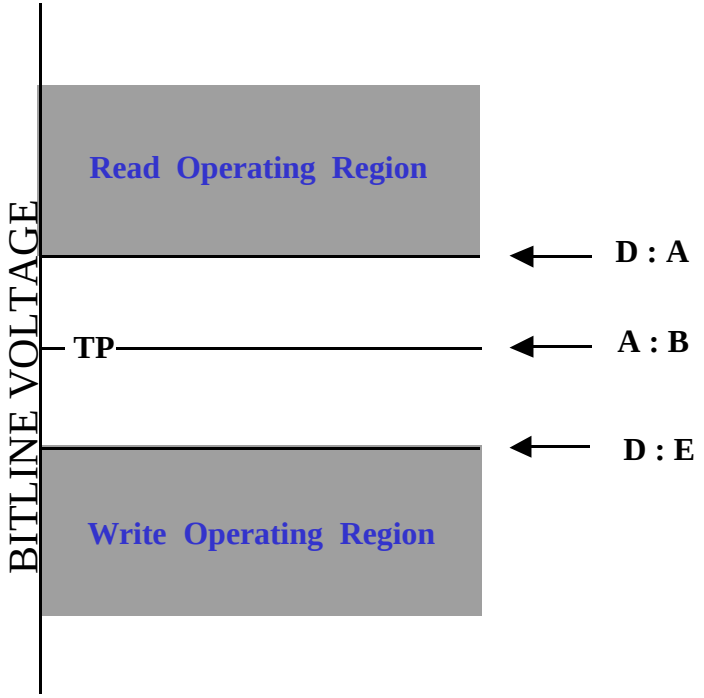
Read/Write Margin Analysis





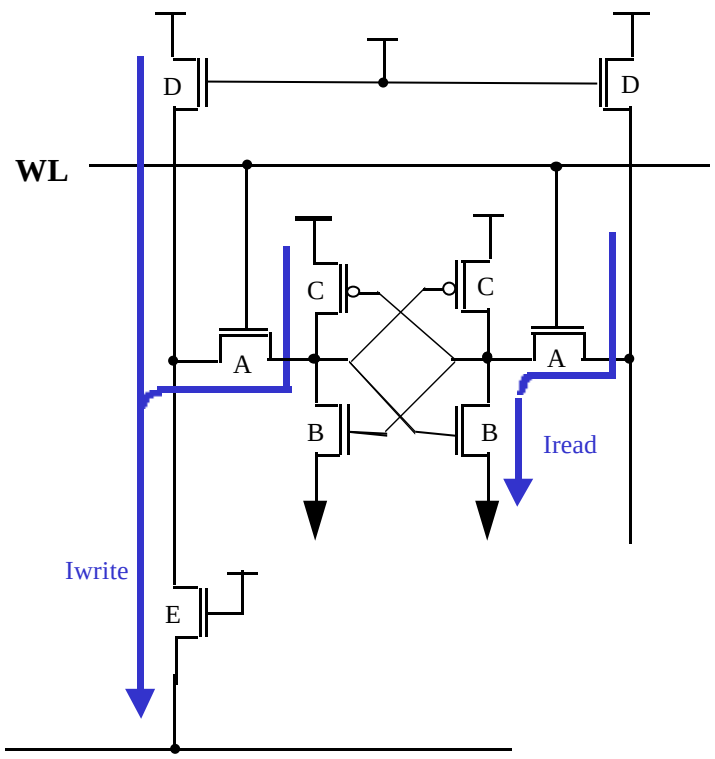
2-2-1. Poly Load Cell Read/Write Operation

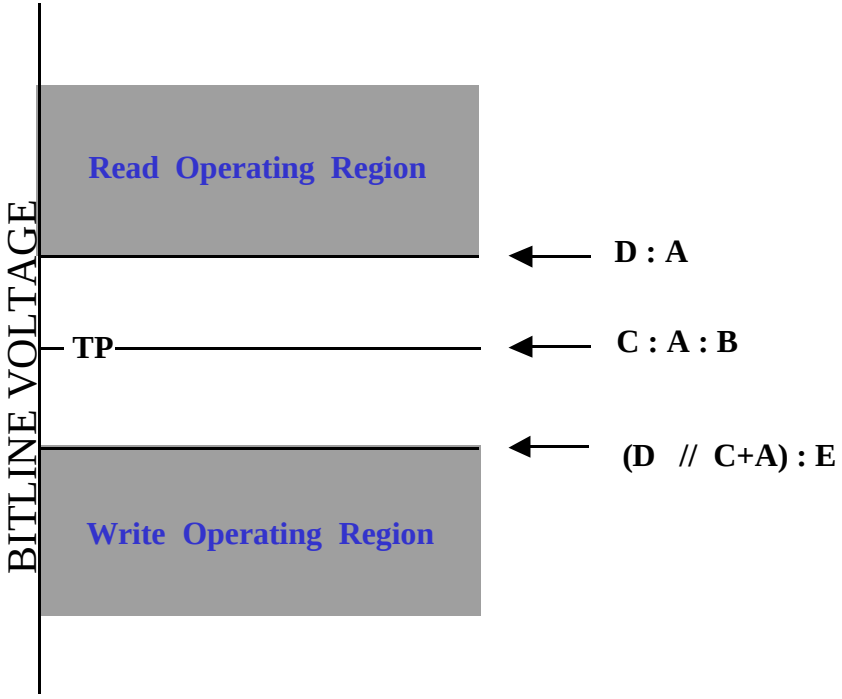




TP: MEMORY CELL TRIP VOLTAGE

2-2-2. Full CMOS Cell Read/Write Operation



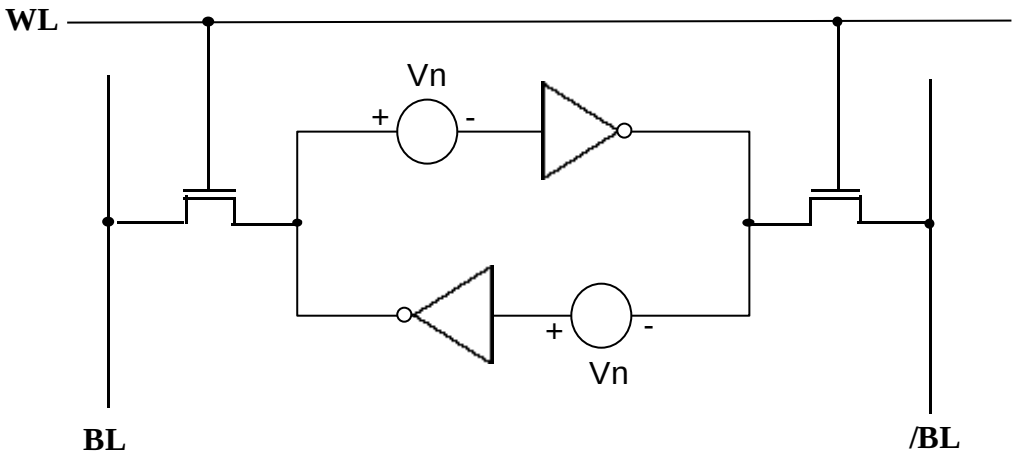


TP: MEMORY CELL TRIP VOLTAGE

2-3. SRAM Cell Stability

2-3-1 Static-Noise Margin (SNM)

What is the Static-Noise margin (SNM)?



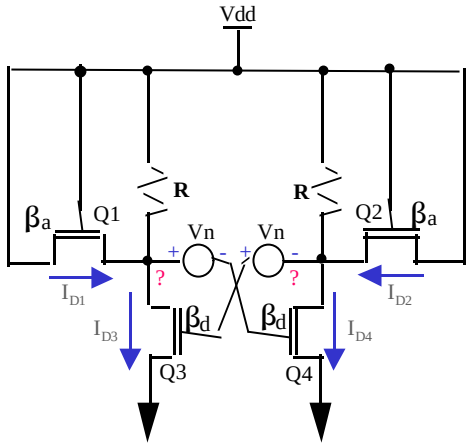
Vn : Static Noise Source

SNM : Maximum Value of Vn

Static-Noise margin (SNM) for Poly Load Cell (From E. Seevink. et al. [12], 1987)

Assumption

- Q1, Q2, Q3 : Saturation Region
- Q4 : Linear Region



MOS Models

- $Id = 1/2\,\beta\,(Vgs - Vth)^2$ Saturation Region
- $Id = \beta\,Vds\,(Vgs - Vth - 1/2\,Vds)$ Linear Region

where $\beta = W/L \cdot \mu\,eff\,Cox$

Analytic Expressions

- Kirchhoff Current Equation

  Id1 = Id3 , Id2 = Id4
- Kirchhoff Voltage Equation

  Vgs3 = Vn + Vds4

  Vgs1 = Vdd - Vn - Vgs4

  Vgs2 = Vdd - Vds4

Results

$$SNM\,(Vn_{(MAX)}) = \frac{\sqrt{\gamma} - 1}{\sqrt{\gamma} + 1}\,Vth + \frac{\gamma + 1 - \sqrt{2\gamma^{3/2} + \gamma + 1}}{\gamma\,(\sqrt{\gamma} + 1)}\,(Vdd - Vth)$$

where γ (Cell Ratio) $= \beta_d / \beta_a$

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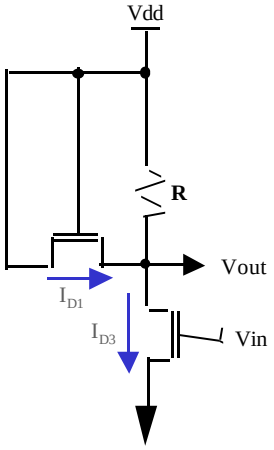
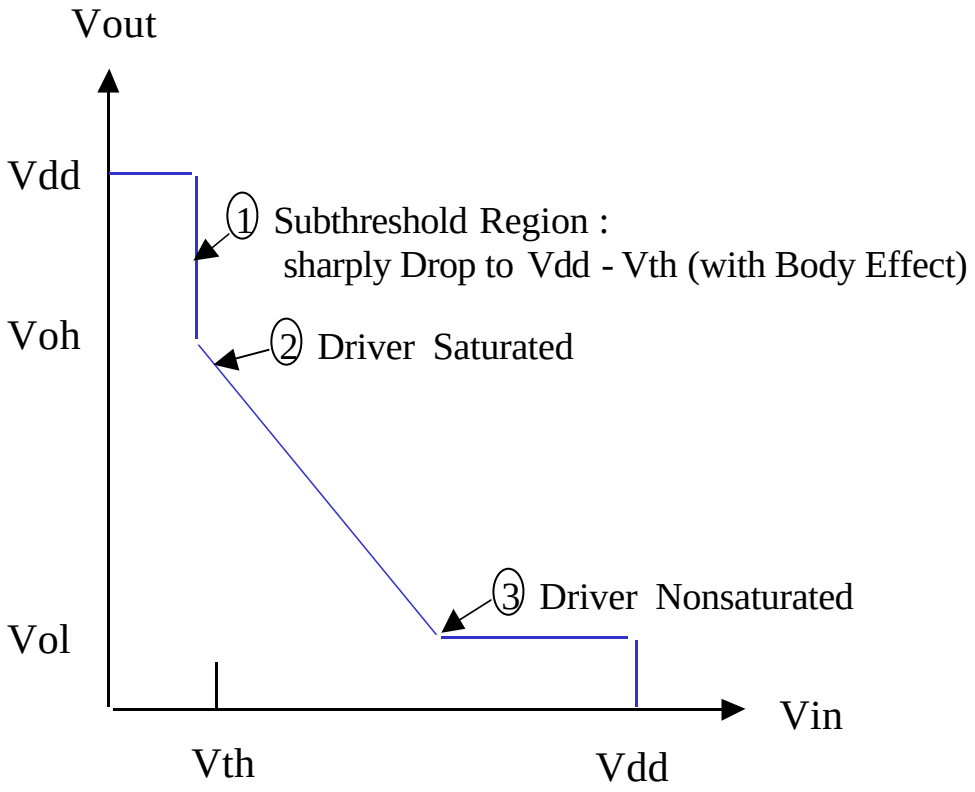
Saturated Enhancement Load Inverter





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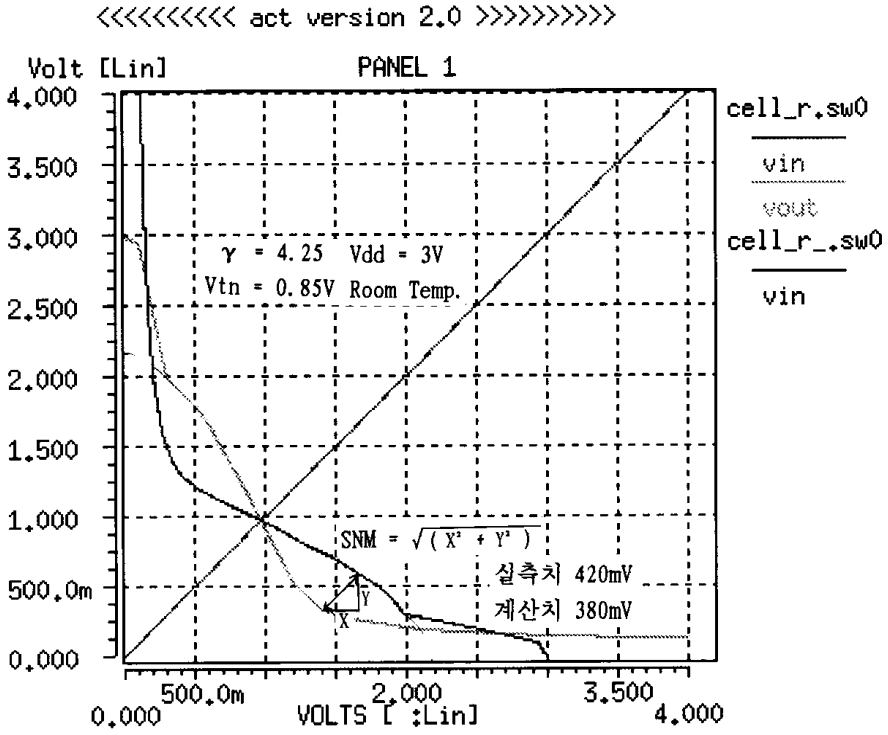
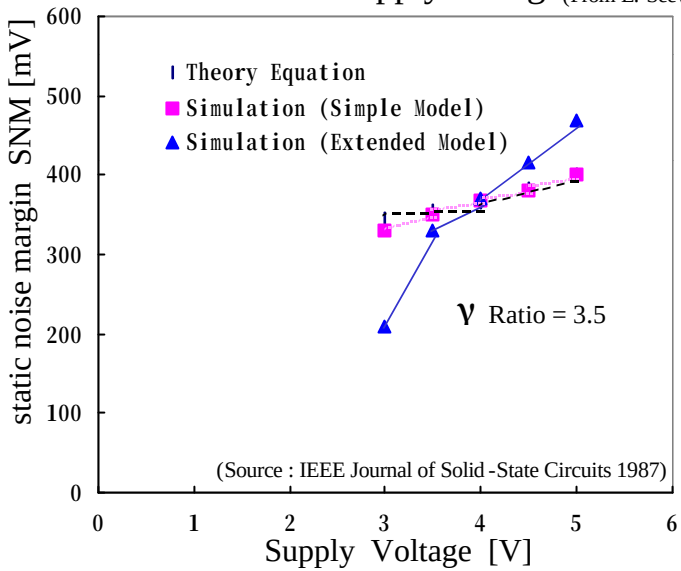
SNM of Poly Load Cell

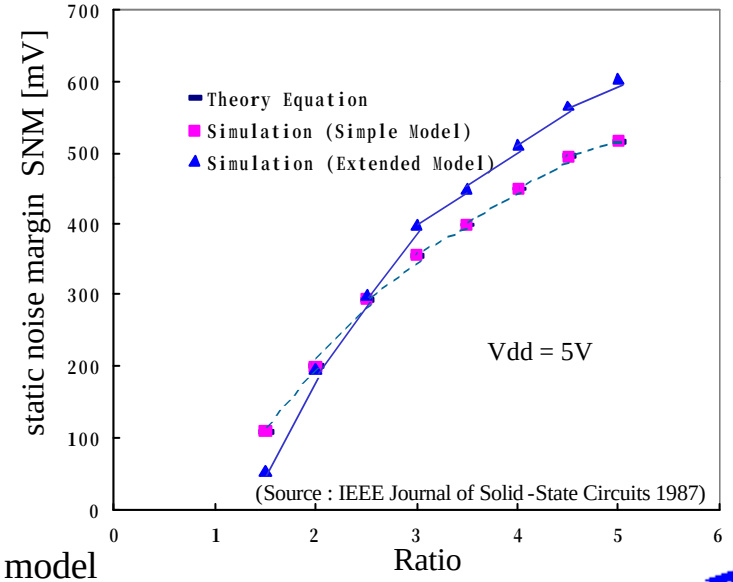
DC Transfer Characteristics



SNM with Supply voltage (From E. Seevink. et al. [12], 1987)



SNM with Cell ratio (From E. Seevink. et al. [12], 1987)



- Good correlation between theory equation and simple model
- Slope difference for the extended model simulation
  --> caused by omitted short channel effect from the simple model

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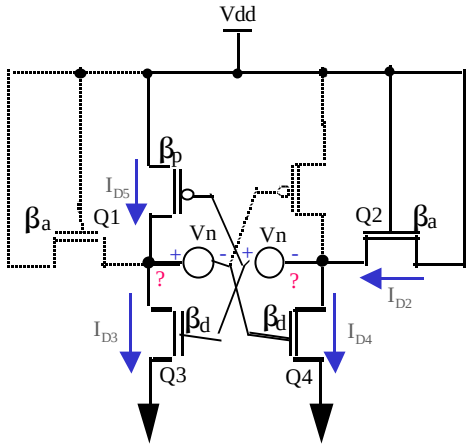
Static-Noise margin (SNM) for Full CMOS Cell (From E. Seevink. et al. [12], 1987)

Assumption

- Q2, Q3 : Saturation Region
- Q4, Q5 : Linear Region



MOS Models

- $Id = 1/2\,\beta\,(Vgs - Vth)^2$ Saturation Region
- $Id = \beta\,Vds\,(Vgs - Vth - 1/2\,Vds)$ Linear Region

  where $\beta = W/L \cdot \mu\,eff\,Cox$

Analytic Expressions

- Kirchhoff Current Equation

  $Id3 = Id5$, $Id2 = Id4$

- Kirchhoff Voltage Equation

  $Vgs3 = Vn + Vds4$

  $Vgs5 = Vdd - Vn - Vds4$

  $Vds5 = Vdd - Vn - Vgs4$

  $Vgs2 = Vdd - Vds4$

Results

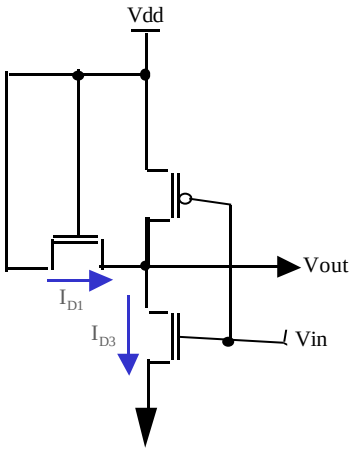
$$SNM\,(Vn_{(MAX)}) = Vth - \frac{1}{(k+1)}\left[\frac{Vdd - \frac{2\gamma+1}{\gamma+1}Vth}{1 + \frac{\gamma}{k(\gamma+1)}} - \frac{Vdd - 2Vth}{1 + k\frac{\gamma}{q} + \sqrt{\frac{\gamma}{q}\left(1 + 2k + k^2\frac{\gamma}{q}\right)}}\right]$$

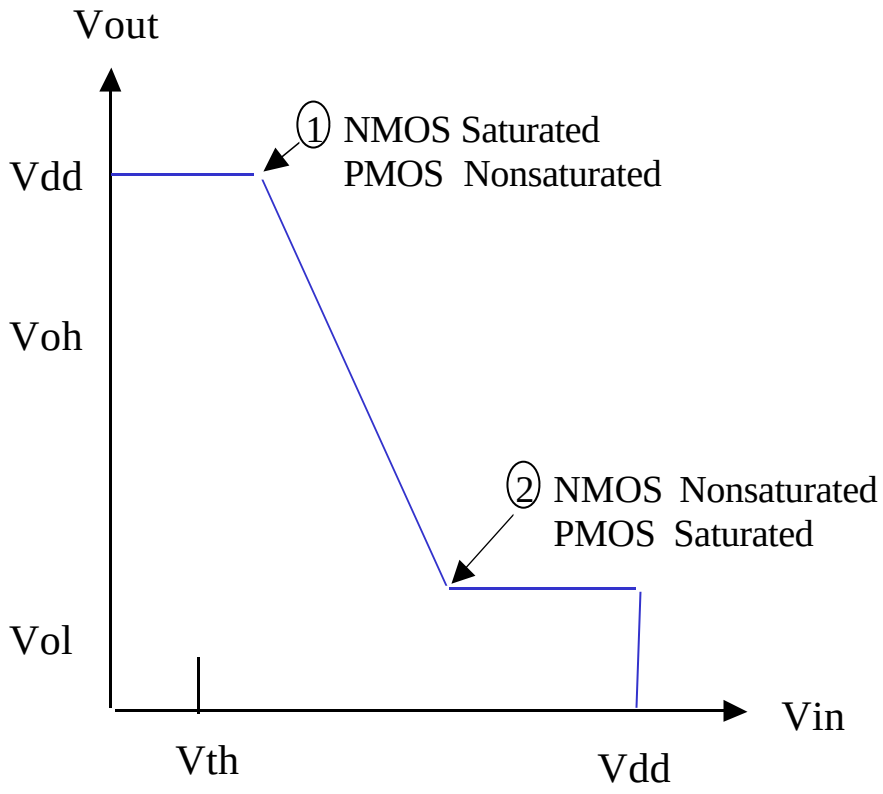
where γ (Cell Ratio) $= \beta_d / \beta_a$ $\quad q = \beta_p / \beta_a$

$$k = \frac{\gamma}{\gamma+1}\left(\sqrt{\frac{\gamma+1}{\gamma+1 - Vs^2/Vr^2}} - 1\right) \qquad k = Vs - \frac{\gamma}{\gamma+1}Vth$$

$$Vs = Vdd - Vth$$

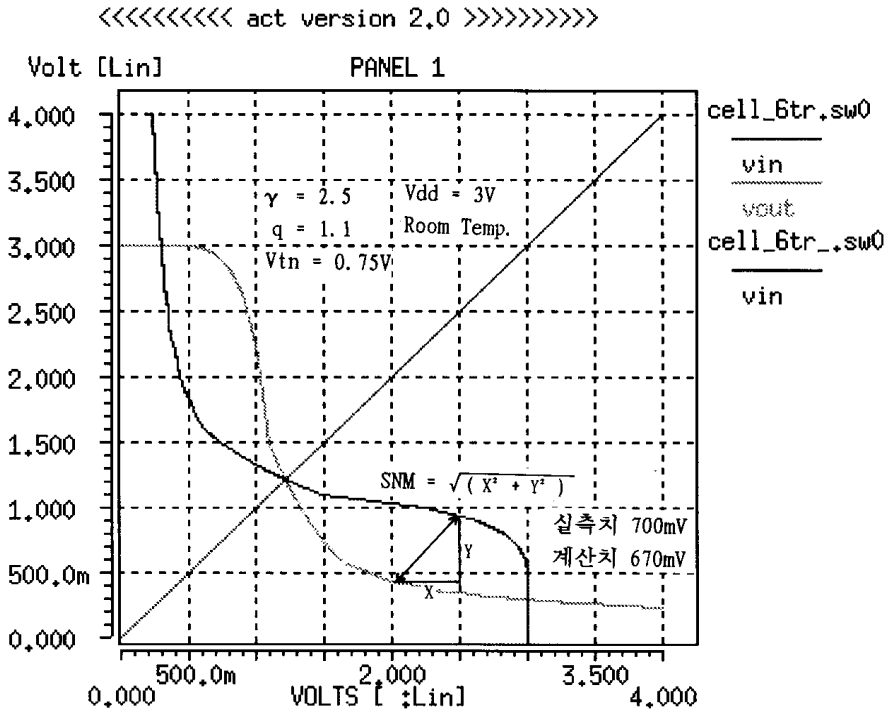
Saturated Enhancement Load Inverter





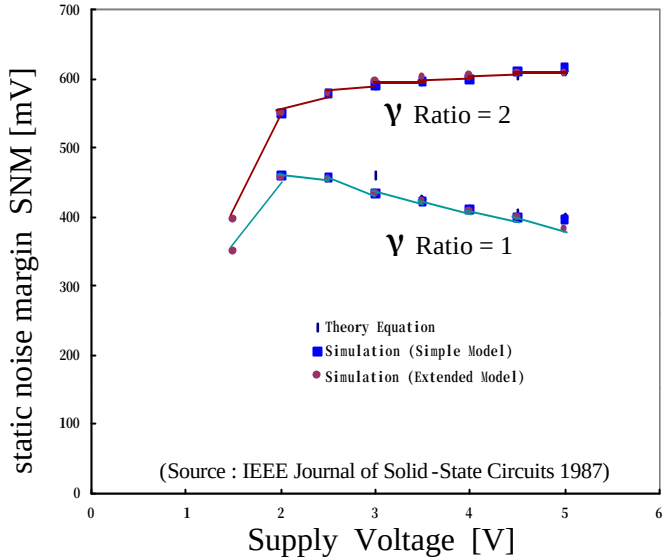
SNM of Full CMOS Cell

DC Transfer Characteristics

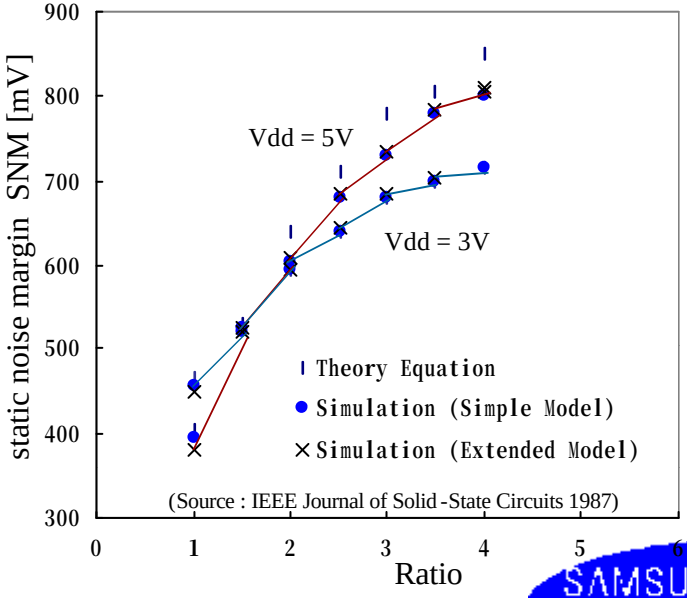


- Good correlation between theory equation and simulation
  --> Short channel effect is compensated by the PMOS transistor.
- Optimum SNM can be obtained through proper choice of ratio (r and q) for Vdd.

SNM with Supply voltage (From E. Seevink. et al. [12], 1987)



SNM with Cell ratio (From E. Seevink. et al. [12], 1987)



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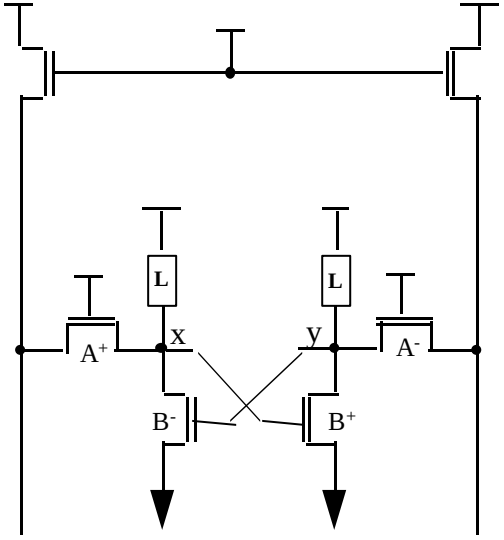
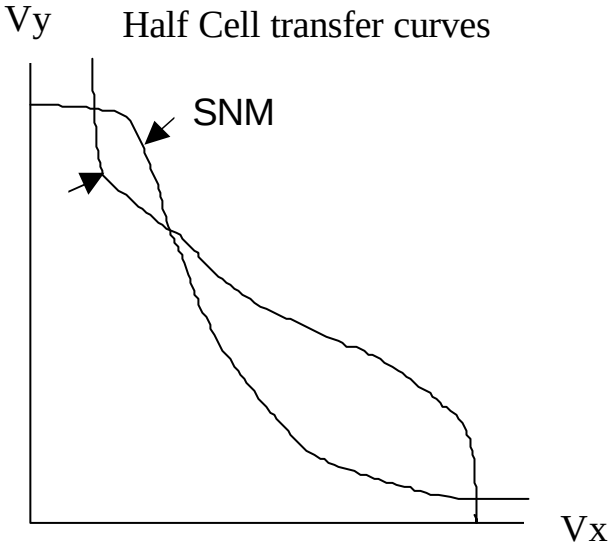
Static-Noise Source (Vn)

- DC Disturbance
  - . Layout Pattern Offset
  - . Process mismatches
    - : Non-uniformity of ion-implantation or Gate oxide thickness etc.
- Dynamic Disturbance
  - . Alpha(α) Particles
  - . Crosstalk
  - . Voltage supply ripple
  - . Thermal noise

Memory cell Asymetry





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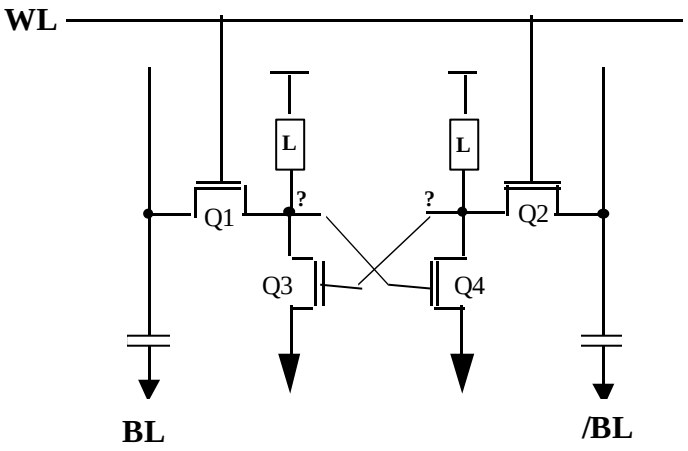
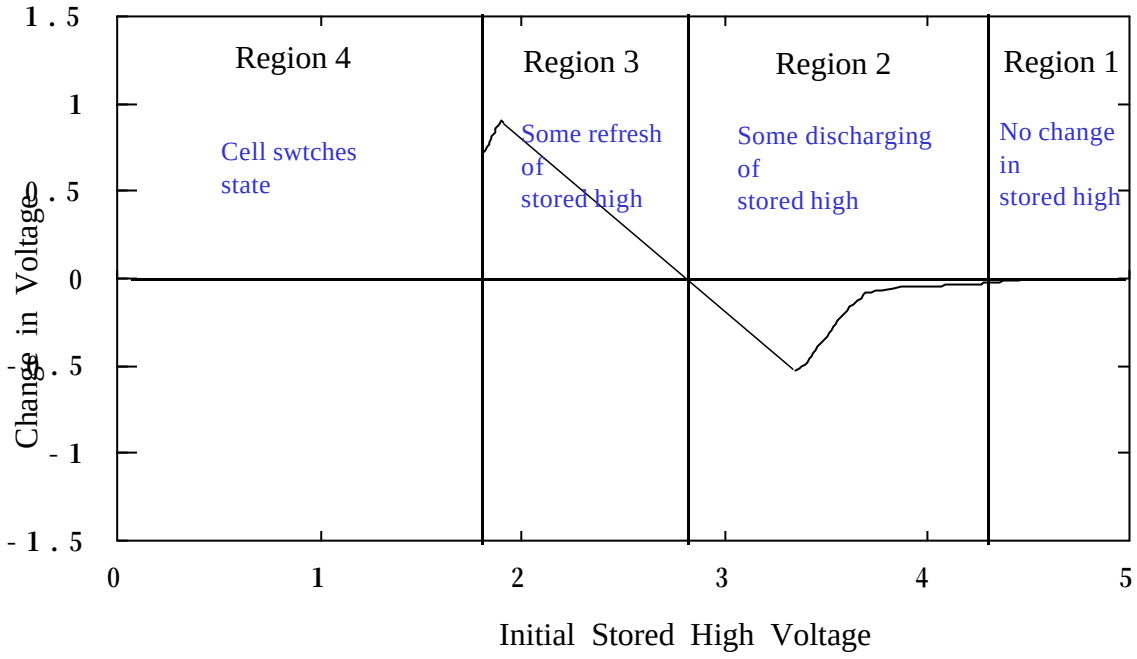
2-3-2. Dynamic-Noise Margin (DNM) (From Barbara Chappel. et al. [13], 1985)



Assumptions

- Q2, Q3 : Weaker Device
  - . High Threshold Voltage
  - . Longer channel Length
  - . Narrow channel width
- BL and /BL are precharged to Vdd



(1) Region 1

- The device on the high node of the cell (Q3) did not conduct during the read.

(2) Region 2

- Current through Q3 caused some discharging of the stored high during the read
- the voltage on the low node ??having increased enough to turn Q3 momentarily while the large precharged bitline capacitance was being discharged.

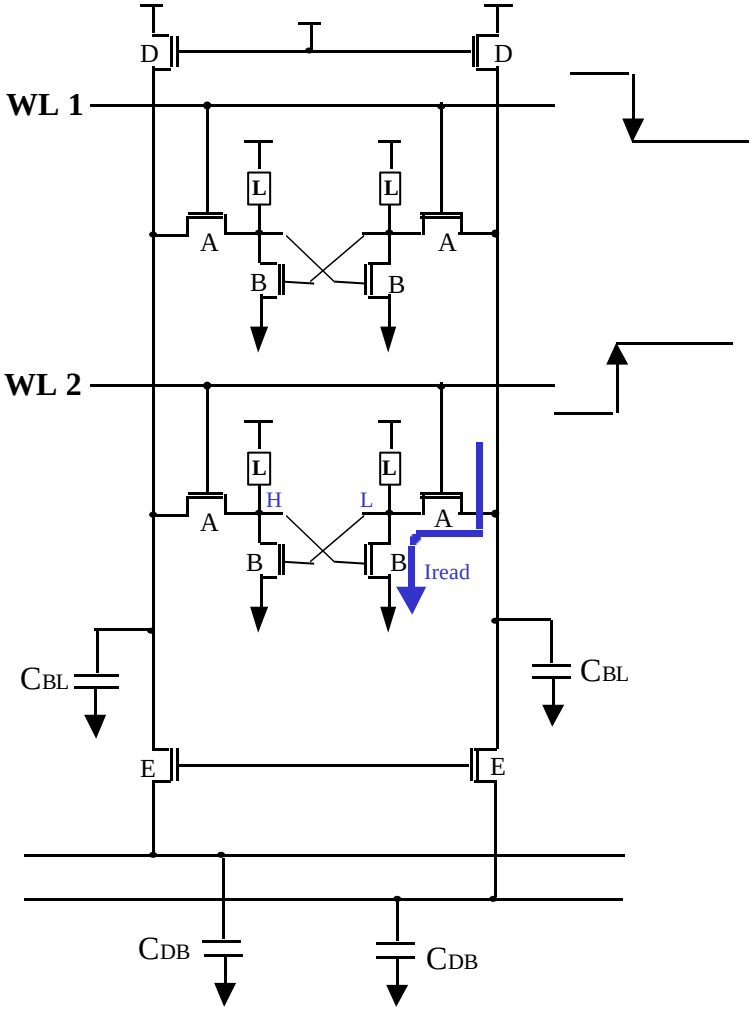
(3) Region 3

- The current through Q3 more than compensated the discharge current through Q1.

(4) Region 4

- The cell switches to the opposite state because the devices have been mismatched.

2-4. SRAM Cell Speed and Power



$$dt = [\ Ctot\ /\ Iread\ ]\ dV$$

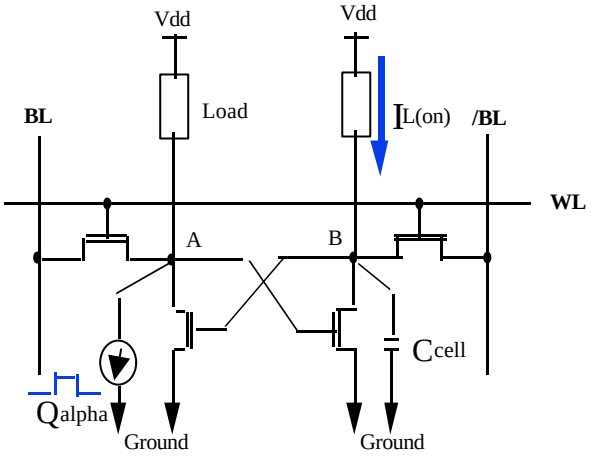
Where **dt** is read speed for core(bit line and data bus line) operation.

Ctot is capacitance load fixed by SRAM density.

Iread is cell current fixed by pass gate size (A)

dV is voltage swing fixed by ratio (D : A)

2-5. Memory Cell Alpha Particle Sensitivity



delta V = Qalpha / Ccell

To improve SER immunity

- Decreasing Q alpha [14]
  - . Polyimid coating (blocks alphas)
  - . Adopting a p-well structure is useful in reducing the collection efficiency
  - . The area ratio of n+ storage region(A and B) to the other n+ region(Vdd and Ground., etc) has to be small to reduce the collection efficiency
  - . The two individual storage nodes(A and B) are placed closely.
- Decreasing Charging Time of the High Storage Node [15]
  - . use DWL(Divided Word Line) architecture to increase average interval time (t_i)
  - . use TFT(Thin Film Transistor) Load or Full CMOS cell to decrease Charging time (t_{ch})
- Balance the Load characteristics to improve the stability
- Increasing cell capacitance and cell stability (Cell size issue)

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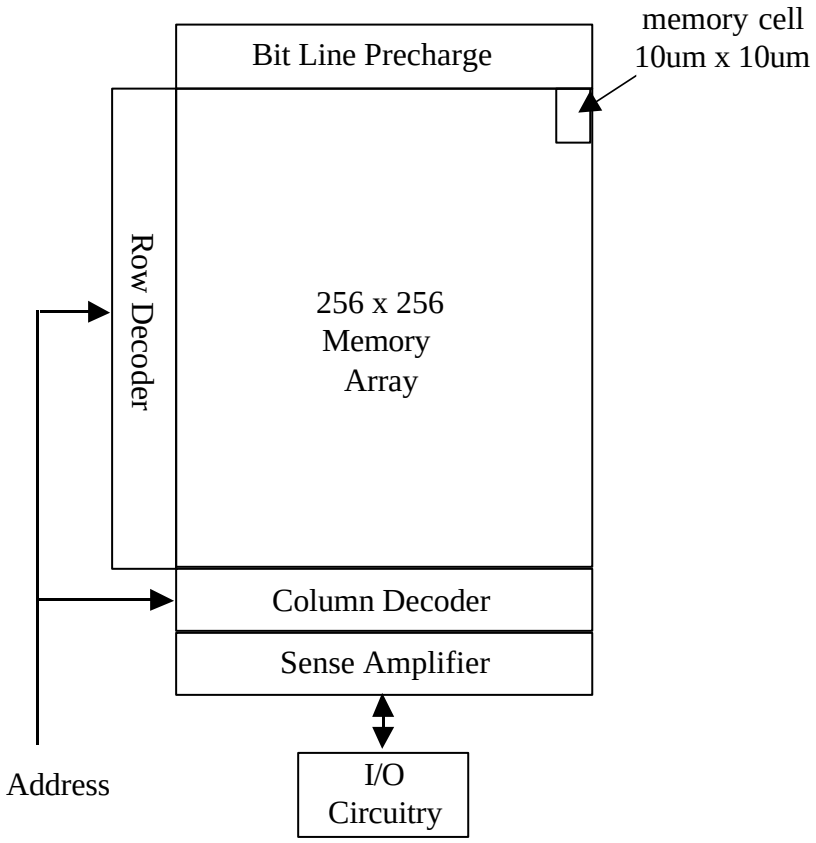
3. SRAM Chip Architecture

3-1. High Density SRAM Array

3-1-1. Problems

Example of 64K SRAM Architecture



- Power Dissipation for Read operation
  : 256 Column @ 100uA/Column
  = **25.6mA**

- Word Line Speed
  : Resistance (R) 256 x10um/1um x 5 Ohm/□
  = 12.8 Kohm
  : Capacitance (C) 2 x 256 Gates @ 2fF
  = 1.024 pF
  RC Delay = 13.1ns

- Bit Line Speed
  : Capacitance (C) 256 cells x 3.9fF/cell
  = 1 pF
  : Bit Line Slew Rate (dV/dt=Iread/C_{BL}) = 100mV/ns
  2ns for 200mV swing

Where Iread = 100uA/Column
Poly1(for Word Line) Resistance 5 Ohm/□
Line Width 1um
capacitance 2fF/gate
Bit Line Capacitance (C_{BL}) 3.9 fF/cell

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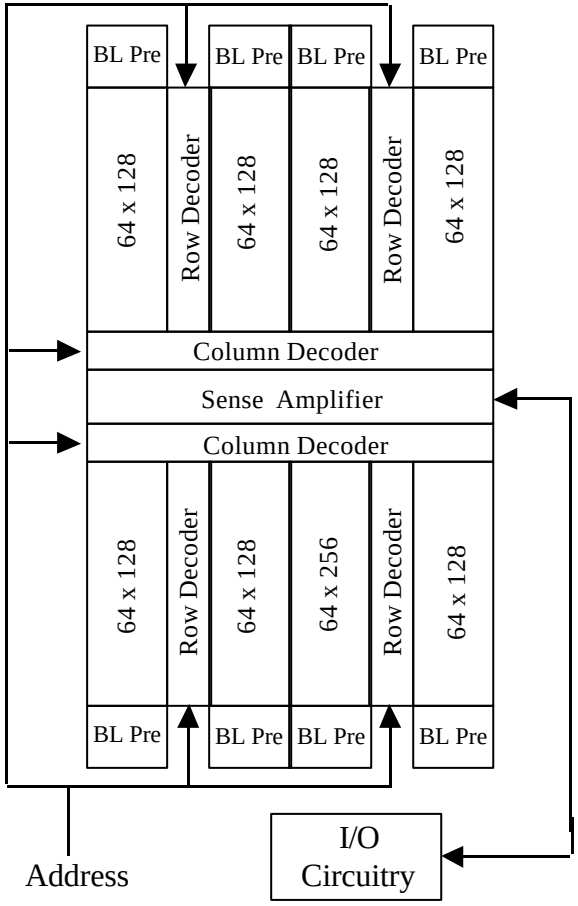
3-1-2. Divided Word Line & Bit Line Architecture

Example of 64K SRAM Architecture



- Power Dissipation for Read operation
  : 64 Column @ 100uA/Column
  = **6.4mA**

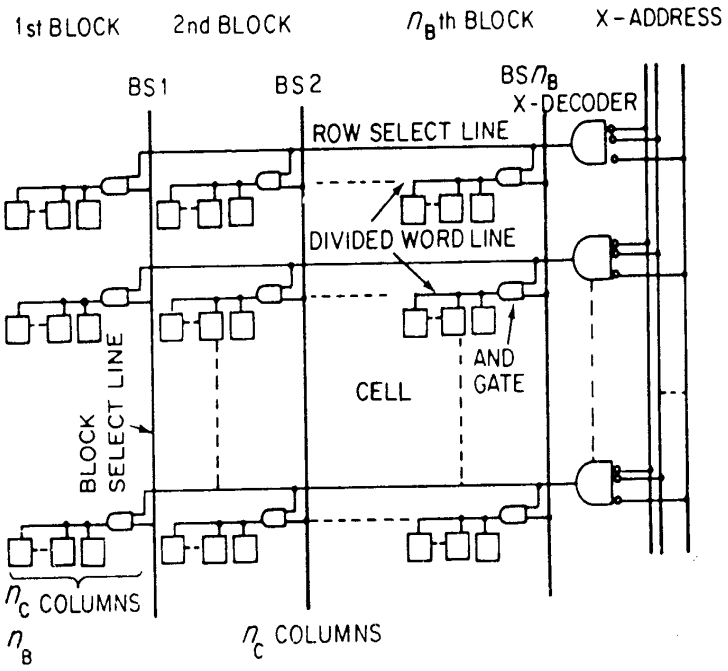
- Word Line Speed
  : Resistance (R) 64 x10um/1um x 5 Ohm/□
  = 3.2 Kohm
  : Capacitance (C) 2 x 64 Gates @ 2fF
  = 0.256 pF
  RC Delay = 0.8ns

- Bit Line Speed
  : Capacitance (C) 128 cells x 3.9fF/cell
  = 0.5 pF
  : Bit Line Slew Rate (dV/dt=Iread/C_{BL}) = 200mV/ns
  1ns for 200mV swing

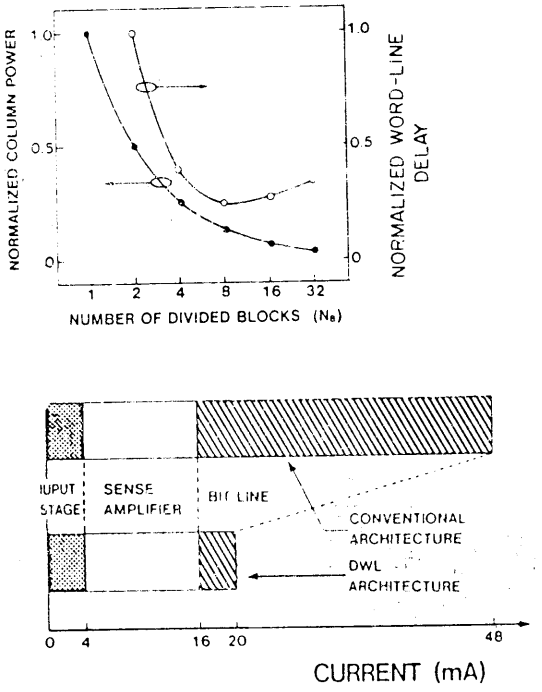
Where Iread = 100uA/Column
Poly1(for Word Line) Resistance 5 Ohm/□
Line Width 1um
capacitance 2fF/gate
Bit Line Capacitance (C_{BL}) 3.9 fF/cell

3-2. Chip Architecture for High Density SRAM

3-2-1. Divided word line (DWL) structure[16]

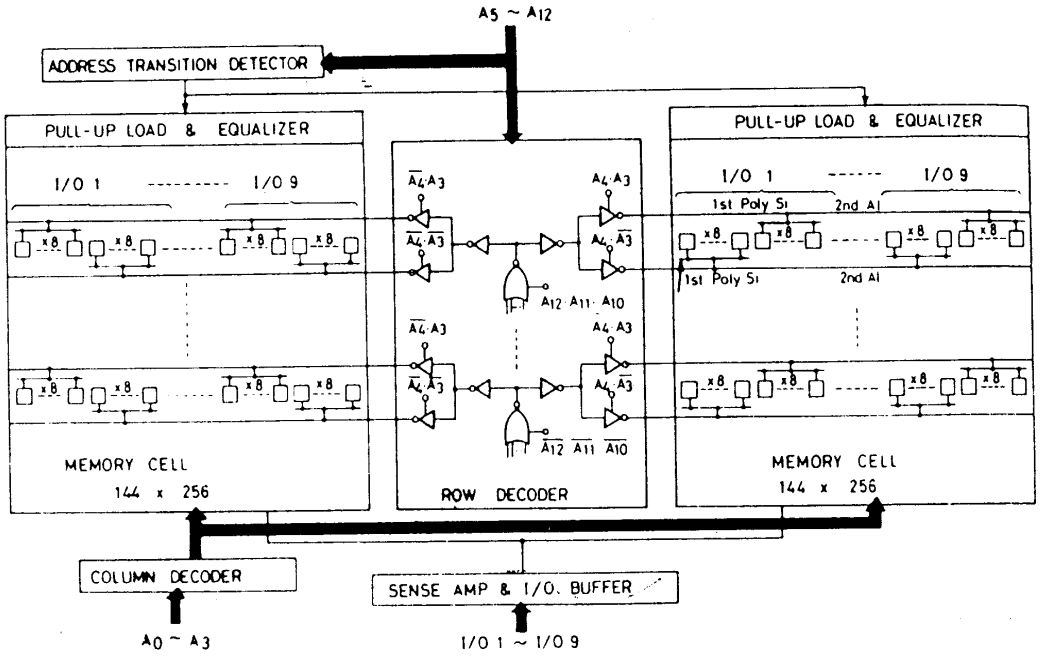


Simplified schematic concept of DWL



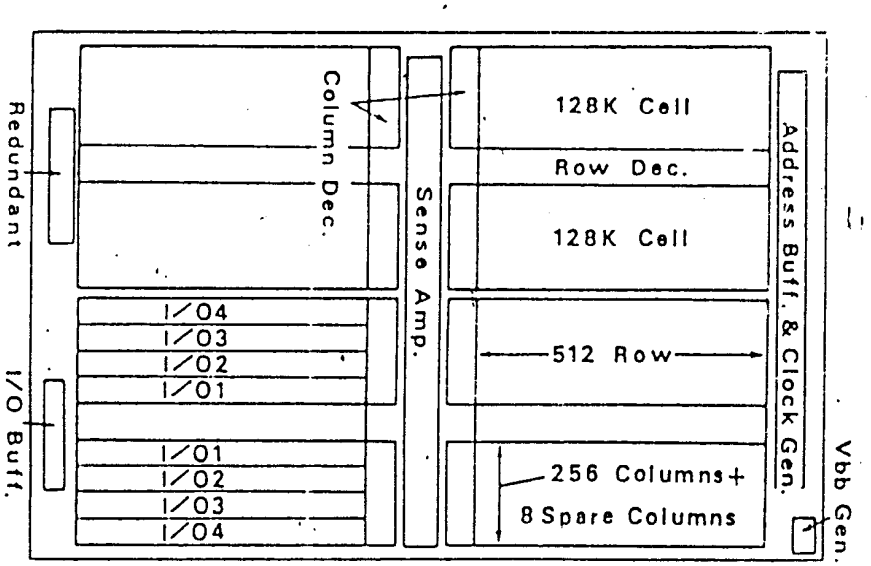
Performance enhancement on 64K RAM

3-2-2 Shared word-line and hierarchical word-line structure[17]



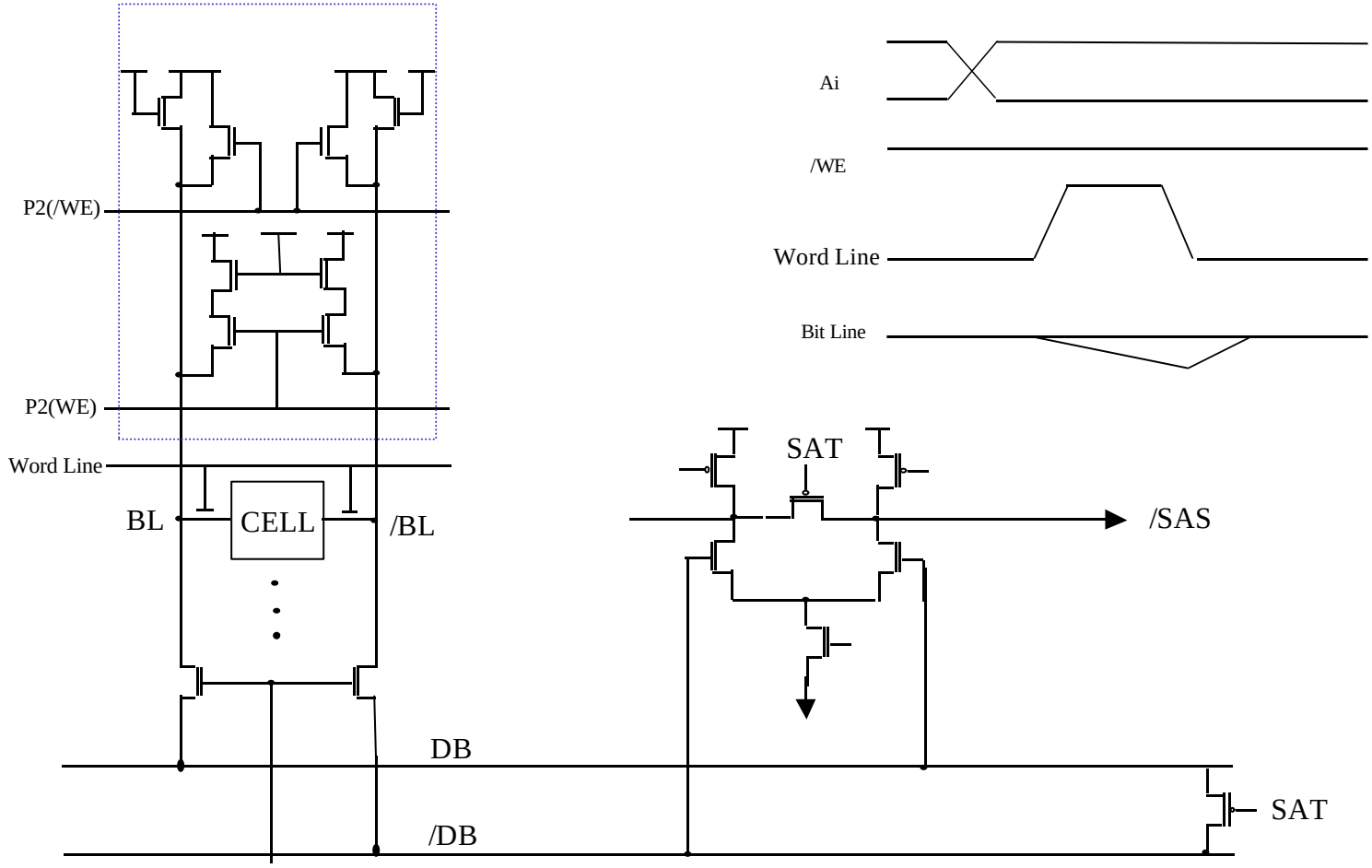
Shared word-line structure for a 72K SRAM

3-2-3 Divided bit-line structure[18]



Block diagrams of shorten the bit-lines

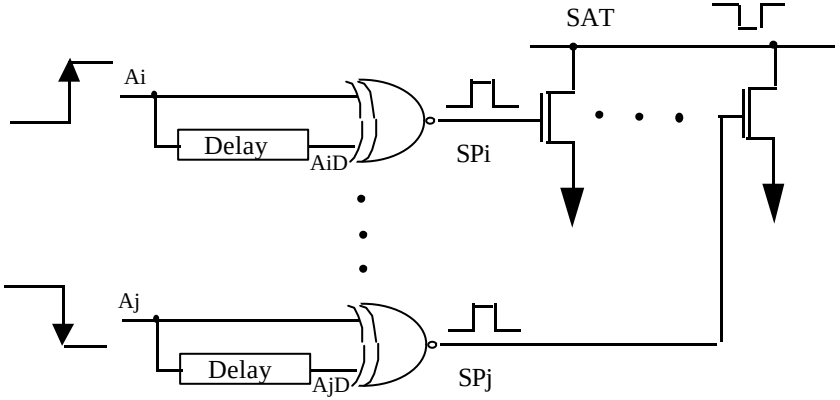
3-2-4. Variable Impedance Bitline Loads[19]

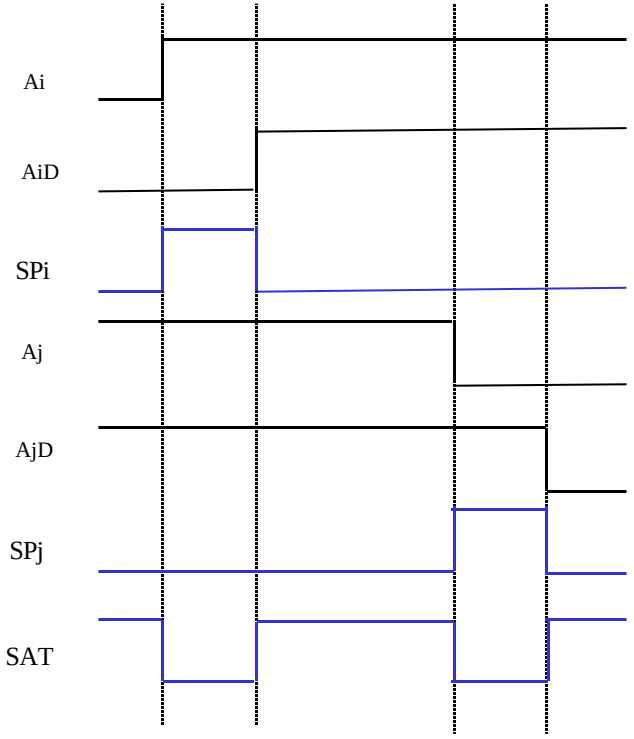


4. High Speed SRAM Circuit Technique

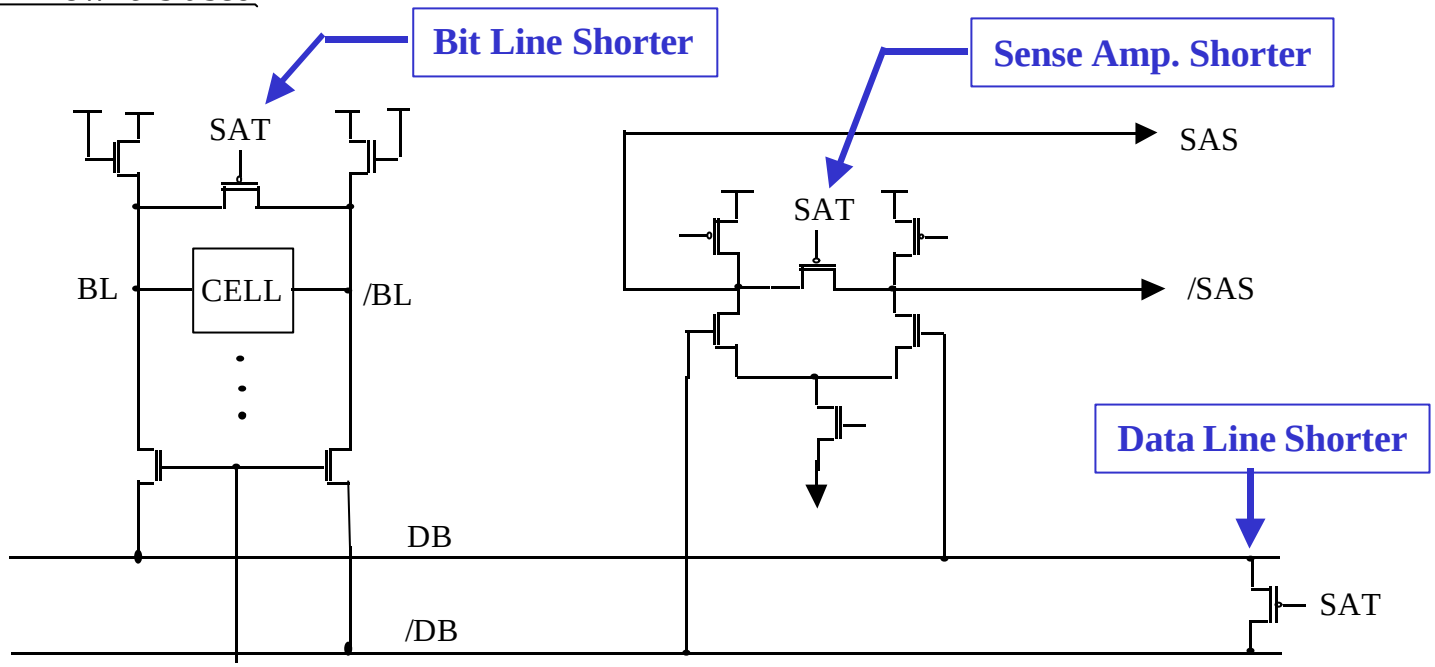
4-1. Address transition detection (ATD) for improved speed[20]

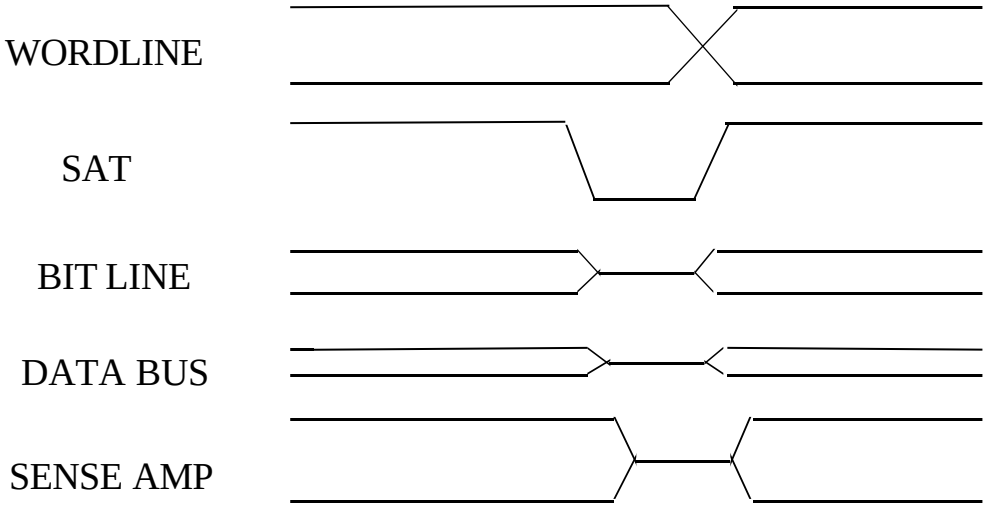
ATD - Address transition Detection





ATD - How it is used



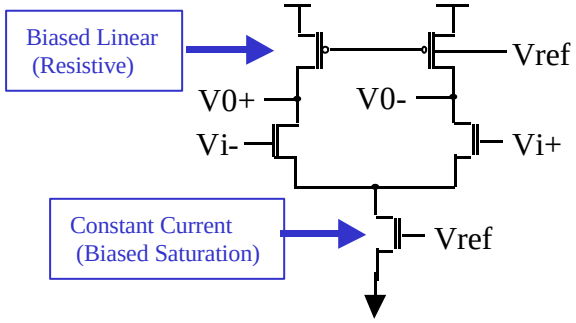


4-2. Fast sense amplifier

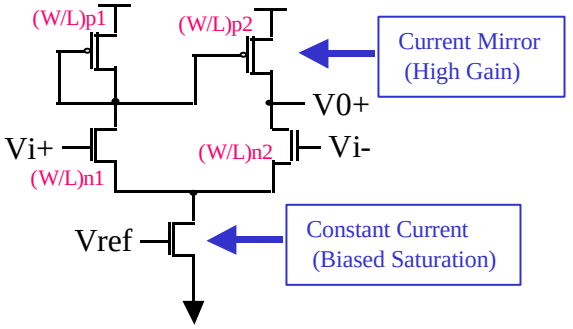
- Determine the sense amplifier scheme[21]
  . Current mirror amplifier with high CMRR(Common -mode rejection ratio)
  . Current multiplier with high driving capability
- Determine the number of stage

Data Sensing Scheme

CLASICAL
FULL DIFFERENTIAL



CURRENT MIRRIOR
SINGLE ENDED

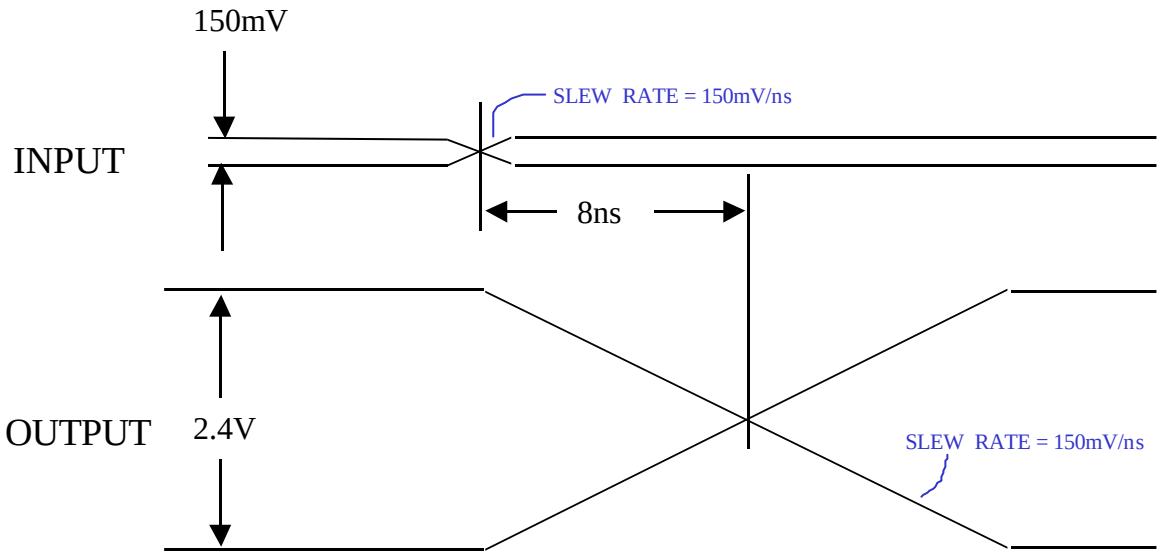


Current Mirrior: $\frac{(W/L)n2}{(W/L)n1} = \frac{(W/L)p2}{(W/L)p1} = 1$

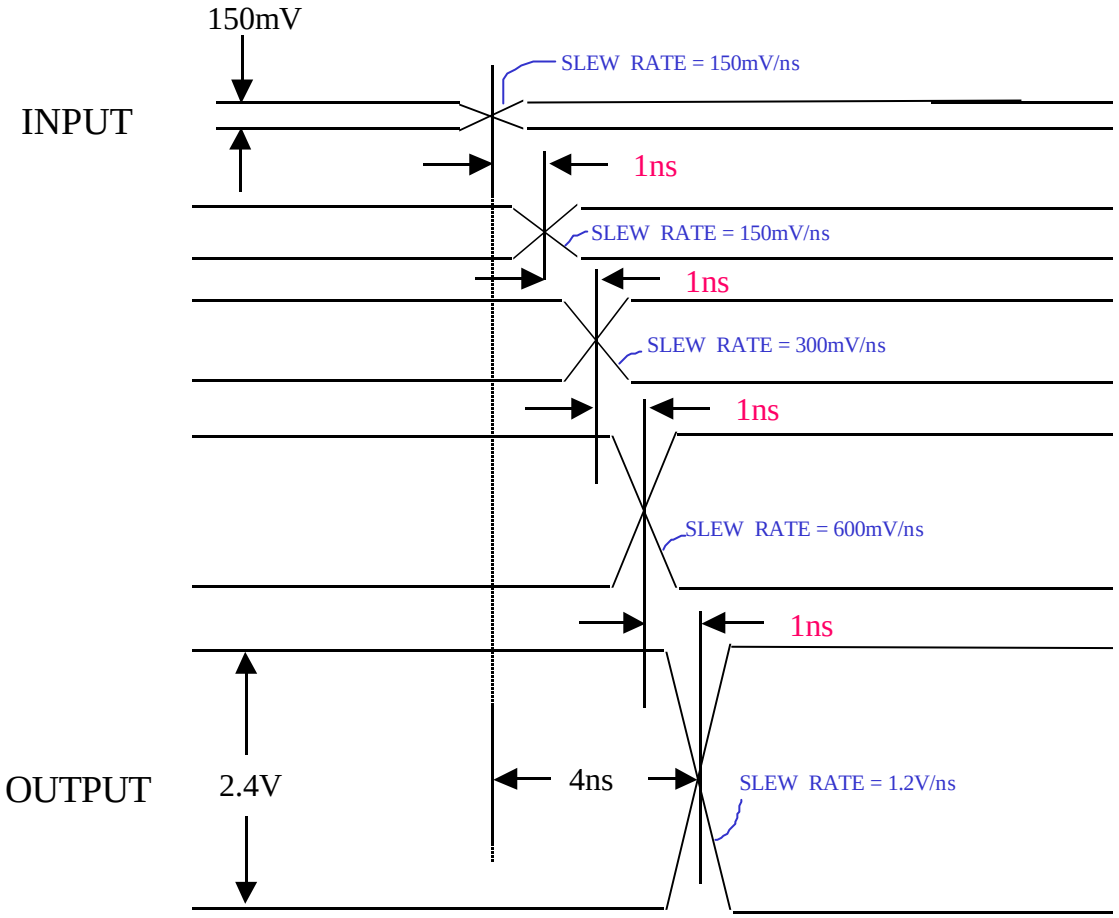
Current Multiplier: $\frac{(W/L)n2}{(W/L)n1} = \frac{(W/L)p2}{(W/L)p1} = N > 1$

Speed vs. Gain - How many stages?

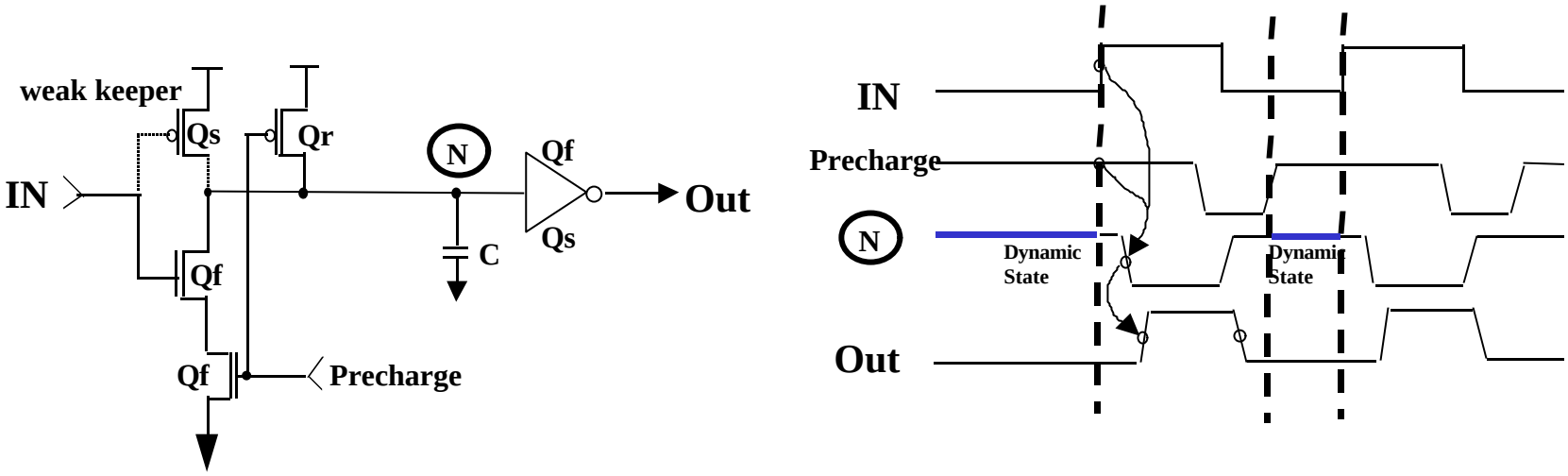
CASE 1: 1 Stage - A = 16



CASE 2: 4 Stage - A = 2



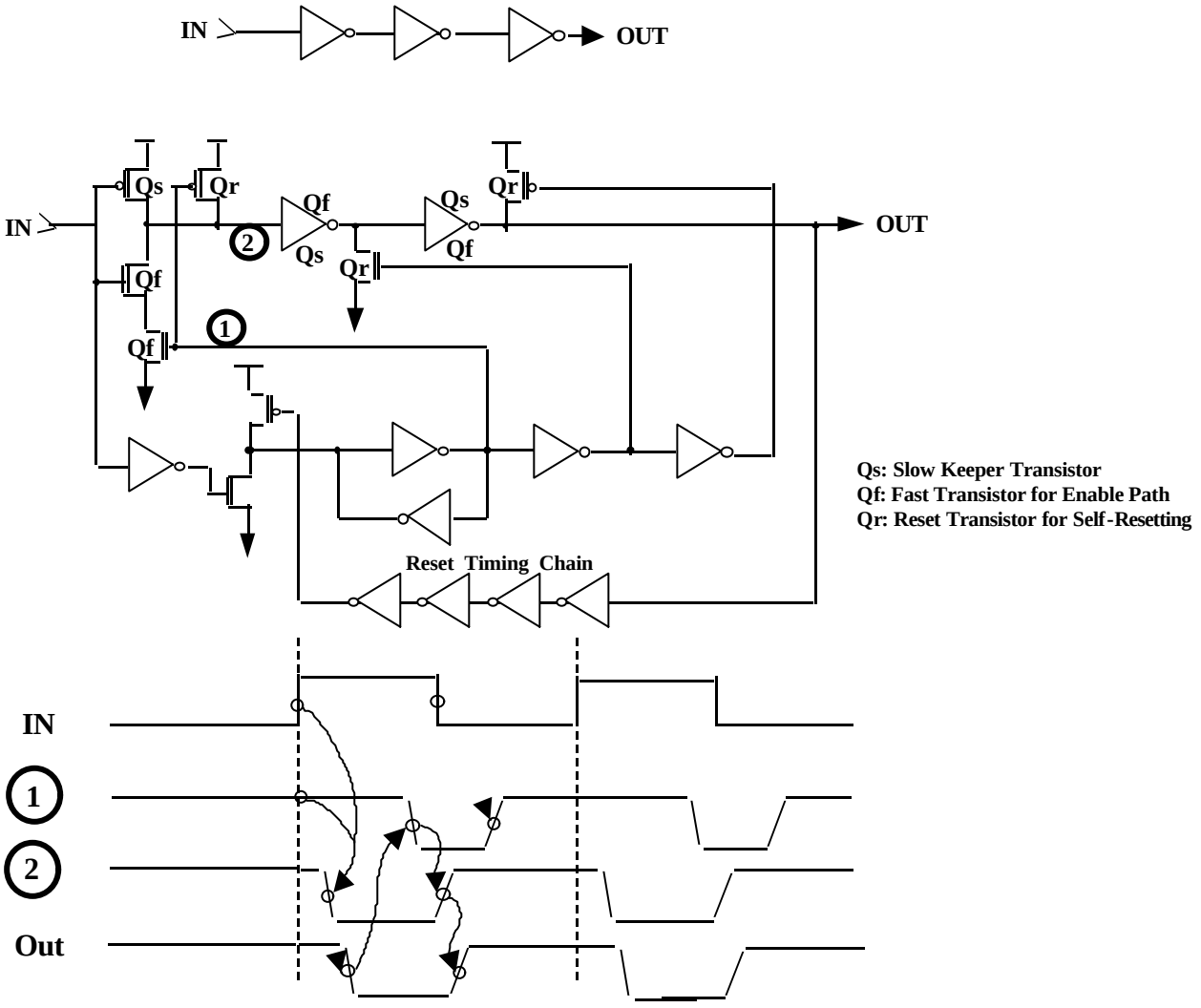
4-3. Dynamic circuitry[22]



- Separate pull-up and pull-down operation during transition time.
- Lower the loading on output driver.
- Decrease the switching logic threshold.

Basic Dynamic gate

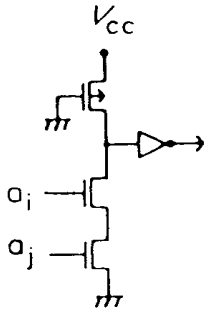
(From T. Chappell et al. [23], 1991)



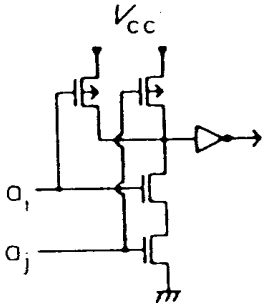
4-4. Fast datapath (From Sasaki, K. et al. [24], 1988)

- Reduce the address decoder delay using PMOS load decoders and Divided wordline Architecture
- Short bit-line & Data Bus using 90^{o} rotated architecture

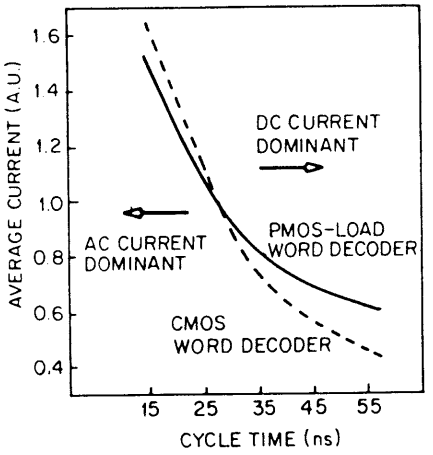
Address Decoder



PMOS load decoder

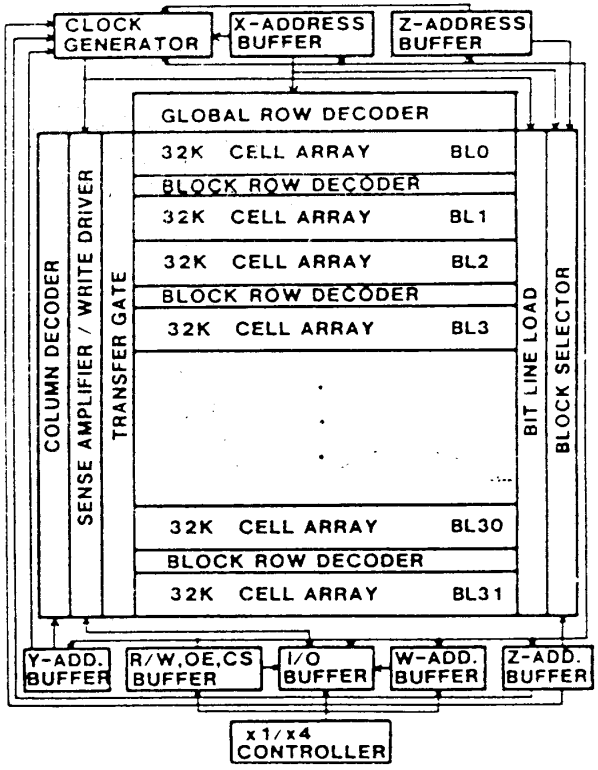


CMOS load decoder



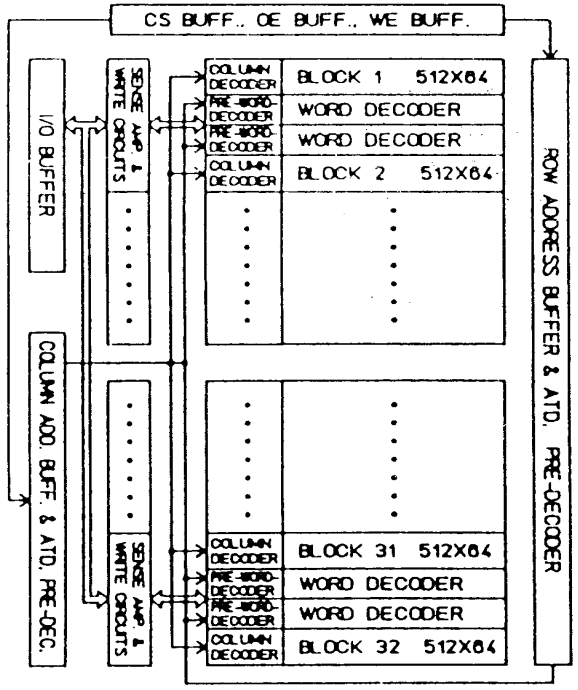
trade-off in current and cycle time

Short bit-lines Architecture



traditional orientation of word-lins and bit-lines

(From Kohno, Y et al. [25], 1988)



layout at 90 ^{o} to traditional orientation intended to shorten the bit-lines

(From Sasaki, K. et al. [24], 1988)

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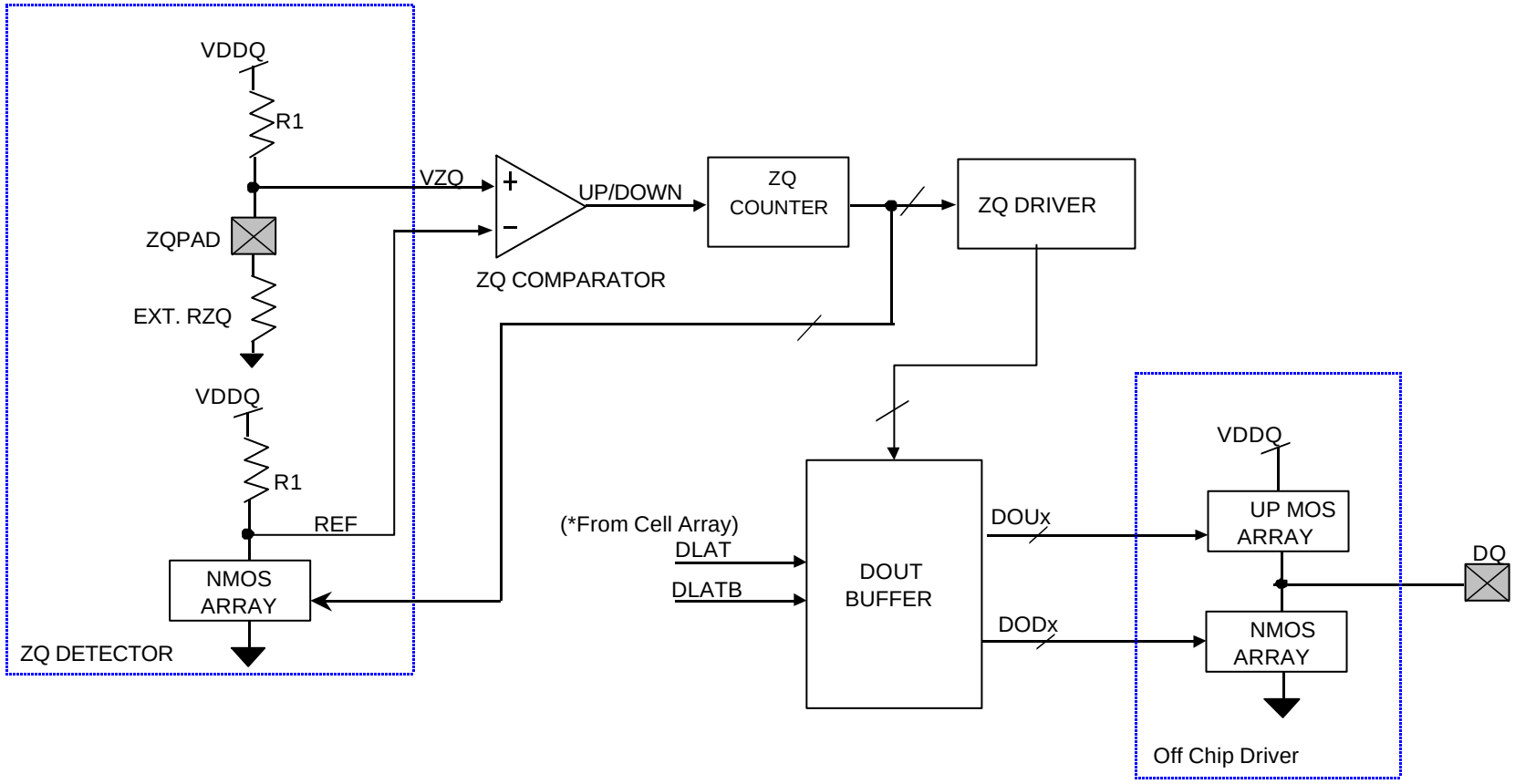
4-5. Interface Circuit Technique

- Reduce the impedance variation with temperature and voltage

Impedance Controlled Output Driver Scheme (From Pilo, H. et al. [26], 1996)



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