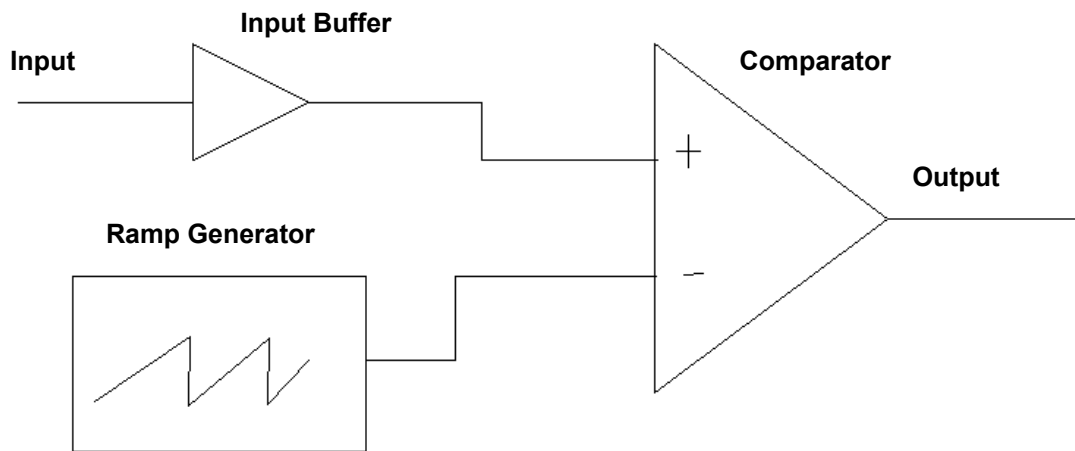
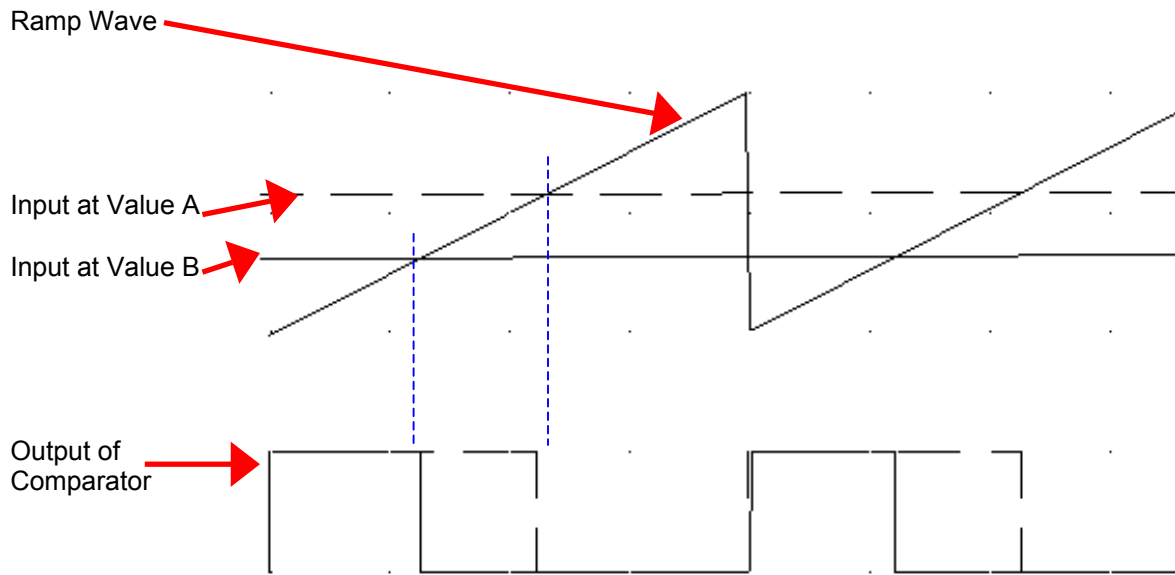


Pulse Width Modulator

Pulse Width Modulators, often simply called PWMs, are common to many systems where an average value is needed. These can be digital signals that produce a crude analog signal by adding bits and totally analog systems that use the changing pulse width to control. Prominent examples are switched mode power supplies that change the pulse width to vary the output voltage, efficient DC motor drives that vary pulse widths vary the motor shaft speed or such things as changing the perceived brightness of an LED. All of these make use of the three simple parts of the PWM: the Ramp Generator, the Input Buffer, and the Comparator.



First a quick discussion of the theory of operation of a Pulse Width Modulator. The three parts of a PWM are the comparator, the ramp generator, and the input buffer. The pulse comes out of the comparator and the rising edge occurs when the ramp wave falls below the input. The pulse stays high until the input is greater than the ramp voltage. This is shown in the figure below. The essential relationship is that the larger the input the longer the pulse lasts. (Value A is greater than Value B.) The two extremes of this are when the input is always greater than the ramp the comparator output is always high and when the input is less the ramp the output is always low.



Creating a Pulse Width Modulator in an Anadigmvortex IC requires three simple parts: the ramp or sawtooth generator, the input buffer, and the comparator.

The ramp generator sets the frequency or period of the stream of pulses produced by the PWM. A sawtooth or ramp waveform fixes one edge of the pulse so it is easier to understand than a triangle wave, which causes both edges of the pulse to vary, but either is valid. Attachments to this note are sawtooth wave files for 10kHz, 20kHz, 25kHz, and 40kHz. The choice of frequency depends on the precise application of the PWM and is a trade off between wider bandwidth for greater granularity. An additional consideration is whether the pulse frequency causes interference with other circuit elements or even audible noise.

The comparator CAM compares the input to the ramp and is simple with only 2 settings. The “Compare to” needs to be set to “dual input”. You can also choose a hysteresis value.

The Input Buffer needs a Sample and Hold function but has many possibilities. A simple gain and hold stage can be inserted such as the **GAIN HOLD CAM** which would save on chip resources. It is also easy to add Lead-Lag compensation with the **Filter Bilinear CAM** in a **Pole & Zero** mode. To this compensation could be added a summing

The screenshot displays the Proteus ISIS simulation environment. The main workspace shows a circuit diagram of a SAR ADC. The circuit includes an AN221E04 comparator, a Z⁻¹ delay block, a H2 histogram block, and a 10 mV voltage source. The circuit is connected to a power supply and ground. The Resource Panel on the right shows the components used in the circuit, including the AN221E04 comparator and the Z⁻¹ delay block.

07Sep04