Reduction of CMOS Inverter Ring Oscillator Close-In Phase Noise by Current Mode Instead of Voltage Mode Supply

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***Abstract*—A reduction of low frequency flicker noise caused close-in phase noise in single-ended CMOS inverter ring oscillators is observed when a current mode supply is used instead of a voltage mode supply. Measurements show a 4 to 6 dB reduction at the same oscillation frequency and oscillator core power consumption. An analytical explanation of the reduction is derived by calculating the deviation of the oscillation cycle time resulting from a slowly changing perturbation of the drain average peak currant of a particular MOSFET for both cases. It is shown that the perturbed drain current causes all the other MOSFETs' drain currents to deviate contrary to the causing perturbation in current mode, thus reducing the overall cycle time deviation and close-in phase noise. The current mode supply is shown to be realizable by a large gate area MOSFET operating as a current source.**

I. INTRODUCTION

CMOS ring oscillators can offer extremely wide frequency tuning range and maximum operating frequencies in the several GHz range when implemented in modern CMOS-technologies [1]-[3]. This large tuning range would be interesting for applications in coming ultra-wideband (UWB) systems, in reconfigurable multi-frequency systems and in multi-bit-rate transmission systems. But due to the lack of a high quality resonator, ring oscillators usually have much larger phase noise [4] than small tuning range LC-oscillators. In particular, the flicker noise caused $1/\Delta f^3$-region of their phase noise spectrum is wide. Thus, some method to reduce the flicker noise caused phase noise of CMOS inverter ring oscillators could expand their field of application.

The oscillation frequency of a CMOS inverter ring oscillator can be tuned either by adjusting its core supply voltage V_{DD} or its core supply current I_{DD} (Fig. 1). Apart from implementation issues of the variable voltage or current supply, the two methods first seem to be equivalent if appropriate V_{DD}- or I_{DD}-values are set up to get a desired oscillation frequency. But the two supply modes differ with respect to the close-in phase noise. An analytical comparison will be presented in the 2nd section of this paper. The 3rd section presents the simulation of a ring oscillator with ideal voltage and current mode supply. Section 4 presents measurement results of a ring oscillator with MOSFET current source, and section 5 concludes.

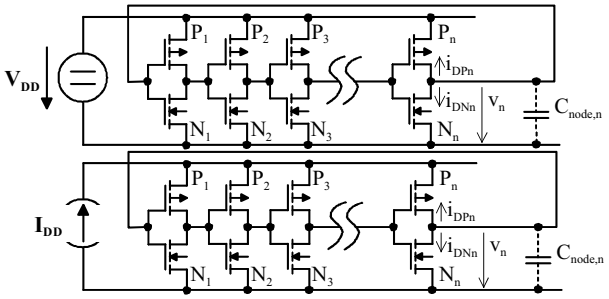

Figure 1. Ring oscillator with voltage mode (top) and current mode supply (bottom).

II. CYCLE TIME DEVIATION ANALYSIS

The basic idea of the analysis is that close-in phase noise in the $1/\Delta f^3$-region originates from low frequency fluctuations of the CMOS inverter propagation delay times. The delay time fluctuations again are caused by slowly changing perturbations of the MOSFETs' drain average peak currents due to low frequency flicker noise [5].

First, the cycle time T of the ring oscillator is determined. This calculation is valid both for voltage mode supply and for current mode supply. The rise and fall times of the i^{th} oscillator node voltages $v_i(t)$ can be expressed as

$$t_{HLi} = \frac{C_{node,i} V_{DD}}{\hat{I}_{DNi}}, \quad t_{LHi} = \frac{C_{node,i} V_{DD}}{\hat{I}_{DPi}}, \qquad (1)$$

where $\hat{I}_{DNi}$ and $\hat{I}_{DPi}$ are defined as the average peaks (average referred to the time interval t_{HLi} or t_{LHi}) of the NMOS and PMOS drain currents i_{DNi} and i_{DPi} that discharge and charge

the node capacitance $C_{node,i}$. The propagation delays for falling and rising edges are estimated as

$$t_{pHLi} = \tfrac{1}{2} t_{HLi}, \quad t_{pLHi} = \tfrac{1}{2} t_{LHi}. \tag{2}$$

The sum of all n falling- and n rising-edge propagation delays is the cycle time T of the n-stage ring:

$$T = \sum_{i=1}^{n} (t_{pHLi} + t_{pLHi}). \tag{3}$$

For identical CMOS inverters and for noiseless currents, the cycle time T_0 is

$$T_0 = \sum_{i=1}^{n} \left(t_{pHL} + t_{pLH}\right) = n\left(t_{pHL} + t_{pLH}\right). \tag{4}$$

To ease the calculations, an oscillator with symmetric inverters (i.e. the inverters optimized for equal PMOS and NMOS average peak currents) is investigated:

$$\hat{I}_{DN} = \hat{I}_{DP} = \hat{I}_D. \tag{5}$$

The propagation delay time t_p and the cycle time T_0 of the noiseless oscillator are then given as:

$$t_{pHL} = t_{pLH} = t_p, \tag{6}$$

$$T_0 = \sum_{i=1}^{n} \left(t_{pHL} + t_{pLH}\right) = 2nt_p. \tag{7}$$

Now, one particular NMOS transistor in the k^{th} stage that exhibits flicker noise is considered. It causes a different cycle time deviation in voltage and current mode. To ease the following analysis, all other transistors and the core supply voltage V_{DD} or the core supply current I_{DD} are assumed to be noiseless. The overall cycle time deviation power is the sum of all cycle time deviation powers that originate from the individual MOSFET noise sources.

The gate referred flicker noise voltage of the MOSFET causes a low frequency modulation of the drain average peak current $\hat{I}_{DNk}$. As the temporal change of this noise voltage is in the kHz to MHz range and the oscillation signal is in the GHz range, the perturbation $\Delta\hat{I}_{DNk}$ of the drain average peak current from its nominal value $\hat{I}_D$ can be regarded as approximately constant during a lot of oscillation cycles:

$$\hat{I}'_{DNk} = \hat{I}_D + \Delta\hat{I}_{DNk} = \hat{I}_D\left(1 + \Delta_{Nk}\right), \quad \Delta_{Nk} << 1. \tag{8}$$

The normalized perturbation Δ_{Nk} of the drain average peak current causes a deviation ΔT of the cycle time T from its nominal value T_0. A simple calculation of perturbations is now applied to determine ΔT separately for voltage mode and current mode supply.

A. Voltage Mode Supply

The disturbed delay for the falling edge in inverter k is approximated as (with (8)):

$$t'_{pHLk} = \frac{C_{node} V_{DD}}{2\hat{I}'_{DNk}} \approx t_p\left(1 - \Delta_{Nk}\right). \tag{9}$$

As the supply voltage V_{DD} is constant and all other drain currents are considered to be noiseless, the other delays do not change:

$$t'_p = \frac{C_{node} V_{DD}}{2\hat{I}_D} = t_p. \tag{10}$$

By adding all delay times according to (3), we can calculate the deviated cycle time $T_{V\text{-}mode}$ in voltage mode due to the NMOS drain current normalized perturbation Δ_{Nk} in the k^{th} stage:

$$T_{V-mode} = (2n-1)t'_p + t'_{pHLk} \approx T_0\left[1 - \frac{\Delta_{Nk}}{2n}\right]. \tag{11}$$

The normalized deviation of the cycle time is

$$\Delta_{T,V-mode} = -\frac{\Delta_{Nk}}{2n}. \tag{12}$$

B. Current Mode Supply

For current mode supply, we have to consider the oscillator core current I_{DD}. By assuming that each NMOS average peak current $\hat{I}_{DNi}$ flows during the time interval t_{HLi} within the oscillation period, the current I_{DD} can be calculated as the average current that sums up at the negative supply rail of the oscillator core (see fig. 1):

$$I_{DD} = \sum_{i=1}^{n}\left(\frac{t_{HLi}}{T}\hat{I}_{DNi}\right) = \frac{2n}{\sum_{i=1}^{n}\left(\frac{1}{\hat{I}_{DNi}} + \frac{1}{\hat{I}_{DPi}}\right)}. \tag{13}$$

If we assume the considered particular drain current to be increased (decreased) by flicker noise, then all the other currents have to decrease (increase) from their nominal value, as the current I_{DD} is forced to be constant by the external current source.

The deviation of the noiseless currents due to the single NMOS introducing the flicker noise perturbation at node k can be calculated with (13):

$$\hat{I}'_D \approx \hat{I}_D\left(1 - \frac{\Delta_{Nk}}{2n}\right). \tag{14}$$

The decrease (increase) of the noiseless currents requires the core oscillator voltage V_{DD} to decrease (increase) to a new value V'_{DD}. The capacitance of the oscillator core V_{DD}-node to ground has to be small to make the reaction of the voltage V_{DD} to the causing drain current perturbation faster than the temporal change of the perturbation itself. The new value V'_{DD} is governed by the current law $\hat{I}_D(V_{DD})$ (which is closely related to the DC current law $I_D(V_{GS})$). An approximate first order series expansion of this current law results in

$$\hat{I}'_D = \hat{I}_D + g_m\left(V'_{DD} - V_{DD}\right), \tag{15}$$

and the new core voltage V'_{DD} follows:

$$V'_{DD} = V_{DD}\left(1 + \frac{\hat{I}'_D - \hat{I}_D}{g_m V_{DD}}\right). \tag{16}$$

Inserting (14) in (16) results in

$$V'_{DD} = V_{DD}\left(1 - \frac{\hat{I}_D}{g_m V_{DD}} \frac{\Delta_{Nk}}{2n}\right). \quad (17)$$

Now, the deviated delay times t'_{pHLk} for the falling edge in stage k and t'_p for the rising and falling edges in all the other stages can be calculated (with (8), (14) and (17)):

$$t'_{pHLk} = \frac{C_{node} V'_{DD}}{2\hat{I}'_{DNk}} \approx t_p\left(1 - \Delta_{Nk}\right) \quad (18)$$

$$t'_p = \frac{C_{node} V'_{DD}}{2\hat{I}'_D} \approx t_p\left(1 + \left(1 - \frac{\hat{I}_D}{g_m V_{DD}}\right)\frac{\Delta_{Nk}}{2n}\right) \quad (19)$$

Now, the new cycle time can be calculated:

$$T_{I-mode} = (2n-1)t'_p + t'_{pHLk} \approx T_0\left[1 - \frac{\hat{I}_D}{g_m V_{DD}} \frac{\Delta_{Nk}}{2n}\right] \quad (20)$$

By comparing (20) with (11), we get

$$\Delta_{T,I-mode} = -\frac{\hat{I}_D}{g_m V_{DD}} \frac{\Delta_{Nk}}{2n} = \frac{\hat{I}_D}{g_m V_{DD}} \Delta_{T,V-mode}. \quad (21)$$

Concluding, the cycle time deviation is reduced in current mode compared to voltage mode by the factor

$$R = \frac{\hat{I}_D}{g_m V_{DD}}. \quad (22)$$

Assuming an ideal quadratic current law and a zero threshold voltage ($\hat{I} = ½ \beta V_{DD}^2$, $g_m = \beta V_{DD}$), (22) gives

$$R = \frac{½\beta V_{DD}^2}{\beta V_{DD}} = \frac{1}{2}. \quad (23)$$

With these simplifying assumptions for the current law, the cycle time deviation in current mode is just half the amount of the deviation in voltage mode. This corresponds to a reduction of close-in phase noise of 6 dB.

A real MOSFET has a threshold voltage larger than 0 V, operates with approximately quadratic current law for small gate voltages and more linear for larger gate voltages. For a threshold voltage larger than 0 V and quadratic current law, the reduction according to (22) is larger than 6 dB for small V_{DD} and approaches 6 dB for larger V_{DD}. For a (theoretical) ideal linear device ($\hat{I} = g_m V_{DD}$, g_m = const), the reduction of phase noise in current mode according to (22) disappears. Thus, for a MOSFET operating more and more linear when entering the short channel current law for large V_{DD}, the reduction decreases. To summarize, the presented theory predicts a close-in phase noise reduction in current mode larger than 6 dB for small V_{DD}, the reduction decreasing with increasing V_{DD} to values smaller than 6 dB.

III. Simualtion Results

The simulated oscillator is implemented in 0.18 µm CMOS technology. It applies symmetrical CMOS inverters in a 9-stage ring. The simulation setup is shown in Fig. 1: either an ideal voltage or an ideal current source with appropriate value to arrive at the desired oscillation frequency is applied to the core circuit. Phase noise is simulated with the periodic noise (pnoise) analysis of SpectreRF that follows a periodic steady-state (pss) analysis. This simulation method takes into account the cyclostationary behavior of the MOSFET noise sources. The transistor model is "MOS Model, level 9.03" with the 1/f noise model level "NFMOD = 0" [6]. This 1/f noise model predicts a gate voltage independent power spectral density (PSD) of the gate-referred 1/f noise voltage. It may thus oversimplify the real bias dependence of the MOSFET 1/f noise [7]. But as the main goal of the simulation is to confirm the theory prediction of phase noise *reduction* in current mode *relative* to voltage mode, and as the periodic gate voltage is the same in current and voltage mode (at the same oscillation frequency), the exact modeling of the gate voltage dependence of 1/f noise is not relevant here.

TABLE I. Simulated 9-Stage Ring Oscillator Phase Noise at 1 MHz Offset in Voltage Mode and Current Mode.

f_{osz} [GHz]	V_{DD} [V]	I_{DD} [mA]	£$_V$ [dBc/Hz]	£$_I$ [dBc/Hz]	£$_I$ - £$_V$ [dB]
3.0	2.3	5.4	-101.0	-105.0	**-4.0**
2.5	1.8	3.5	-99.2	-104.8	**-5.6**
1.7	1.3	1.6	-98.0	-105.5	**-7.5**
0.6	0.8	0.3	-97.8	-107.0	**-9.2**

Table I shows the simulated phase noise at 1 MHz offset (this is well within the $1/\Delta f^3$- region of phase noise for this kind of oscillator) in both modes of operation and the reduction in current mode for oscillator core supply voltages ranging from 0.8 V to 2.3 V. In line with the presented theory, the reduction is 9 dB for small V_{DD} and decreases to 4 dB for large V_{DD}, where the MOSFETs operate in a more short-channel and thus linear fashion.

IV. Experimental Results

Although available as chip, the current mode supply measurement is difficult for the 9-stage ring oscillator. On-chip decoupling capacitors are connected to the V_{DD}-rail and prevent the implementation of a broadband high impedance supply. Therefore, a second oscillator with an integrated current mirror is measured. It is also realized in 0.18 µm CMOS. The technology is from another supplier and thus differs from the technology used for simulation.

The measured oscillator is shown in Fig. 2. It applies a 7-stage ring of asymmetric inverters, i.e. the PMOS width is reduced compared to a symmetrical inverter design. A PMOS current mirror is connected between the oscillator core V_{DD} node and an additional V_{Bat+} node with 3.3 V supply. The current mirror uses 3.3 V I/O transistors. The circuit can operate either in voltage mode (switch to $V_{DD,supp}$ connected) or in current mode (supply V_{Bat+} and switch to $I_{DD,supp}$ connected). The current source transistor has to operate in saturation in order to have high output impedance. The current mirror's own noise has to be low in order that it doesn't compensate the reduction that is achieved in current-mode. Its flicker noise is minimized by

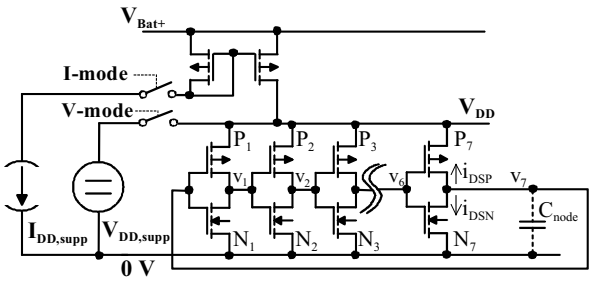

Figure 2. 7-stage CMOS ring oscillator with PMOS current mirror and the connections for voltage mode and current mode supply.

using large gate area transistors and its thermal noise is minimized by using a relatively large gate overdrive voltage without leaving the saturation region. The circuit applies a tapered CMOS inverter chain as output driver with an extra supply terminal.

All measurements are made on-wafer using the spectrum analyzer Anritsu MS 2668C. Fig. 3 shows the measured spectrum at 2 GHz oscillation frequency both in voltage and in current mode. The reduction of the noise sidebands in current mode is clearly visible. Phase noise is measured using the build-in carrier-to-noise marker function.

Table II shows the measured phase noise in both modes and the reduction in current mode at 1 MHz offset for several core supply voltages. As can be seen, the phase noise in current mode is up to 6 dB lower than in voltage mode. However, the phase noise reduction in current mode does not increase for lower V_{DD}-values, rather the reduction decreases for this circuit. That characteristic is caused by the additional noise of the current mirror: the voltage mode phase noise of the asymmetric 7-stage ring decreases with decreasing V_{DD}, making the current mirror noise contribution more relevant for lower values of V_{DD}. The noise summaries of SpectreRF simulations indicate that the contribution of the current mirror thermal noise to the overall phase noise at 1 MHz offset is negligible for I_{DD} = 4.0 mA, but this contribution is already the largest one at I_{DD} = 0.5 mA. Nevertheless, the reduction of phase noise in current mode with a real current source transistor remains significant over a broad oscillation frequency range. Moreover, advanced low-noise current sources may be implemented in other technologies like BICMOS.

V. CONCLUSION

A theory about the influence of slowly perturbed drain currents on the oscillation cycle time and close-in phase noise of single-ended CMOS inverter ring oscillators is presented both for the case of a constant supply voltage and for the case of a constant supply current. The theory predicts a reduction of close-in phase noise of several dB in the case of a constant supply current. This prediction was confirmed by simulations and measurements. The simulated reduction with an ideal noiseless current source is between 4 and 9 dB. The reduction demonstrated experimentally with an integrated PMOS current mirror is between 4 and 6 dB.

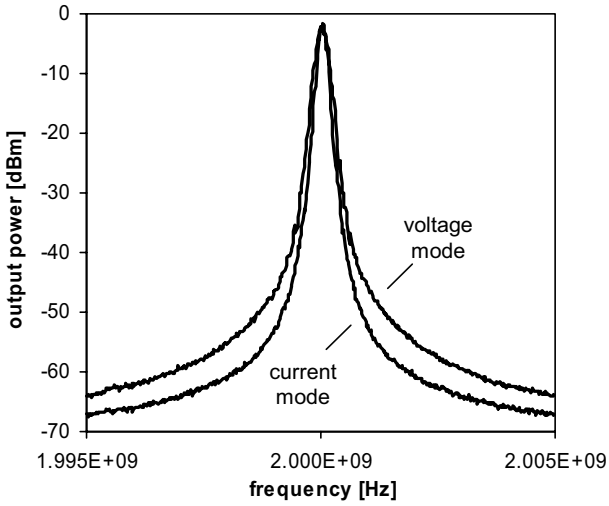

Figure 3. Measured 7-stage ring oscillator spectrum for voltage mode supply (V-switch connected) and for current mode supply (I-switch connected) at f_{osz} = 2.0 GHz, V_{DD} = 2.1 V. (RBW = 100 kHz, VBW =100 Hz)

TABLE II. MEASURED 7-STAGE RING OSCILLATOR PHASE NOISE AT 1 MHZ OFFSET IN VOLTAGE MODE (V-SWITCH CONNECTED) AND CURRENT MODE (I-SWITCH CONNECTED)

f_{osz} [GHz]	V_{DD} [V]	I_{DD} [mA]	$£_V$ [dBc/Hz]	$£_I$ [dBc/Hz]	$£_I - £_V$ [dB]
2.0	2.1	4.0	-98.6	-104.9	**-6.3**
1.3	1.7	2.0	-99.3	-104.9	**-5.6**
0.8	1.4	1.0	-101.3	-106.0	**-4.7**
0.5	1.2	0.5	-102.5	-106.5	**-4.0**

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