PRASAD PANDIT

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Blog : *www.vhdlcodes.com*
Youtube : https://www.youtube.com/user/pulsee250i

Summary of Qualification:

- Good understanding of ASIC and FPGA design flow
- Very good knowledge and experience of writing RTL models in Verilog and VHDL
- Experience in writing Test benches in SystemVerilog and UVM
- Good knowledge of verification methodologies(UVM)
- Experience in using industry standard EDA tools for front-end design and verification

Professional Qualification:

Completed *Advanced VLSI design and Verification Certification* at Maven Silicon VLSI Design and Training Center, Bangalore

Year: 2013

VLSI Domain Skills:

HDLs	**:**	Verilog and VHDL
HVLs	**:**	SystemVerilog and PSL
Verification methodologies	**:**	Coverage Driven Verification Assertion Based Verification
TB Methodology	**:**	UVM
EDA tools	**:**	ModelSim, Quartus II and ISE
Domain	**:**	ASIC/FPGA Design Flow, Digital Design Methodologies
Knowledge	**:**	RTL Coding, FSM based design, Simulation, Code Coverage, Functional Coverage, Synthesis, Static Timing Analysis

Other Skills:

Expertise Area:	Embedded Systems Design, 2-Layer PCB Designing, SMD Soldering/Desoldering.
Programming Languages:	C, JAVA, Embedded C.
Tools (Software):	OrCAD, Eagle, NetBeans, Keil, AVR Studio, CodeVision AVR, Code Composer Studio for TI uC, Eclipse, AppInventor, Matlab, Linux.
Tools(Hardware):	Altera DE1 Board, ATmega uC, Arduino, all SMD soldering and desoldering tools, PCB design and fabrication prototyping tools, Bluetooth Modules, Wireless Interfacing Modules, Android.

Publications:

Papers: Paper on "Graphene – The New Emerging Technology" Presented by Prasad Pandit and Tejas Telmasre at SPANDAN 2011, YCCE Nagpur (17-18 Feb, 2011).

Blogs: Posted VHDL and Embedded system projects for students on vhdlcodes.com. The blog is used for VHDL tutorials in Simon Fraser University, USA. Also by VHDL coders as a starting point all over the world.

Major Projects:

Verilog Projects:

1. Real Time Clock – RTL Design and verification
2. Dual Port RAM – Verification
3. FIFO – Design and Verification

   EDA Tools: Modelsim, Questa – Verification Platform and ISE

   - Designed using Verilog HDL
   - Verified the RTL model using SystemVerilog/UVM
   - Generated functional and code coverage for the RTL verification sign-off
   - Synthesized the design

4. PHY IP core(Ethernet IP) – Design and Verification

   EDA Tools: Modelsim, ISE

   The PHY IP core is Physical Layer of OSI model, the IP core consist of a PCS and PMA module. It is designed to operate at 125 MHz, and the 8bit/10bit Encoder-Decoder are completely designed with combinational block for power, speed and space optimization.

   - Designed PHY IP using Verilog HDL
   - Architected the module based verification environment using Verilog
   - Verified the RTL model using Verilog TB
   - Synthesized the design

VHDL Projects: 2009 to till now : Tools – Quartus II, ModelSim

5. Power Section: Power Management System for Wind, Solar and Power Grid
6. Game Development: PONG Game, PacMan, Block Breaker
7. Protocol: UART Protocol IP, 16x2 LCD Driver IP, Memory Interface IP.
8. Others: Calculator, RTC, Image Viewer, Frequency Counter, Stop watch and Countdown Timer, Pattern generator On VGA monitor.

Intelligent Driver Assistance Technology (IDiAT), *sponsored by IEDC, DRDO* **2011-12**

Organization - G. H. Raisoni College of Engg. **(Team Size – 4)**

Domain area: Embedded System, Android, Java.

Description: The project is basis of integration of part of Augmented Reality concept on Windshield of the Automobile. It is to ensure Driver safety and to enhance the driving experience through displaying Navigational as well as Media info which primarily includes Calls and Message Notifications on windshield of car via a Virtual image. The motto is to provide such

technology to middle-class car segments at cheaper costs and simplistic software so anyone can use.

Embedded System Projects:

Auto-Load Switch, Transformer System, Android Accelerometer Based Robot, SenseCap for Blind and Deaf, Osciduino, BluHome, ShopMart.

Achievements:

- Started a blog website www.vhdlcodes.com helping VHDL coders over the world to learn about basic VHDL projects.
- Had secured 2nd place in Circuit Designing competition Matrix in icon'11, YCCE and 1st place in Circuit Designing competition Matrix in icon'12, YCCE.
- Secured 1st position in Project Competition at GHRCE.
- Was in top 6 teams at IIT Bombay TechFest'12 for Umeed-E-Milap, India vs Pakistan Wrist Movement Controlled Robot Competition.

Academic Qualification:

Year/ Semester	School/ College	Period	Percentage	Board/University
B.E. in Electronics Engineering	G.H. Raisoni College of Engineering, Nagpur	2008 - 2012	72% (Aggr.)	G. H. Raisoni College of Engineering (An Autonomous Institute)affiliated to R.T.M.N.U.
HSC (XIIth)	Hislop College, Nagpur	2006 - 2008	83.33%	Maharashtra State Board, Pune.
SSC (Xth)	Somalwar High School, Nagpur	2005 - 2006	83.06%	Maharashtra State Board, Pune.

Personal Information:

- Date of Birth : 20-11-1990
- Passport No. : J9740276

Other Certifications:

- I am a Certified Diamond Grader with Certification of Gemological Institute of India.

Prasad Pandit
OCT. 17, 2013