BJT Frequency Response

Design a single stage common emitter with emitter bypass capacitor Pre-amplifier circuit to amplify a 50mVp @ 10KHz input signal to up to 2Vp, with cutoff frequency set to 1KHz and 50 KHz.

Use voltage divider circuit and RL = 10k-ohm

Required:

a) Design computation

b) Simulation graphs (input and output comparison)

b1) 50mVp @ 60 Hz sine

b2) 50mVp @ 10 KHz sine

b3) 50mVp @ 100 KHz sine

b3) 50mVp @ 1MHz sine

c) Low frequency response (bode plot and phase plot)

d) Schematic and PCB foil pattern

DESIGN SOMPUTATION

$V_{CC} := 10V$ $V_{in} := 50mV$ $V_{CE} := 7.5V$ $I_C := 8.69mA$ $C_C := 1\mu F$ $C_S := 1\mu F$

$V_O := 2V$ $V_{BE} := 0.7V$ $I_B := 50\mu A$ $f_1 := 10KHz$ $R_L := 10k\Omega$ $C_E := 15\mu F$

$V_E := \frac{V_{CC}}{10} = 1\,V$ $R_C := 475\Omega$

$V_B := V_{BE} + V_E = 1.7\,V$

$I_E := (\beta + 1)I_B = 8.74\,mA$

$R_E := \frac{V_E}{I_E} = 114.416\,\Omega$

$R_2 := \frac{\beta \cdot R_E}{10} = 1.989\,k\Omega$

$R_1 := \left(\frac{R_2 \cdot V_{CC}}{V_B}\right) - R_2 = 9.709\,k\Omega$

$re := \frac{26mV}{I_E} = 2.975\,\Omega$

$V_C := V_{CC} - I_C \cdot R_C = 8.5\,V$

$R_B := \frac{R_1 \cdot R_2}{R_1 + R_2} = 1.651 \times 10^3\,\Omega$

$Z_I := \frac{R_B \cdot (\beta \cdot re)}{R_B + (\beta \cdot re)} = 393.698\,\Omega$

$Z_O := \frac{R_C \cdot R_L}{R_C + R_L} = 169.683\,\Omega$

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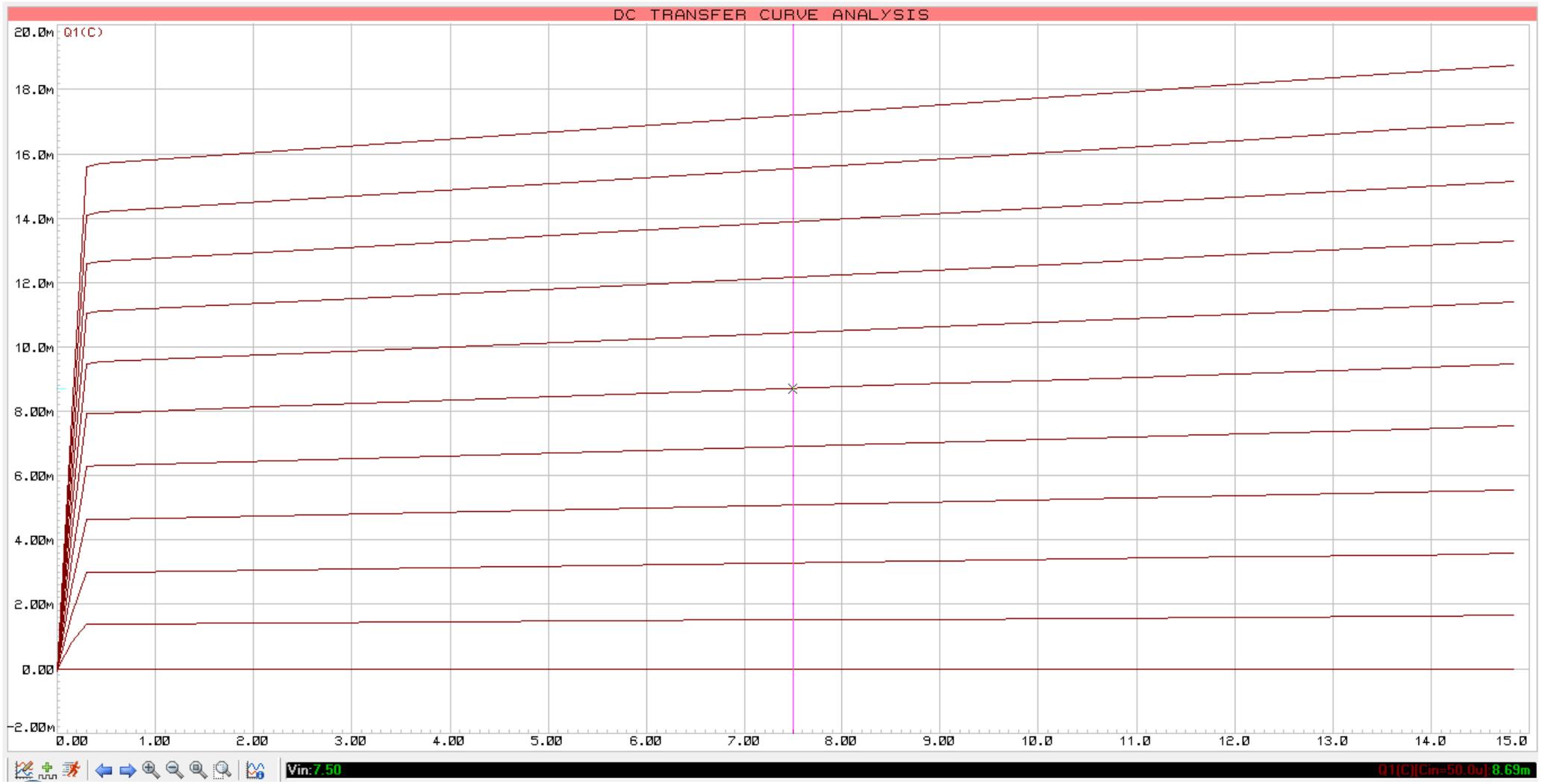
DC TRANSFER CURVE



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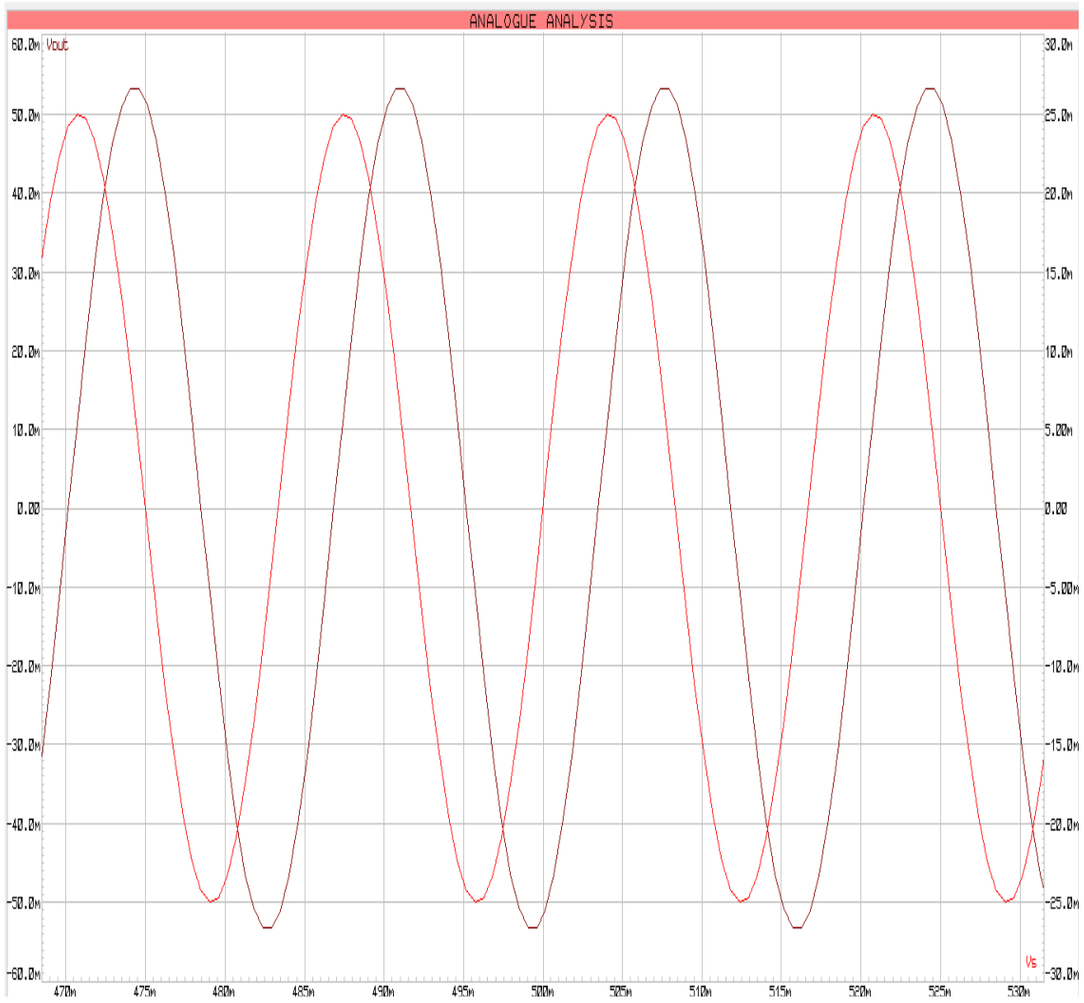
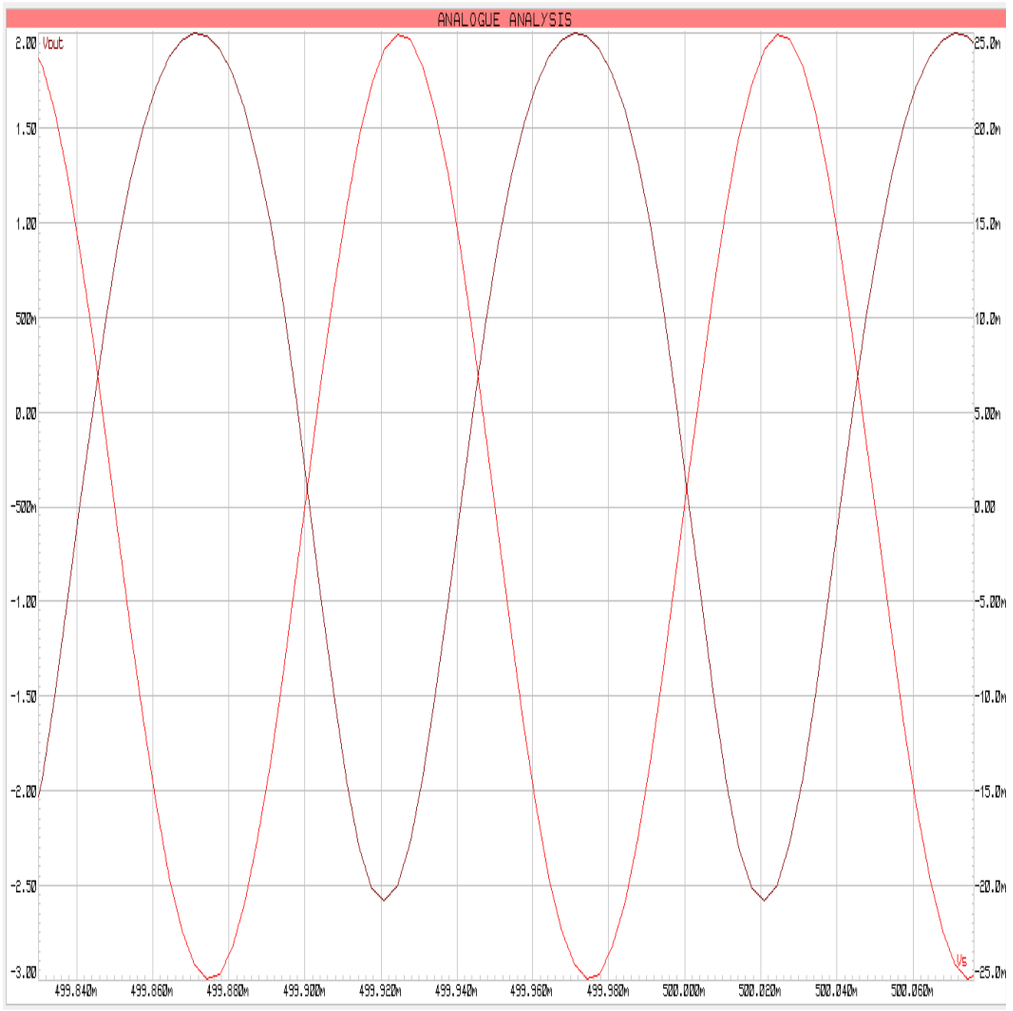
SIMULATION GRAPHS

50mVp @ 60 Hz



50mVp @ 10 KHz



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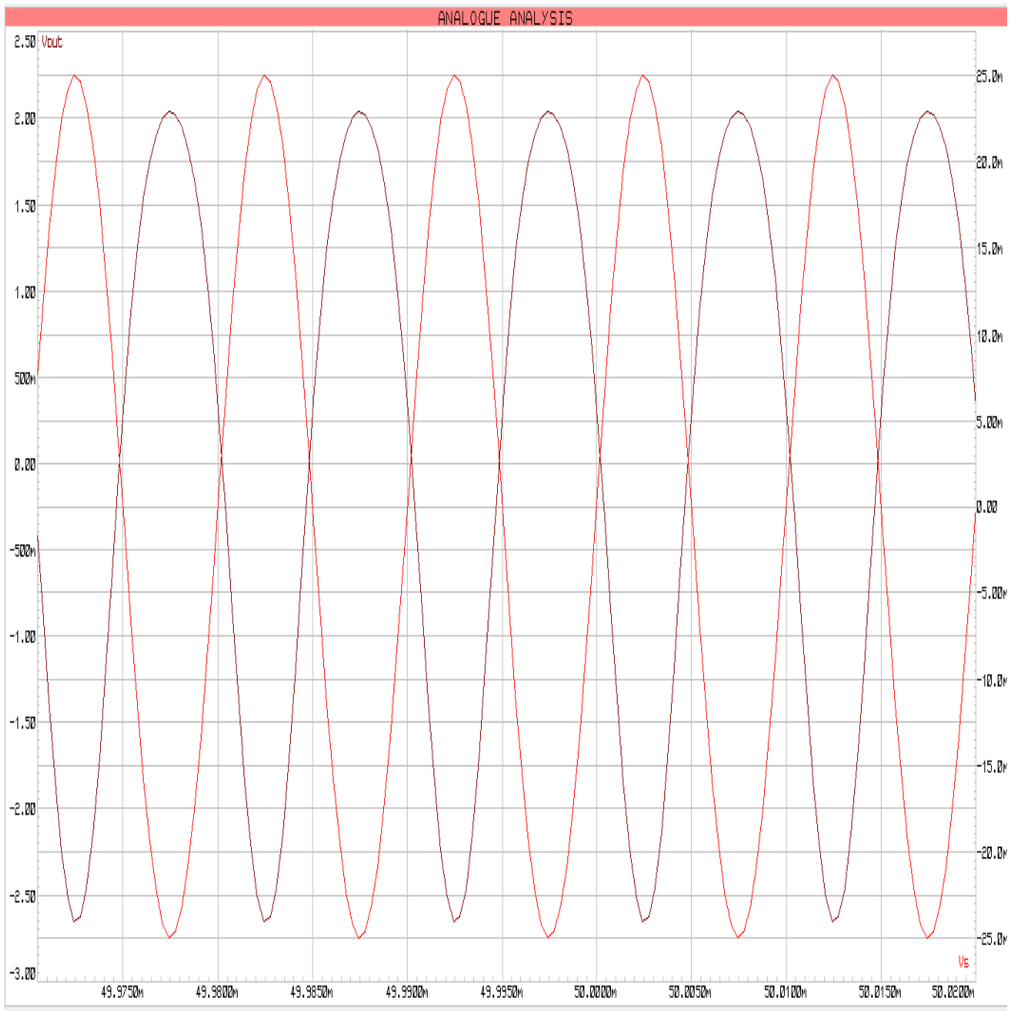
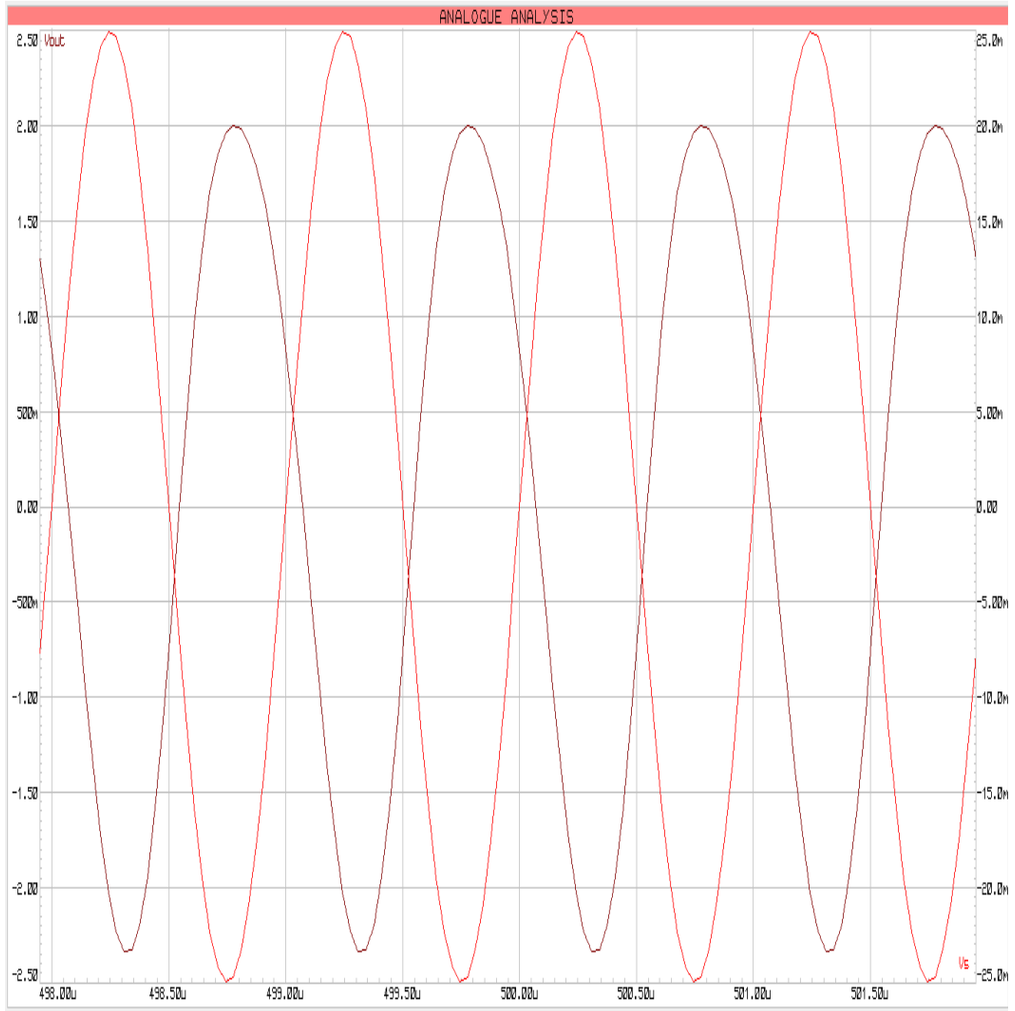
50mVp @ 100 KHz



50mVp @ 1 MHz



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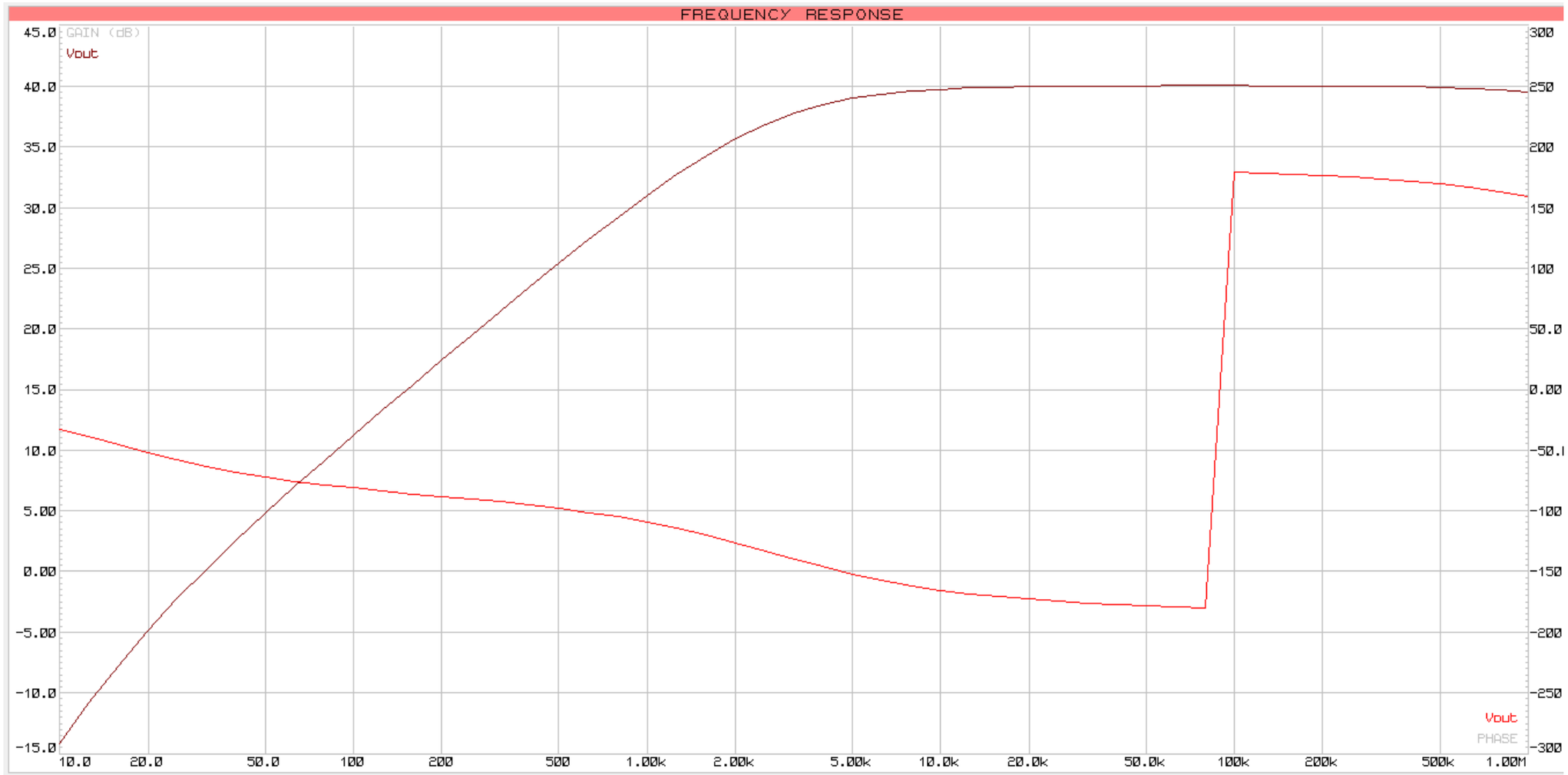
LOW FREQUENCY RESPONSE



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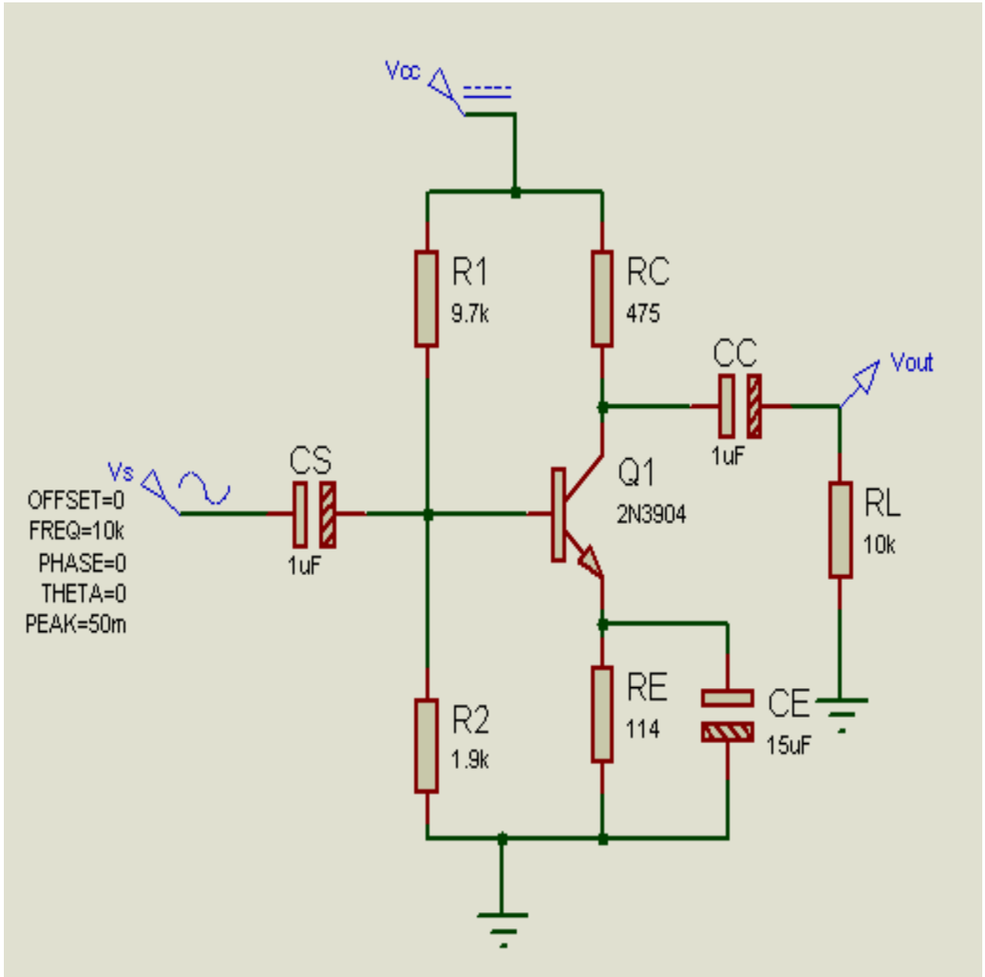
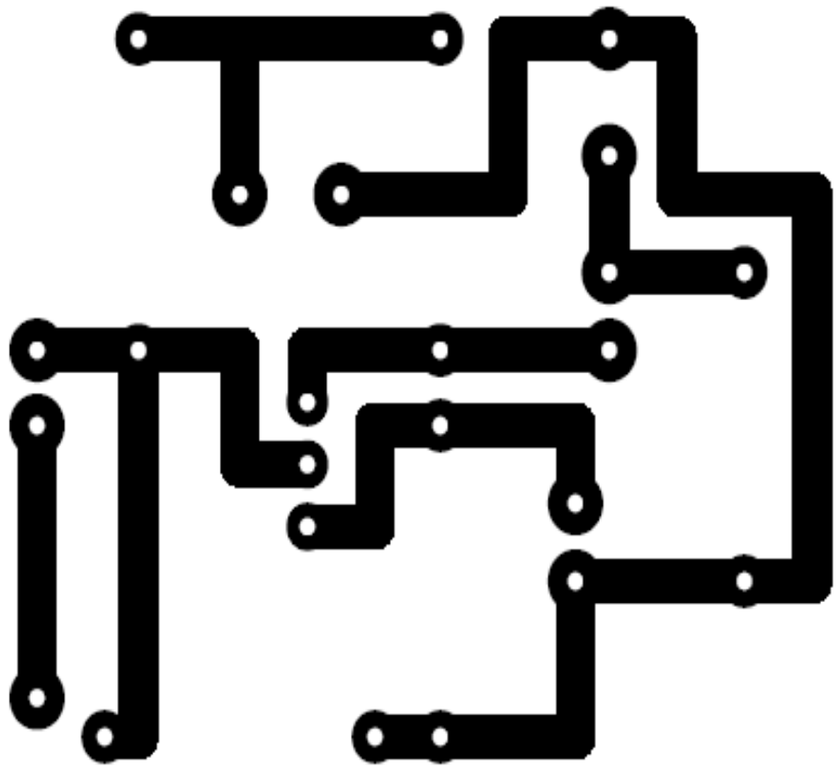
SCHEMATIC DIAGRAM



PCB FOIL PATTERN



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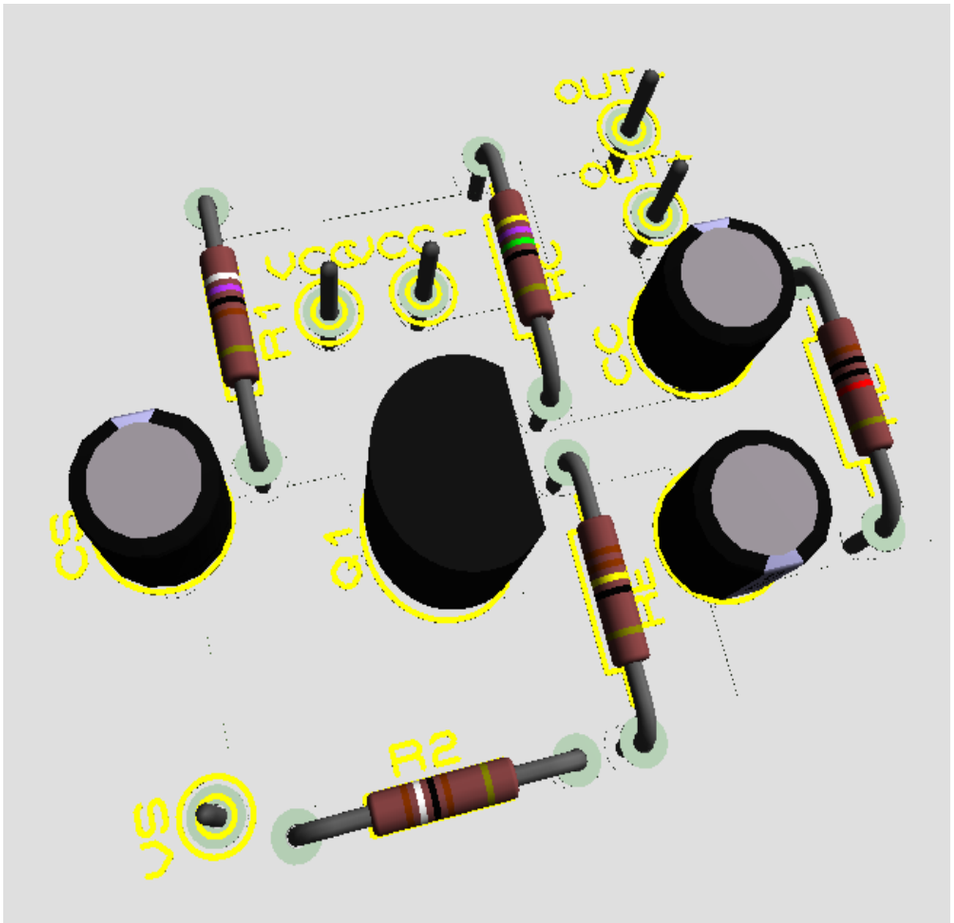
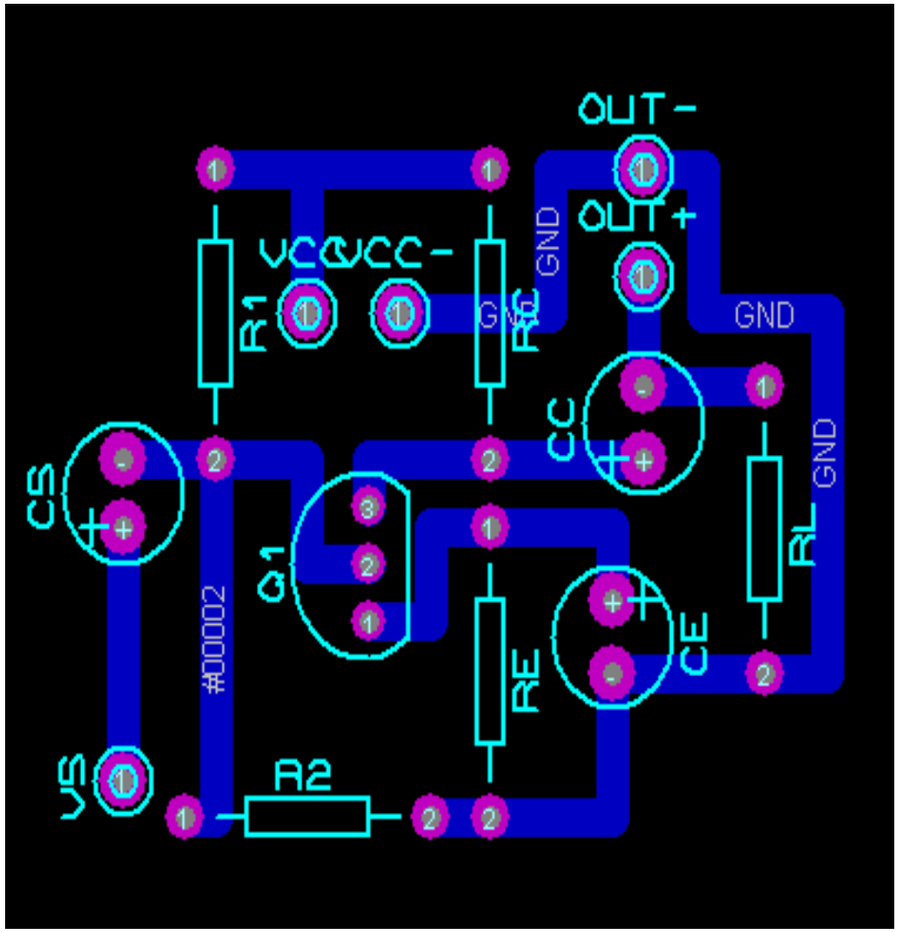
3D DESIGN



SCHEMATIC DIAGRAM



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