

## Key considerations when connecting MOSFETs in parallel



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Power MOSFETs are the switching device of choice in most modern power solutions. Continuous development by semiconductor companies means that MOSFET performance and capacity is continually increasing. However, sometimes it is necessary to use two MOSFETs in parallel.

While this is generally easier than with bipolar devices, there are still some pitfalls that are best avoided. In this whitepaper, Toshiba Electronics Europe will look at the best practice for operating MOSFETs in a parallel configuration.

### Introduction

Power MOSFETs generally offer outstanding thermal stability and do not suffer thermal runaway. This makes connecting them in parallel easier than with bipolar transistors.

Bipolar transistors need a current to flow in the base to operate. As a result, the current balance is disrupted by any fluctuation of the base-emitter voltage (VBE), making parallel connections more challenging. Because power MOSFETs are voltage driven, parallel connection is easier - it is only necessary to supply a drive voltage to each parallel FET.

However, it is essential to avoid current concentration and oscillations. In addition, designers should ensure a well-balanced, uniform flow of current to all devices under all possible load conditions when using MOSFETs in parallel.

Variations in device characteristics and / or circuit equivalent impedance can cause imbalance leading to circuits performing in unpredictable ways. Let us consider the use of a buck converter circuit with parallel MOSFETs.

Figure 1 shows the schematic for the buck converter. In a real-world implementation there are many parasitic impedances as shown Figure 2.

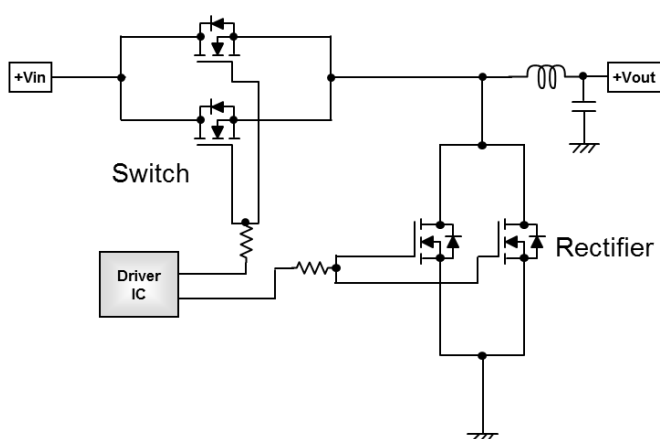


Figure 1 – Schematic for a buck converter with parallel MOSFETs

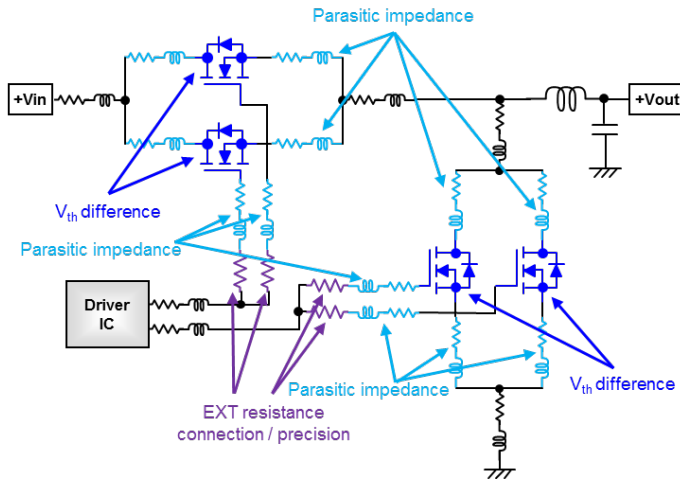


Figure 2 – Parasitic impedances in a real-world buck converter

Individual device characteristics can vary within the tolerances of the datasheet specifications. The threshold voltage ( $V_{th}$ ) is susceptible to variation and can cause current imbalance. Using MOSFETs with matched values of  $V_{th}$  is preferred to reduce variations in switching times.

Figure 3 shows a buck circuit with a MOSFET pair that exhibits maximum  $V_{th}$  variation.  $I_{pathA}$  is current passing through the MOSFET with the lowest  $V_{th}$ .  $I_{pathB}$  is the path for the highest  $V_{th}$  MOSFET. Other parameters for each current path are the same in this simulation.

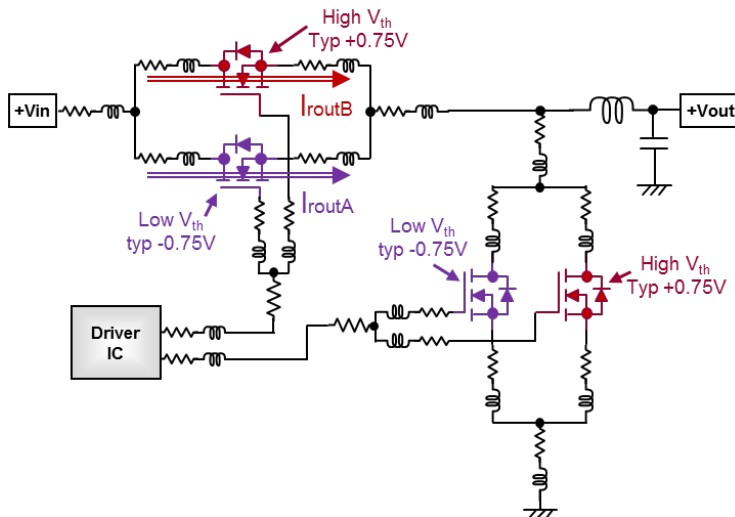


Figure 3 – Effects of  $V_{th}$  variation on current paths

Figure 4 shows the simulation result for the switching side MOSFET current waveform. The peak current through  $I_{pathA}$  (purple trace) is twice that for  $I_{pathB}$  (pink trace).

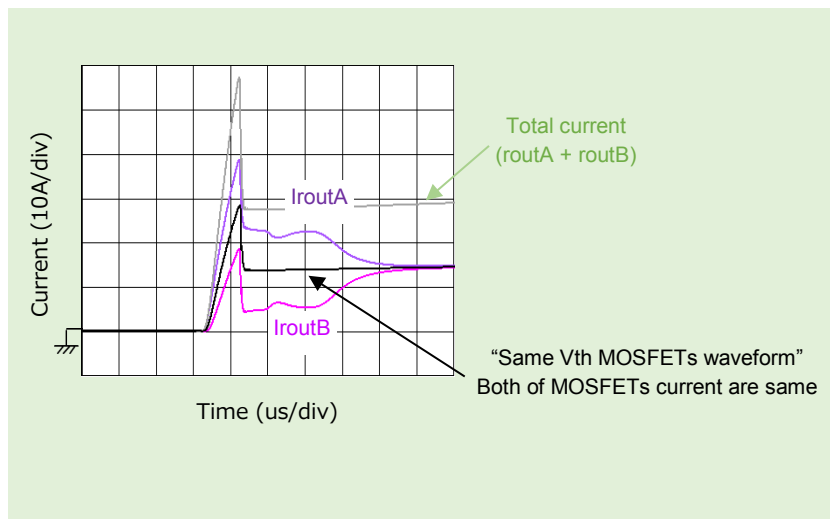


Figure 4 –  $V_{th}$  affects current balance

Although, the  $V_{th}$  difference is the maximum in this example, the difference is not so pronounced in MOSFET pairs from the same lot / batch.

Figure 5 shows an example distribution for MOSFETs from the same lot where the  $V_{th}$  variation is less than the specification maximum.

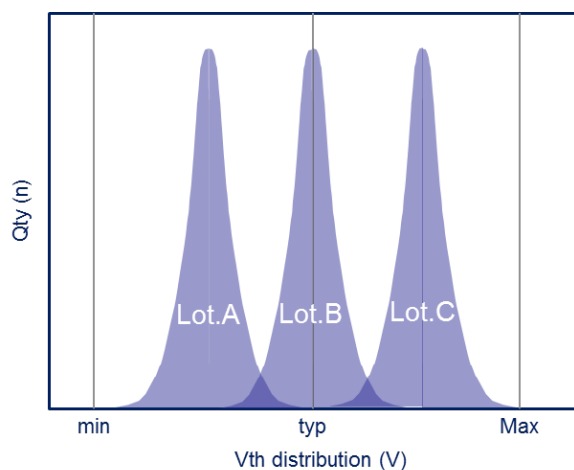


Figure 5 – Example  $V_{th}$  distribution with MOSFETs from the same lot

Current unbalance can also occur as a result of the drive condition. In some cases, external resistances (with a 0.5% to 5% tolerance) are used to control switching speed. If an external gate resistance ( $R_g$ ) is connected each MOSFET as shown in Figure 6, any variation will affect current balance.

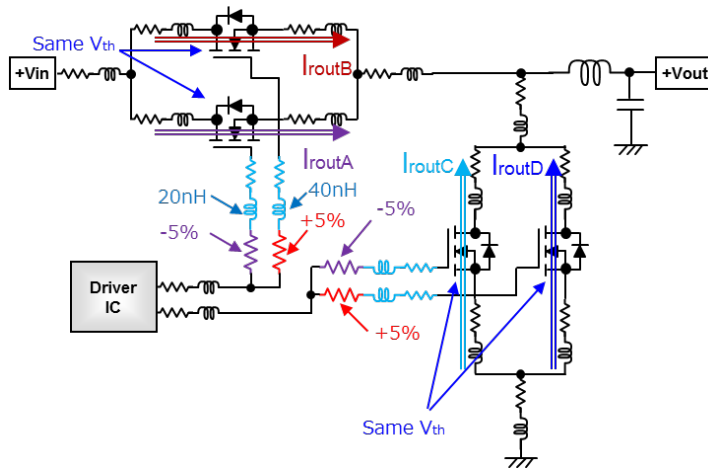


Figure 6 – External  $R_g$  connected to each MOSFET gate

Figure 7 shows the result of simulating the current waveform. If  $R_g$  has a 5% variation and the parasitic inductance variation is double (20nH/40nH), then there is a 30% current difference between  $I_{pathA}$  and  $I_{pathB}$ .

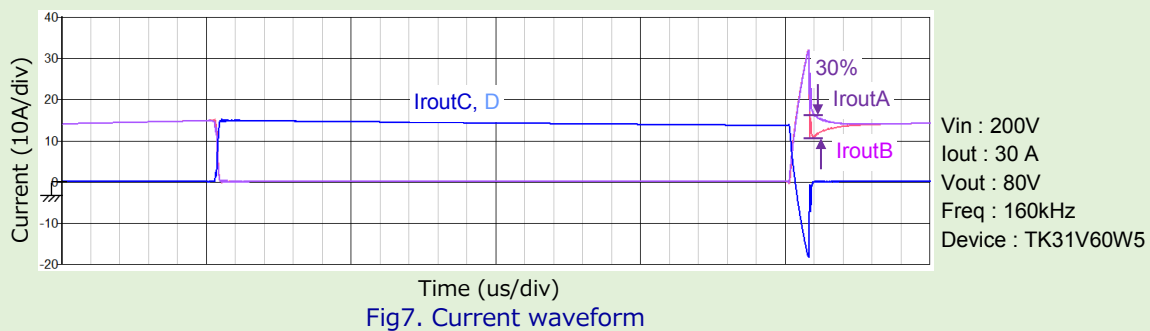


Figure 7 – Current waveform simulation

External  $R_g$  variation does not affect the rectifier circuit current balance ( $I_{pathC}$  and  $I_{pathD}$ ) in this simulation. In the case of an open-circuit then device damage can occur.

When using an external gate resistor for parallel MOSFETs, each gate pin trace must be kept as short as possible. This avoids resistance accuracy problems and reduces the parasitic resistance and inductance at the same time. Short traces can also smooth each MOSFETs  $V_{gs}$  level if there is a difference in the capacitances.

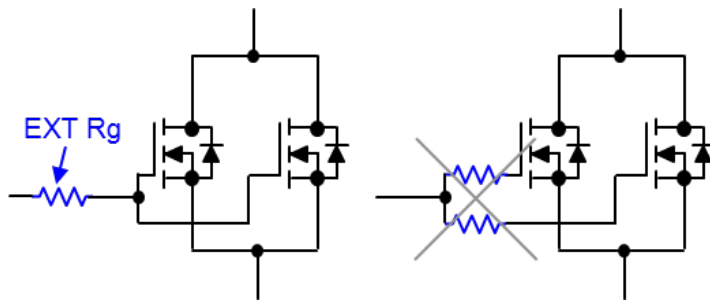


Figure 8 – External  $R_g$  usage recommendation

It is difficult to completely avoid parasitic impedance. In high speed switching applications this can sometimes lead to oscillation. In this case, adding an additional small  $R_g(\text{sub})$  in each arm can be a solution.  $R_g(\text{Sub})$  should be smaller than  $\text{EXT } R_g(\text{Main})$  and less than  $1\Omega$ .

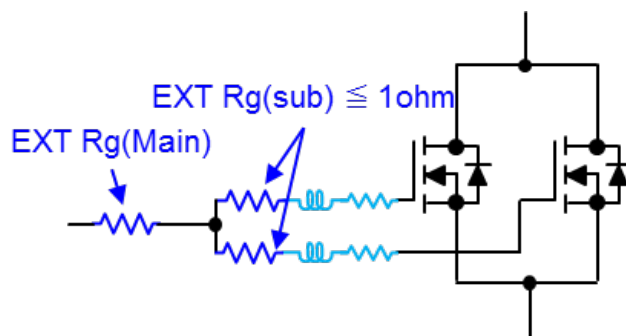


Figure 9 – Circuit design to reduce any parasitic impedance effect

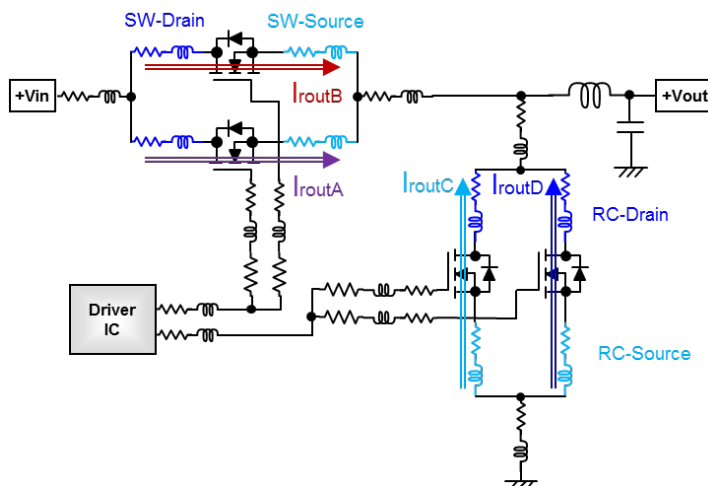


Figure 10 – Parasitic impedance of current paths

It is generally accepted to design power traces to be as short as possible. However, this can be difficult due to limited space, the drive circuit or other reasons. Symmetrical length traces are needed to each parallel MOSFET, as shown in Figure 11.

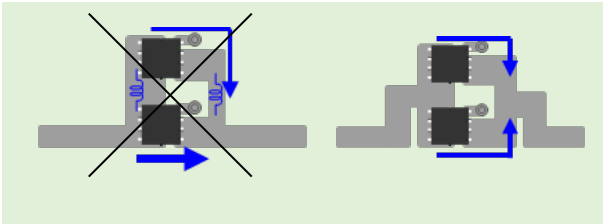


Figure 11 – PCB Layout recommendation

Different trace lengths will cause oscillation due to unbalanced impedances as shown in the simulation results in Figure 12. This will damage the MOSFETs.

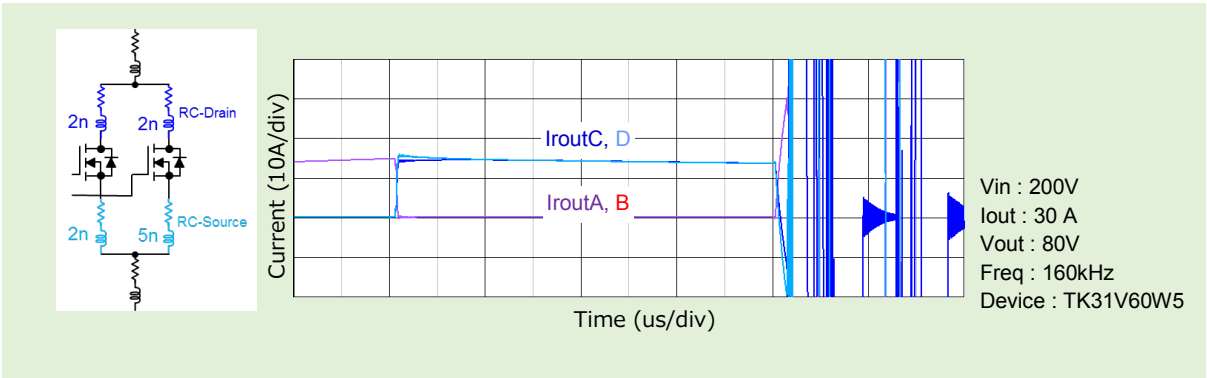


Figure 12 – Simulation results showing oscillation due to impedance imbalance

Using surface-mount devices is one effective solution to decrease parasitic impedance, especially parasitic inductance. Figure 13 shows the example parasitic inductances for a circuit with a pin-through TO-220. The total parasitic inductance in the current path is 24nH. Figure 14 shows the same for a circuit using a surface mount device where the total parasitic inductance is only 4.7nH.

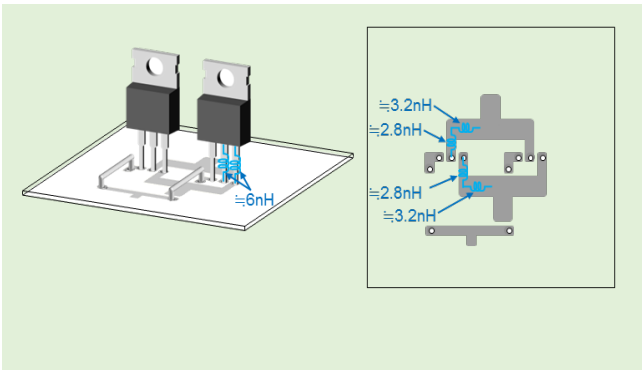


Figure 13 – Parasitic inductance for a pin-through TO-220 device

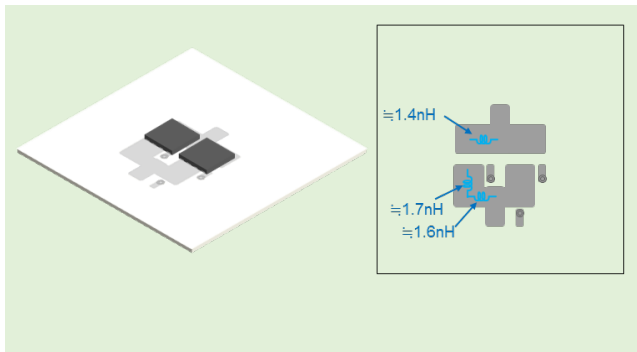


Figure 14 – Parasitic inductance for a surface mount DFN8x8 device

## Summary

Designing circuits with parallel MOSFETs is an important requirement in applications such as buck converters. The best solutions will be based on a careful selection of MOSFET devices and a balanced approach to circuit design. This is especially important in terms of managing the parasitic impedances that can occur in external resistances and PCB traces. Effectively addressing these issues can significantly simplify the implementation and effectiveness of parallel MOSFET architectures.



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