Design and Test Challenges of High Performace Data Converters

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Test of A/D Converters

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Introduction

Test Goals:

- To determine if the product produced by manufacturing process are appropriate and will function as desired
- To generate information that can be used to improve process yield and reduce the costs.
- To bin parts based upon their performance (e.g., pass/fail test)

Test process could account for half of the final cost of a chip.

Introduction (cont.)

Test for Different Circuits:

- Digital Circuits Test
- Analog & Mixed Signal (AMS) Circuits Test

In many circuits, the digital core like DSP is surrounded by peripheral analog circuitry, such as part of A/D and D/A converters. The analog component occupies a small fraction of silicon area, but the its design and test needs more efforts and knowledge rather than the digital component.

Analog and Mixed Signal IC test is one of the hottest issues in the test research and development.

Introduction (cont.)

Examples of Mixed-Signal Circuits:

- Comparator (Simplest AMS circuit)
- Programmable Gain Amplifier (PGA)
- Analog-to-Digital Converter (ADC)
- Digital-to-Analog Converter (DAC)
- Phase Locked Loop (PLL)
- Cellular telephone (Complex AMS Circuit)
- Hard Disk Drives
- Modems
- Multimedia Audio and Video

Introduction (cont.)

AMS Test Issues:

- Analog Circuit Behavior: the number of values of an analog signal is generally infinite.
- Measurement Accuracy: it is not possible to measure signals with infinity resolution.
- Performance: there is not a clear distinction between functionality and performance.

Introduction (cont.)

Built-In-Self-Test (BIST):

BIST methods aim to control rising tester costs by moving test stimulus generation and result observation on to the IC. The output of the BIST hardware is a simple pass/fail signal.

Advantages:

- Reduce the cost of testing
- Possibility of the test in the field

Disadvantages:

- Increase chip area
- Reduce yield
- More sophisticated circuit design

Introduction (cont.)

Importance of Test Methodology:

Understanding the test methodology is the first step toward understanding the manufacturer's data sheet and how a product fits in your application.

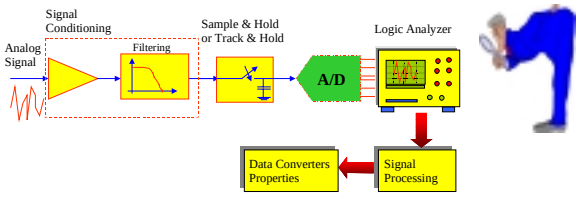
There is no standard method of testing for some of performance metrics of data converters. Depending on how the specification is tested, different performance characteristics can be concluded from the experimental results.

Introduction (cont.)

Errors of Test Setup:

The errors due to the test setup equipments affect the quality of the results. Errors due to the voltage reference, sample and hold, or input buffer amplifier are difficult to separate from the imperfections of the converter under test.

Generally speaking, the resolution and quality of the setup equipment should be greater than the ones of data converter under test.



Test of A/D Converters

1- Introduction

2- Static Test

3- Dynamic Test

4- Conclusions

Static Testing

General:

In static testing the accuracy of the converter under test is determined by repeatedly applying a series of precision input DC voltage level and measuring the digital output signal. As a result, the transfer characteristic is determined.

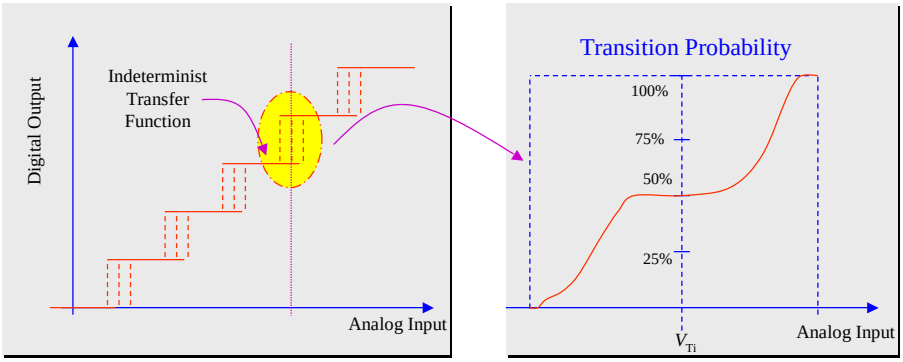
Disadvantage:

The nonlinearity due to the dynamic variation of the input signal cannot be measured during the static testing.

Static Testing (cont.)

Transition Level:

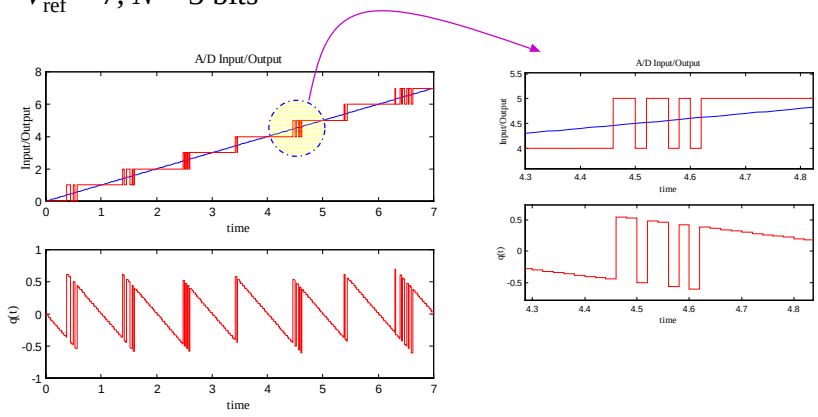
Due to the circuit noise, the transition level in the real A/D converter is not deterministic.



Static Testing (cont.)

Example: Electronic Noise

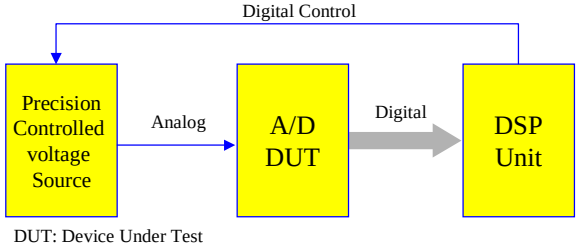
$V_{ref} = 7$, $N = 3$ bits



Static Testing: Ramp Test Method

ADC Test:

A precision controlled voltage source is used to generate a DC analog input signal. At each input level, ADC samples several times. When ADC under test converts a new code at least 50% of the time, the analog input voltage level is considered as a transition level for that code.

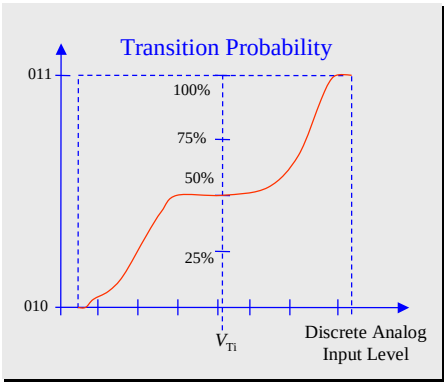


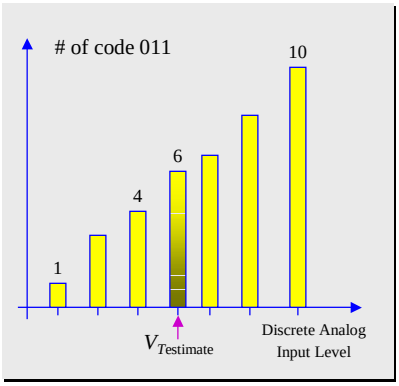
DUT: Device Under Test

Static Testing: Ramp Test Method (cont.)

Example:

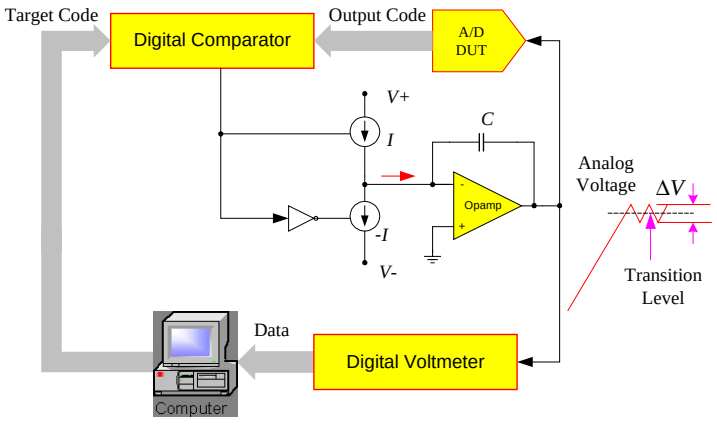
Consider that 10 samples for each input level are taken. The transition level from 010 to o11 is investigated.





Static Testing: Servo-Loop Test

This test is another method of determining the 2^N-1 transition levels of the ADC's input voltage.



Static Testing: Servo-Loop Test (cont.)

Measuring Transition Levels:

When a new target code is set by the computer, the integrator output increases linearly towards the transition level for the code. Then it will oscillate around the transition level. In the locked state, the analog output will be triangle wave, centered on the transition level with the peak-to-peak voltage:

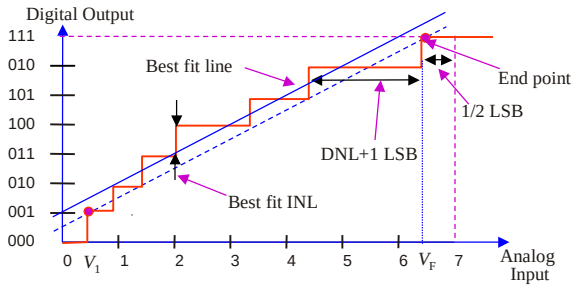
$$\Delta V = \frac{I}{C} T_s$$

where T_s is sampling period of the test setup. In practice, ΔV defines the resolution of the test and should be kept as small as possible (1/16 LSB or less).

Result of Static Testing

Summarizing Transfer Characteristic:

From the transfer characteristic, one can immediately determine DNL and INL of the ADC under test. In practice, the “best fit” method is used to determine INL. This method results in less INL than the standard method. The best fit line is obtained from “least-squares” cure-fitting method.



Result of Static Testing

Calculating the Specifications:

$$\mathrm{LSB}_{nom} = \frac{V_F - V_1}{2^N - 2}$$

$$\mathrm{DNL}_i = \frac{V_{i+1} - V_i}{\mathrm{LSB}_{nom}} - 1 \ \text{(LSB)}; \ i = 1,...,2^N - 2$$

$$\mathrm{DNL}_0 = \mathrm{DNL}_{2^N - 1} = 0$$

INL base of end-points definition:

$$\mathrm{INL}_i = \frac{V_i - [(i-1)\mathrm{LSB}_{nom} + V_1]}{\mathrm{LSB}_{nom}} = \sum_{j=0}^{i-1} \mathrm{DNL}_j \quad ; \ i = 1,...,2^N - 1$$

$$\mathrm{INL}_1 = \mathrm{INL}_{2^N - 1} = 0$$

Test of A/D Converters

Dynamic Testing

Properties:

For dynamic test, the input signal is a periodic rather than a DC input level. This input voltage has some frequency components up to the operating frequency range of the ADC.

Advantages:

- ✓ Well suited to Automatic Test Equipment (ATE), e.g., Teradyne
- ✓ Faster
- ✓ Less expensive
- ✓ Reveal nonlinearity related to input frequencies.

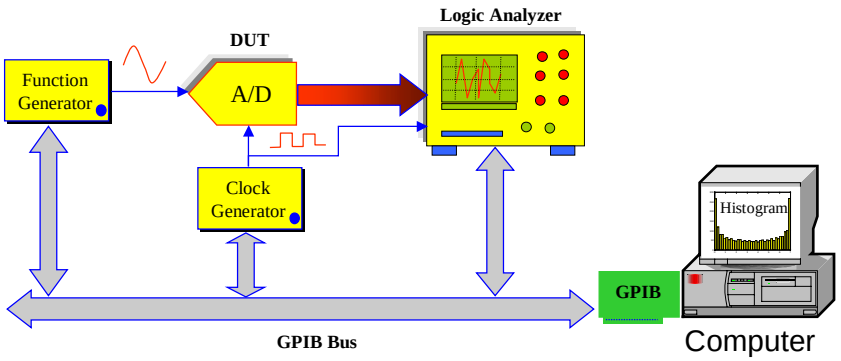
Disadvantage:

- ❖ Mask some important ADC's imperfections, e.g., monotonicity

Dynamic Testing

Computer-Based Test for High-Speed ADCs:

LabView from National Instruments can be used for the control of test equipment and monitoring the results.

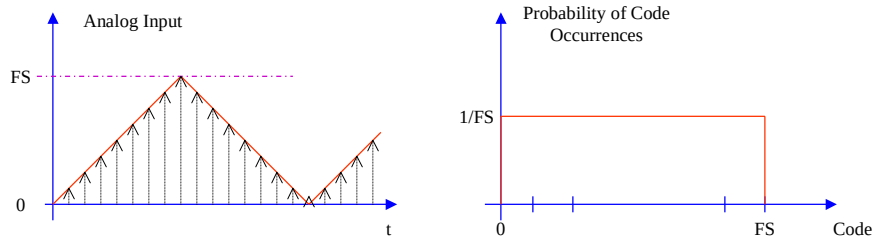


Dynamic Tests: Histogram Testing

Properties:

This test based on the fact that a periodic signal will create a predictable percentage of time within a given code band.

Triangle Waveform:

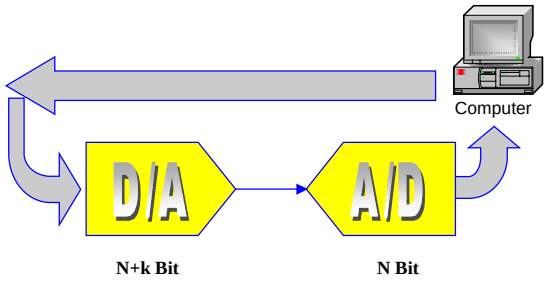


Dynamic Tests: Histogram Testing (cont.)

Implementation:

We can use a DAC in order to generate the input signal of the ADC under test. The DAC should be 2 to 4 bits more precise than ADC.

k is between 2 to 4 bits.



Dynamic Tests: Histogram Testing (cont.)

DNL and INL Measurements:

The INL and DNL can be calculated according to the histogram.

We assume that the input is a triangle wave.

$$\mathrm{DNL}_i = \frac{h_{actual}(i) - h_{ideal}(i)}{h_{ideal}(i)} \qquad h_{ideal}(i) = \frac{N'_{total}}{2^N - 2}$$

Lowest and highest codes are excluded!

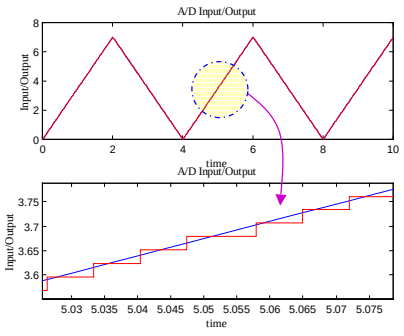
End-point INL: $\mathrm{INL}_i = \sum_{j=0}^{i-1} \mathrm{DNL}_j$

where N'_{total} is total sample size (excluded lowest and highest bin), and $h(.)$ is number of occurrences in a bin related to the code.

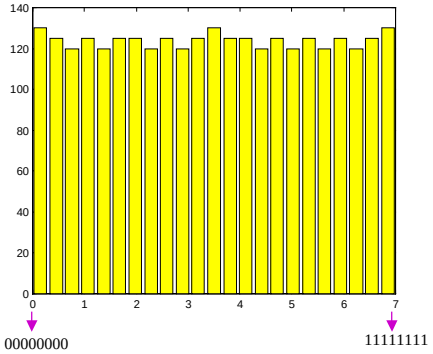
Dynamic Tests: Histogram Testing (cont.)

Example: Triangle Input Signal

N = 8 bits; V_{ref} = 7 V, DNL= 0.1 LSB



Histogram of Output Code



Dynamic Tests: Histogram Testing (cont.)

Uncertainty of DNL Estimation:

The estimation error is defined as

$$\varepsilon_{DNL}(i) = DNL_i - \hat{DNL}_i = 1 - \frac{h_{actual}(i)}{N_{tot}\, p_i}$$

where p_i is the code probability of the ith code. We have

$$\sigma(\varepsilon_{DNL}(i)) = \frac{1}{2N_{tot}\, p_i} \qquad (\varepsilon_{DNL}(i))_{\max} = \pm\frac{1}{N_{tot}\, p_i}$$

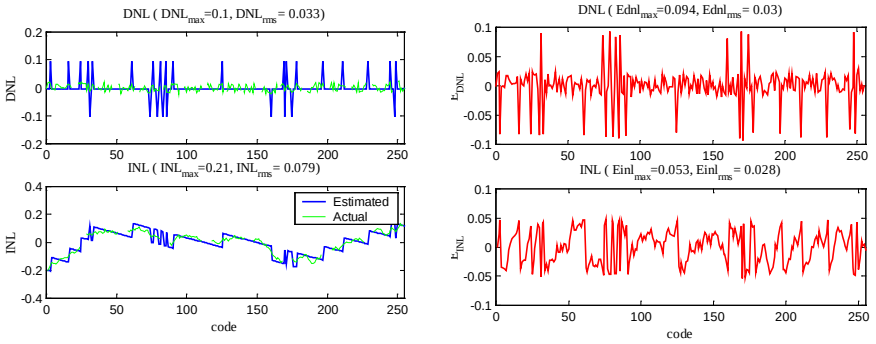
Example: for having a maximum error of 0.1 LSB

$$N_{tot} > 10 \times 2^N$$

Dynamic Tests: Histogram Testing (cont.)

Example: Triangle Input Test Signal

N = 8 bits; V_{ref} = 2 V, INL= 0.2 LSB, $N_s = 10 \times 2^8$

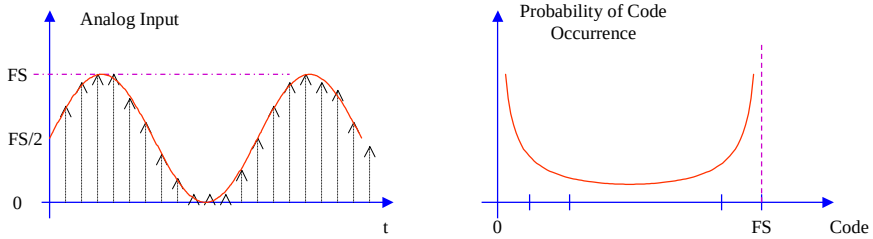


Dynamic Tests: Histogram Testing (cont.)

Sinusoidal Waveform [18]:

Linear ramp signals are very difficult to generate at high frequencies. Sinewave is used in practice.

$$y = A + A\sin(2\pi t) \qquad f(y) = \frac{1}{\pi\sqrt{A^2 - (y-A)^2}}; \quad A = \frac{FS}{2}$$



Dynamic Tests: Histogram Testing (cont.)

Sinusoidal Test Input:

If the bias of input sinewave is at $V_{ref}/2$, then the probability of ith code is

$$p_i = \frac{1}{\pi}\left\{\sin^{-1}\left(\frac{b_i - (V_{ref}/2)}{A}\right) - \sin^{-1}\left(\frac{b_{i-1} - (V_{ref}/2)}{A}\right)\right\}; \quad i \neq 0, 2^N - 1$$

$$b_i = \frac{V_{ref}}{2^N - 1}(i + 0.5)$$

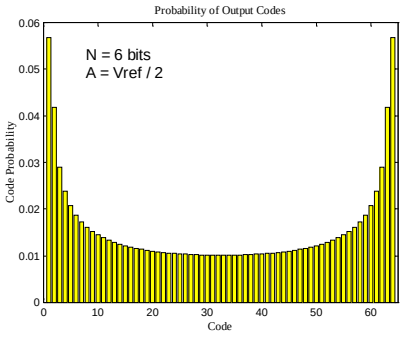
The amplitude can be estimated by

$$\hat{A} = \frac{V_{ref}\left(1 - \frac{1}{2^N - 1}\right)}{2\sin\left(\frac{\pi}{2}.\frac{N_{Tot} - h(0) - h(2^N - 1)}{N_{Tot}}\right)} \qquad \mathrm{DNL}_i = \frac{h(i)}{N_{Tot}\,p_i} - 1\,\mathrm{LSB}$$

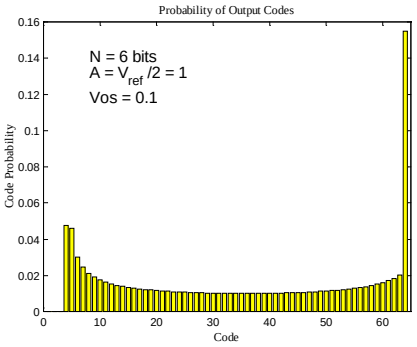
Dynamic Tests: Histogram Testing (cont.)

Code Probability for Sinusoidal Input:

$$V_{in} = 1 + \sin(2\pi\ f\ t)$$



$$V_{in} = 1 + \sin(2\pi\ f\ t) + \underbrace{0.1}_{V_{os}}$$



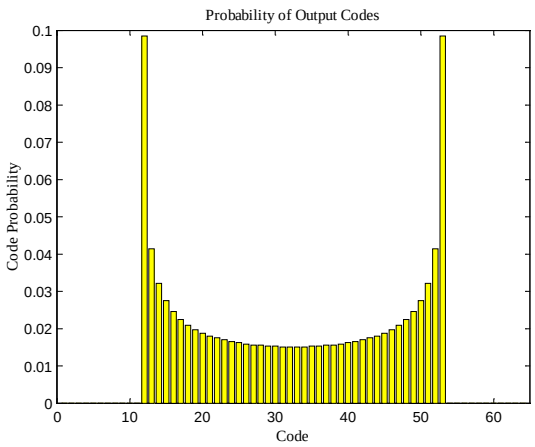
Dynamic Tests: Histogram Testing (cont.)

Code Probability for Subrange Sinusoidal Input:

$$V_{in} = 1.5 + \sin(2\pi\ f\ t)$$

$$V_{ref} = 3\ \text{V}$$

$$V_{os} = 0$$

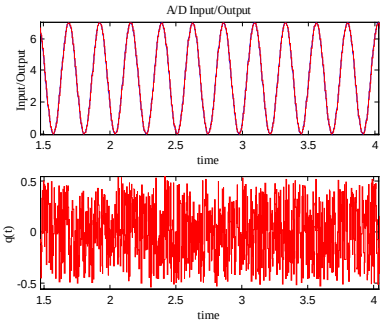


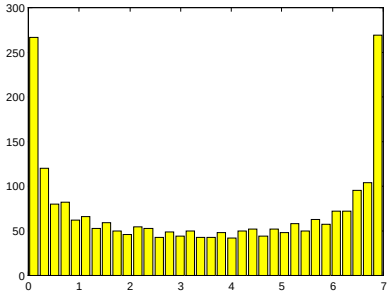
Dynamic Tests: Histogram Testing (cont.)

Example Sinusoidal Input Signal:

N = 8 bits; V_{ref} = 7 V, INL= 0.1 LSB

Histogram of Output Code





Dynamic Tests: Histogram Testing (cont.)

Minimum Number of Samples:

The minimum average number of samples occurs for the mid code and is equal to

$$\langle N_i \rangle_{\min} = \frac{2N_{total}}{\pi\left(2^{N_b}-1\right)}$$

$$\sigma(\varepsilon_{DNL})_{\max} = \frac{\pi}{4}\cdot\frac{2^N}{N_{tot}} \qquad \max\left[(\varepsilon_{DNL}(i))_{\max}\right] = \pm\frac{\pi}{2}\cdot\frac{2^N}{N_{tot}}$$

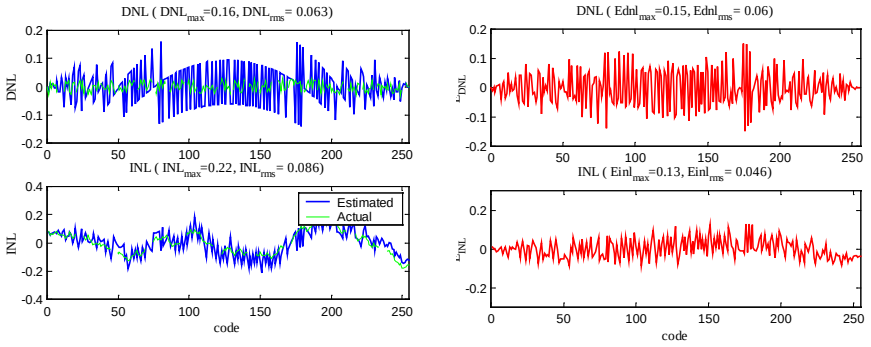
To have an error better than 0.25 LSB, we have

$$N_{total} > \pi 2^{N+1}$$

Dynamic Tests: Histogram Testing (cont.)

Example: Sinusoidal Input Test Signal

N = 8 bits; V_{ref} = 2 V, INL= 0.5 LSB, $N_s=10\times2^8$



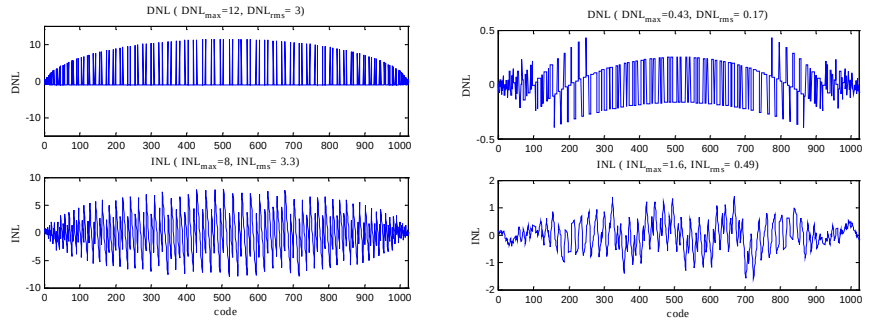
Dynamic Tests: Histogram Testing (cont.)

Example: Sinusoidal Input Test Signal

N = 10 bits; V_{ref} = 2 V, INL= 1.5 LSB, N_s=128

Without DNL Averaging

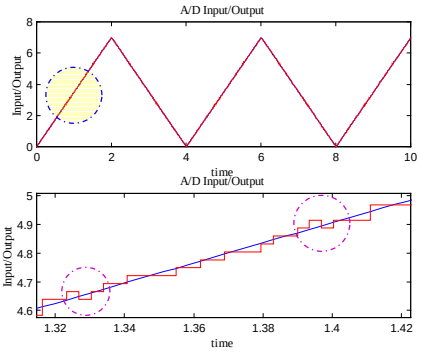
With DNL Averaging



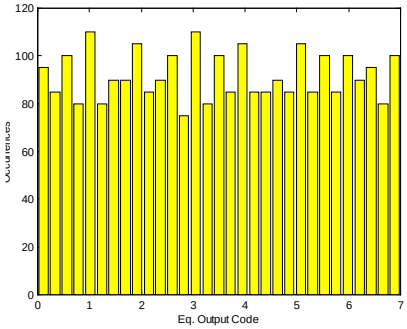
Dynamic Tests: Histogram Testing (cont.)

Disadvantage:

Monotonicity and noise cannot be easily detected by histogram testing. N = 8 bits; V_{ref} = 7 V, INL= 0.6 LSB



Histogram of Output Code



Dynamic Tests: Histogram Testing (cont.)

Selection of Input Test Signal:

It is of great importance that the input signal must not drift in amplitude, frequency, and shape. This test is based upon that the ADC samples a well-defined waveform and will spend a certain amount of time in each of the code bin.

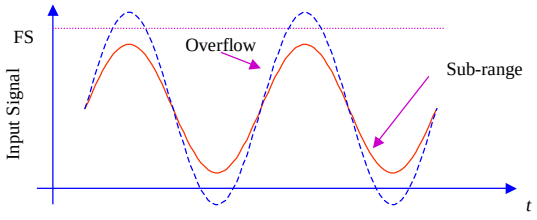
Sinusoidal signals can be easily generated accurately and stably with a relative simple circuit. That is why the sinusoidal input signal is usually for the ADC histogram testing. Even though the interpretation of the resultant data is more difficult than the triangle waveform.

Dynamic Tests: Histogram Testing (cont.)

Effect of Input Amplitude:

The amplitude of the input signal is also critical. In order to cover all code bins, the input signal has to sweep the entire of the input range, i.e. zero to V_{ref}.

- Out of range input results in extra numbers of zero and full-scale code.
- Covering a sub-range of the input results in not testing the ADC entirely.

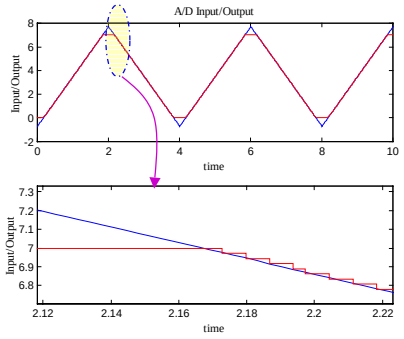


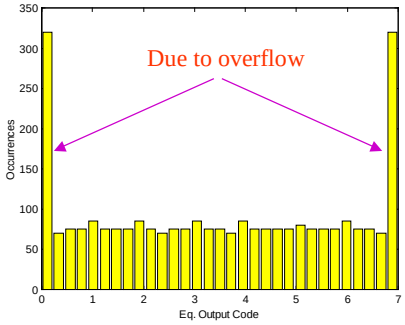
Dynamic Tests: Histogram Testing (cont.)

Example: Overflow input signal:

N = 8 bits; V_{ref} = 7 V, DNL= 0.1 LSB

Histogram of Output Code



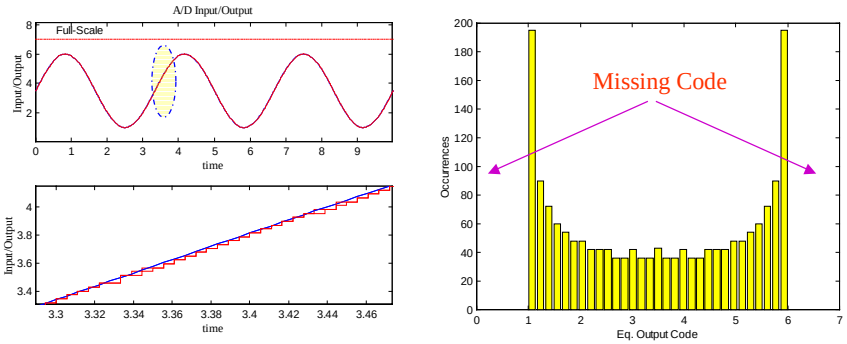


Dynamic Tests: Histogram Testing (cont.)

Example: sub-range input signal:

N = 8 bits; V_{ref} = 7 V, DNL= 0.1 LSB

Histogram of Output Code



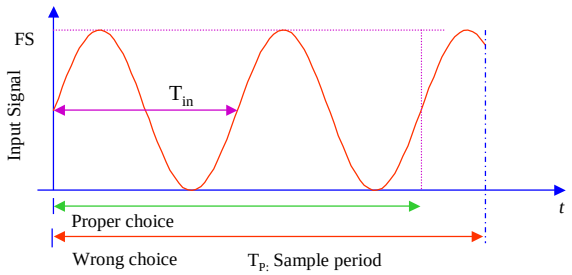
Dynamic Tests: Histogram Testing (cont.)

Sampling Technique:

In order to make sure that all the code bins are exercised properly, we should take special cares to the input signal frequency and sampling rate.

One should select multiples of the input signal period as the total sample period (T_P).

$$T_P = mT_{in} = \frac{m}{f_{in}}$$

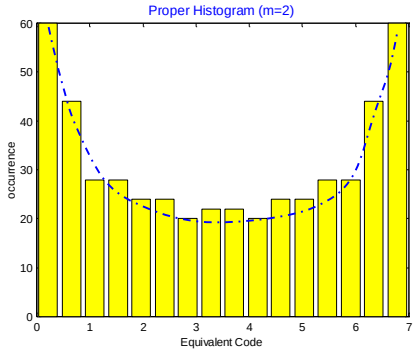


Dynamic Tests: Histogram Testing (cont.)

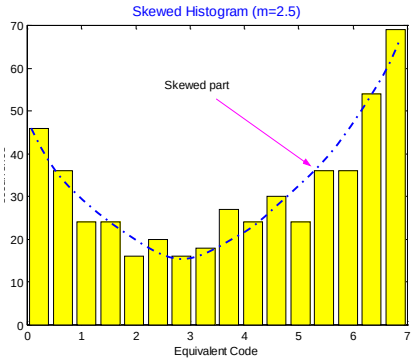
Selecting Sample Time:

Improper sample time TP results in skewed histogram.

Proper Selection m=2



Improper Selection m=2.5

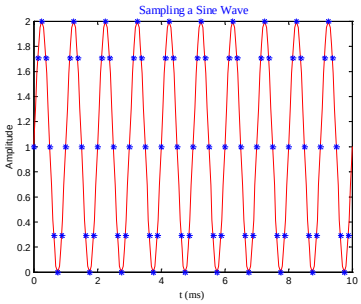


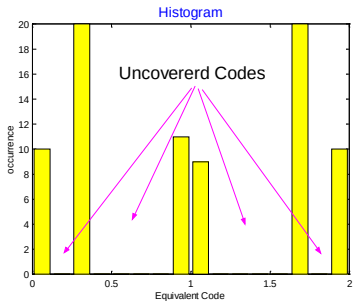
Dynamic Tests: Histogram Testing (cont.)

Sampling Technique:

In order to cover the codes as many as possible, one should avoid sampling around the same point at the consecutive cycles. In order to do that m and N_S should be mutually prime.

Example: m=10, N_S=80, N=4 bits

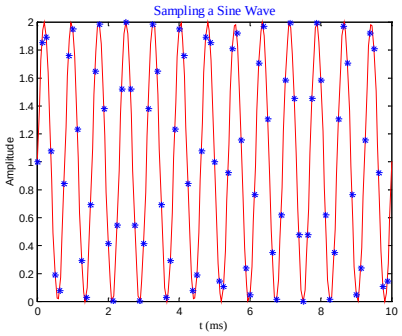


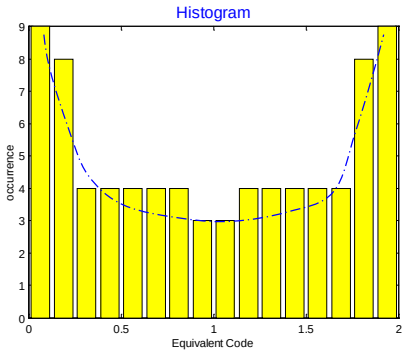


Dynamic Tests: Histogram Testing (cont.)

Example: Mutually prime selection

m=13, N_S=80, N=4 bits





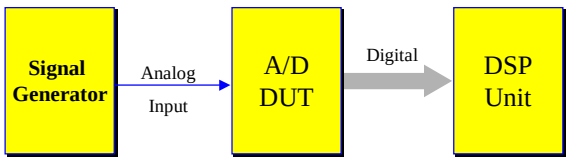
Dynamic Tests: FFT Testing

Generality:

One of the important signal processing methods is Fast Fourier Transform (FFT). This analysis provides us with how well the ADC converts a known input signal. A sinusoidal input signal is usually used for this test.

Advantages:

- ✓ All error sources are included in the results
- ✓ Useful sampling rate and input bandwidth can be used.



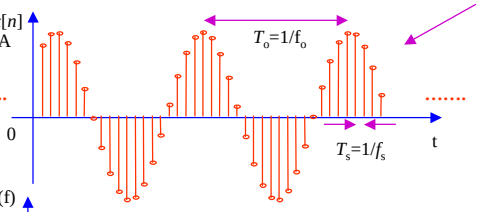
DUT: Device Under Test

Dynamic Tests: FFT Testing (cont.)

Fourier Transform for Discrete Signals:

This transformation is used for discrete signals and in general with unlimited samples.

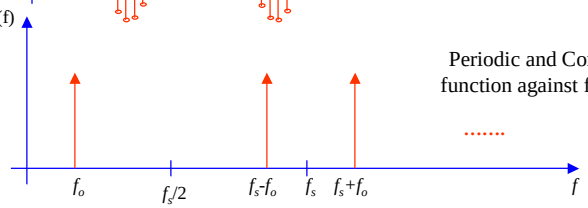
$$x[n] = T_s \int_{f_s} X(f) e^{\frac{j2\pi f}{f_s} n} df$$



Infinity samples

Sampled sine wave is not necessarily a periodic signal !

$$X(f) = \sum_{n=-\infty}^{n=\infty} x[n] e^{-j\frac{2\pi f}{f_s} n}$$



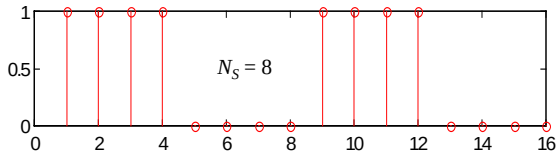
Periodic and Continuous function against frequency

Dynamic Tests: FFT Testing (cont.)

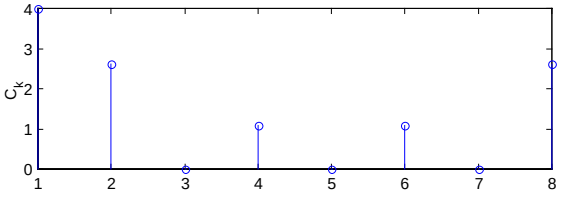
Discrete Fourier transform (DFT):

This transformation is used for discrete signals, which are periodic with a periodicity of N_S.

$$x[n] = \frac{1}{N_S} \sum_{k=0}^{k=N_S-1} c_k e^{j\frac{2\pi k}{N} n}$$



$$c_k = \sum_{n=0}^{n=N_S-1} x[n] e^{-j\frac{2\pi k}{N} n}$$



Dynamic Tests: FFT Testing (cont.)

Fast Fourier Transform (FFT):

FFT is DFT for which the number of samples N_S is a power of two.

Technique:

In order to have graphics which are easy to interpret , we should have:

$$x(t) = \sin(2\pi\ f_o t)$$

$$f_s = 1/T_s$$

$$x[n] = \sin(2\pi\ f_o n T_s)$$

$$f_o n T_s = m \Rightarrow f_o = \frac{m}{N_S} f_s$$

This condition creates a periodic discrete sine wave, which results in a DFT with one nonzero component at the f_o.

Frequency resolution in FFT:

N is also called number of bins, and m is bin number.

$$f_{res} = \frac{f_s}{N_S}$$

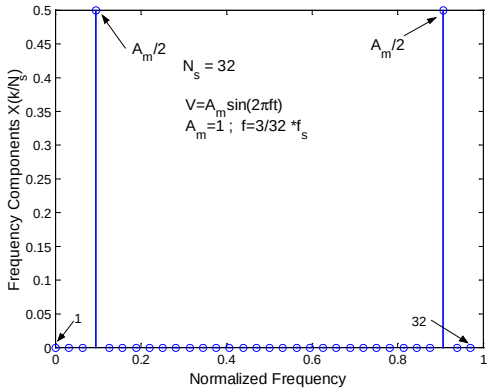
Dynamic Tests: FFT Testing (cont.)

Signal Frequency Components:

In order to find the frequency component of a truncated signal, the DFT must be normalized.

$$X(k) = \left| \frac{1}{N_S} \sum_{n=0}^{n=N_S-1} x[n] e^{-j\frac{2\pi\ k}{N} n} \right|$$

$$= \left| \frac{1}{N_S} FFT(x) \right|$$

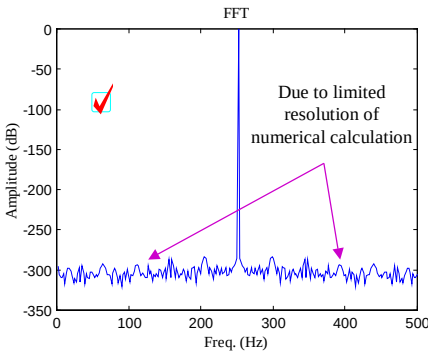


Dynamic Tests: FFT Testing (cont.)

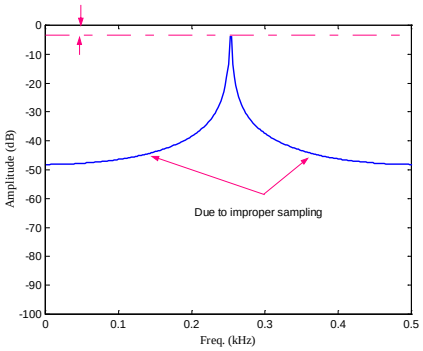
Example: Sine wave (sampling technique)

$x(t) = \sin(2\pi\ f_o t); \quad f_s = 1000; \quad N_S = 512; \quad f_{res} = 1.9531$

$f_o = 128\, f_{res} = 250$



$f_o = 128.512\, f_{res} = 251$



Dynamic Tests: FFT Testing (cont.)

Input frequency:

The frequency of the input sine wave have to be chosen as the bin number m and numbers of bins N_S be mutually prime.

Advantages:

- ✓ Quantization noise tends to be more randomly distributed (no unwanted harmonics).
- ✓ Mutually prime frequencies tend to cover and test most of code levels of the A/D converter.

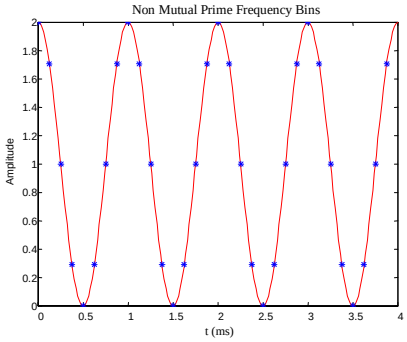
Dynamic Tests: FFT Testing (cont.)

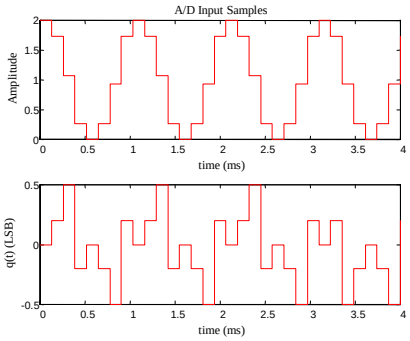
Example: 4-bit A/D Converter:

5 code levels are covered and to be tested among 16 levels!

$x(t) = \cos(2\pi\ f_o t);\quad f_s = 8\text{kHz};$

$N_S = 32;\quad m = 4;\qquad f_o = 1\text{kHz}$





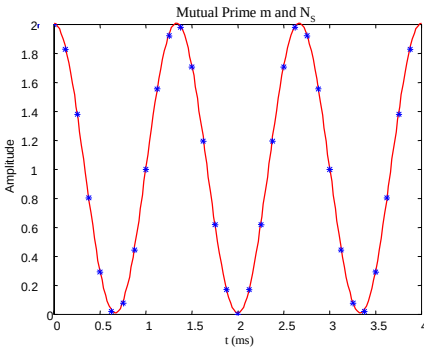
Dynamic Tests: FFT Testing (cont.)

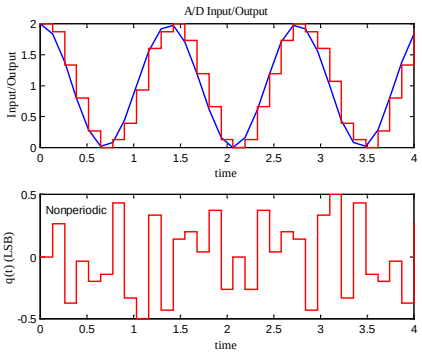
Example: 4-bit A/D Converter (16 code levels):

Most of the code levels are covered.

$f_s = 8\text{kHz};\quad N_S = 32;\quad m = 3;$

$f_o = 0.75\text{kHz}$



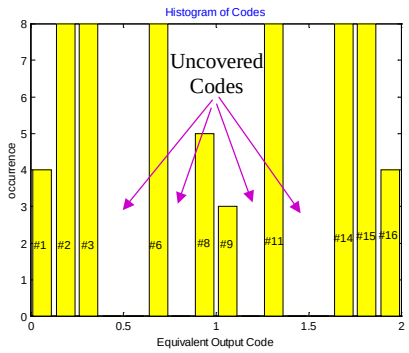


Dynamic Tests: FFT Testing (cont.)

Example: Code coverage for 4-bit ADC:

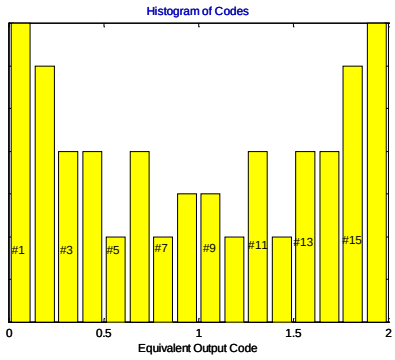
$$f_s = 8\text{kHz};\quad N_S = 64;$$

$m = 4;\quad f_o = 0.5\text{kHz}$



Non-mutual prime

$m = 3;\quad f_o = 0.375\text{kHz}$



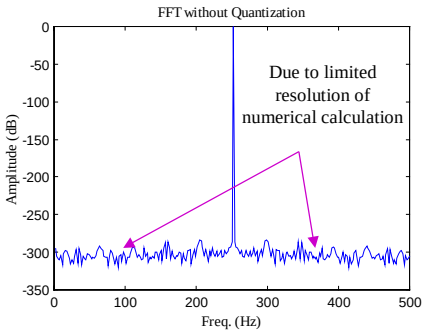
Mutual prime

Dynamic Tests: FFT Testing (cont.)

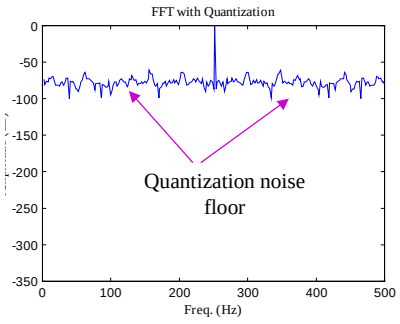
Example: Sine wave with quantization noise

8-bit ADC $\quad f_s = 1000;\quad N_S = 512;\ f_o = 250$

Input Signal



Digital Output Signal

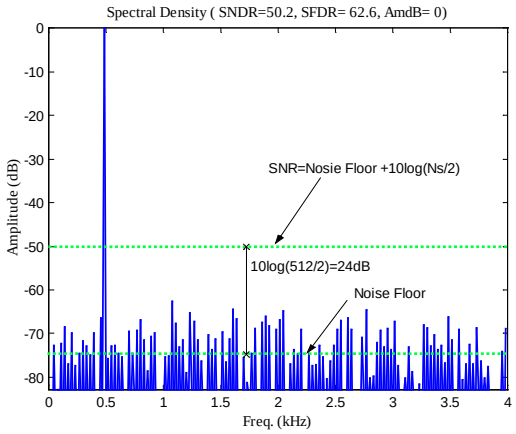


Dynamic Tests: FFT Testing (cont.)

SNR Based on Noise Floor:

8-bit ADC $\quad f_s = 8\text{kHz};\quad N_S = 512;\quad f_o = (31/512)\, f_s$

It is seen that the noise floor goes down when the number of samples increases.

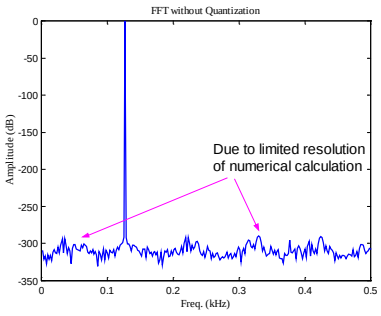


Dynamic Tests: FFT Testing (cont.)

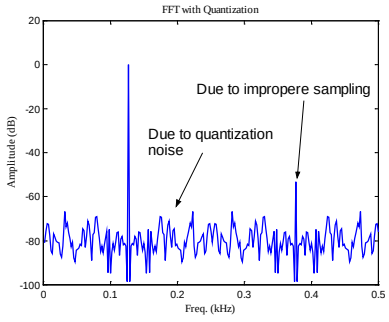
Example: Sine wave with quantization noise

8-bit ADC $\quad f_s = 1\,\text{kHz};\quad N_S = 512;\; f_o = (1/8)\times f_s = 125$

Input Signal



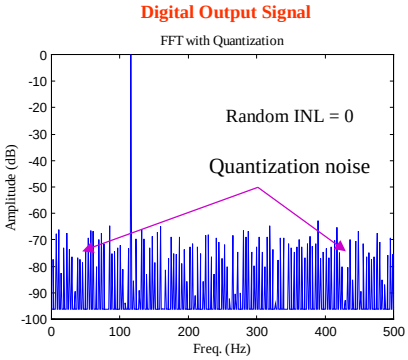
Digital Output Signal

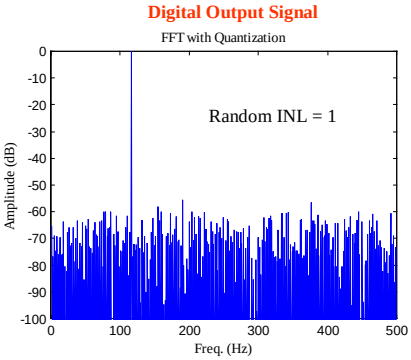


Dynamic Tests: FFT Testing (cont.)

Example: Sine wave with quantization noise and INL

8-bit ADC $f_s = 1000$; $N_S = 1024$; $f_o = 115.23$





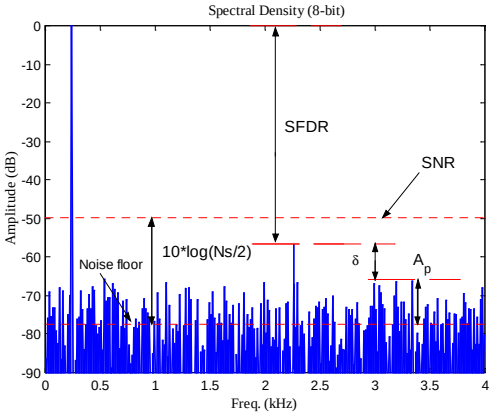
Dynamic Tests: FFT Testing (cont.)

Number of Samples for SFDR:

In order to measure SFDR, δ must be grater than zero.

$$N_S > 2\left(1+\frac{P_n}{P_q}\right)\cdot 10^{(0.3N_b-0.8+0.1A_P)}$$

Where Pn is power of electronic noise and Pq power of quantization noise. Ap is the peak value of noise to the noise floor. Typical value of Ap is 7dB.

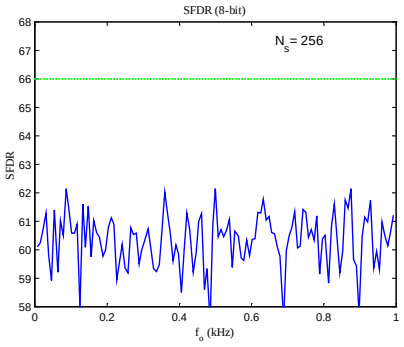


Dynamic Tests: FFT Testing (cont.)

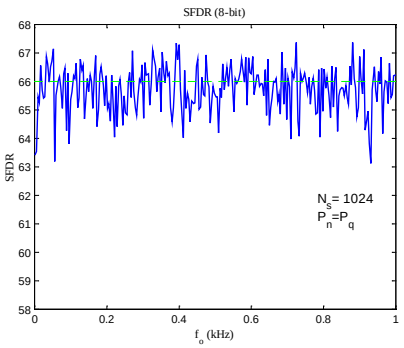
Example: SFDR Measurement

8-bit A/D

Minimum Ns is unsatisfied



Respect the Minimum Ns

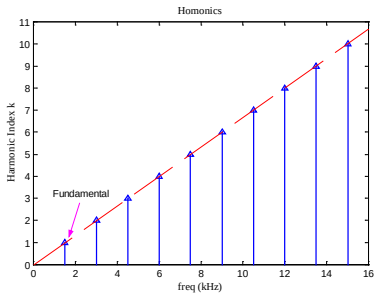


Dynamic Tests: FFT Testing (cont.)

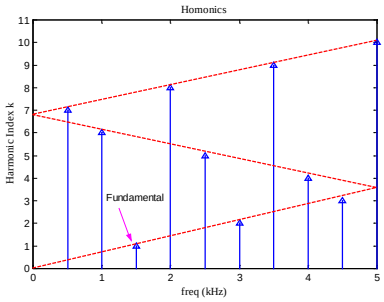
Harmonics:

If a signal with harmonics is sampled, the harmonics seen in FFT are folded and will be dislocated.

Harmonic Index before Sampling



Harmonic Index after Sampling



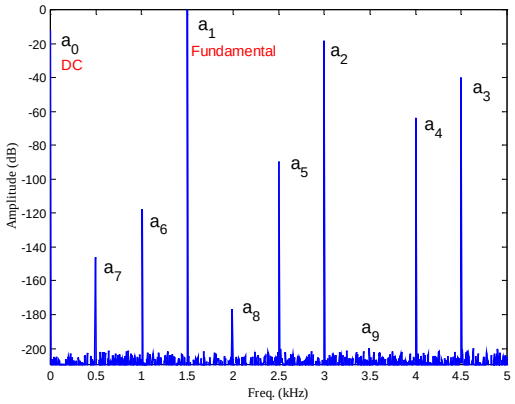
$f_s = 10$ kHz; $f_o = 1.5$ kHz with 10 harmonics

Dynamic Tests: FFT Testing (cont.)

Example: Sine wave with exponential nonlinearity

$f_s \cong 10\,\text{kHz};\quad N_S = 1024;\ f_o = 1.5\,\text{kHz}$

The noise floor must be lower than the level of desired harmonics.

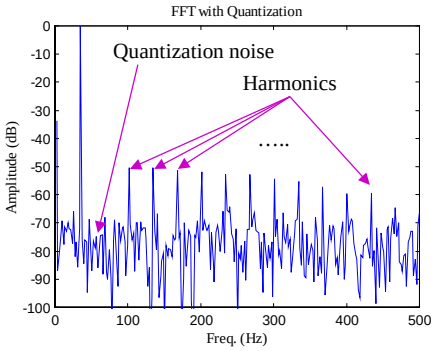


Dynamic Tests: FFT Testing (cont.)

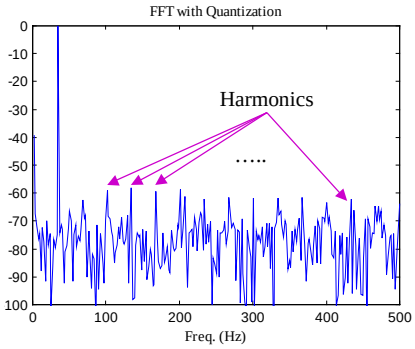
Example: Sine wave with quantization noise and nonlinearity

8-bit ADC $f_s = 1000;\quad N_S = 512;\ f_o = 33.2$ with Parabolic INL

High Nonlinearity (INL=4)



Low Nonlinearity (INL =2)



Dynamic Tests: FFT Testing (cont.)

Non Coherent Test:

If the signal generator and sampling clock are not synchronized, the test is called noncoherent.

$$f_o \neq \frac{m}{N_S} f_s$$

The direct FFT results are not exploitable. Windowing can be used to enhance the spectral density. However, windowing process has different gain for signal and noise. This phenomenon is not well-known.

$$G_S = \left[\frac{1}{N_S}\sum_{n=0}^{N_S-1} w[n]\right]^2 \quad \text{signal power gain}$$

$$G_N = \frac{1}{N_S}\sum_{n=0}^{N_S-1} w^2[n] \quad \text{noise power gain}$$

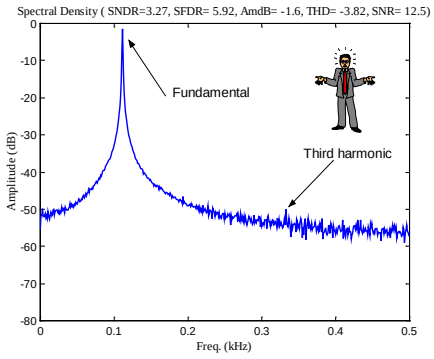
Dynamic Tests: FFT Testing (cont.)

Example: Sine wave with jitter noise and nonlinearity

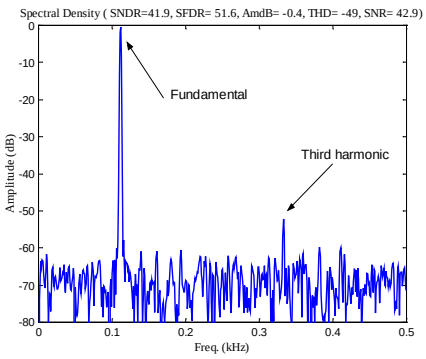
$f_s = 1\,\text{kHz};\quad N_S = 1024;\quad f_o = 0.11\,\text{kHz}$

$T_j = 0.01$

No windowing



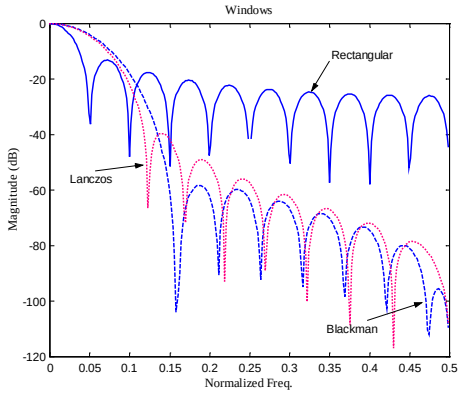
Blackman Windowing



Dynamic Tests: FFT Testing (cont.)

Selection of Windows

Selection of windows is based on the side lobs of its spectrum

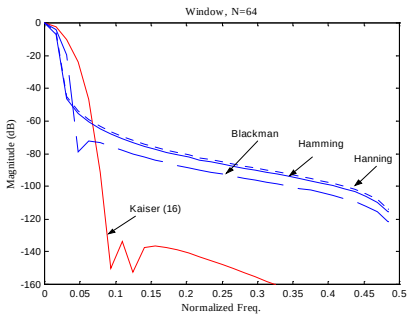


Dynamic Tests: FFT Testing (cont.)

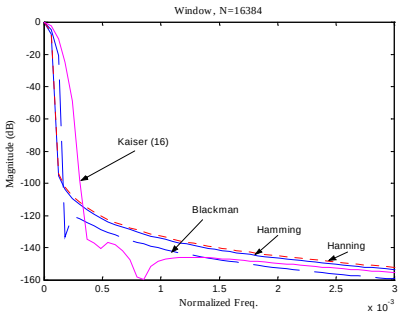
Side lobs in Coherent Sampling

Side lobs in coherent sampling are function of Ns and type of window.

Ns = 64



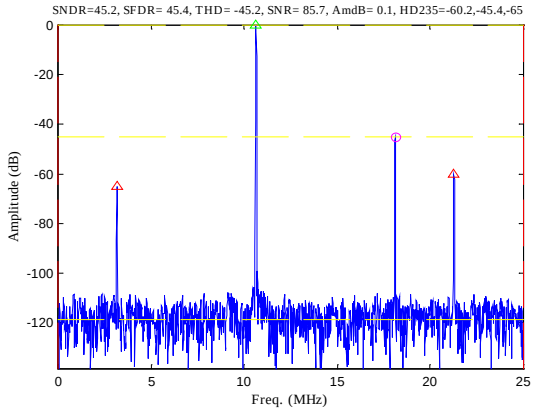
Ns = 16384



Dynamic Tests: FFT Testing (cont.)

Different Spectral Densities:

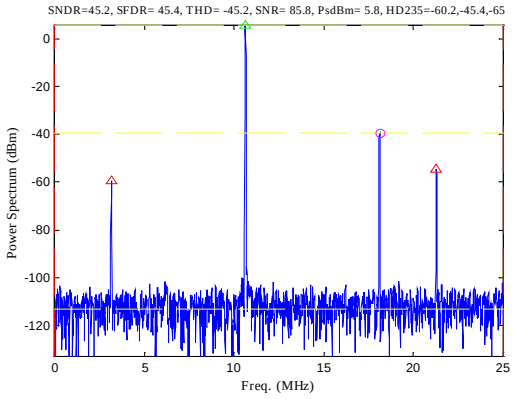
Signal Amplitude in dB for 14-bit A/D with nonlinearity.



Dynamic Tests: FFT Testing (cont.)

Power Spectral Density dBm

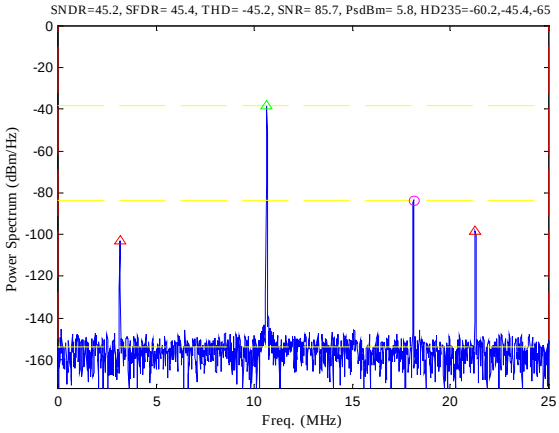
We consider a reference R and $P = 10\log\left(1000\frac{V_{rms}^2}{R}\right)$



Dynamic Tests: FFT Testing (cont.)

Power Spectral Density dBm/Hz

We consider a reference R and the power is dBm per Hz

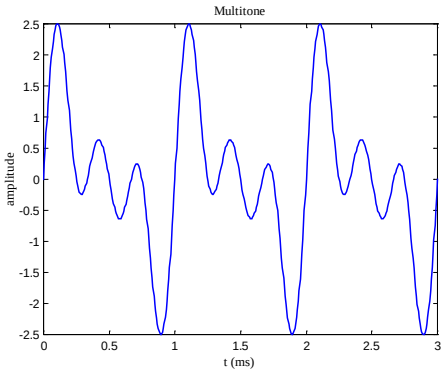


Dynamic Tests: FFT Testing (cont.)

Multitone Input Signal:

In order to characterize the A/D converter at several frequencies in one test, a multitone input signal can be used.

Three tones at 1 , 2, and 3kHz with amplitude 1 and coherent phase of zero.



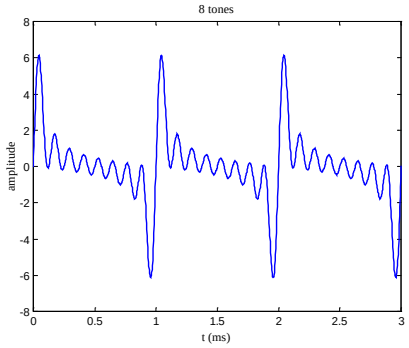
Dynamic Tests: FFT Testing (cont.)

Peak–to-RMS of Multitone Signal:

The input signal of an ADC must be in the predefined input range of ADC. This results in a better resolution and characterization of ADC.

The ratio of peak-to-RMS is pretty high for multitone signals. As a result, some codes are rarely hit. This ratio increases against number of tones.

Peak-to-RMS=3.1



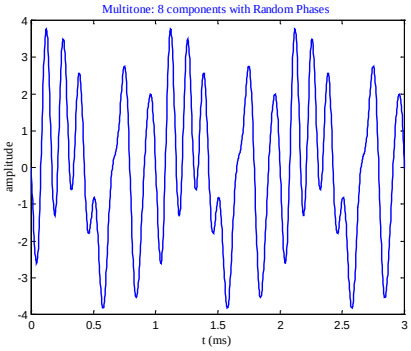
Dynamic Tests: FFT Testing (cont.)

Adjust the Peak–to-RMS of Multitone Signal:

The peak-to-RMS is a function of the phase of tones. Unfortunately, there is no explicit form which describes this relationship.

The best ratio can be found by choosing random phases and calculate the ratio. This process is done in a loop until the desired ratio obtained.

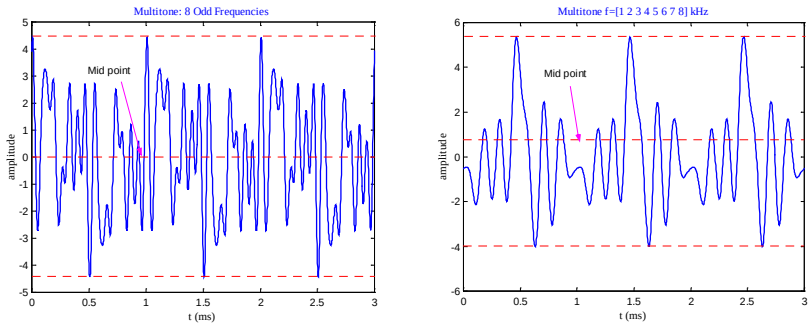
Peak-to-RMS=1.9



Dynamic Tests: FFT Testing (cont.)

Mid-point range for Random Phases:

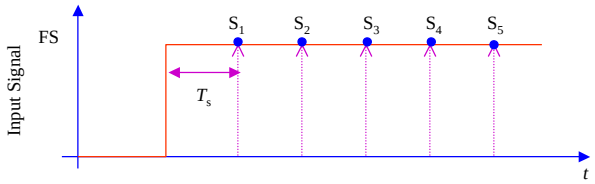
The mid point range of multitone signal with random phases is not symmetric. If negative peak maps to zero and positive peak to FS, then the signal have a DC component with respect to FS/2. This problem is avoided by choosing odd frequencies.



Dynamic Tests: Pulse Test

Description:

ADC's with multiplexed input channels have pulsed input signal. This type of signal contains frequency components well above the input bandwidth. In the pulse test, a step function is sampled at the nominal conversion rate. If the subsequent converted codes are within 1 LSB of each other, then the ADC meets the pulse test specifications.



Conclusions

- Static Testing
- Dynamic Testing
  - Histogram Testing
  - FFT Testing
  - Pulse Testing

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