the VPP pad current (Ivpp) are therefore smaller than 1 μA before two kinds of stresses. Table III illustrates ESD testing results of two IC pin combinations, VPP-VDD and VPP-VSS. ESD currents flow from the VPP pad to the VDD or VSS pad (VDD and VSS in 0 V), respectively. ESD testing results show this test-chip can pass human body mode (HBM) in 2.5 kV and machine mode (MM) in 250 V without OTP memory false-programmed issues. Finally, Table IV shows that there are no falsely-programmed events under latch-up overstress conditions. Regardless of whether there are positive/negative current stresses $(+\mathrm{IT}/-\mathrm{IT})$ 200 mA or positive voltage stress $(+\mathrm{VT})$ 8.25 V, this test-chip can successfully pass the latch-up testing criteria [15], and its power and VPP pad currents can be kept smaller than 0.2 μA.

VI. Conclusion

After silicon data verification, this new circuit architecture has been proven to provide power-switch functions in one I/O pad very well. Both functions of programming the OTP memory and processing the I/O signal can work well. Circuit designers can adopt this scheme to save one bonding pad. Furthermore, the functionalities of ESD protection and latch-up prevention for the IC product can also be approached.

This architecture can be applied for all technologies, and a similar architecture has also been proved in the micro-electro-mechanical-systems product processed in 0.18 μm.

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Analog Implementation of a Novel Resistive-Type Sigmoidal Neuron

Golnar Khodabandehloo, Mitra Mirhassani, and Majid Ahmadi

***Abstract*—An important part of any hardware implementation of artificial neural networks (ANNs) is realization of the activation function which serves as the output stage of each layer. In this work, a new NMOS/PMOS design is proposed for realizing the sigmoid function as the activation function. Transistors in the proposed neuron are biased using only one biasing voltage. By operating in both triode and saturation regions, the proposed neuron can provide an accurate approximation of the sigmoid function. The neuron circuit is designed and laid out in 90-nm CMOS technology. The proposed neuron can be potentially used in implementation of both analog and hybrid ANNs.**

***Index Terms*—Activation function, analog neuron, sigmoid function, sigmoidal neuron.**

I. Introduction

Artificial neural networks (ANNs) are used in a wide range of applications from signal processing systems to miscellaneous control devices [1]–[5]. Realization of activation function of neurons is one of the major challenges in hardware implementation of ANNs.

Both digital and analog modules can be used to realize the activation function in hardware implementations depending on the type of the neural network. Neural networks can be generally categorized into three groups: digital, analog, and hybrid (mixed-signal) neural networks.

In digital neural networks, both synaptic weight storage cells and activation function are realized by digital gates such as lookup tables (LUTs) which are generally used to approximate the activation function [6]–[8]. In analog neural networks, on the other hand, analog circuits are used both to estimate the activation function and to store the synoptic weights [1], [9]–[11].

The third group of neural networks are hybrid neural networks (HNNs) which are a combination of digital and analog gates [4], [5], [12]–[20]. In HNNs, analog circuits are employed to realize the activation function while weights are stored digitally.

Area and power consumption of analog activation functions are generally less than that of digital implementations [11], [17]–[19]. However, analog circuits are more vulnerable to mismatch and process violations. In addition, digital implementation usually results in a better estimation of the ideal activation function. Consequently, it is important to make analog implementation of neurons more accurate to profit from both an area/power efficient design and an appropriate realization at the same time.

Activation function produces the output of each layer in the feed forward neural networks according to the value of its input. Several activation functions are generally used such as step function, tangent hyperbolic and sigmoid function. The last two ones are nonlinear functions which generate an S shaped curve. In this work, the sigmoid function is realized with an output between 0 and 1.

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For many years, transistor characteristics in different operating regions (triode and saturation) has been used for function realization in analog implementations [9], [21]. A previously reported neuron employs the transistor square law in saturation region to generate the sigmoid function [4], [5], [15]–[17]. This neuron is a resistive-type neuron as it has a current input/voltage output characteristic. However, transistors are working only in off or saturation regions. Transistors jumping from one region to the other one introduces noise spikes to the power line. In addition, all the transistors are off for a certain range of inputs which makes the output unreliable for that range.

In this paper, a new resistive-type neuron is designed which generates the sigmoid function based on the transistor characteristics in both triode and saturation regions; consequently, it approximates the sigmoid function smoother and with more precision compared to the previous design. Furthermore, the proposed neuron offers a linear relation between input current and output voltage for a certain range of inputs which matches the linear approximation of the sigmoid function using Taylor series.

The proposed neuron is designed and simulated in 90-nm STM CMOS technology and simulation results are compared to those of the previously reported neuron. Simulations show that the proposed neuron is less sensitive to process variations, and the area consumption of the proposed neuron is less than that of the previous design.

This paper is organized as follows. The proposed neuron specifications are discussed in Section II. Section III includes the sigmoid function approximation. In Section IV, simulation results and comparisons are reported followed by the conclusion.

II. Resistive-Type Sigmoidal Neuron

Sigmoid function is a nonlinear function which maps each input to an output in the range of $[0, 1]$. The sigmoid function considered in this paper is also known as the logistic function and is defined as follows:

$$f(t) = \frac{1}{1 + e^{-t}}. \tag{1}$$

Analog realization of the activation function [4], [5], [12]–[17] provides a fast and power efficient realization compared to the digital realization in a noticeably smaller area [11], [17]–[19]. Analog compact realizations, however, suffer from lack of precision and are vulnerable to mismatch and circuit variations.

Based on the resistive-type neuron introduced in [14], a resistive-type neuron with low sensitivity to circuit variations has been employed in [4], [5], [15]–[18] to generate a sigmoid-like function for analog implementations of neural networks. Since the transistors are jumping from saturation region to off region and vice versa, this neuron intrinsically has a spiking character. This issue increases the total noise of the circuit specially in a system-on–chip (SoC) design with lots of neurons. Furthermore, it fails to follow the sigmoid function for a range of currents near zero where all of its transistors are off.

The proposed neuron is designed such that it can use transistors in both triode and saturation operation regions. Fig. 1 shows the proposed circuit to approximate the sigmoid function.

In the neuron presented in Fig. 1, the input to the neuron is the summation current from the synapses. Depending on the value of the input current, a voltage is generated at the output node. This neuron, named a resistive-type neuron, has a resistive-like nature.

The proposed design needs only one reference voltage to bias the transistors as VB_1 is equal to VB_2. Transistors $M5$ and $M6$ are sized to generate the biasing voltage of $V_B = Vdd/2$ while transistors $M1$, $M2$, $M3$, and $M4$ generate the sigmoid function. Transistor sizes are outlined in Table I; the value for L is selected equal to 0.2 μm for all the transistors.

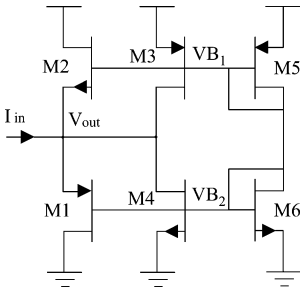

Fig. 1. Schematic of the proposed resistive-type sigmoidal neuron.

TABLE I
Transistor Sizes of the Proposed Neuron

Transistor	$M1$	$M2$	$M3$	$M4$	$M5$	$M6$
(W/L)	5.3/1	2.7/1	4/1	1.3/1	4/1	1.3/1

TABLE II
Operating Regions of the Proposed Neuron

Region	I_{in}	V_{out}	$M1$	$M2$	$M3$	$M4$
I	< 0	$0 \le V_{out} \le V_B - V_{tn}$	off	sat	sat	triode
II	< 0	$V_B - V_{tn} \le V_{out} \le V_B$	off	off	sat	sat
	$= 0$	$V_{out} = V_B$				
	> 0	$V_B \le V_{out} \le V_B + \mid V_{tp} \mid$				
III	> 0	$V_B + \mid V_{tp} \mid \le V_{out} \le Vdd$	sat	off	triode	sat

The proposed neuron of Fig. 1 operates in three regions as are summarized in Table II.

Input current, $I_{\rm in}$, in each region is calculated according to the region of operation of the transistors. For ease of calculation, threshold voltage of NMOSs, V_{tn}, is considered to be equal to that of PMOSs, V_{tp}, in all the equations ($V_{tn} = V_{tp} = V_t$). The input/output node is at the source of $M2$ and $M1$ and the drain of $M3$ and $M4$.

In region I, the input current sinking from the neuron causes a small voltage in the output node. Therefore, transistor $M1$ turns off and $M4$ enters the triode region while the other two transistors are in saturation region. Currents of transistors $M2$ and $M3$ enter the input/output node while current of $M4$ exits the node; however, this current is smaller than the current of the other two transistors. The Input current in this region is defined as follows:

$$\begin{aligned} I_{\rm in} = & -\frac{1}{2}k_n S_2 (V_B - V_{\rm out} - V_t)^2 (1 + \lambda (V_{dd} - V_{\rm out})) \\ & - \frac{1}{2}k_p S_3 (V_{dd} - V_B - V_t)^2 (1 + \lambda (V_{dd} - V_{\rm out})) \\ & + k_n S_4 \left((V_B - V_t) V_{\rm out} - \frac{1}{2} {V_{\rm out}}^2 \right) \end{aligned} \tag{2}$$

where S is defined as (W/L).

The output voltage increases as the input current increases which causes a change in operating region of transistors. In region II, both $M3$ and $M4$ are in saturation region while the other two transistors are off. Region II can be divided into three subregions. The first subregion is when the current is negative. A negative current means that the current coming from $M3$ to the input/output node is greater than the current exiting through $M4$. As the output voltage increases, the current of $M4$ increases while the current of $M3$ decreases. Second subregion starts when the output voltage reaches $V_{dd}/2$; in this case,

the current is equal to zero which means that the currents of $M3$ and $M4$ are canceling each other. With increasing output voltage more, the current of $M4$ becomes greater than that of the $M3$, which is the third subregion. Current in this region is approximated as follows:

$$I_{\text{in}} = -\frac{1}{2}k_pS_3(V_{dd} - V_B - V_t)^2(1 + \lambda(V_{dd} - V_{\text{out}})) + \frac{1}{2}k_nS_4(V_B - V_t)^2(1 + \lambda V_{\text{out}}). \quad (3)$$

The input current is positive in region III. The corresponding value of the output voltage makes $M1$ and $M3$ to operate in saturation and triode regions, respectively, while the regions of operation for the other two transistors remain unchanged. The input current in this region is as follows:

$$I_{\text{in}} = \frac{1}{2}k_pS_1(V_{\text{out}} - V_B - V_t)^2(1 + \lambda V_{\text{out}}) + \frac{1}{2}k_nS_4(V_B - V_t)^2(1 + \lambda V_{\text{out}}) - k_pS_3((V_{dd} - V_B - V_t)(V_{dd} - V_{\text{out}}) - \frac{1}{2}(V_{dd} - V_{\text{out}})^2). \quad (4)$$

In region II, (3), in order to have I_{in} equal to zero while V_{out} is equal to $Vdd/2$, k_pS_3 is chosen equal to k_nS_4. This will set the center line of the output curve. Also, in Table I, S_2 is equal to $2S_4$ and $3S_1$ is equal to $4S_3$. These transistor ratios are necessary in order to keep the symmetry around the center point $I_{\text{in}} = 0$.

To solve (2)–(4) for V_{out}, a constant voltage, V_{cons}, is defined as $V_B - V_t = V_{dd} - V_B - V_t = V_{\text{cons}}$. For (2) and (4), channel modulation effect is ignored ($\lambda = 0$).

The following equations show the value of V_{out} in each region

$$\text{Region(I)}V_{\text{out}} = V_{\text{cons}} - \sqrt{\frac{I_{\text{in}} + (2k_pS_3 - 1)V_{\text{cons}}{}^2}{2k_pS_3}} \quad (5)$$

$$\text{Region(II)}V_{\text{out}} = \frac{I_{\text{in}}}{\lambda V_{\text{cons}}^2 k_pS_3} + \frac{V_{dd}}{2} \quad (6)$$

$$\text{Region(III)}V_{\text{out}} = \frac{1}{7}V_{\text{cons}} + \frac{3}{7}V_{dd} + \sqrt{\frac{6I_{\text{in}}}{7k_pS_3} + D} \quad (7)$$

where D is calculated through the following equation:

$$D = \frac{6V_{\text{cons}}V_{dd}}{7}(1 + V_{\text{cons}}) - \left(48\frac{V_{\text{cons}}}{7}\right)^2 - 12\left(\frac{V_{dd}}{7}\right)^2. \quad (8)$$

Equation (6) shows that V_{out} is a linear function of I_{in} in region II where both $M3$ and $M4$ operate in their saturation regions; this equation can be represented as follows:

$$V_{\text{out}} = RI_{\text{in}} + V_B, \quad R = \frac{1}{\lambda V_{\text{cons}}^2 k_pS_3}. \quad (9)$$

Input/output characteristic of the proposed neuron is shown in Fig. 2 for input currents between -70 and 70 μA.

III. Sigmoid Function Approximation

Several approximation methods have been previously used for sigmoid function approximation such as centered recursive interpolation (CRI) [6], [23]. Taylor series are used in this section to approximate the sigmoid function in order to prove that the proposed neuron in an appropriate realization of such function. This section shows that using the Taylor series results in an accurate approximation of the sigmoid function with negligible error of less than 1.3%.

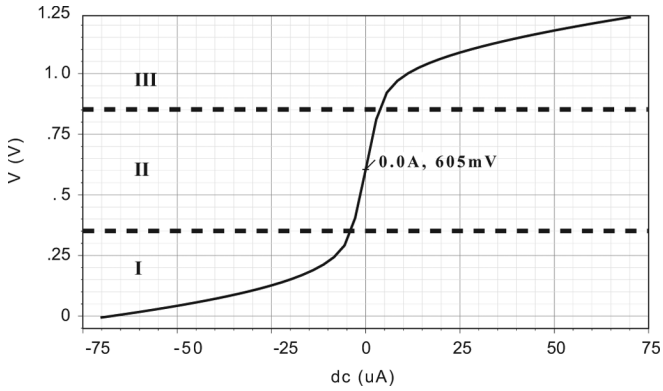

Fig. 2. Simulation result of the proposed neuron.

Sigmoid function of (1) can be rewritten as follows for $-\infty < t < +\infty$:

$$f(t) = \begin{cases} 1, & \text{for } t \to +\infty \\ \frac{e^t}{(1+e^t)}, & \text{otherwise} \\ 0, & \text{for } t \to -\infty. \end{cases} \quad (10)$$

Replacing e^t with $1 + \alpha(\alpha > 0)$ for $t > 0$ and applying the Taylor series expansion of $1/(1 - x)$ for $-1 < x < 1$ will result in the following equation:

$$\frac{e^t}{1 + e^t} = 1 - \frac{1}{2}\left[1 - \frac{\alpha}{2} + \frac{\alpha^2}{4} - \cdots\right] = \frac{1}{2} + \frac{\alpha}{4} \text{ for } 0 < \alpha \ll 1. \quad (11)$$

Similarly, the following equation is achieved for $t < 0$:

$$\frac{e^t}{1 + e^t} = \frac{1}{2} - \frac{\alpha}{4} \text{ for } 0 < \alpha \ll 1. \quad (12)$$

According to the Taylor series expansion of e^x for $-\infty < x < +\infty$, e^t can be estimated by the following equation:

$$e^t = 1 + t + \frac{t^2}{2!} + \cdots = 1 + t \text{ for } |t| \ll 1. \quad (13)$$

Recalling that e^t is replaced with $1 + \alpha$ or $1 - \alpha$ in (11) and (12), t is almost equal to $\pm\alpha$ for $|\alpha| \ll 1$.

To give an example to clarify the last statement, suppose α is equal to ± 0.1. Thus, $e^t = \alpha + 1$ will be equal to 1.1 or 0.9. From (13), t is equal to $0.095 \simeq 0.1$ or $-0.105 \simeq -0.1$ for $e^t = 1.1$ or $e^t = 0.9$, respectively.

From (11) and (12), the sigmoid function is linear while $|t| \ll 1$ and can be estimated by $1/2 + t/4$.

Calculations show that sigmoid function of (10) is linear for $-0.6 < t < 0.6$ with an error smaller than 1.3%. In addition, the sigmoid function can be approximated outside the range of -6 and 6 by 0 and 1, respectively, with an error less than 0.3%. Therefore, (10) can be potentially estimated by the following equation:

$$f(t) = \begin{cases} 1, & 6 < t \\ \frac{e^t}{(1+e^t)}, & 0.6 < t < 6 \\ \frac{1}{2} + \frac{t}{4}, & -0.6 < t < 0.6 \\ \frac{e^t}{(1+e^t)}, & -6 < t < -0.6 \\ 0, & t < -6. \end{cases} \quad (14)$$

Consequently, the linear function of (6) successfully realizes the sigmoid function for a certain range of I_{in}.

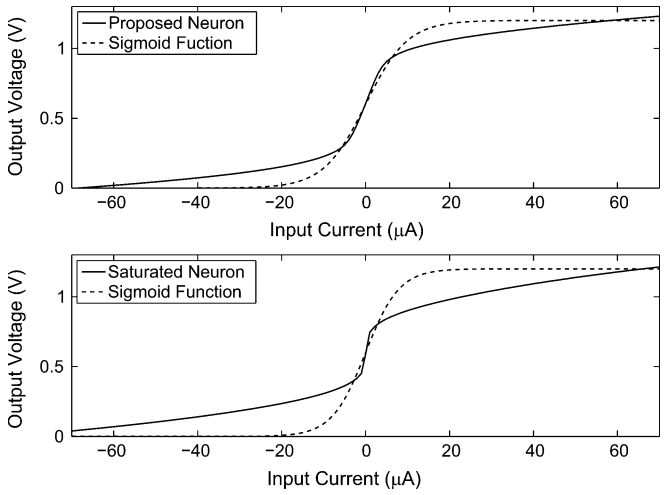

Fig. 3. Comparing the (top) proposed neuron and the (bottom) saturated neuron to the ideal sigmoid function.

IV. Simulation Results and Comparisons

The proposed resistive-type neuron has three advantages over the previously reported resistive-type neuron [16]. First, it has no off region; off region refers to a range of input values near zero for which the output remains unchanged. Second, it has a linear region which matches the sigmoid function linear region. Finally, only two of the four transistors jump from off to saturation and the other two change gradually from triode to saturation and vice versa. Therefore, the output curve is smoother in the proposed design which can provide a more accurate estimation of the sigmoid function in its nonlinear region.

The proposed neuron is simulated in 90-nm CMOS technology using power supply voltage of 1.2 V. The previously reported neuron [16] is also simulated in the same technology for comparison. In the previously reported neuron, transistors are either off or in saturation region; therefore, in this paper, it will be referred as saturated neuron.

Fig. 3 compares the output voltage of the proposed neuron and the saturated neuron to the original sigmoid function.

The maximum error between the proposed neuron and the sigmoid function for the current input range of -6 to 6 μA is 7.67%, while the average error is 4.12%. For the saturated neuron within the same input range, the maximum and average errors are 59.52% and 14.08%, respectively.

Corner analysis for different conditions FF (Fast NMOS Fast PMOS), SS (Slow NMOS Slow PMOS), FS (Fast NMOS Slow PMOS), and SF (Slow NMOS Fast PMOS) are performed for both the proposed and saturated neurons.

In the worst case scenario, corner analysis shows that the maximum output voltage variations from TT (Typical NMOS Typical PMOS) condition, are 5.76% and 4.86% for the proposed and saturated neuron, respectively, for $-6\ \mu\text{A} < I_{\text{in}} < 6\ \mu\text{A}$. For the same range of input currents, the maximum output voltage variations from the ideal sigmoid function are 37.42% and 74.37% for the proposed neuron and the saturated neuron, respectively.

Consequently, while the maximum output voltage variation of the proposed neuron from the TT condition is slightly (less than 1%) more than voltage variation of the saturated neuron, its maximum voltage variation from the ideal function is almost half of the voltage variation of the saturated neuron.

In addition, the effect of the temperature on the output voltage is studied. The temperature is changed between $-55\,^{\circ}$C and 125 $^{\circ}$C and the corresponding voltages are measured. For the proposed design, the voltage variations from the voltage value in 27 $^{\circ}$C are 0.7% and 1.4% for $-55\,^{\circ}$C and 125 $^{\circ}$C, respectively. These values for the saturated neuron are changing to 0.5% and 0.2% for $-55\,^{\circ}$C and 125 $^{\circ}$C, respectively. Although the proposed neuron shows more voltage variations with the temperature compared to the saturated one, its voltage variations are still less than 1.4%. Consequently, the proposal works properly in a wide range of temperatures between $-55\,^{\circ}$C and 125 $^{\circ}$C.

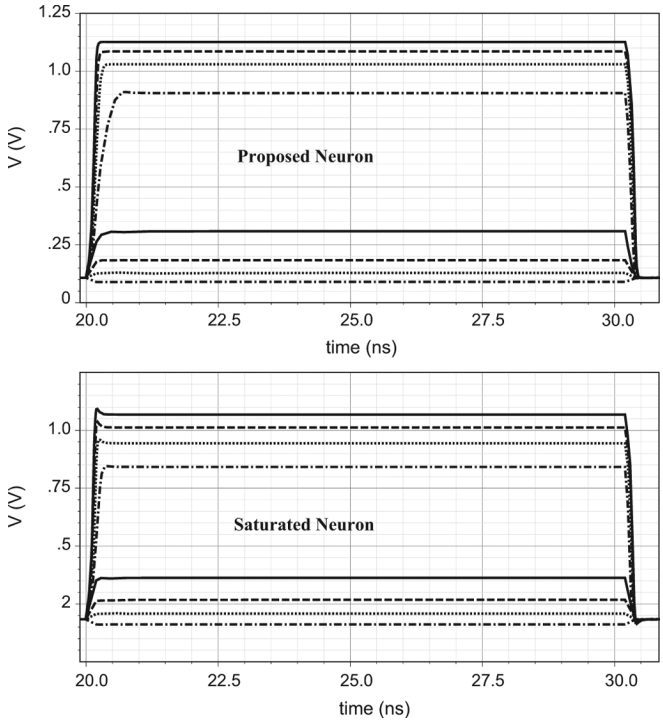

Fig. 4. Transient simulation result of the proposed and saturated neurons.

A combination of temperature and corner analysis is also performed on the both neurons. The operation of the circuits in $-55\,^{\circ}$C and 125 $^{\circ}$C for different corner conditions is observed. Simulations show that the proposed neuron has an average variation of 20.9% from the TT condition in the room temperature (27 $^{\circ}$C). This voltage variation is equal to 13.04% for the saturated neuron. Consequently, the proposed neuron is more vulnerable to temperature variation compared to the saturated neuron by less than 8%.

Fig. 4 shows the transient simulations of the proposed neuron and saturated neuron. Here, the input current changes from -30 μA to a range of currents between -35 and 35 μA with step size of 10 μA. Therefore, in Fig. 4, for curves from bottom to top, the relevant currents are -35, -25, -15, -5, 5, 15, 25, and 35 μA.

As is shown in Fig. 4, there are ringings in the saturated neuron at the edges when the current is changing from one value to the other one. These ringings are eliminated in the proposed neuron.

The proposed neuron layout is shown in Fig. 5. Area of the saturated neuron is reported 36.5 μm $\times$ 19.4 μm in 1.2-μm CMOS process [16]. However, to make it comparable with the proposed neuron, layout of the optimized saturated neuron is extracted in 90-nm STM CMOS technology. Table III summaries some of the comparison results, it also shows that the proposed neuron consumes less area compared to the saturated one.

Analog neurons are generally prone to mismatch and the proposed resistive-type analog neuron is not an exception. Parametric analysis is used to study the mismatch in the proposed neuron. The simulations show that even with 20% mismatch in $M1$ and $M2$ transistor ratios, the circuit can work properly.

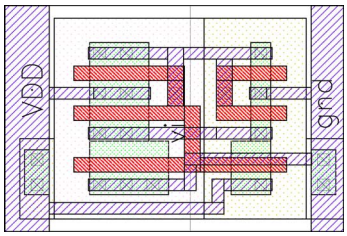

Fig. 5. Layout of the proposed neuron.

TABLE III
COMPARISON BETWEEN THE PROPOSED NEURON AND THE SATURATED NEURON

Neuron	Error from Ideal		Corner Analysis		Corner+Temp.	Area
Structure	Max.	Ave.	Max.	Ave.	Ave.	Consumption
Saturated	59.52%	14.08%	74.37%	4.86%	13.04%	$11.319(\mu m)^2$
Proposed	7.67%	4.12%	37.42%	5.76%	20.9%	$7.9576(\mu m)^2$

There are some methods to reduce the vulnerability to mismatch of the proposed neuron for implementing a neural network. One method is to use a current buffer as an interface for the synapse output current before entering the neuron. This buffer will prevent the feedback from the neuron to the synapse output. Another method is to use the differential structure [12], [13], [17].

V. CONCLUSION

A sigmoidal I-to-V neuron is proposed which makes use of only one biasing voltage. Nevertheless, it uses transistors in both triode and saturation region to realize the sigmoid function. The simulation results show that the new design approximates the sigmoid function more accurately compared to the previous design specially in its linear region, while it consumes less area. The proposed sigmoidal neuron can be used in analog implementation of activation functions for both pure analog neural networks and HNNs.

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