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D-Type Flip-Flop with Asynchronous Clear

NL17SZ175

The NL17SZ175 is a single, positive edge triggered, D−type CMOS Flip−Flop with Asynchronous Clear operating from a 1.65 V to 5.5 V supply.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.6 ns t_{PD} at V_{CC} = 5 V (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Sink 32 mA at 4.5 V
- Available in SC−88, SC−74 and UDFN6 Packages
- Chip Complexity < 100 FETs
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

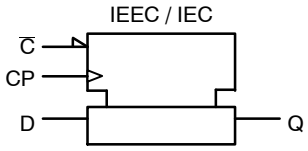

Figure 1. Logic Symbol

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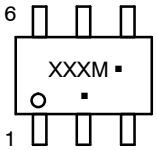
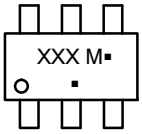
MARKING DIAGRAMS

SC−88
CASE 419B−02

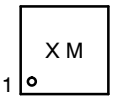


SC−74
CASE 318F−05



UDFN6
1.45 x 1.0
CASE 517AQ

UDFN6
1.0 x 1.0
CASE 517BX



X, XXX = Specific Device Code
M = Date Code*
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

Connection Diagrams

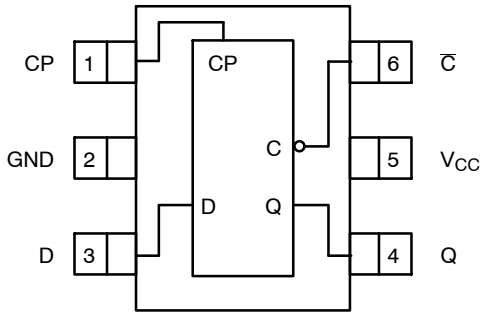


Figure 2. SC−88/SC−74 (Top View)

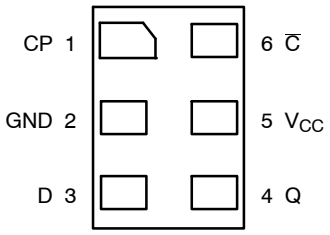


Figure 3. UDFN6(Top Through View)

PIN DESCRIPTIONS

Pin Name	Description
D	Data Input
CP	Clock Pulse Input
$\overline{C}$	Clear Input
Q	Flip−Flop Output

FUNCTION TABLE

Inputs			Output
CP	**D**	**$\overline{C}$**	**Q**
↑	L	H	L
↑	H	H	H
↓	X	H	Qn
X	X	L	L

H = HIGH Logic Level
L = LOW Logic Level
Qn = No Change in Data
X = Immaterial

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_{OUT}	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SC−88 SC−74 UDFN6	377 320 154	°C/W
P_D	Power Dissipation in Still Air	SC−88 SC−74 UDFN6	332 390 812	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)		± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm−by−1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0 0 0	20 20 10 5	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−55°C ≤ T_A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65 to 1.95	0.65 V_{CC}	–	–	0.65 V_{CC}	–	V
			2.3 to 5.5	0.70 V_{CC}	–	–	0.70 V_{CC}	–	
V_{IL}	Low−Level Input Voltage		1.65 to 1.95	–	–	0.35 V_{CC}	–	0.35 V_{CC}	V
			2.3 to 5.5	–	–	0.30 V_{CC}	–	0.30 V_{CC}	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −100 μA I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	 1.65 to 5.5 1.65 2.3 3 3 4.5	 V_{CC} − 0.1 1.29 1.9 2.4 2.3 3.8	 V_{CC} 1.52 2.1 2.7 2.5 4	 – – – – – –	 V_{CC} − 0.1 1.29 1.9 2.4 2.3 3.8	 – – – – – –	V
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = 100 μA I_{OH} = 4 mA I_{OH} = 8 mA I_{OH} = 16 mA I_{OH} = 24 mA I_{OH} = 32 mA	 1.65 to 5.5 1.65 2.3 3 3 4.5	 – – – – – –	 – 0.08 0.12 0.24 0.26 0.31	 0.1 0.24 0.3 0.4 0.55 0.55	 – – – – – –	 0.1 0.24 0.3 0.4 0.55 0.55	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	1.65 to 5.5	–	–	±0.1	–	±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0	–	–	1.0	–	10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5	–	–	1.0	–	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

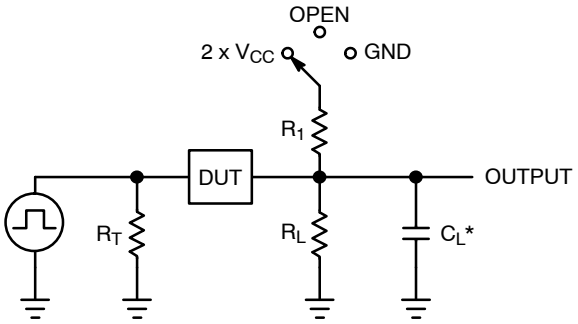
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency (Figure 4, 5)	1.65	C_L = 50 pF, R_L = 500 Ω	–	–	–	100	–	MHz
		1.8		–	–	–	100	–	
		2.3 to 2.7		–	–	–	125	–	
		3.0 to 3.6		–	–	–	150	–	
		4.5 to 5.5		–	–	–	175	–	
t_{PLH}, t_{PHL}	Propagation Delay, CP to Q (Figure 4, 5)	1.65	C_L = 15 pF, R_L = 1 MΩ	–	9.8	15.0	–	16.5	ns
		1.8		–	6.5	10.0	–	11.0	
		2.3 to 2.7		–	3.8	6.5	–	7.0	
		3.0 to 3.6		–	2.8	4.5	–	5.0	
		4.5 to 5.5		–	2.2	3.5	–	3.8	
		3.0 to 3.6	C_L = 50 pF, R_L = 500 Ω	–	3.4	5.5	–	6.2	
		4.5 to 5.5		–	2.6	4.0	–	4.7	
t_{PHL}	Propagation Delay, $\overline{C}$ to Q (Figure 4, 5)	1.65	C_L = 15 pF, R_L = 1 MΩ	–	9.8	13.5	–	15.0	ns
		1.8		–	6.5	9.0	–	10.0	
		2.3 to 2.7		–	3.8	6.0	–	6.4	
		3.0 to 3.6		–	2.8	4.3	–	4.6	
		4.5 to 5.5		–	2.2	3.2	–	3.5	
		3.0 to 3.6	C_L = 50 pF, R_L = 500 Ω	–	3.4	5.3	–	5.8	
		4.5 to 5.5		–	2.7	4.0	–	4.5	
t_S	Setup Time, CP to D (Figure 4, 5)	2.3 to 2.7	C_L = 50 pF, R_L = 500 Ω	–	–	–	2.5	–	ns
		3.0 to 3.6		–	–	–	2.0	–	
		4.5 to 5.5		–	–	–	1.5	–	
t_H	Hold Time, CP to D (Figure 4, 5)	2.3 to 2.7	C_L = 50 pF, R_L = 500 Ω	–	–	–	1.5	–	ns
		3.0 to 3.6		–	–	–	1.5	–	
		4.5 to 5.5		–	–	–	1.5	–	
t_W	Pulse Width, CP (Figure 4, 5)	2.3 to 2.7	C_L = 50 pF, R_L = 500 Ω	–	–	–	3.0	–	ns
		3.0 to 3.6		–	–	–	2.8	–	
		4.5 to 5.5		–	–	–	2.5	–	
	Pulse Width, $\overline{C}$ (Figure 4, 5)	2.3 to 2.7	Clock HIGH or LOW C_L = 50 pF, R_L = 500 Ω	–	–	–	3.0	–	ns
		3.0 to 3.6		–	–	–	2.8	–	
		4.5 to 5.5		–	–	–	2.5	–	
t_{rec}	Recovery Time, $\overline{C}$ to CP (Figure 4, 5)	2.3 to 2.7	C_L = 50 pF, R_L = 500 Ω	–	–	–	1.0	–	ns
		3.0 to 3.6		–	–	–	1.0	–	
		4.5 to 5.5		–	–	–	1.0	–	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	4.0	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	4.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Test	Switch Position	C_L, pF	R_L, Ω	R_1, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	2 x V_{CC}	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care

Figure 4. Test Circuit

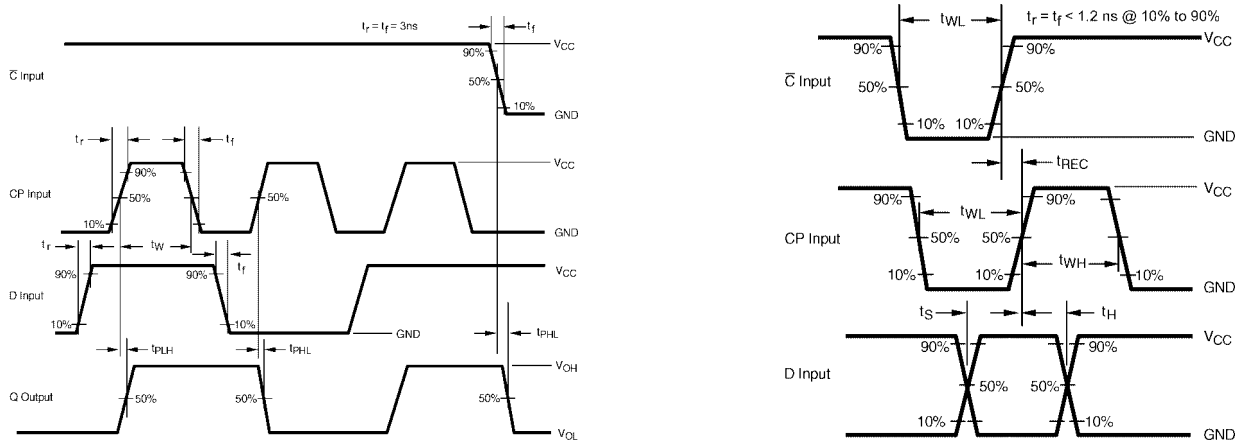


Figure 5. Switching Waveforms

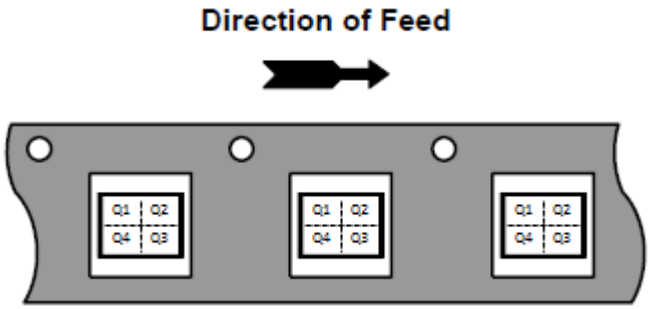
V_{CC}, V	V_{mi}, V	V_{mo}, V		V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	
1.65 to 1.95	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	0.15
2.3 to 2.7	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	0.15
3.0 to 3.6	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	0.3
4.5 to 5.5	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	0.3

DEVICE ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping†
NL17SZ175DFT2G (In Development)	SC−88	TBD	Q4	3000 / Tape & Reel
NL17SZ175DBVT1G	SC−74	AT	Q4	3000 / Tape & Reel
NL17SZ175MU1TCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P	TBD	Q4	3000 / Tape & Reel
NL17SZ175MU3TCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P	TBD	Q4	3000 / Tape & Reel

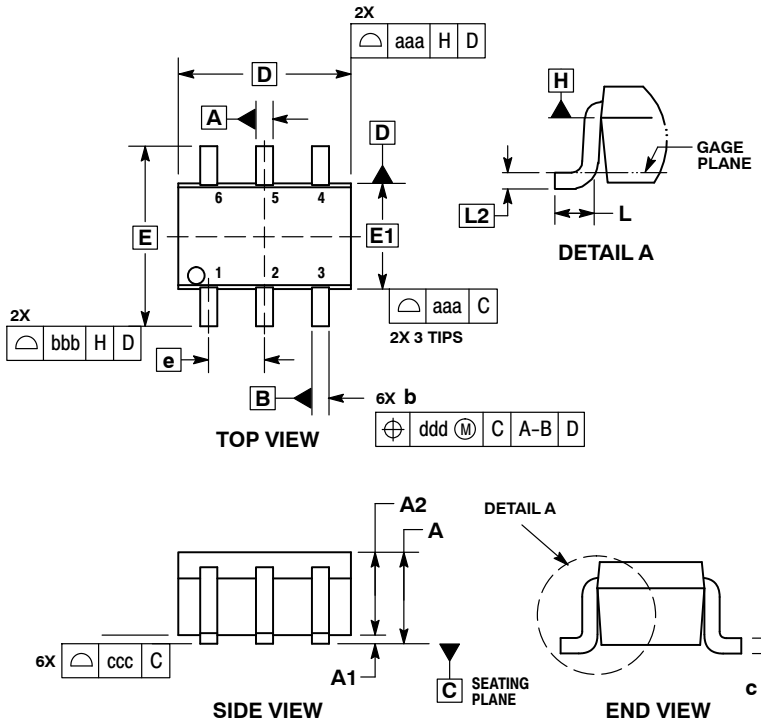
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin 1 Orientation in Tape and Reel



PACKAGE DIMENSIONS

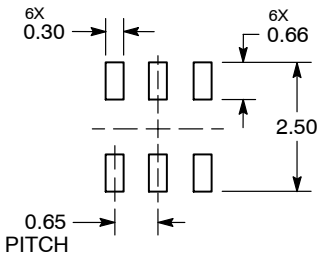
SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*

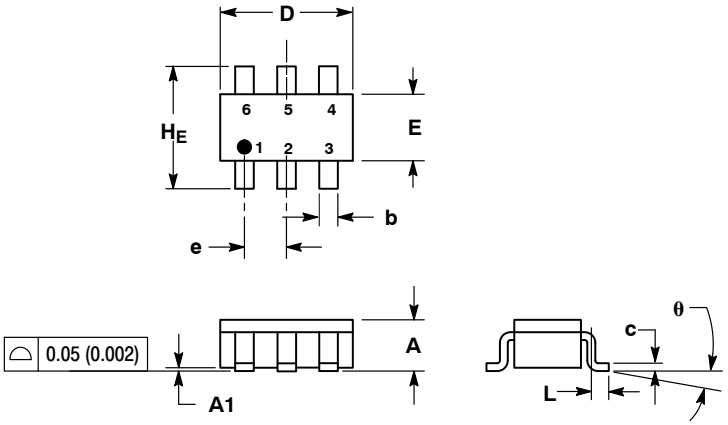


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

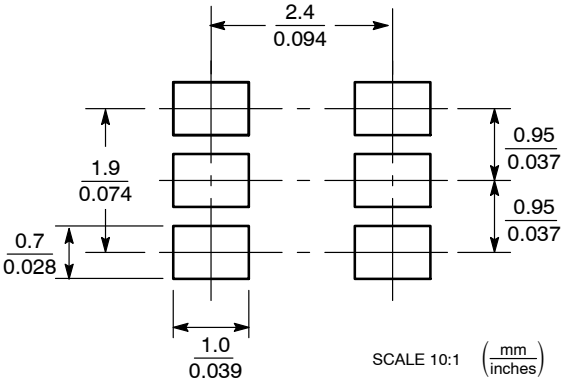
SC−74
CASE 318F−05
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1

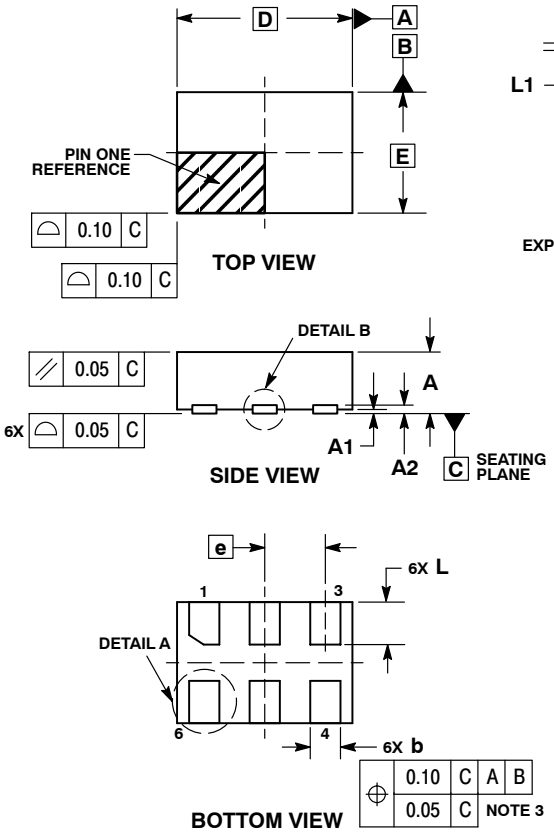
STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

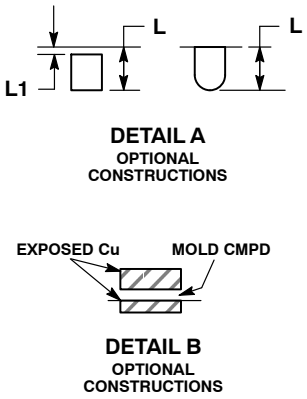
STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O

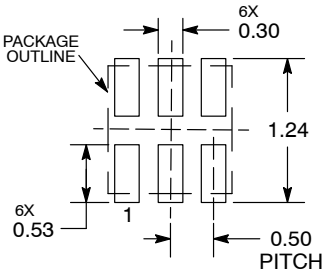




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT

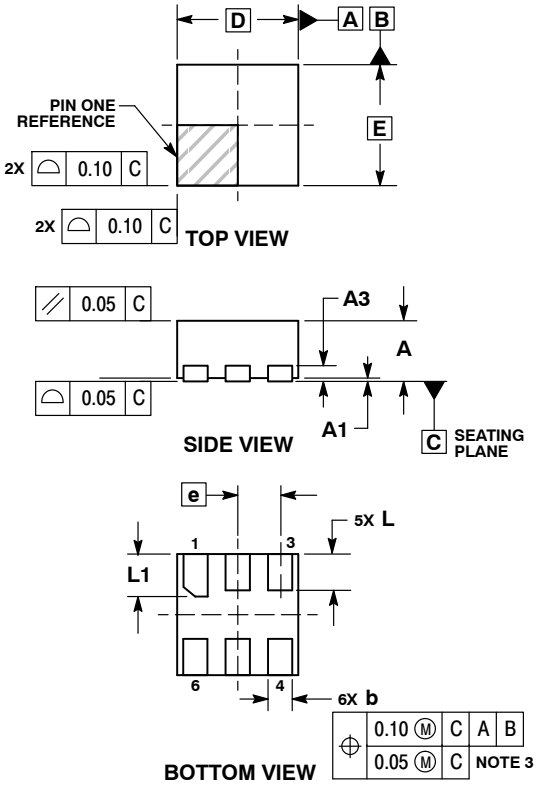


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

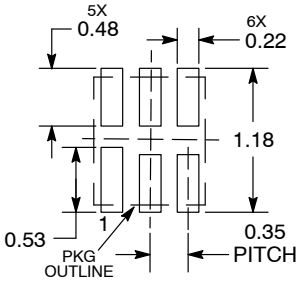
UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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