

# Converting GaAs FET Models For Different Nonlinear Simulators

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## INTRODUCTION

This paper addresses the issues involved in converting GaAs models for different nonlinear simulators.

There may be slight differences in the way a model is implemented in commercial simulators. These differences can usually be reconciled by consulting the simulator's accompanying documentation, mapping parameters from one simulator to another, recognizing default values of parameters and their effects, and modifying the simulation schematic.

The high frequency output conductance network can be implemented external to the nonlinear model with good results.

Although the same model exists in multiple simulators, each simulator may use slightly different variable names. For example, most GaAs FET models contain a zero bias gate-source junction capacitance. In PSPICE and MDS this capacitance is defined as the variable CGS; in LIBRA and COMPACT it is defined as CGSO. These differences require the user to translate model parameters to conform to the syntax of their specific simulator.

Another example where conversion is necessary is when one simulator implements circuit elements inherent to the nonlinear model, but these elements do not exist in the basic nonlinear model of other simulators. One such instance is with a series RC network shunting the output of the Triquint FET model (TOM) in the Libra simulator. This RC network is integral to the Libra TOM but nonexistent in the MDS and PSPICE simulators. The Libra TOM parameters can be used in PSPICE after some minor conversions.

There are many different GaAs FET models in use today. California Eastern Laboratories (CEL) uses the model that fits the widest range of biases and frequencies possible. In addition, nonlinear models are chosen that are available in most commercial simulators.

## GaAs FET MODELS

Three nonlinear GaAs FET models are the Curtice[2], the Statz-Pucel [3], and the TOM (Triquint's Own Model) [4]. The Curtice model was one of the first high frequency nonlinear GaAs FET models to be implemented in commercial simulators. This model does an excellent job of predicting device behavior for a single bias point. For a wide range of biases however, CEL has found that the Curtice model doesn't fit the measured AC and DC performance simultaneously with the same set of model parameters as accurately as the TOM and Statz models. CEL's modeling philosophy is to fit the widest range of biases and frequencies as possible, therefore, the TOM and Statz models are used for our generic multi-bias model.

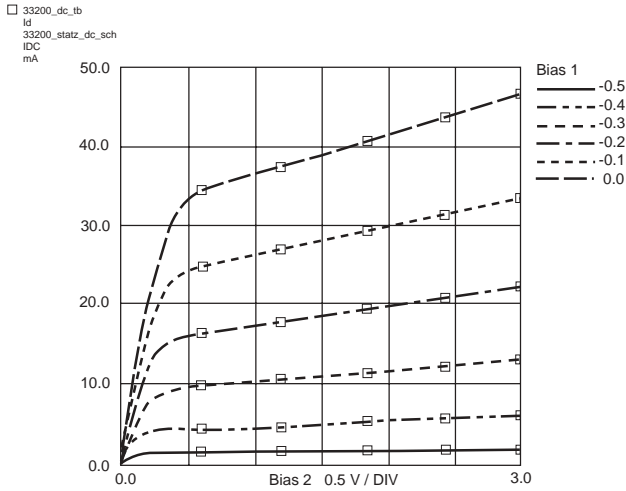
## MODEL DESCRIPTION

There are two major differences between the TOM and Statz models: (1) how the DC drain-source current is modeled, and (2) how the high frequency output conductance is modeled. The DC drain-source current formulation is reviewed. The DC I-V curve equations for the Statz and TOM are implemented the same in the four simulators evaluated and are therefore not reviewed.

Next, the high frequency output conductance model differences are reviewed. Unlike the DC drain-source current, simulator implementations of the high frequency output conductance are different and are therefore included in this review.

### DC drain-source current

The Statz DC I-V curves (Figure 1) result in an almost *constant* drain current with increasing drain voltage at lower gate voltages. The TOM in comparison (Figure 2) exhibits an almost *linear increase* in drain current with increasing drain voltage. At higher drain voltages, the I-V curves in the Statz model exhibit an approximate *linear increase* in drain current with respect to drain voltage, while the TOM drain current becomes approximately *constant* with increasing drain voltage.



**Figure 1. NEC NE33200 Modeled IV curves using the Statz Model.**

Model differences can be quantified by scrutinizing how each author formulates the DC drain-source current. Since the Statz and TOM models are modified versions of the Curtice equation, we will first examine the Curtice model DC I-V curve formulation.

The Curtice model defines the drain current with respect to the drain-source and gate-source voltages as:

$$I_{ds}(V_{gs}, V_{ds}) = \beta(V_{gs} - V_{TO})^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \quad (1)$$

where  $V_{TO}$  is the threshold voltage,  $\beta$ ,  $\lambda$ , and  $\alpha$  are model parameters.

The Statz model modifies Curtice's formulation, equation (1), by replacing the more computationally intensive hyperbolic tangent function with a truncated series representation. More importantly, the Statz model changes  $I_{DS}$  such that the square-law approximation is only in effect for small  $(V_{GS} - V_{TO})$  values. For larger values of  $(V_{GS} - V_{TO})$ ,  $I_{DS}$  becomes almost linear.

The Statz  $I_{ds}$  equation then becomes:

$$I_{ds}(V_{gs}, V_{ds}) = \frac{\beta(V_{gs} - V_{TO})^2 (1 + \lambda V_{ds}) [1 - [1 - (\alpha V_{ds})/3]^3]}{1 + b(V_{gs} - V_{TO})} \quad (2)$$

for  $0 < V_{ds} < 3/\alpha$

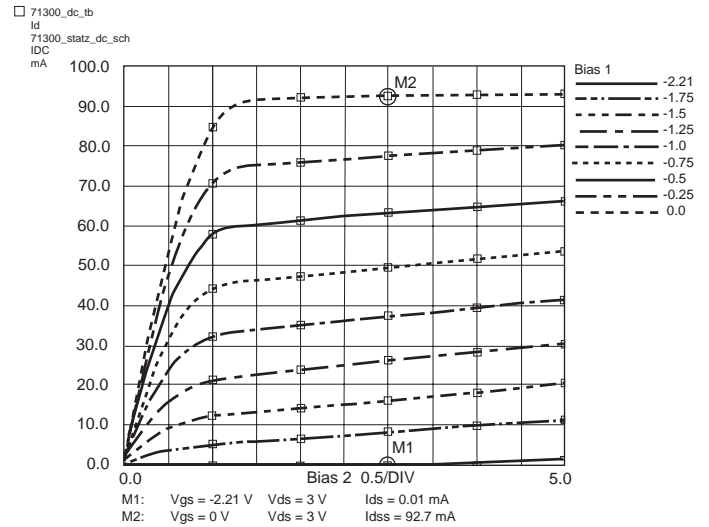
and:

$$I_{ds}(V_{gs}, V_{ds}) = \frac{\beta(V_{gs} - V_{TO})^2 (1 + \lambda V_{ds})}{1 + b(V_{gs} - V_{TO})} \quad (3)$$

for  $V_{ds} \geq 3/\alpha$

where  $[1 - [1 - (\alpha V_{ds})/3]^3]$  is the truncated series representation of  $\tanh(\alpha V_{ds})$  and  $\beta$  is a model parameter.

The Statz model only fits drain conductance for small ranges of drain current. When larger ranges of drain current are simulated, the Statz model tends to predict a conductance that is too large.



**Figure 2. NEC NE71300 Modeled IV Curves using TOM.**

TOM recognized the fact that not all device behavior is well predicted by the square-law assumption, so the exponent in the expression  $(V_{GS} - V_{TO})^2$  is changed from a constant 2 to the variable  $Q$ . For the TOM, the drain-source current becomes:

$$I_{dso}(V_{gs}, V_{ds}) = \beta(V_{gs} - V_{TO})^Q [1 - [1 - (\alpha V_{ds})/3]^3] \quad (4)$$

for  $0 < V_{ds} < 3/\alpha$

and:

$$I_{dso}(V_{gs}, V_{ds}) = \beta(V_{gs} - V_{TO})^Q \quad (5)$$

for  $V_{ds} \geq 3/\alpha$

with:

$$I_{ds}(V_{gs}, V_{ds}) = \frac{I_{dso}}{1 + \delta(I_{dso})(V_{ds})} \quad (6)$$

The TOM also uses a parameter  $\delta$  to model the decreased drain conductance at low gate-source biases. TOM also allows for scaling of  $V_{TO}$ , or pinch-off voltage, to account for drain-source voltage dependence.

How the equations relate to actual device performance is shown above in Figures 1 and 2. These figures show modeled I-V curves derived from the above equations. The models match actual device measurements quite well. Figure 1 is a model of the NEC NE33200 I-V curves using the Statz model. Figure 2 is a model of the NEC NE71300 I-V curves using TOM. Both models are those implemented by the HP-EEsof Series IV Libra simulator.

### High Frequency Output Conductance Model

The high frequency output conductance model for the Statz and TOM models is best illustrated by examining the schematics in Figure 3 and Figure 4. For the Statz model of Figure 3, the drain-source series RC network (CRF and RC) provides a correction to the AC output conductance at a specific bias condition. To implement a full bias range model, the RC network is tuned at a bias in the middle of the bias range. In the TOM, Figure 4, the drain-source RC network ( $C_{bs}$  and  $R_{db}$ ) controls the frequency when the

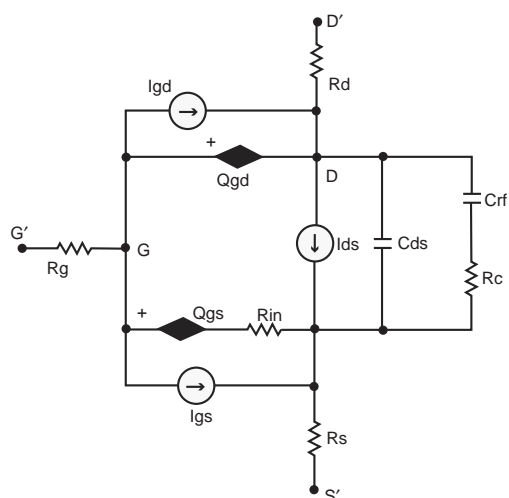


Figure 3. Statz Model Schematic, Libra Series IV.

current source  $I_{db}$  becomes a factor. As with the Statz model, TOM is tuned to the measured data in the middle of the device's bias range.

### Simulator Implementation

The ability to specify the high frequency output conductance is not programmed in all simulator models. To determine if the Statz model or TOM you are using in your simulator has this compensation built in, inspect the nonlinear model simulator documentation.

If the compensation is not programmed into the simulator model, you can implement the output conductance by adding the RC network as an external resistor and capacitor as shown in Figure 6. The components RDB and CBS in Figure 6 represent this external compensation. PSPICE and MDS are two of the nonlinear simulators that do not have the output conductance programmed into their TOM.

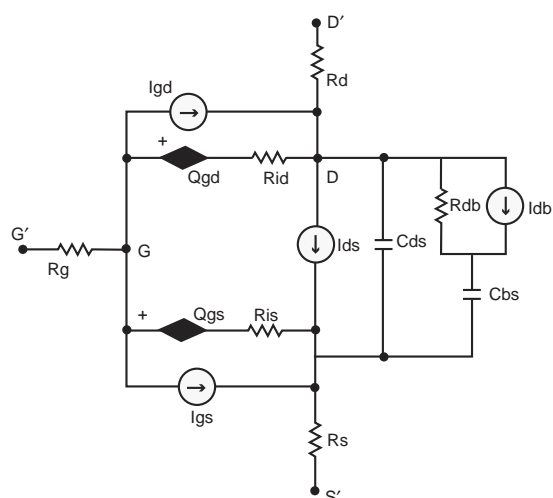


Figure 4. TOM Schematic, Libra Series IV.

### OUTPUT CONDUCTANCE CONVERSION

The following example shows how to convert *Libra Series IV* TOM into *PSPICE* TOM. This example uses the NE71300 L to K band low noise N-Channel GaAs MESFET device. This is a 280 $\mu$ m gate width by 0.3 $\mu$ m gate length device with a typical noise figure of 0.6 dB and an associated gain of 14 dB at 4 GHz. The maximum drain to source voltage is 5.0 V and the maximum drain current is 10 mA typical and 30 mA maximum.

Figure 4 shows the schematic for the basic TOM. Note the presence of Rdb and Cbs from the drain to the source. Figure 5 shows the LIBRA Series IV schematic for the TOM. Note that while there is no external Rdb and Cbs in the schematic, the model variables RDB and CBS are present in the listing of variables in Figure 5. This shows

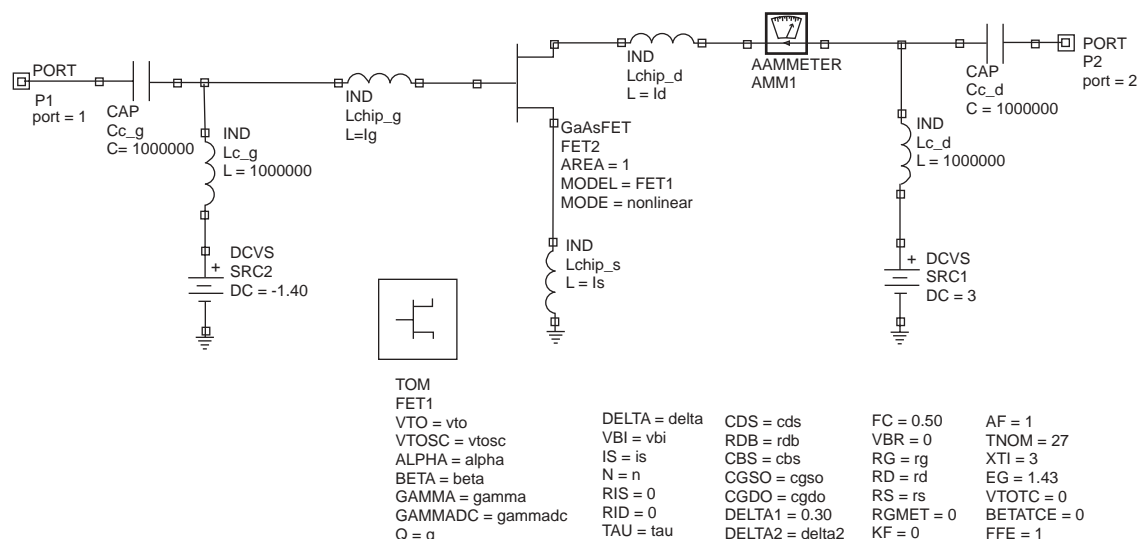
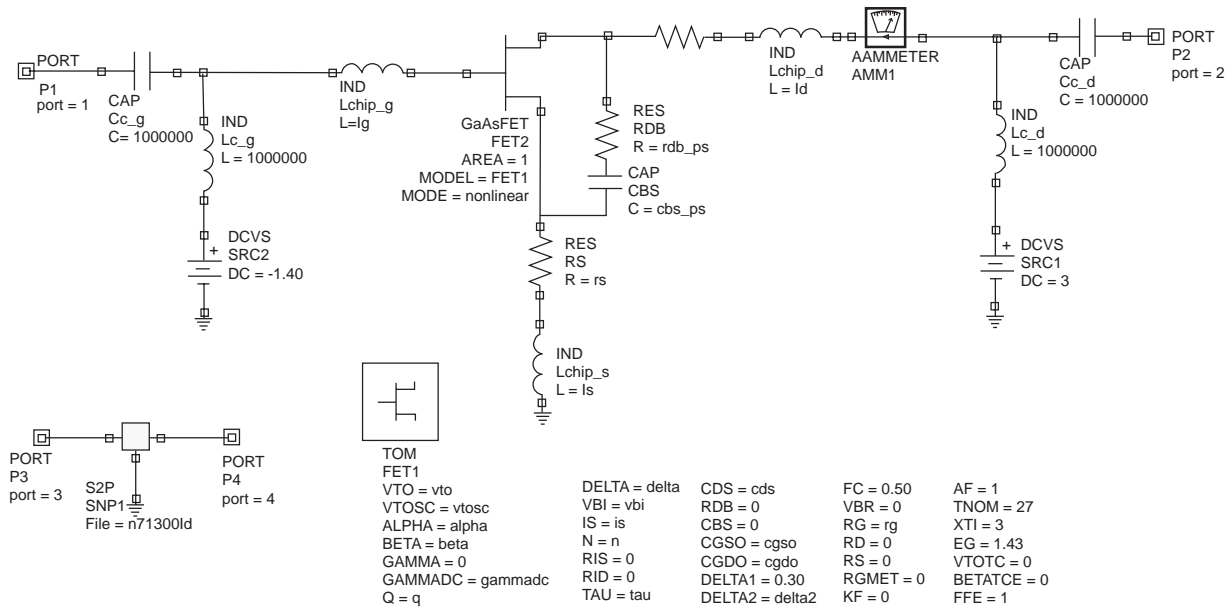


Figure 5. Libra Series IV Schematic with Internal RC Network.



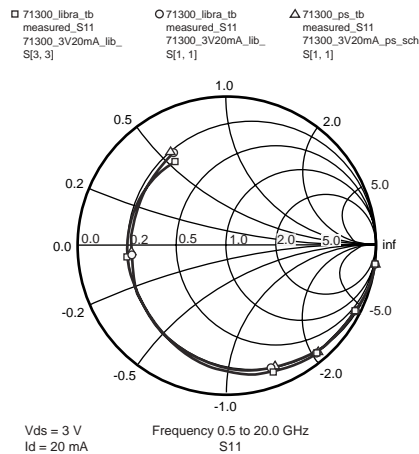
**Figure 6. Libra Series IV Schematic with External Network.**

conclusively that the output conductance is programmed into Libra's TOM.

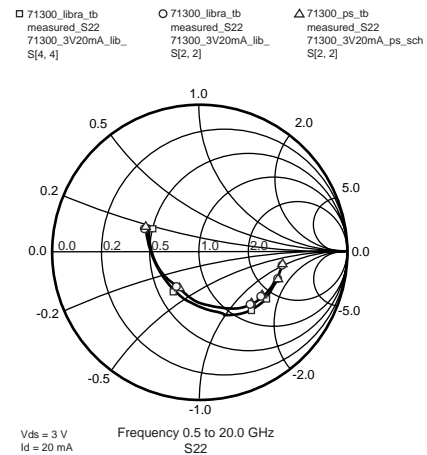
If using a simulator that doesn't have the compensation programmed into the model, add RDB and CBS as external circuit components, as shown in Figure 6. Figure 6 uses the Libra simulator, therefore, RDB, CBS, RD and RS are set to 0 in the programmed list of model variables because these parameters are added externally as components.

### Comparison Of Internal Compensation To External Compensation

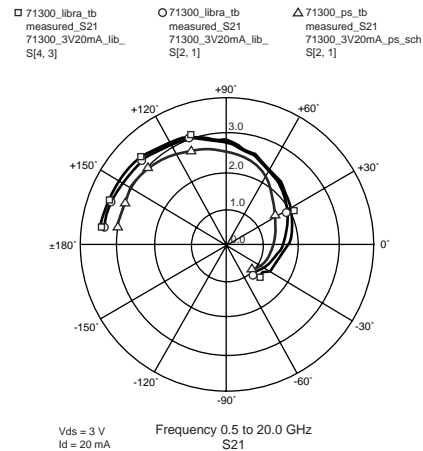
Figures 7 through 10 show a comparison of implementing the high frequency output conductance control externally. In the following figures,  $\square$  is the CEL measured data,  $\circ$  is the results using the schematic with the internal compensation (Figure 5) and  $\triangle$  is the results using the schematic with external compensation (Figure 6).



**Figure 7. S11 Compensation Comparison.**



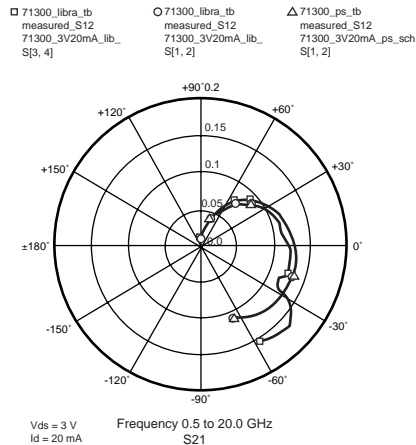
**Figure 8. S22 Compensation Comparison.**



**Figure 9. S21 Compensation Comparison.**

LIBRA PARAMETERS	DEFINITION	PSPICE PARAMETER[6]
BETA	transconductance parameter or coefficient	BETA
VTO	threshold voltage (called the pinch-off voltage in PSpice)	VTO
ALPHA	current saturation parameter (called the saturation voltage parameter in PSpice)	ALPHA
LAMBDA	output conductance parameter (called channel-length modulation in PSpice)	LAMBDA
THETA	parameter which controls $I_{ds}$ - $V_{gs}$ characteristic transition from quadratic to linear behavior (called the doping tail extending parameter in PSpice)	B
TAU	transit time under gate (called conduction current delay time in PSpice)	TAU
VBR	gate-drain junction reverse bias breakdown voltage	not implemented
IS	gate junction reverse saturation current (called the gate p-n saturation current in PSpice)	IS
N	gate junction reverse saturation current (called the p-n emission coefficient in PSpice)	N
VBI	built-in gate potential (called the gate p-n potential in PSpice)	VBI
FC	coefficient for forward bias depletion capacitance	FC
RC	used with CRF to model frequency dependent output conductance	not implemented
CRF	used with RC to model frequency dependent output conductance	not implemented
RD	drain ohmic resistance	RD
RG	gate ohmic resistance	RG
RS	source ohmic resistance	RS
RIN	channel resistance	not implemented
CGSO	zero bias gate-source junction capacitance	CGS
CGDO	zero bias gate-drain junction capacitance	CGD
DELTA1	capacitance saturation transition voltage parameter	not implemented
DELTA2	capacitance threshold transition voltage parameter	VDELTA
CDS	drain-source capacitance	CDS
CGS	gate-source capacitance	not implemented
CGD	gate-drain capacitance	not implemented
KF	flicker noise coefficient	KF
AF	flicker noise exponent	AF
XTI	temperature exponent for saturation current	XTI
EG	energy gap or band gap voltage	EG
VTOTC	VTO temperature coefficient	VTOTC
BETATCE	BETA exponential temperature coefficient	BETATCE
FFE	flicker noise frequency exponent	not implemented
not implemented	gate p-n grading coefficient	M
not implemented	capacitance limiting voltage	VMAX

**Table 1: Statz Model Parameters.**



**Figure 10. S12 Compensation Comparison.**

It can be seen by examining Figure 9 that the gain resulting from the model in Figure 6 is lower than the measured gain and the modeled gain from the schematic in Figure 5. This is due partly to the fact that some simulators do not

implement the AC gamma parameter (GAMMAAC). In addition, when GAMMAAC is set to its default of zero, the value for Rdb (called rdb\_ps in Figure 6) must also be adjusted to match S22. In the above example, rdb = 2000 ohms and rdb\_ps = 300 ohms. Table 1 and Table 2 compare the parameters as implemented in HP-EEsof Series IV Libra simulator[5] and MicroSim PSpice[6] for the Statz model (Table 1) and for TOM (Table 2). Figures 7, 8 and 10 indicate that, properly implemented, the external compensation network provides almost identical results for S11, S22 and S12.

## CONCLUSIONS

1. The Curtice model is useful when extracting a model at a single bias point.
2. The Statz model is more accurate when the  $I_{ds}$  for a device behaves quadratically (square-law approximation) for small values of  $(V_{gs} - V_{TO})$  and linearly for large values of  $(V_{gs} - V_{TO})$ .
3. TOM is more accurate when the square-law approximation does not predict device performance well and when the device drain conductance varies with gate-source bias.

LIBRA PARAMETERS	DEFINITION	PSPICE PARAMETER[6]
VTO	threshold voltage (called the pinch-off voltage in PSpice)	VTO
VTOSC	scaleable portion of the threshold voltage	not implemented
ALPHA	current saturation parameter (called the saturation voltage parameter in PSpice)	ALPHA
BETA	transconductance parameter or coefficient	BETA
GAMMA	AC drain pull coefficient	not implemented
GAMMADC	DC drain pull coefficient (called the static feedback parameter in PSpice)	GAMMA
Q	power law exponent	Q
DELTA	output feedback coefficient	DELTA
VBI	built-in gate potential (called the gate p-n potential in PSpice)	VBI
IS	gate junction reverse saturation current (called the gate p-n saturation current in PSpice)	IS
N	gate junction ideality factor (called the gate p-n emission coefficient in PSpice)	N
RIS	source end channel resistance	not implemented
RID	drain end channel resistance	not implemented
TAU	transit time under gate (called conduction current delay time in PSpice)	TAU
CDS	drain-source capacitance	CDS
RDB	dispersion source output impedance	not implemented
CBS	drain-source capacitance	not implemented
CGSO	zero bias gate-source junction capacitance	CGS
CGDO	zero bias gate-drain junction capacitance	CGD
DELTA1	capacitance saturation transition voltage parameter	not implemented
DELTA2	capacitance threshold transition voltage parameter	VDELTA
FC	coefficient for forward bias depletion capacitance	FC
VBR	gate-drain junction reverse bias breakdown voltage	not implemented
RD	drain ohmic resistance	RD
RG	gate ohmic resistance	RG
RS	source ohmic resistance	RS
RGMET	gate metal resistance	not implemented
KF	flicker noise coefficient	KF
AF	flicker noise exponent	AF
XTI	temperature exponent for saturation current	XTI
EG	energy gap or band gap voltage	EG
VTOTC	VTO temperature coefficient	VTOTC
BETATCE	BETA exponential temperature coefficient	BETATCE
FFE	flicker noise frequency exponent	not implemented
not implemented	gate p-n grading coefficient	M
not implemented	capacitance limiting voltage	VMAX

Table 2. TOM Parameters.

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