Low Power SC CMFB Folded Cascode OTA Optimization

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***Abstract*- This paper describes a design of a switched capacitor common mode feedback (SC CMFB) folded cascode operational transconductance amplifier for low power and high-speed sigma-delta modulators. An algorithmic driven methodology is developed ending to the optimal transistor geometries. Using a 0.35µm CMOS process, the OTA circuit has been designed to achieve 82.94dB DC gain, 526MHz unity-gain frequency, 560V/µs slew rate with 1.8V power supply voltage and a power consumption of only 1.19mW. The simulated OTA circuit has been applied in a SC integrator to illustrate the versatility of the circuit.**

I. INTRODUCTION

The complexity of integrated electronic circuits being designed nowadays is continuously increasing as advances in process technology make it possible to create mixed-signal integrated SoC designs. Reducing the supply voltage puts more constraints on the design of the amplifier. Since reduced supply voltage forces the power consumption to increase [1]. For the circuit implementation, SC circuits are still good candidates even under very low-voltage. Operational amplifier is an integral part of many analog and mixed signal systems. Its topology plays a critical role in low-voltage, low-power sc design. The design of op amps continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. In this work, our interest is focused on low power switched capacitor CMFB folded cascode OTA optimization working for frequencies that lead to a base band circuit design for wide band applications.

The outline of the paper is as follows. In Section II, we present an algorithmic driven methodology for folded cascode OTA optimization. In Section III, we apply the OTA circuit in a SC integrator. Finally, section IV details the conclusion drawn from this work and presents the scope for future research.

II. FOLDED CASCODE OTA OPTIMIZATION

Circuit sizing is an optimization process by its nature and one can find quite extensive literature in this area. Various optimization tools were developed. All the performances of an OTA circuit are closely related to the transistors scaling. The question is then how to scale these transistors to get the best performances. The folded cascode OTA can be designed using g_m/I_D methodology introduced by Flandre and Silveira [2]. Nevertheless, we can optimize only the characteristics containing g_m/I_D parameter within expression's models [3]. Thus, a new design approach is presented in this paper. It describes an optimization tool based on heuristic algorithms. We fixed our choice in this step on the technology 0.35 µm CMOS of AMS. We used in the folded cascode OTA optimization the following series of criteria:

- The static gain A_v is maximized.
- The transition frequency f_t is maximized.
- The common mode rejection ratio (CMRR) is maximized.
- The positive power-supply rejection ratio (PSRR) is maximized.
- The input referred noise ($V_{T,in}^2$) is minimized.
- The silicon area of the whole OTA circuit is minimized.

The objective function to maximize can thus be formulated as follows:

$$F_o = \theta_1 A_v + \theta_2 f_t + \theta_3 CMRR + \alpha \quad (1)$$

$$\text{Where } \alpha = \theta_4 PSRR + \frac{\theta_5}{V_{T,in}^2} + \frac{\theta_6}{\sum W_i L_i} \quad (2)$$

Where $\theta_1,\ldots, \theta_6$ are positive coefficients used for normalization.

The first step in the optimization is the expression of the different criteria by a technology dependent model. For accurate modeling, a small signal analysis of the folded cascode OTA is carried out to explicit the different characteristics intended optimized. From folded cascode OTA structure presented in Fig. 1, the open-loop voltage gain and gain bandwidth are given by (1) and (2) below:

$$A_V = g_{m9}\left(g_{m5} r_{05} r_{07}\right) // \left(g_{m3} r_{03}\left(r_{01} // r_{09}\right)\right) \quad (3)$$

$$GBW = \frac{g_{m9}}{C_L} \quad (4)$$

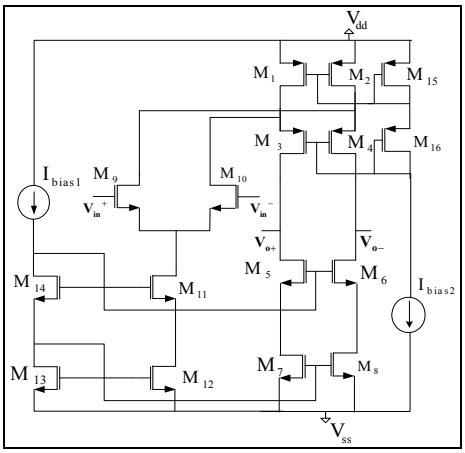

Figure 1. Folded cascode OTA topology

Where, g_{m3}, g_{m5} and g_{m9} are respectively the transconductances of transistors M_3, M_5 and M_9. r_{01}, r_{03}, r_{05}, r_{07} and r_{09} are respectively the drain-source resistances of transistors M_1, M_3, M_5, M_7 and M_9. C_L is the capacitance at the output node.

The positive power-supply rejection ratio (PSRR) is expressed as:

$$PSRR^{+} = \frac{A_V\left(R_{01}+R_{02}+r_{03}\right)\left(R_{01}+R_{02}+r_{03}-R_{01}r_{03}g_{m3}\right)}{R_{02}\left(R_{01}+R_{02}+r_{03}-\beta_1+\beta_2\right)} \quad (5)$$

$$\beta_1 = R_{01}r_{03}g_{m3} \quad (6)$$

$$\beta_2 = r_{03}g_{m3}\left(R_{02}+r_{03}\right) \quad (7)$$

$$R_{01} = r_{01}//r_{09} \quad (8)$$

$$R_{02} = r_{05}r_{07}g_{m5} \quad (9)$$

The common mode rejection ratio (CMRR) can be approximated as:

$$CMRR = 20\mathrm{Log}_{10}\left(\frac{2g_{m9}R_Lr_{011}}{r_{03}+\left(r_{01}//r_{09}\right)}\right) \quad (10)$$

The input referred thermal noise voltage of the folded cascode OTA can be expressed as [4]:

$$\overline{V_{in,th}^{\,2}} = 4kT\left(2\frac{2}{3g_{m9,10}}+2\frac{2g_{m1,2}}{3g_{m9,10}^{\,2}}+2\frac{2g_{m7,8}}{3g_{m9,10}^{\,2}}\right) \quad (11)$$

Where k is the Boltzmann's constant and T is the temperature.

The input referred flicker noise voltage of the folded cascode OTA can be written as:

$$\overline{V_{in,1/f}^{\,2}} = 2\frac{KF}{C_{ox}\left(WL\right)_{1,2}f}+2\frac{KF}{C_{ox}\left(WL\right)_{7,8}f}\frac{g_{m1,2}^{\,2}}{g_{m9,10}^{\,2}}+\Psi \quad (12)$$

$$\text{Where } \Psi = 2\frac{KF}{C_{ox}\left(WL\right)_{7,8}f}\frac{g_{m7,8}^{\,2}}{g_{m9,10}^{\,2}} \quad (13)$$

Where KF is the flicker noise coefficient, f is the frequency; C_{ox} is a constant for a given process. W and L are the sizes of transistors and g_m defines the transconductance of transistors differential pair.

We apply then in the optimization process, a Heuristic programmed with C++ software, which is an algorithm driven methodology [5]. This approach was followed in many analog circuit designs and gave promising results [6]. It starts with an initialization of the parameters vectors which include the sizing of the different transistors interfering in the above expressions (Fig.2). A random choice of the variables vector is then done followed by a verification of the preliminary conditions. These conditions are imposed to ensure that the different transistors are in the inversion mode of operations. If these conditions are fulfilled, the vector parameters are candidates for the following steps, otherwise we do another choice. Next, we compute the objective function. If it is decreasing, when compared to the previous iteration, the parameter vector is saved; otherwise, we keep this vector unchanged. After a series of trials with the randomly chosen parameters, the parameter vector corresponding to the minimal objective function is obtained. When the number of trials is important, this solution corresponds to an optimal solution. This method does not suffer from any divergence problems seen when applying gradient-based methods, but its efficiency is closely related to the number of iterations. Indeed, with a high number of trials, we manage to explore in a simple random way all the proposed tuning range of the different parameters and good performances are ensured.

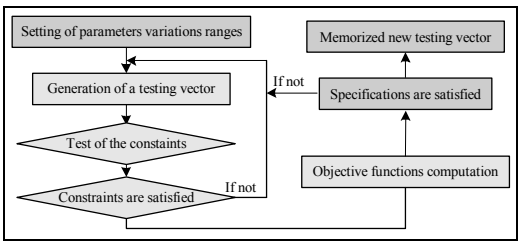

Figure 2. Optimization algorithm procedure

Simulation conditions are the following: the supply voltage is 1.8V, the bias current Ibias1.is 60µA and the capacitor load is 0.1pF. We notice that the optimization process can be done in the same way for other simulation conditions. Table 1 shows the optimal device scaling that we get after applying the optimization approach.

TABLE I. OPTIMAL DEVICE SIZING

Device name	Aspect ratio (µm)
$W_{1, 2, 15, 16}$	34.85/1
$W_{3, 4}$	23/1
$W_{5, 6, 7, 8, 11, 12, 13, 14}$	47.15/1
$W_{9, 10}$	49.9/1

A. Simulation results

The designed folded cascode OTA has a gain of 82.94dB, a large unity-gain frequency of 533.3MHz with phase margin of 41.86 degrees and a slew rate of 545V/µs (Fig.3). The simulated specifications are compared to theoretical design in table II. It is seen that the optimization is almost satisfactory.

TABLE II. SPECIFICATIONS COMPARISON

Specifications	Theoritical values	Measured values
DC Gain (dB)	82.89	82.94
GBW (MHz)	533.55	533.3
Slew Rate (V/µs)	600	545
CMRR (dB)	93.56	94.2
PSRR p, n (dB)	73.23	77.68

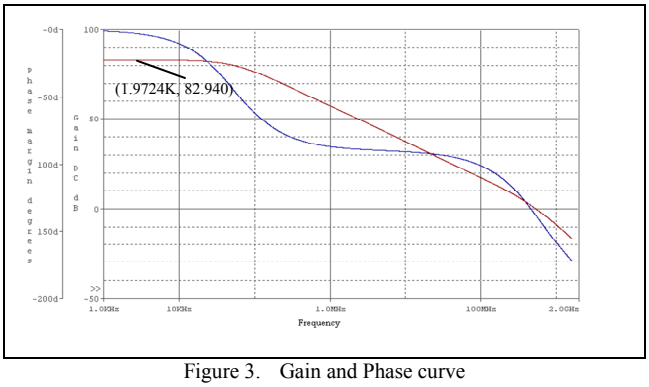

Figure 3. Gain and Phase curve

All the folded cascode OTA performances are summarized in table III.

TABLE III. PERFORMANCES FOLDED CASCODE OTA

Specifications	Values
DC Gain (dB)	82.94
GBW (MHz)	533.3
Phase margin (degrees)	41.86
CMRR (dB)	94.2
PSRR p, n (dB)	77.68
Slew Rate (V/µs)	545
Settling time (ns)	23
Output swing (V)	[-1.13; 1.59]
Input swing (V)	[-1.22; 1.75]
Supply voltage (V)	±1.8
I_1 current (µA)	60
I_2 current (µA)	90
Transconductance (uS)	330.41
Input referred noise voltage (nV)	17.56
Power consumption (mW)	1.19

B. Switched capacitor CMFB

The CMFB is necessary when designing a fully differential operational amplifier. It must be considered in parallel with the amplifier design. SC CMFB circuit is adopted to stabilize the common mode level at its outputs.

In the CMFB block in Fig. 4, $V_{cm\text{-}ref}$ represents the desired output common mode voltage; V_{bias} is the desired biasing voltage for the OTA current sources M_1 and M_2 in order to get desired common mode level at the OTA output.

During Φ_1, C_2 is pre-charged to the difference between the biasing voltages $V_{cm\text{-}ref}$ and V_{bias}; during Φ_2, the charges are redistributed between C_1 and C_2. Therefore, the convergence of the output common mode level can be derived as:

$$\left[V_{o,cm}(n+1) - V_{cmfb}(n+1)\right] = \left[1 - \left(\frac{C_1}{C_1 + C_2}\right)^{n+1}\right]\left(V_{cm,ref} - V_{bias}\right) \quad (14)$$

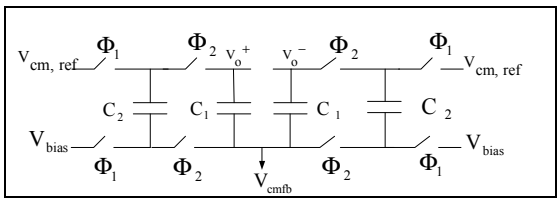

Figure 4. CMFB circuit

Clearly, the output common mode level would eventually converge to the desired common-mode voltage $V_{cm\text{-}ref}$.

After optimizing the folded cascode OTA, the CMFB circuit should be also well designed, so that the OTA performance of the differential mode would not be degraded [7]. We simulate the folded cascode OTA with CMFB circuit, we observe that the gain bandwidth product decreases from 533.3Mhz to 526Mhz, this can be explained by that the SC CMFB inject nonlinear clock feedthrough noise into the OTA output nodes and increase the load capacitance that needs to be driven by the OTA circuit. The other performances are maintained.

For a fully differential operational amplifier, the common mode is largely depending on the bias voltage of the current source. This means that for a process variation, the gain is largely depending on the accuracy of these bias voltages. The additional CMFB circuit that set the common voltage to a desire value can largely decrease the dependence of the gain towards the different bias voltage. The Fig. 5 shows the DC gain dependence on the input common mode with a CMFB.

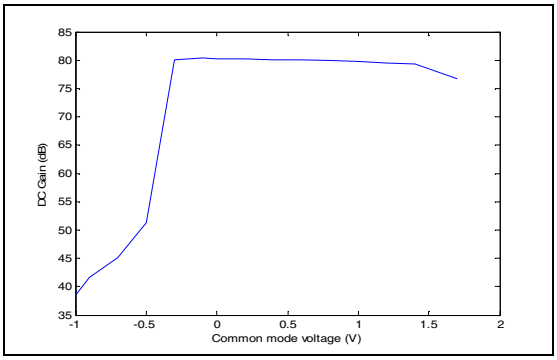

Figure 5. DC Gain with CMFB circuit

The performances of the SC CMFB OTA circuit have been compared to recent OTA circuit design given in [8, 9] (table IV).

When discussing the comparison, this work achieves the lowest power consumption. Moreover, the OTA circuit is fast, it has an important DC gain and a large bandwidth that are required to fulfill high speed application. Therefore, the phase margin and the PSRR are lower than given by Ling Zhang.

TABLE IV. PERFORMANCES COMPARISON

Performances	Ling Zhang [2005]	This work
OTA architecture	Folded cascode	Folded cascode
Technology (µm)	0.18	0.35
Gain DC (dB)	68.5	82.94
GBW (MHz)	435	526
Phase margin (degrees)	76	42.3
Supply voltage (V)	1.8	1.8
Biais current (mA)	1.5	0.06
CMRR (dB)	101.5	94.2
PSRR (dB)	102	77.68
Slew Rate (V/µS)	220	560
Input referred noise voltage (nV)	14.55	17.56
Power consumption (mW)	7.22	1.19

III. SC INTEGRATOR APPLICATION

To underline the suitability of the proposed simulated OTA, it was applied in a first-order SC integrator (Fig. 6). The integrator is controlled by two-phases nonoverlapping clocks Φ_1 and Φ_2, where the input signal is sampled on Φ_1 and integrated on Φ_2. If the clocks phases are complementary, and the transistor is in the ohmic mode, then the equivalent on-resistance of the switch is given by:

$$R_{on} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{dd} - V_{in} - V_{tn})} // \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{in} - V_{tp})} \qquad (15)$$

In order to make the switch on-resistance independent of input voltage, we take the complementarity between the NMOS and PMOS transistors into account.

More critical about the switch on-resistance is that it results in settling error [10, 11]. The design method adopted during this study consists of improving the settling precision by fixing the length of the two transistors at the minimal value of technology (0.35µm). Then the parameter W is computed to satisfy the settling time requirement. The R_{on} value chosen is about 200Ω value to have the fastest settling of V_{in}. The design of capacitors has to take care of design rules of AMS so that the capacitor mismatch is smaller than 0.5%. The values C_s=0.5p and C_f=1p satisfy this requirement.

We simulate the SC integrator of Fig. 6 for a 100 Mhz sampling frequency. Fig. 7 shows a transient simulation where the integrator response for a constant input signal can be seen in this graph. Fig. 8 shows the results of a transient simulation using a 10 Mhz differential input signal.

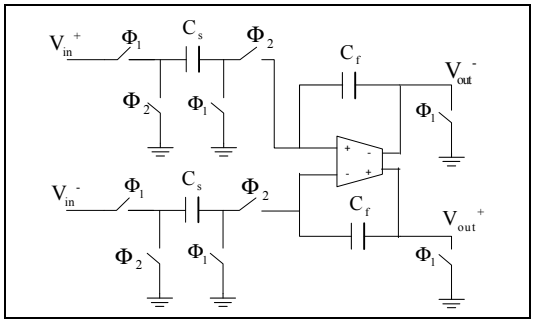

Figure 6. SC integrator

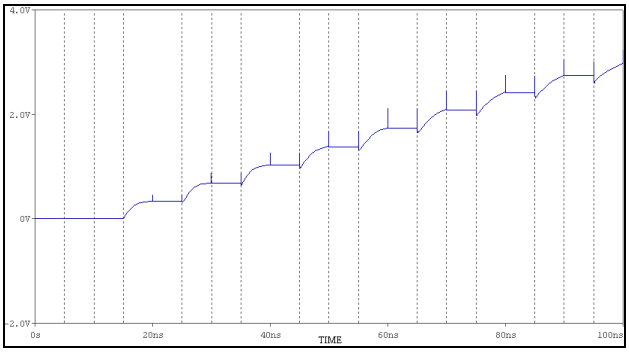

Figure 7. Differential output voltage

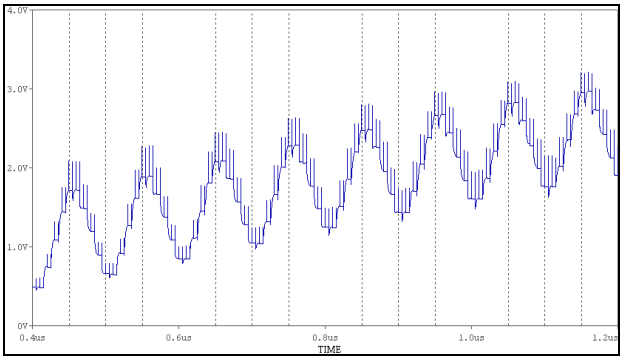

Figure 8. Differential output voltage

IV. CONCLUSIONS AND FUTURE DIRECTIONS

A SC CMFB fully differential folded cascode OTA has been optimized using a heuristic algorithm efficient tool. The key advantage of the circuit is that high open-loop DC gain, fast settling, and large bandwidth are simultaneously under low-power operation. As an example of illustration, we apply the simulated OTA circuit in SC integrator that function for a given 100 Mhz sampling frequency. The proposed OTA is thus suitable for low-voltage high-speed switched-capacitor applications.

Some future directions for research involve the use of folded cascode OTA for low consumption and wide band applications in sigma delta modulators.

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