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Section 3.7.1.5. The high on-state, effective gate–source voltage, $V_{EFF} = V_{GS} - V_T = V_{DD} - V_T$, combined with the usual minimum channel length used for digital devices, results in significant velocity saturation reduction of on-state current, especially for nMOS devices that have lower values of critical, horizontal electric field, E_{CRIT}, compared to pMOS devices. The reduction of on-state current unfavorably increases the ratio of off- to on-state current. Increased off-state current results from width increases required to maintain a given level of on-state drive current when velocity saturation is significant.

Equations 3.190–3.192 show that the off-state current and the off- to on-state current ratio increase significantly as V_T decreases because $-V_T$ appears in exponential terms. The off-state current and off- to on-state current ratio increase for a worst case combination of decreasing process V_T in smaller-geometry processes, decreasing V_T for the minimum channel length device, decreasing V_T for non-zero V_{DS}, and decreasing V_T with increasing temperature. Process V_T decreases with decreasing process V_{DD} in smaller-geometry processes to maintain adequate on-state current. V_T decreases for the usual minimum channel length device because of V_T roll-off. This is caused by charge sharing where the nearby source and drain depletion regions cut off some of the normal, substrate, depletion-region control below the channel, lowering V_T [15, pp. 259–263]. V_T decreases further for non-zero V_{DS}, especially for the minimum channel length device, due to charge sharing or DIBL described earlier in Section 3.8.4.2. As mentioned in Section 3.8.4.2, higher retrograde doping below the channel surface and higher halo doping near the source and drain reduce the depletion regions under the channel and near the source and drain, reducing charge-sharing and DIBL effects. Finally, V_T decreases with temperature as described earlier in Section 3.5.4 and shown in Figure 3.6.

The off-state current given by Equations 3.190 and 3.191 increases by nearly a factor of 50 for an operating die temperature increase of 100 °C from 300 to 400 K (27 to 127 °C). This assumes a 1 mV/C decrease in V_T from 250 mV at 300 K, a 0.086 mV/C increase in U_T from 25.9 mV at 300 K, and $n = 1.4$ for nMOS devices in the process mentioned earlier. The current increase is dominated by the exponential term in the equations as the preceding technology current term, $I_0 = 2n_0\mu_0 C'_{OX} U_T^2$, increases by only about 15 % over the 100 °C range as seen in Figure 3.5 for a different process I_0 having a same mobility temperature exponent of $BEX = -1.5$. Since temperature dependency in the off-state current dominates temperature dependency in the on-state current, the off- to on-state current ratio experiences a similar, significant increase with temperature as the off-state current. Low process V_T combined with the V_T decrease resulting from elevated die temperature significantly increases the off-state current and off- to on-state current ratio in large digital circuits.

Since off-state, subthreshold drain leakage current usually exceeds the current associated with dynamic switching in digital circuits, considerable research is underway to manage the subthreshold leakage current [247]. Techniques to manage the leakage current include the use of stacked transistors where the presence of reverse bias V_{GS} and non-zero V_{SB} for at least one transistor significantly reduces the subthreshold current [247]. The current is reduced through the negative value of V_{GS} and the increase in V_T associated with non-zero V_{SB}. Additionally, multiple V_T, dynamic V_T using switched V_{SB} levels, V_{DD} scaling, and dynamic V_{DD} techniques can be used to reduce subthreshold leakage current [247]. Although this discussion has considered subthreshold drain leakage current, the drain–body leakage current, due to GIDL and band-to-band tunneling (Section 3.12.3), and gate leakage current (Section 3.12.1.1) can be signicant contributors to digital circuit leakage current in smaller-geometry processes [247, 251].

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