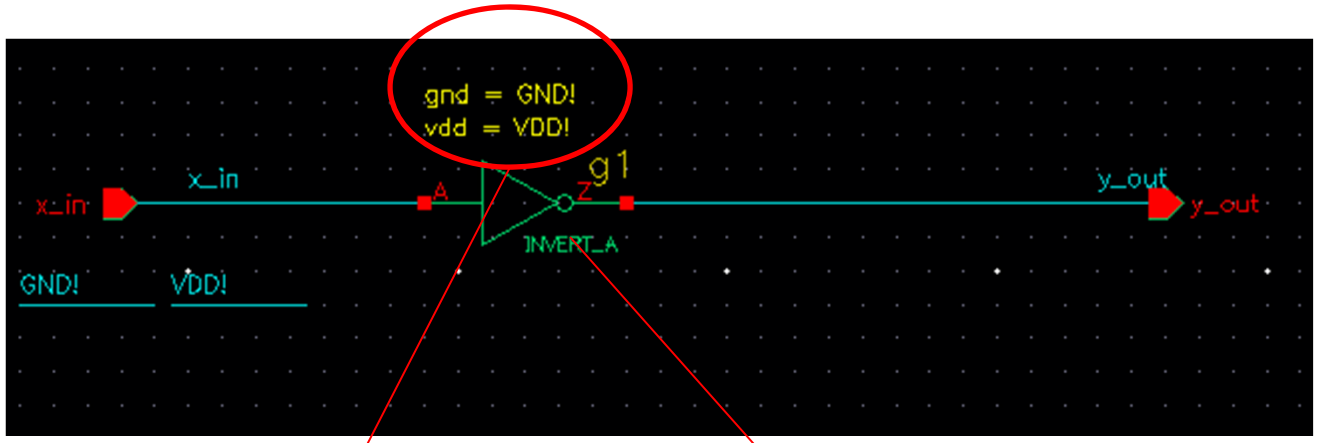
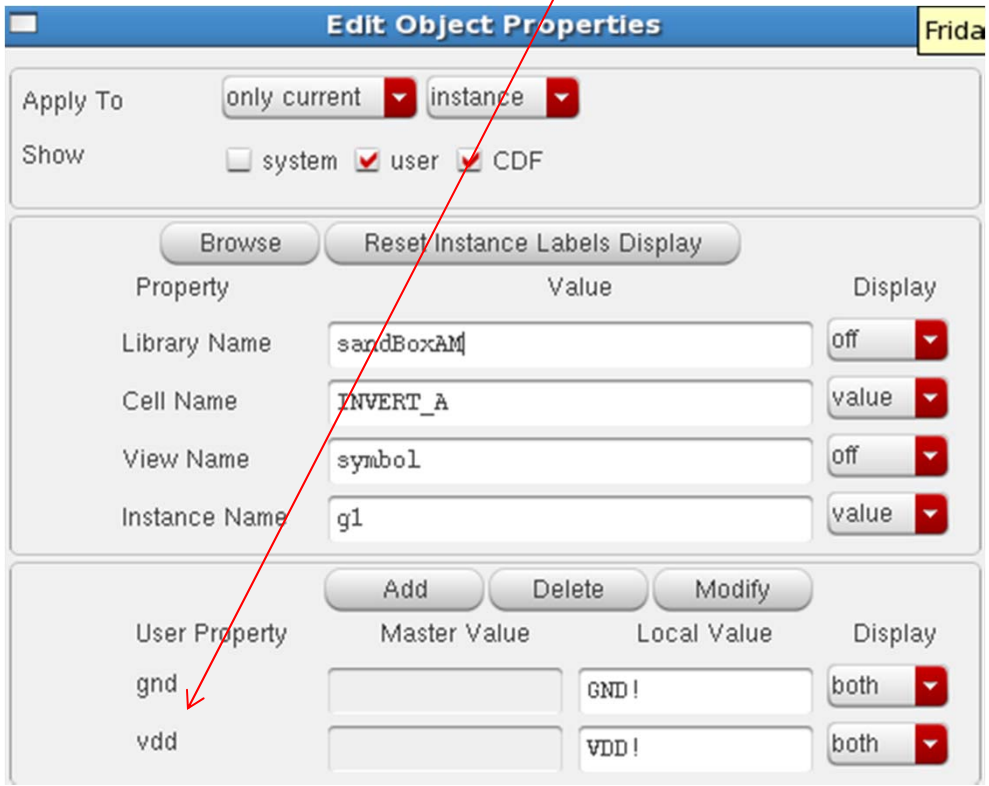
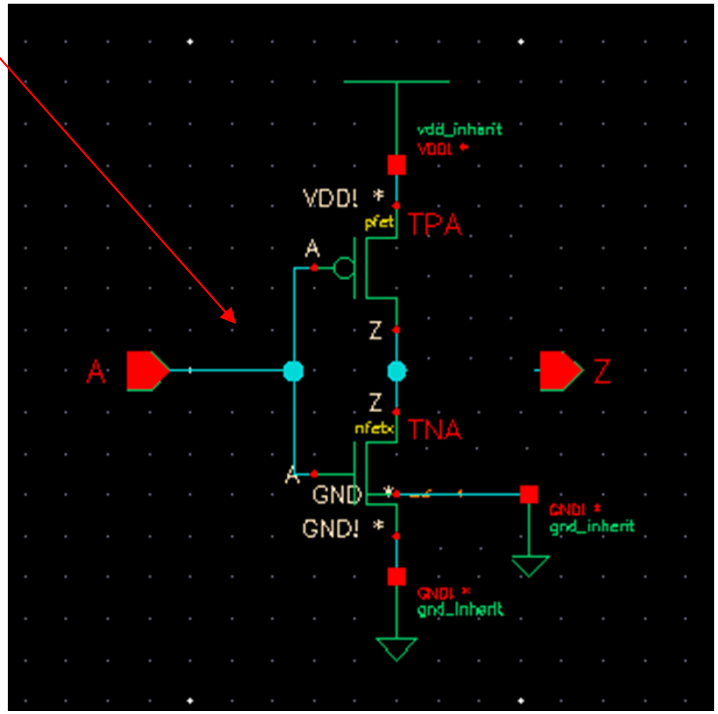
Top level schematic: inherit







VDD! and GND! Inherited from the top level schematic.

Schematic Netlist

```
*|CDS    : Assura VNL File
*|Version: 1.0
*|Date   : Fri Jul 25 22:40:37 2014

c nfet Generic  D B     G B     S B     B B   ;;
* 4 pins
* 4 nets
* 0 instances
e

c pfet Generic  D B     G B     S B     B B   ;;
* 4 pins
* 4 nets
* 0 instances
e

c "INVERT_A schematic sandBoxAM" Cell  A I        Z O        gnd! G
  vdd! P   ;;
* 4 pins
* 4 nets
* 2 instances
i TPA pfet Z    A     vdd! vdd!;  gcon 1     idg 0      l 1.8e-07  m 1
  mSwitch 0  nf 1       par "1"     psp 0      rf 0       wt 4e-07 ;
i TNA nfet Z    A     gnd! gnd!;  bentgate 0  gcon 1      idg 0       l 1.8e-07
  m 1         mSwitch 0   nf 1        par "1"     psp 0       rf 0
  wt 4e-07  ;
e

c "inherit schematic sandBoxAM" Cell  y_out O     x_in I      GND! G(g)
  VDD! P(g) ;;
* 4 pins
* 4 nets
* 1 instances
i g1 "INVERT_A schematic sandBoxAM" x_in  y_out GND!  VDD! ;;
e
```

VDD! and GND! from inherit (the top level cell) are passed to INVERT_A!!

Layout netlist

```
c "INVERT_A layout sandBoxAM" Cell  VDD! P     GND! G     A NONE     Z NONE
  avC5 N(f);;
* 5 pins
* 6 nets
* 2 instances
i avD20_1 nfet A    GND! Z     avC5;  ad 2.48e-13
  as 6.88e-13                       blockParasiticsBetween "PC sub"
  gcon 1                            gns 0
  l 1.8e-07                         m 1
  mSwitch 0                         nf 1
  nrd 0.764706                      nrs 0.764706
  par 1                             pd 2.16e-06
  ps 4.24e-06                       psp 0
  rf 0                              stis 2
  w 4e-07                           wt 4e-07                        ;
i avD41_1 pfet A    VDD! Z     avC6;  ad 2.48e-13
  as 6.88e-13                       blockParasiticsBetween "PC sub"
  gcon 1                            gns 0
  l 1.8e-07                         m 1
  mSwitch 0                         nf 1
  nrd 0.764706                      nrs 0.764706
  par 1                             pd 2.16e-06
  ps 4.24e-06                       psp 0
  rf 0                              w 4e-07
  wt 4e-07                        ;
e

c "inherit layout sandBoxAM" Cell  VDD! P      GND! G      x_in NONE
  y_out NONE;;
* 4 pins
* 5 nets
* 9 instances
i I__0 "INVERT_A layout sandBoxAM" VDD!  GND!  x_in  y_out avC5 ;;
i I__13 "inherit_VIA0 layout sandBoxAM";;
i I__14 "inherit_VIA0 layout sandBoxAM";;
i I__5 "inherit_VIA0 layout sandBoxAM";;
i I__6 "inherit_VIA0 layout sandBoxAM";;
```

VDD! and GND! from the top level layout (inherit) are not passed to the lower level layout. (INVERT_A).