

# 2

## Linear Power Amplifier Design

This chapter shows how some of the concepts in Chapter 1 can be developed into a simple but complete strategy for the design of linear RF PAs. Essentially, a linear PA can be designed using the same basic matching principles used for small signal designs, but with a power-matched output that will not appear to be conjugately matched. In some respects, PA design becomes an analogous process to low noise amplifier (LNA) design, in which to achieve the best possible noise performance from the device being used, its input needs to be presented with a reflection coefficient that will differ significantly from the conjugate match of the input impedance. In the linear PA case, the device has to be presented with a power match on the output to extract the maximum power from the device in question.

For many years, the exact value of the power match impedance at RF and microwave frequencies was regarded as something that could be measured only experimentally. Much like noise match data, it was something that designers had to measure for themselves or, preferably, that was available from the device manufacturer. Thus, the art and science of “load-pull” was founded and remains with us to this day in the form of not inexpensive but very powerful computer-controlled measurement systems. This chapter introduces load-pull techniques and their application in linear PA design. It also shows that there is a simple underlying theory, which can do a fairly decent job of predicting the experimentally generated load-pull data.

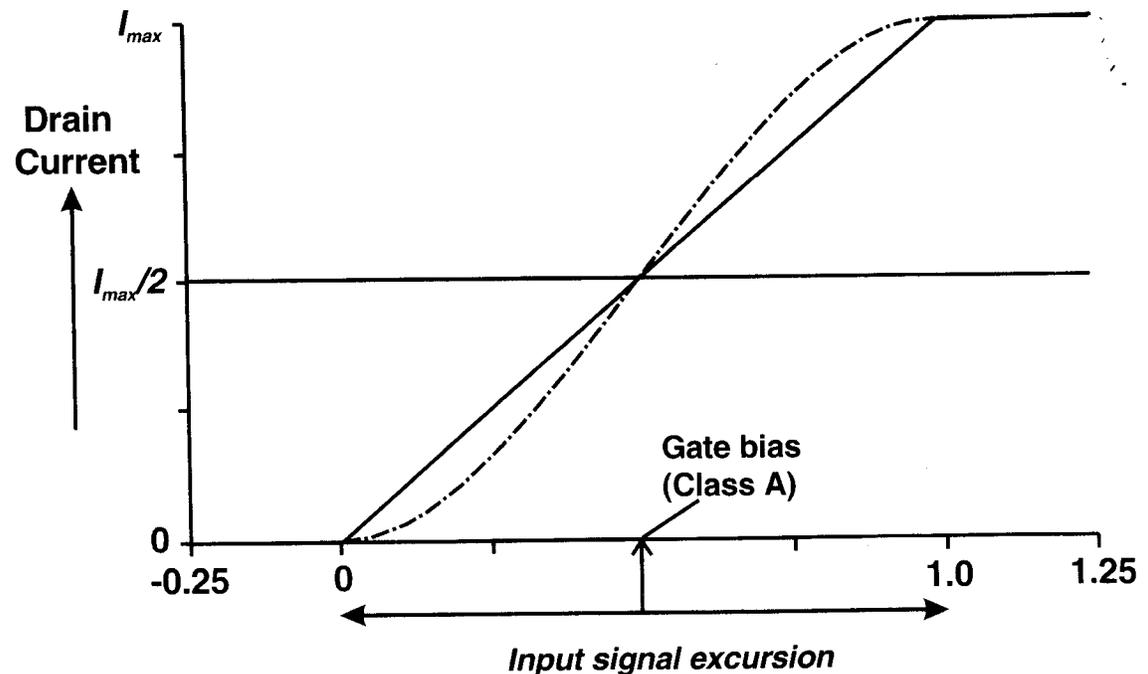
First, however, it is necessary to define two terms that are used throughout this book: *class A amplifier* and *linear amplifier*.

## 2.1 Class A Amplifiers and Linear Amplifiers

It is widely assumed that the terms *class A* and *linear* are almost synonymous, certainly as far as RF PAs are concerned. In fact, class A amplifiers are often by no means linear, and highly linear amplifiers are not necessarily, or even frequently, of the class A type.

Class A is easy to define in its classical manner. Figure 2.1 recalls the ideal strongly nonlinear device transfer characteristic from Chapter 1 (see Figure 1.3). Such a device is assumed to be perfectly linear in the region between cutoff and saturation. If an amplifier is constructed using the exact midpoint of the linear range as the bias point, perfectly linear operation will result, providing the RF drive signal never exceeds the boundary values,  $V_t$  and  $V_{op}$ . If the RF drive signal is perfectly sinusoidal, the output current also will be sinusoidal with no harmonic content. That is a classical class A amplifier.

The amplifier in Figure 2.1 clearly is also a linear amplifier, provided the drive signal does not exceed the stated limits. So in the ideal case, a class A amplifier is linear for that limited range of drive. In practice, of course, the linear region contains weak nonlinearities, as discussed in Section 1.2 and indicated in Figure 2.1. The “weakness” of these nonlinearities becomes less evident as the signal drive level increases; clearly, to make a class A PA, it is necessary to



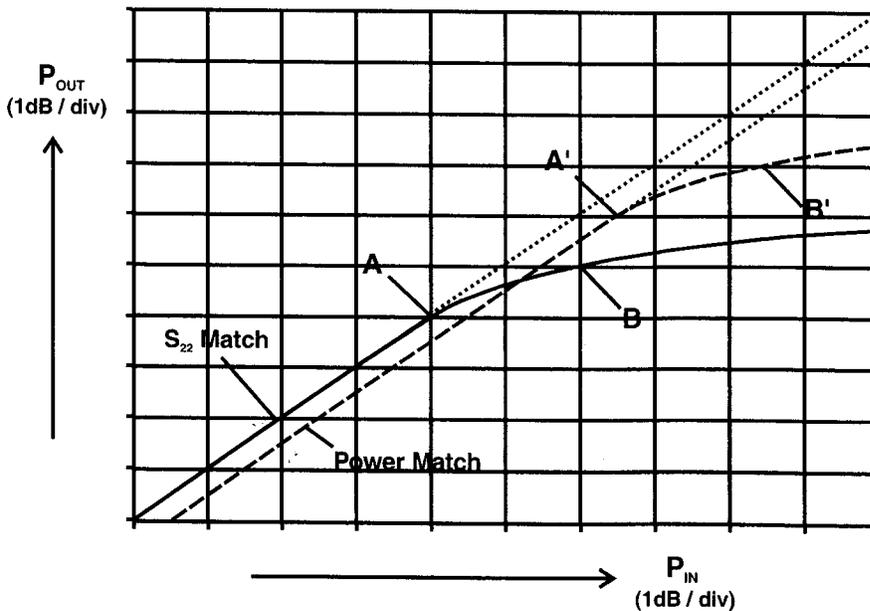
**Figure 2.1** FET class A bias point (see also Figure 1.3). Solid line represents an ideal strongly nonlinear response, used for simplified analysis; dotted line shows the more realistic weakly nonlinear response, with low-level harmonic generation even at low signal amplitudes.

swing the device through the increasingly nonlinear perturbations of the transfer characteristic to reach the hard-clipping limits. In that case, the current in the output generator has a significant harmonic content. In practice, of course, the output current generator is working into a reactive matching network that transforms the  $50\Omega$  environment to the required load resistance value. Such networks typically are low pass, and the harmonics generated by the transconductive nonlinearities will be greatly attenuated. That gives such an amplifier an unfairly clean image, which rapidly fades when a variable envelope, or modulated signal is substituted, and quite high levels of spectral spreading or intermodulation are seen.

This can hardly be classified as a linear amplifier anymore, although it still can be (and usually is) regarded as a class A configuration. Chapter 3 considers in more detail the effects of those weak nonlinearities on PA operation and finds some surprising results. For the present, however, we assume the simple ideal model shown in Figure 2.1.

## 2.2 Gain Match and Power Match

Figure 2.2 shows the power transfer characteristic of a class A amplifier with two different output matching conditions. The solid line shows the response for an amplifier that has been conjugately matched at much lower drive levels. The



**Figure 2.2** Compression characteristics for conjugate ( $S_{22}$ ) match (solid curve) and power match (dotted curve). 1 dB gain compression points (B,B') and maximum linear power points (A,A') show similar improvements under power-matched conditions.

two points, A and B, refer to the maximum linear power and the 1 dB compression power, respectively. It has become something of a standard in the RF amplifier community to use the 1 dB compression point as a general reference point for specifying the power capability of an amplifier or an amplifying device (transistor). It also represents a practical limit for "linear" operation. We see in due course that the 1 dB compression point actually represents a moderate, rather than a weakly, nonlinear point. This chapter focuses primarily on point A, which represents the point at which nonlinear behavior (gain compression) can be initially detected.

In a typical situation, the conjugate match yields a 1 dB compression power about 2 dB lower than that which can be obtained by the correct power tuning, shown by the dotted line in Figure 2.2. That means the device would deliver 2 dB lower power than the device manufacturers specify. Unfortunately, power transistors often are the most expensive individual components in a system, and such a waste of performance can be translated directly into unnecessary cost. So the power-matched condition has to be taken seriously, despite the fact that the gain at lower signal levels (i.e., the lower left corner in Figure 2.2) may be 1 dB or so less than the conjugate-matched condition. Compare the two curves in Figure 2.2 with the pair of lines in Figure 1.5. The behavior has the same root cause in each case, although in the RF world one has only the circumstantial evidence of RF power, rather than direct current and voltage readings, to go by.

It is important to note in Figure 2.2 that no matter which criterion is used for RF power, the power match gives about the same 2 dB improvement. That is to say, the maximum linear power ( $A - A'$ ) increases with power tuning by about 2 dB as well as the 1 dB compression power ( $B - B'$ ). That is a typical observation; across a wide range of devices and technologies, the actual difference may vary over a range of 0.5 to 3 or 4 dB, but the improvement with power match will be fairly constant over a range of gain compression.

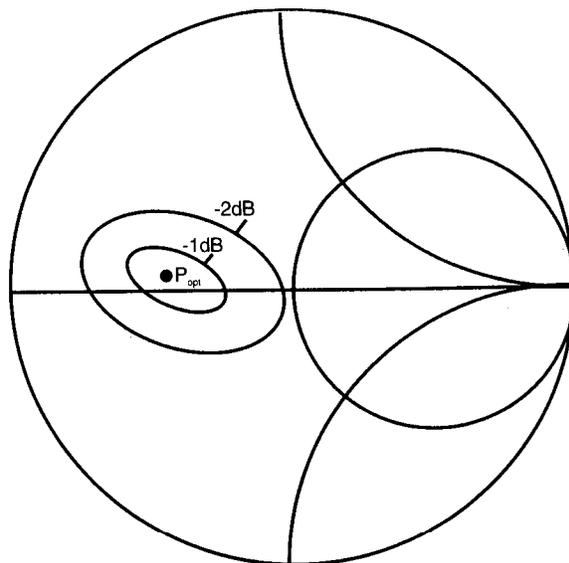
### 2.3 Introduction to Load-Pull Measurements

The two power sweep measurements in Figure 2.2 indicate that there is some kind of functional relationship between output power and output match. The logical next step is to measure more than two data points. Such a measurement is termed a load-pull measurement, presumably originating from analogous measurements performed on RF oscillators. In its simplest form, a load-pull test setup consists of the device under test with some form of calibrated tuning device on its output. The input probably also will be tunable, but this is mainly to boost the power gain of the device, and the input match typically will be fixed

close to a good match at each frequency. Some kinds of RF transistor, particularly bipolars, show significant dependency between output power and input load. It is, in practice, quite difficult to differentiate between true source-pull effects and simple input matching. Devices that show the most prominent source-pulling effects usually operate close to their maximum usable frequency, and this situation is best avoided by using a higher frequency technology.

The hardware itself is considered further in Section 2.4, but a typical set of load-pull data is shown in Figure 2.3. Such a set of data may take weeks, days, or minutes to compile, depending on the degree of complexity, expense, and time invested in the equipment. The results show closed contours, marking the boundaries of specified output power levels. For most practical purposes, the PA designer is concerned mainly with the 1 dB and 2 dB contours, which represent levels relative to the maximum or optimum power output of the device at the test frequency.

The most obvious immediate observation in looking at the data in Figure 2.3 is that the constant power contours are not circular. Unlike noise and linear mismatch (gain) circles, they resolutely refuse to display a circular profile, no matter how carefully the equipment is calibrated. Over the years, they have been variously compared with eggs, potatoes, and English rugby balls, but they definitely are not oranges or soccer balls. This was always assumed to be a manifestation of nonlinear behavior, but a curious twist was largely unobserved; the contours are still roughly the same shape, even if the criterion for power measurement is shifted to the *maximum linear power*, that is, points A, A' in Figure 2.2. This led to a simple explanation for the noncircular shape of the contours, which is considered in detail in Section 2.5.

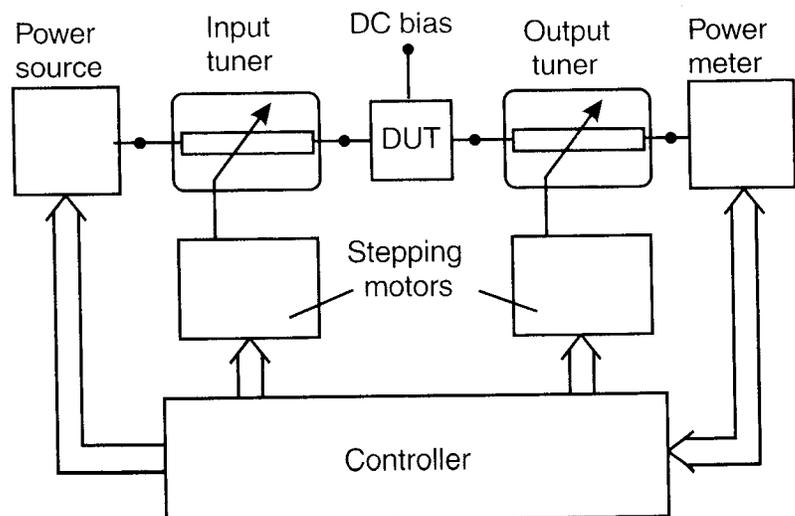


**Figure 2.3** Typical load-pull data.

Load-pull data has been the mainstay of RF and (especially) microwave PA design for many years. It gives the designer a simple target area on the Smith chart on which to base the strategy for suitable matching network design; it essentially converts an intractable nonlinear problem into one that can be attacked and solved using linear techniques and even linear simulators. With the much more recent availability of good, fast, nonlinear simulators and slowly improving large signal models, it could be fairly speculated that load-pull equipment may go down the same road to oblivion, albeit nostalgic and grateful oblivion, as the slide rule and the slotted line. This certainly is not evident yet. Indeed, the most stringent test that can be applied to a simulator is to simulate a load-pull test, and the results from such comparisons (reluctantly and rarely performed, it seems, requiring substantial cooperation between antagonistic parties) are at best only fair. The role of the load-pull setup probably will settle in to one similar to the vector network analyzer in many laboratories, providing the basic measurements required to derive and fine-tune model parameters for different devices as they become available.

## 2.4 Commercial Load-Pull Equipment

Most commercially available load-pull test setups use some form of computer-controlled tuning device. A typical block diagram is shown in Figure 2.4. Such a system probably would rely on off-line calibration, whereby the impedances of many hundreds or thousands of tuner settings are measured with a calibrated network analyzer. It should be noted that an alternative technique is available that uses active techniques, in which a test signal is actually applied to the output of the device, and tuning effects are simulated by varying the amplitude and



**Figure 2.4** Typical load-pull configuration.

phase of the applied signal. The basic principle of active tuning is illustrated in Figure 2.5(a), and a typical RF implementation is shown in Figure 2.5(b). Active techniques have some advantages at much higher frequencies, where the design of mechanical tuners becomes more difficult [1,2]. Mechanical tuners have to be accurately resettable, which presents some design challenges. They typically are controlled by stepping motors, which introduce additional mechanical tolerance problems but also put some substantial time limits on each measurement.

An alternative and elegant tuner design uses electronically switched tuning sections to achieve the necessary tuning ranges [3]. Such a tuner has speed orders of magnitude higher, a major benefit in performing load-pull measurements, which by their nature require hundreds of data points to interpolate the

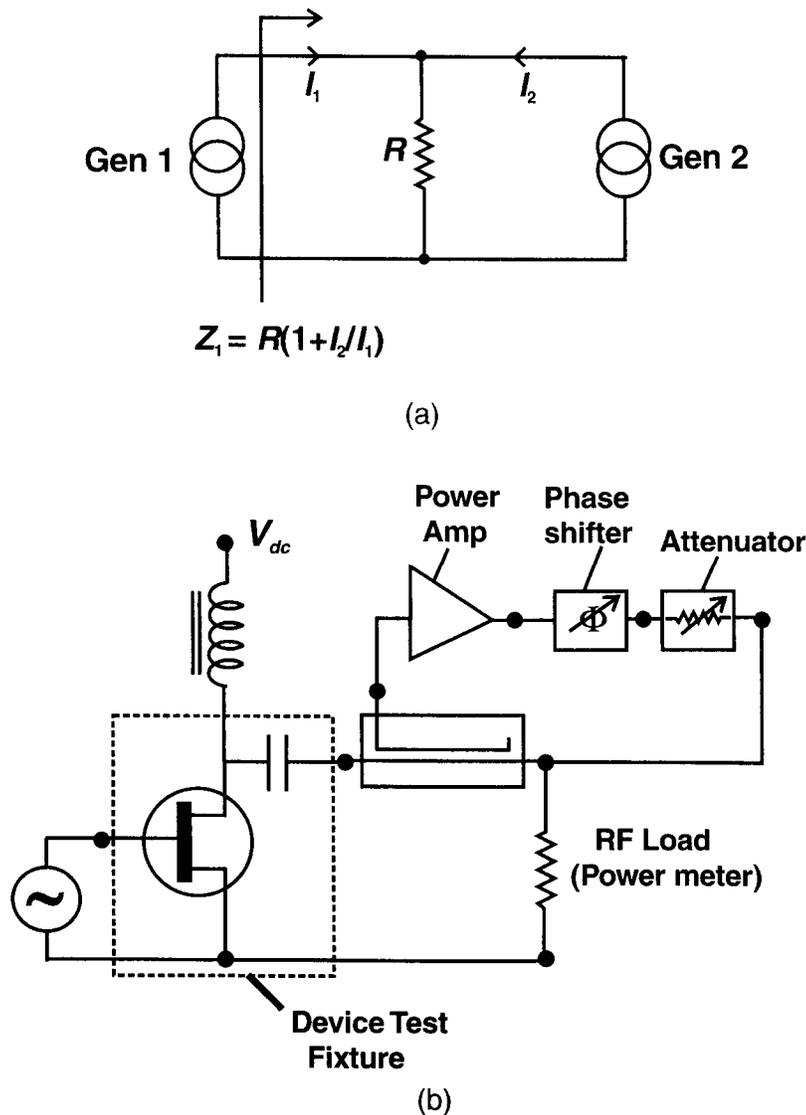


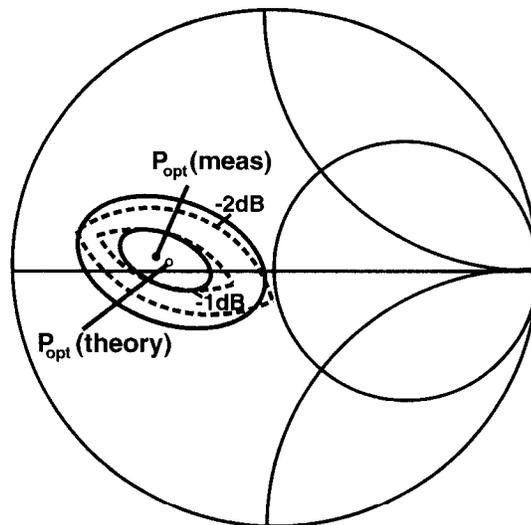
Figure 2.5 Active load-pull: (a) basic principle; (b) RF implementation.

closed contour plots. It also should be fairly stated that the downside is that electronic tuners of this kind have much higher loss than mechanical tuners, and more rigorous calibration is needed, although this usually forms part of the product software.

At this juncture, we are assuming that the matching problem is essentially a linear one; the output current waveform that drives the tuner is perfectly sinusoidal. As we have already observed, this is unlikely to be a valid assumption as the device is driven beyond its maximum linear power point, which in a typical case might be 2–3 dB below its specified 1 dB compression point. This raises some complex issues regarding the predictability and repeatability of the tuner at harmonic frequencies. These issues will be considered further in Chapter 3, but it should be noted that, in principle, all types of tuners can be calibrated at harmonic frequencies as well.

## 2.5 Loadline Theory

In 1983, this author created something of a stir in the microwave PA community by showing that simple loadline principles could be extended to predict load-pull contours for a device kept in its linear range [4]. The biggest surprise was that the resulting contours, plotted on a Smith chart, were areas of intersection between constant resistance and constant conductance circles, displaying a “pointed” version of the familiar flattened circles obtained from load-pull measurements. Figure 2.6 illustrates a typical result, showing a direct compari-

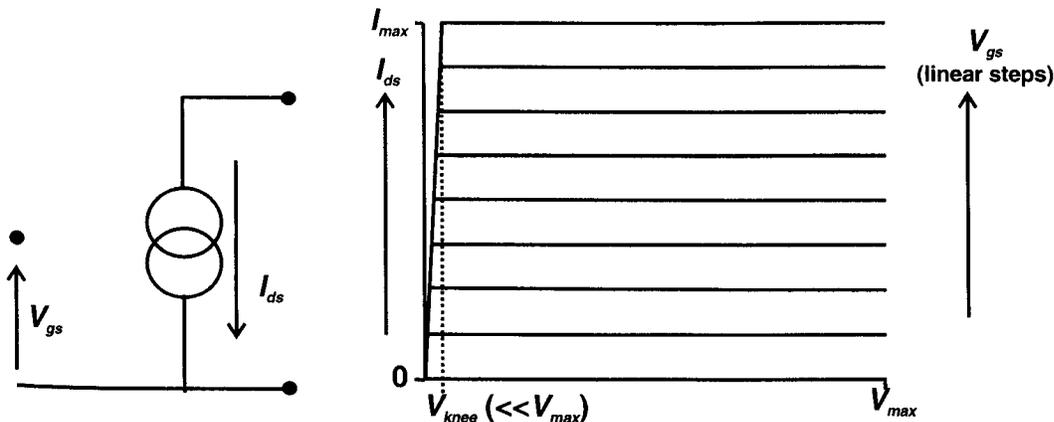


**Figure 2.6** Direct comparison of experimental (solid lines) and theoretically generated (dotted) power contours, using the loadline analysis and equations in this section. (See [4] for device parameter details.)

son between the theoretical prediction and actual measured data. Over the intervening years, several attempts have been made to refine this theory, removing some of the idealizing assumptions made in the original analysis [5]. By and large, however, the simplicity of the original technique has survived attempts to refine it, and it remains a useful *a priori* design method to use as a starting point for a design iteration.

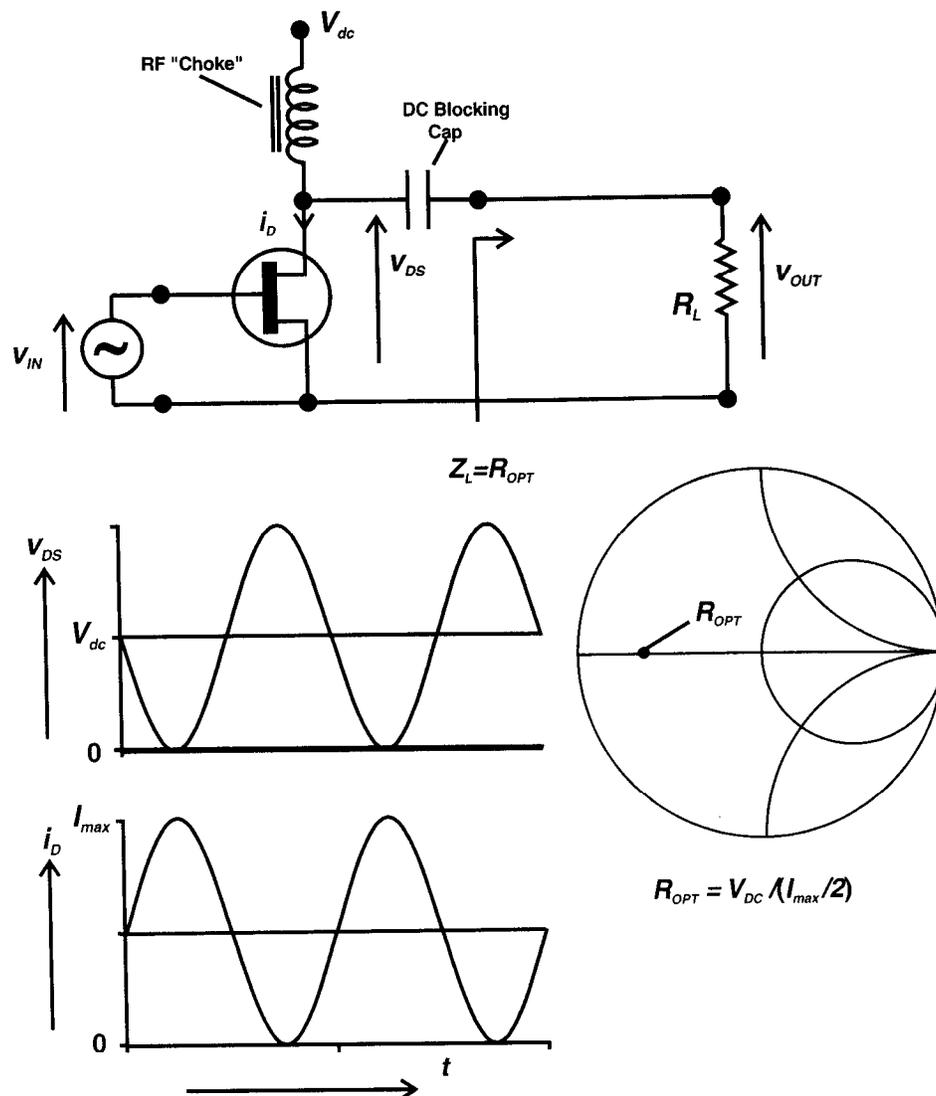
The starting point for this analysis of an RF PA is a heavily idealized device model, shown in Figure 2.7. This ideal strongly nonlinear transconductive device is represented in the figure as a voltage-controlled current source with zero output conductance and zero turn-on (or “knee”) voltage. The transconductance is linear except for its strong nonlinearities represented by pinchoff (for input voltages below  $V_t$ ) and hard saturation at  $I_{max}$ . A key feature of this analysis is that the device is never allowed to breach those limits of linear operation; in this sense, the analysis is valid up to, but not beyond, the onset of gain compression.

Figure 2.8 shows the RF circuit in which the ideal device is analyzed. The output (drain) is ac coupled to an RF load. The dc bias is fed through a separate “choke,” which is assumed to have a very high reactance at the RF frequency.<sup>1</sup> An important detail is that although the transistor is being considered as an ideal voltage-controlled current generator, the RF load may have a reactive component, and the output parasitics of the transistor initially will be considered to be part of the external load.



**Figure 2.7** Ideal strongly nonlinear device model. The “knee” turn-on region is neglected, and between 0 and  $I_{max}$ , the output current generator is linearly controlled by the input generator.

1. Throughout this book, I overrule the grammatical tautology contained in such terms as *RF frequency* and *dc current* in favor of the technical clarity such terms convey.



**Figure 2.8** Class A linear amplifier, with optimum loadline match.

Assuming that the reader is familiar with the concept of a loadline match, we can progress immediately to look at the RF waveforms in Figure 2.8, which show the device under conditions of sinusoidal excitation and optimum loading. The current swings over its maximum linear range (zero to  $I_{max}$ ), that is, with an amplitude of  $I_{max} / 2$ ; the voltage swings over its maximum range of zero to  $2V_{dc}$ . Clearly, the loadline resistor in this optimum power-matched condition has a value of

$$R_{opt} = V_{dc} / (I_{max} / 2) = V_{dc} / I_{dc} \quad (2.1)$$

This is one of the most basic and elementary results of electronics, and it is easy to feel a little deflated in seeing its reappearance at this more advanced level.

Of course, we are making the assumption that currents and voltages at RF frequencies follow the same trajectories as they do on a dc curve tracer. That issue has been the trigger for much controversy over the years, especially in the modeling community [6], but at this juncture we make the quasi-static assumption along with the other idealizations. It is also worth noting that the peak RF voltage of two times the dc supply arises primarily from the symmetry of the assumed sinusoidal waveforms. An RF waveform that is symmetrical about its mean level has to rise to a peak voltage of twice the supply to reach the lowest permissible value on the downward part of the cycle. We see later that when the waveforms become asymmetrical due to harmonic content, the peak voltages can be greater (or less) than  $2V_{dc}$ .

Figure 2.8 shows the device in its optimally matched condition, where it will deliver a power  $P_{opt}$ , where

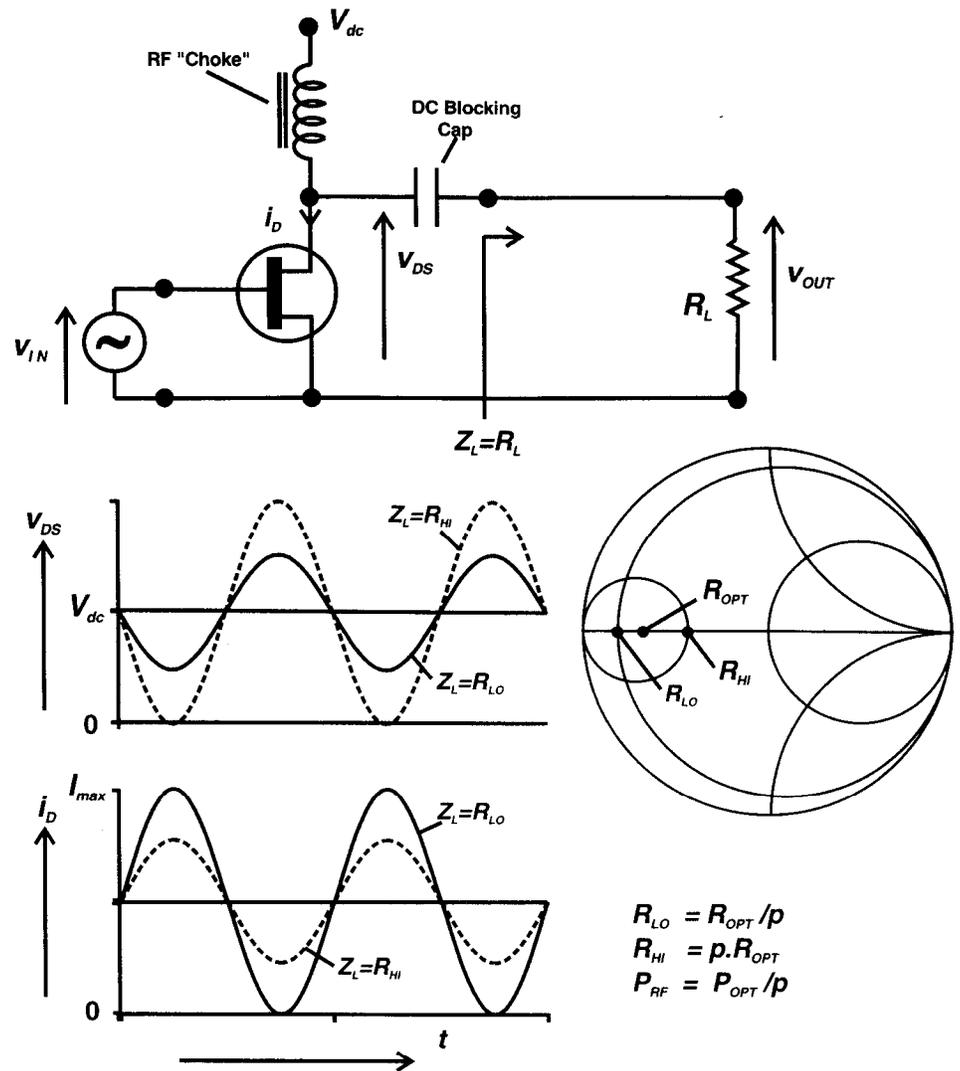
$$P_{opt} = (1/2)V_{dc}I_{dc}$$

Clearly, this represents a classical class A linear amplifier, with a drain efficiency of 50%.

It is now possible to use this simple model and circuit to trace out a load-pull contour by examining the effect of moving the resistive and reactive component of the RF load away from the optimum value of  $R_{opt} + j0$ . In particular, we will determine the range of load terminations that will give a power of  $P_{opt}/p$ , (with  $p = 2$  for initial clarity).

Figure 2.9 shows that there are two resistive terminations that result in a maximum linear power of  $P_{opt}/p$ ;  $pR_{opt}$  and  $R_{opt}/p$ . In the case of the lower resistive load,  $R_{opt}/p$ , the device can swing over the full current range of  $I_{max}$  but the corresponding voltage swing is only  $2V_{dc}/p$ , which corresponds to an RF power output of  $P_{opt}/p$ . In the case of the higher resistive load,  $pR_{opt}$ , the drive level has to be backed off to reduce the current swing and keep the voltage swing at the maximum linear peak value of  $2V_{dc}$ . It clearly can be seen that the current has to be reduced by the ratio of  $p$ , corresponding with a reduced power of  $P_{opt}/p$ .

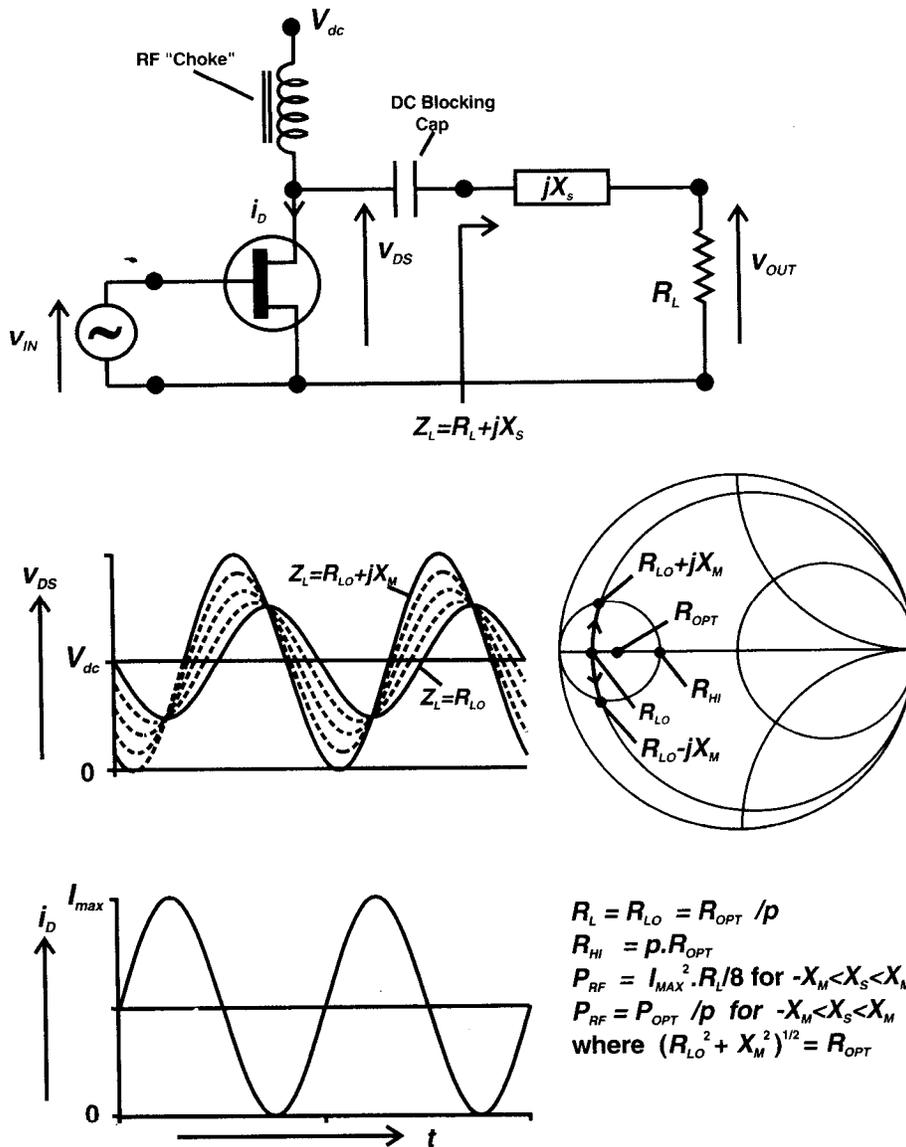
We now have two points on a load-pull contour for a power output level of  $P_{opt}/p$ . Figure 2.10 shows how the  $R_{opt}/p$  point can be extended into a continuous arc segment of constant power if some series reactance is added to the load resistance. The key point is that while the current swing remains at its maximum permissible value, the low voltage swing can be increased by adding series reactance, without affecting the power. This series reactance has a maximum value,  $\pm X_m$ , whose value is such that the series combination of  $X_m$  and  $R_{opt}/p$  gives a complex magnitude of  $R_{opt}$ . In a similar manner, Figure 2.11



**Figure 2.9** Class A linear amplifier case 1: resistive output loads for  $R_L < R_{OPT}$ , RF power output is  $P_{OPT} / p$  ( $I_{pk} = I_{max}$ ). For  $R_L > R_{OPT}$ , RF power output is  $P_{OPT} / p$  ( $I_{pk} = I_{max} / p$ ).

shows that the  $pR_{opt}$  point can be extended into another arc segment of constant power if some shunt susceptance is added to the load conductance. In this case, the maximum voltage swing can be kept constant while the RF current swing is increased, while a corresponding shunt susceptance is added. The limiting case here is that the complex admittance magnitude of the load is equal to  $1 / R_{opt}$  ( $= G_{opt}$ ).

The two arcs of constant power conveniently follow the printed Smith chart circles of constant resistance,  $R = R_{opt} / p$ , and constant conductance,  $G = 1 / (pR_{opt})$ . It remains to be shown that the contour is indeed closed and that the limiting points of constant power, as derived, coincide at the apex of the inter-



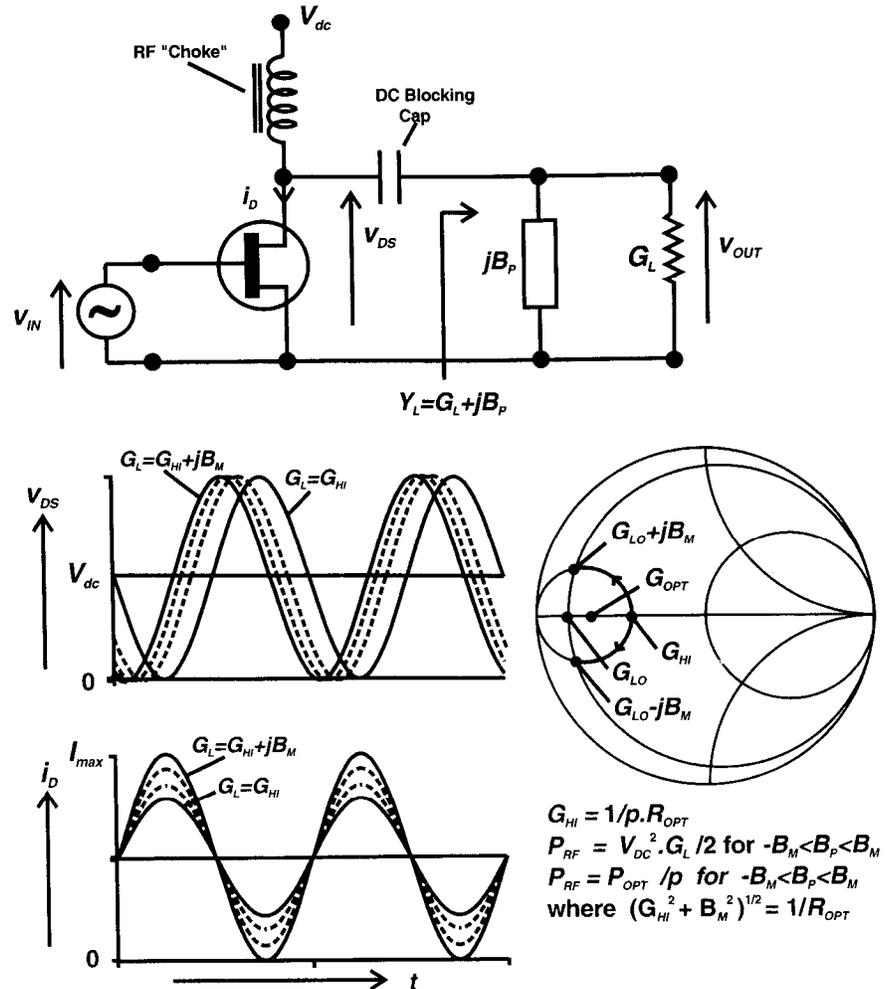
**Figure 2.10** Class A linear amplifier case 2: output load resistive component lower than  $R_{OPT}$ . For  $R_L = R_{OPT} / p$ , RF power output is  $P_{OPT} / p$ , over a range of series reactance  $-X_M < 0 < X_M$

section of the separate arcs. This is the simple exercise of showing that the impedance  $R_{opt} / p + jX_m$  is the same as the admittance  $1 / (pR_{opt}) + jB_m$ , where

$$X_m^2 = R_{opt}^2 (1 - 1/p^2)$$

and

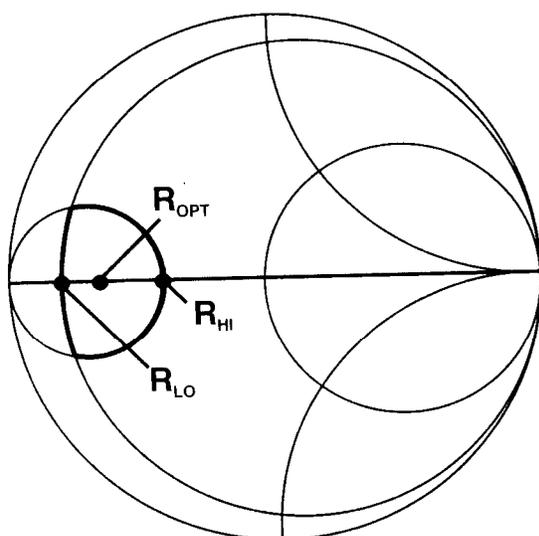
$$B_m^2 = G_{opt}^2 (1 - 1/p^2)$$



**Figure 2.11** Class A linear amplifier case 3: output load resistive component higher than  $R_{OPT}$ . For  $R_L = pR_{OPT}$ , RF power output is  $P_{OPT} / p$ , over a range of shunt susceptance  $-B_M < 0 < B_M$ .

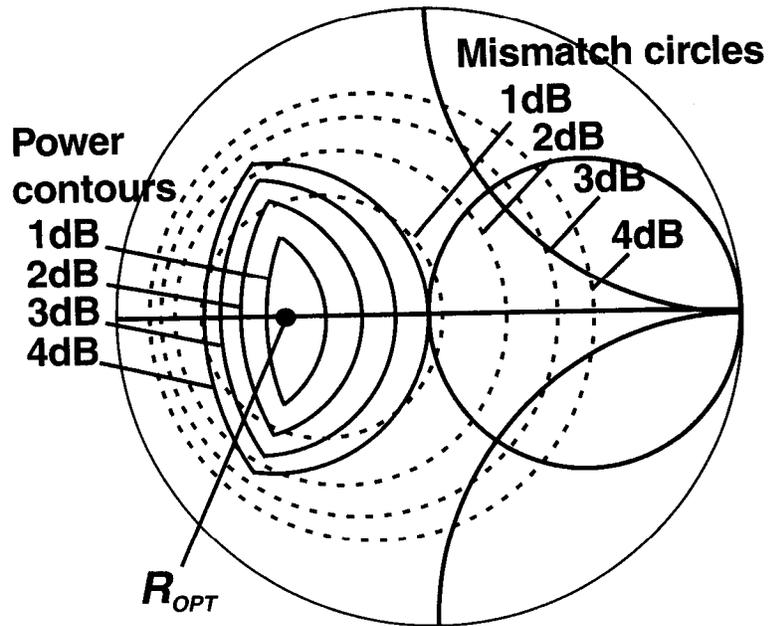
The final result drawn for the case of  $p = 2$  (the 3 dB power contour) is shown in Figure 2.12. The noncircular nature of constant power contours is clearly indicated. Figure 2.13 shows a family of contours, easily constructed as described, for a range of  $p$  values corresponding to 1 dB steps. It is especially interesting to note the small target area represented by the 1 dB contour and the much larger size of a conventional 1 dB mismatch circle centered on  $R_{opt}$  (shown dotted in Figure 2.13). This is further evidence against the notion that power match is a simple manifestation of a “large-signal” movement of  $s_{22}$ .

The contours shown in Figures 2.12 and 2.13 apply at any frequency.



**Figure 2.12** Constant power contour for  $p = 2$  ( $-3$  dB). Closed contour is formed by intersecting circles of constant resistance ( $R = R_{LO} = R_{OPT} / p$ ) and constant conductance ( $G = 1 / R_{HI} = 1 / pR_{OPT}$ ).

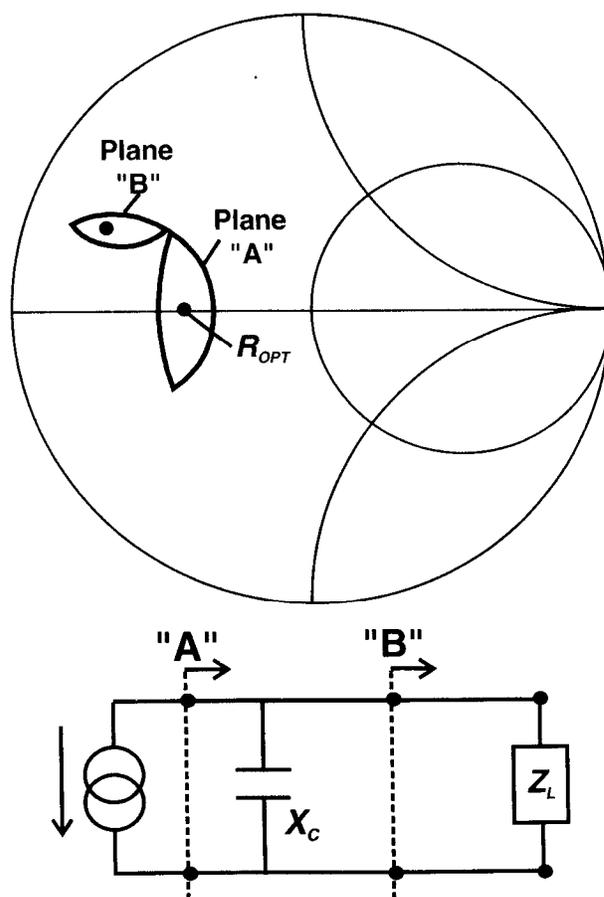
That comes as something of a surprise to load-pull measurement stalwarts, who are accustomed to seeing substantial movement of the measured contours as a function of frequency. The key point is the choice of reference plane for impedance measurement. In this section the reference plane has been the terminals of the transistor output current generator; in practice, the closest physical point for measurement purposes lies outside the immediate chip and package parasitic reactances. Another way of looking at this is to recognize that the impedances represented by the contours as analyzed here are measured in absolute units of ohms, resistive and reactive. Consequently, the external circuit can be analyzed at any frequency and plotted on the same chart as the load-pull contours, as described. If the reference plane is shifted to a point where parasitic reactances with specific values are included between the current generator and the reference point, the contours will become frequency dependent, inasmuch as capacitors, inductances, and transmission lines have frequency-dependent reactances. This de-embedding procedure is necessary to compare the theoretical results derived in this section with actual measured data. It is, nevertheless, a useful feature to be able to remove the frequency dependency of load-pull contours by suitable choice-of-reference-plane location. (This is illustrated in Section 2.7 as a particularly useful aid for broader bandwidth designs.)



**Figure 2.13** Power-match contours (solid, 1 dB to 4 dB contours shown) compared with gain mismatch circles (dotted) based on a source impedance equal to the optimum power match ( $R_{OPT} = 20\Omega$ ).

## 2.6 Package Effects and Refinements to Load-Pull Theory

The load-pull theory developed in Section 2.5 needs a simple extension so that direct comparisons with measured data can be made. Figures 2.14 and 2.15 define the problem in a typical case; the load-pull contours have been derived at plane “A,” the terminals of the transistor current generator. We need to transform this result to plane B, which might represent the output solder tab of the packaged die. The device output capacitance, bondwire inductance, and the package parasitics have to be taken into account at plane B to present an impedance that maps onto the original contour at plane “A.” This is a simple task for a linear circuit simulator, although care is needed in applying the necessary transformations in the correct direction. For example, Figure 2.14 shows the transformation at plane B, where the only significant element is the shunt capacitance. The contour appears to rotate, or slide, around the circle of shunt conductance, in going from plane “A” to plane B. But the direction is opposite to that of an impedance transformation, because here we are compensating, or de-embedding, the shunt element. Clearly, the transformation will be frequency dependent if the capacitor has a fixed value. Figure 2.15 shows the effect, over

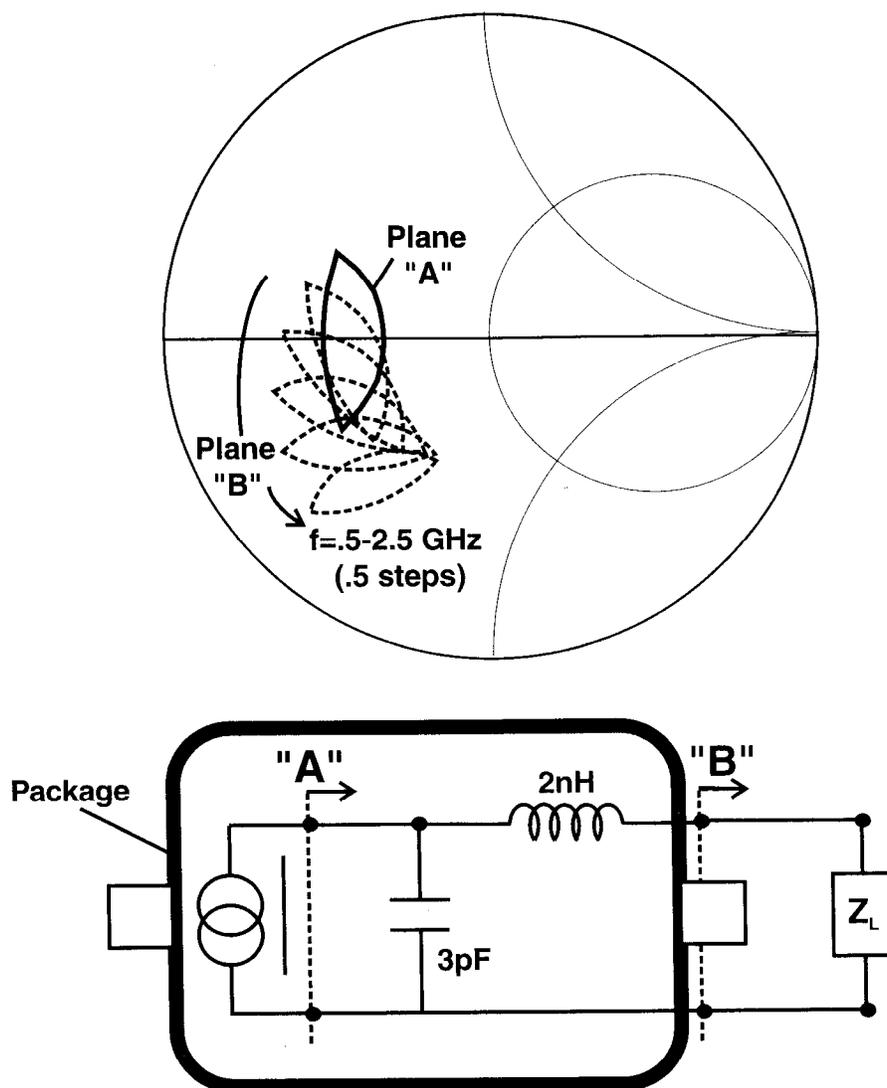


**Figure 2.14** Power contour measured at reference plane A (transistor current generator) and plane B, showing the appropriate compensation (de-embedding) required at B due to the shunt capacitance. Contours plotted for  $R_{OPT} = 20\Omega$ ,  $X_C = 35\Omega$  (5pF @ 2GHz).

frequency, of applying the necessary transformation to a typical transistor and package.

Referring back to Figure 2.6, the theoretical contour (dotted) has been transformed in the manner described to allow for a series bondwire and a device output capacitance, thus appearing to topple over backward from its original upright position. The agreement in Figure 2.6 is good, and general experience is that the loadline theory tends to set slightly tighter design target zones; a perfectly acceptable situation for practical purposes.

The comment often has been made that particularly for narrowband designs, which are common in wireless communication bands, the removal of frequency dependency by transforming the design impedance reference to plane "A" is unnecessarily cumbersome, given that device and package parasitics may



**Figure 2.15** Power contour measured at reference plane A (transistor current generator) and plane B, for a typical set of package parasitic reactances. With fixed reactive components, the plane B contours become frequency dependent.

not be accurately known. A single-frequency, measured load-pull data set would, in principle, enable a design to be done, but the lack of any ability to analyze the performance of different matching networks over frequency is a serious limitation, even for narrowband designs. The design example in Section 2.8 shows that the theoretical load-pull contour approach enables some valuable tolerancing analysis to be done, something that a single data set would not permit. For numerous reasons, it is good RF practice to have some idea of the package parasitics. Reputable device vendors should be able to supply package models, and in the limit, simple package models are not difficult to derive for frequencies up to 2 GHz, so long as access to a vector network analyzer is avail-

able. One approach is to take the  $s$ -parameters of the die by itself (which may be available as a standalone product) and fit a simple package model to the packaged device data.

Although the general agreement between theory and measured data in Figure 2.6 is good, several refinements are advisable in using this method for the design of practical PAs. Most notably, the calculation of the value of  $R_{opt}$  needs to be re-examined. Looking back to Figure 2.8, we can see that the device RF current is shown at a peak value of  $I_{max}$  at the same instant that the drain voltage is at zero. That clearly is a direct result of the ideal turn-on, or knee, characteristic shown in Figure 2.7. To sustain gate-controlled current, it is necessary to reduce the value of the load resistor so that the drain (or collector) voltage is kept above the appropriate knee voltage for the device being used. For Si BJT and GaAs MESFETs, a suitable value for this reduction would be 1V. Diffused metal oxide semiconductor (DMOS) and laterally diffused MOS (LDMOS) devices would require a larger correction (although they probably also would be running at higher supply voltages).

Some comment also is needed on the peak current  $I_{max}$ , which is not a commonly specified parameter on data sheets. It turns out that  $I_{max}$  is not an easy parameter to measure directly; in fact, the best way of estimating its value is to build an optimized class A amplifier and observe the dc supply current. Assuming that the RF current is sinusoidal, the value of  $I_{dc}$  equals  $I_{max} / 2$ . Most data sheets give a typical class A operating condition, including values for RF power input and output, and dc bias, so that a representative value for  $I_{max}$  can be obtained. This approach is particularly useful for bipolar transistors, which compared to FETs do not have such an easily identifiable current saturation characteristic. So the modified value for  $R_{opt}$  is

$$R_{opt} = (V_{dc} - V_k) / I_{dc} \quad (2.2)$$

Some FETs, particularly MESFETs, show significant slope on their I-V characteristics, corresponding to a dc output conductance. It is tempting, therefore, to include that as a physical conductance which acts in parallel with the external load resistor. In practice, and as can be confirmed by running nonlinear time-domain simulations, the slope of the dc characteristics tends to be canceled as the device sweeps over the loadline range of current and voltage, and the assumption of zero ac output conductance seems to give a better approximation than the simple dc conductance correction. The bottom line is that all these approaches are approximations and represent useful starting points. A nonlinear simulator, with an accurate curve fit to the whole I-V function, is the only way to obtain a more accurate answer to the precise optimum value for  $R_{opt}$ . The

difference between that value and the approximate one often may lie inside the global variation of transistor current and threshold specifications.

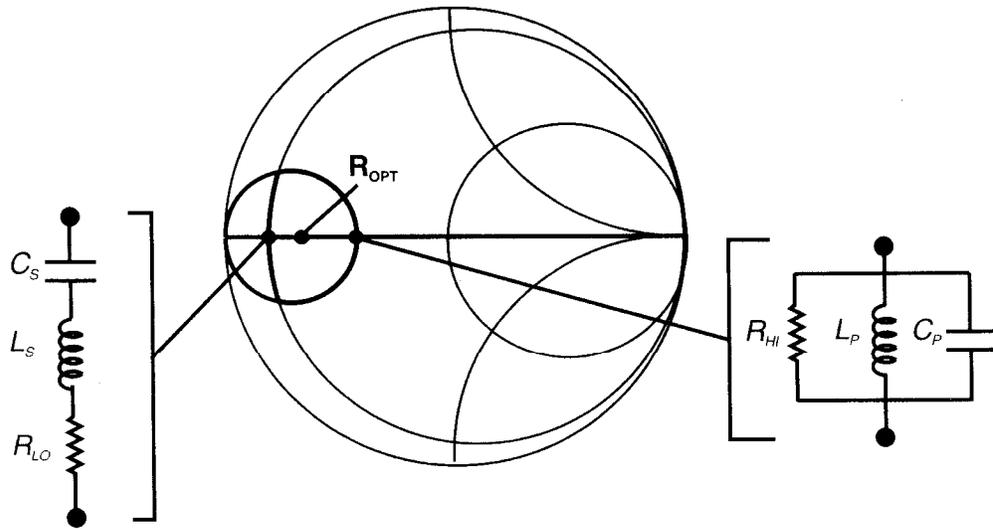
## 2.7 Drawing the Load-Pull Contours on CAD Programs

Although the simplicity of the loadline approach to PA design has found wide appeal in the microwave amplifier community, CAD package developers have not embraced the concept as readily. It would be a simple and useful addition to any linear RF or microwave circuit analysis program to have a routine that plots out the load-pull contours for a simple set of device parameter inputs, in much the same way that noise circles usually are offered. Fortunately, it is a simple matter to trick a circuit analysis program into plotting the contours.

If we refer to Figure 2.12, it is clear that the two arcs of the load-pull contour could be modeled as series and parallel LCR circuits. The values can be chosen such that, over the frequency sweep range in use for the design in question, the impedances of these “dummy” circuits sweep precisely over the area of intersection, defining the actual limits of each contour. Figure 2.16 shows the construction of such circuits and gives equations for the value of the components in terms of the required contour (in decibels) and the frequency sweep range. Obviously, the values have to be changed when the sweep range is changed. Many CAD packages now include some possibility for defining element values in terms of expressions involving the frequency limits and other component values in the circuit, enabling the contours to be plotted independently of frequency sweep settings.

## 2.8 Class A Design Example

We now will perform a simple design example to demonstrate the steps for designing a class A amplifier using the techniques developed in the preceding sections. As stated at the beginning of this chapter, the goal here is to transform a challenging nonlinear design problem into one that can be solved using the simplest of design tools. The procedure is analogous to the classical design of an LNA, in which the input impedance transformation is based on knowledge of the optimum noise match and derivative noise circle family. Here the output matching network is based entirely on the loadline approach and the simple Smith chart construction of 1 dB load-pull contours. The input match is done using the linear  $s$ -parameters; the design is based on a power level that is on the threshold of—but not beyond—the point of measurable gain compression, where the  $s$ -parameters still have values close to those measured at much lower



For "p" dB contour:

$$R_{LO} = R_{OPT} / 10^{p/10}$$

$$R_{HI} = R_{OPT} \cdot 10^{p/10}$$

$$C_S = \frac{1}{X_M} \left( \frac{1}{\omega_1} - \frac{1}{\omega_2} \right)$$

$$C_P = B_M \cdot (\omega_2 - \omega_1)$$

$$\omega_1 \cdot \omega_2 \cdot L_S \cdot C_S = 1$$

$$\omega_1 \cdot \omega_2 \cdot L_P \cdot C_P = 1$$

where  $X_M = \sqrt{R_{OPT}^2 - R_{LO}^2}$ ,

where  $B_M = \sqrt{\left( \frac{1}{R_{OPT}^2} - \frac{1}{R_{HI}^2} \right)}$

and  $\omega_1, \omega_2$  are sweep limits

**Figure 2.16** Construction of load-pull contours on simple circuit analysis programs by use of dummy series and parallel resonant circuits for series and shunt arcs.

signal levels. It already has been shown that a good power match at this point is likely to be close to the optimum for higher levels of compression and in any case represents a good compromise for variable envelope signals.

The design is based on a typical 1W GaAs MESFET at a frequency of 1.9 GHz, a class A design. So this design cannot be expected to meet the efficiency requirements of a cellular handset PA, but it does illustrate the design principles discussed so far.

### 2.8.1 Step 1: Define Target Specs, Select Device, Determine $R_{opt}$

In this case, a transistor specified to give 29 dBm typical power at its 1 dB compression point is selected. The manufacturer's data shows that this power is

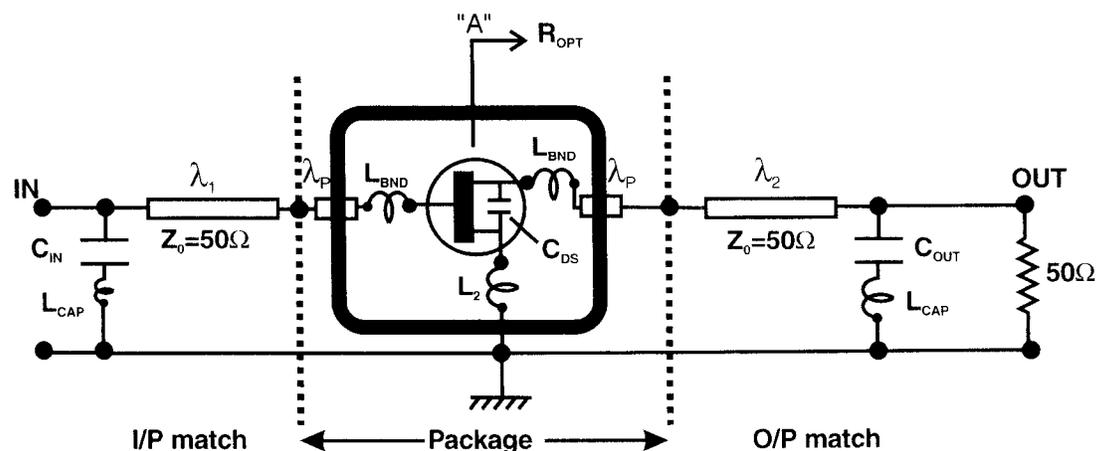
obtained at a class A dc bias of 4.8V and 375mA. The design frequency band is 1.75–1.85 GHz.

Allowing 1V for the knee of a typical GaAs MESFET, (2.2) gives

$$\begin{aligned} R_{opt} &= (4.8 - 1)/0.375 \\ &= 10.1\Omega \end{aligned}$$

### 2.8.2 Step 2: Set Up Schematic and Output Matching Topology to Give $R_{opt}$ at Plane "A"

In Figure 2.17, the output power matching circuit is set up the same way as analyzed in the preceding sections. In this case, it is assumed that we know the values of the transistor output capacitance and the package parasitics. The matching problem, therefore, is to present an impedance of  $10.1\Omega$  at plane "A," a point inside the package and the output capacitance. The initial matching strategy is to present the optimum impedance at the midband point and then look at a swept frequency analysis to determine whether the bandwidth is satisfactory. A simple lowpass section is shown, consisting of a length of  $50\Omega$  microstrip line and a shunt capacitor. These values can be adjusted to give a suitable midband match, as shown in Figure 2.18. Note that the 1 dB contour



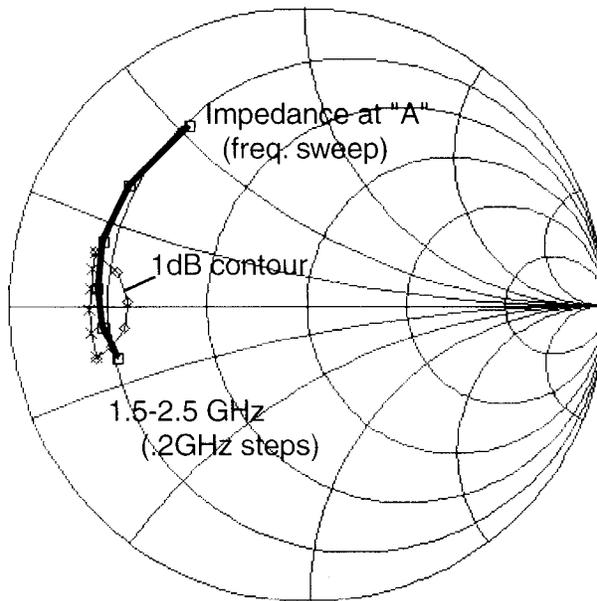
Element values (see text for design details):

$$C_{OUT}=2.7\text{pF}, C_{IN}=4.7\text{pF}, L_{CAP}=0.6\text{nH}, C_{DS}=1.5\text{pF}$$

$$L_S=0.08\text{nH}, L_{BND}=0.2\text{nH}, \lambda_p = 40\text{mil} (\epsilon_r=10, h=10)$$

$$\lambda_1 = 150\text{mil} (\epsilon_r=4.5, h=31\text{mil}), \lambda_2 = 180\text{mil} (\epsilon_r=4.5, h=31\text{mil})$$

Figure 2.17 Schematic of 1.9 GHz 1W linear PA design.



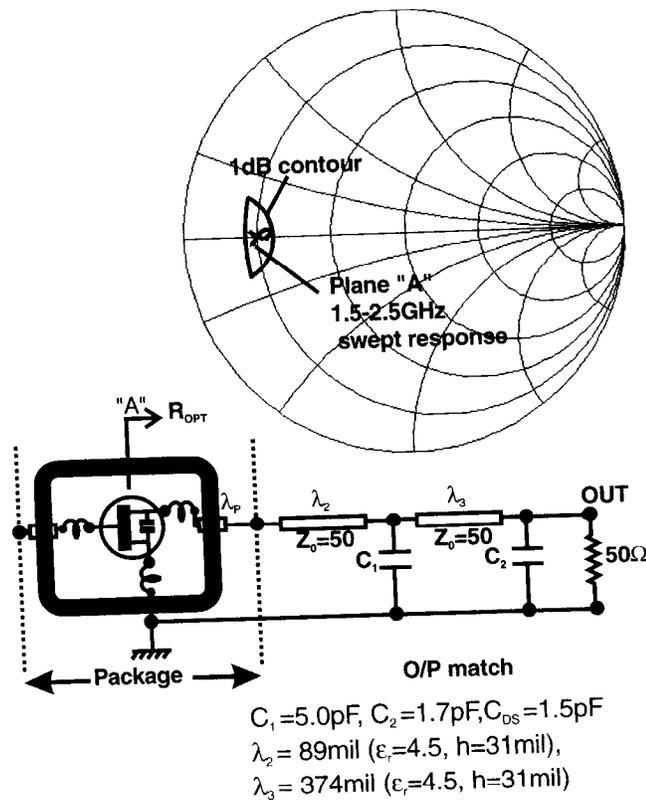
**Figure 2.18** Plane A impedance sweep, with 1 dB power contour (single-section matching network).

has been plotted out as described in Section 2.7, using dummy series and parallel resonant circuits in the analysis file.

Look at the broadband sweep, where it can be seen that although the matching topology is fairly narrowband in nature, the small percentage bandwidth is satisfactory for this particular application. Figure 2.19 shows how much greater bandwidth could be obtained, if necessary, by using a double-section matching network; the whole band from 1.5 to 2.5 GHz shows a good power match, comfortably nestled inside the 1 dB contour. Although this kind of match uses extra components and represents a possible overkill for typical wireless communication bandwidths, it nevertheless is a dramatic demonstration, both of the improved bandwidth of a two-section network and of the utility of the plane-A load-pull reference plane technique.

The single-section matching network can be realized using a length of microstrip line and a surface mount capacitor. Unfortunately, typical capacitors, such as an 0603 surface mount type used here, have substantial parasitics, which need to be included at these frequencies.<sup>2</sup> In Figure 2.17, a series induct

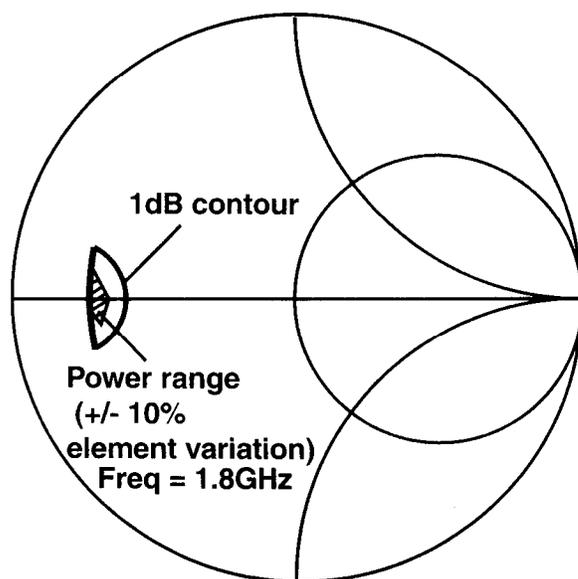
2. 0603 refers to the physical profile of a family of surface mount components, measuring 0.060 inch by 0.030 inch.



**Figure 2.19** Broadband power match (matching capacitor parasitics not included).

tance of 0.6 nH has been included. For a narrowband design of this kind, the effect of such a series parasitic simply is to lower the original design value of capacitance from 4 pF to an effective value of 2.7 pF. Such a simple accommodation of parasitics ceases to be valid, of course, for wider band designs, in which the solution may be to use lower parasitic components.

It is worthwhile, at this point in the design procedure, to take a preliminary look at component and manufacturing tolerancing. Since this is a PA, one of the most important issues is how much the power will vary across a range of manufacturing tolerances for the two key matching elements on the output, the capacitor and the microstrip line. Assuming that the width of the line and the dielectric constant of the material will be held to very tight tolerances, the capacitor value and the length of the line (represented by its exact placement) may vary by as much as 10%. Obviously, the larger the percentage, the lower the cost but the lower the yield. Figure 2.20 shows the impedance variation at plane "A" for a  $\pm 10\%$  variation in the output matching capacitor ( $C_{out}$ ) and the microstrip matching section length ( $\lambda_2$ ). Although the



**Figure 2.20** Power variation due to manufacturing tolerances on output matching elements.

range of impedances (the shaded area in Figure 2.20) still clings to the inside of the 1 dB contour in this specific example, it shows that a better centered pair of design values exists for this simple narrowband design. This ability to view the projected output power variation for both frequency and element tolerances is a powerful, but not widely recognized, feature of this simple design technique.

### 2.8.3 Step 3: Design Input Match Using Linear (*s*-parameter) Methods

Having designed the optimum power match on the output side, it is now permissible to complete the design using standard linear techniques. This results in a similar single-section lowpass input matching network, as shown in Figure 2.17. The whole amplifier linear response can be plotted out, along with the input and output VSWR, as shown in Figure 2.20. Note that the output VSWR measured in terms of the overall  $s_{22}$  is poor, showing around a 3 dB return loss. That is due in part to the reactive input match where  $k$  is close to unity but mainly is due to the power match on the output. Even if the input matched were “de-Q’d” using a lossy element, the output would remain mismatched to  $50\Omega$ . That indeed is the main difference between the design now completed and a simple linear conjugate matched design; the latter gives good output VSWR but maybe 2–3 dB lower maximum power.

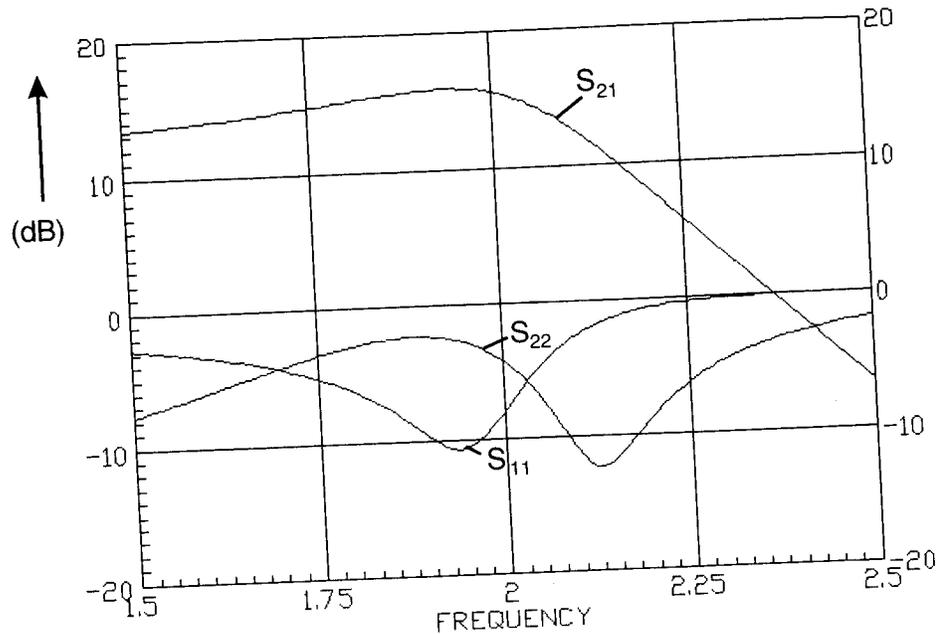


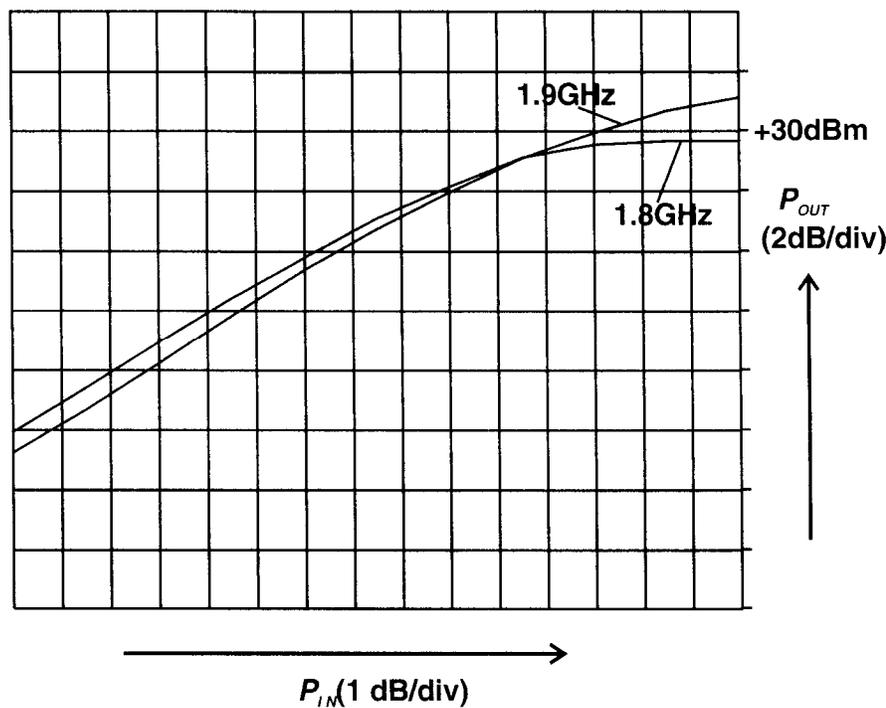
Figure 2.21 Gain and return loss of 1W class A amplifier.

#### 2.8.4 Step 4: Build it!

A linear simulator cannot, of course, give a sweep of the power performance. In general, that would be the point at which the whole design would be analyzed using a nonlinear simulator to remove the idealizations and fine-tune the design values. But for many years, the next step would have been to lay out a test board and build the circuit. Figure 2.22 shows some actual measured data taken on an amplifier built to the above design. The GaAs MESFET device is a low-cost packaged part typical of several on the market. The power sweeps at 1.8 and 1.9 GHz show 1 dB compression of at least 29 dBm. The power performance at 1.9 GHz seems to be somewhat better than at the 1.8 GHz design frequency, but the performance is within expectations.

### 2.9 Summary

This chapter has shown that class A PA design can be reduced to a linear design problem through the use of loadline techniques to determine the optimum power match. Although the material in this chapter may be considered by some to be of an elementary and approximate nature, the basic methods described have been used to design a wide range of RF and microwave amplifiers, from narrowband to broadband, from tens of milliwatts to hundreds of watts, and



**Figure 2.22** Measured swept-power data on class A amplifier design.

from low frequencies to above 100 GHz. Those wishing to implement these methods are encouraged to do so without being overawed by the more advanced concepts introduced in Chapter 3 onward.

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