



Lecture 6

SAR ADC

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Low/Medium Bandwidth ADCs

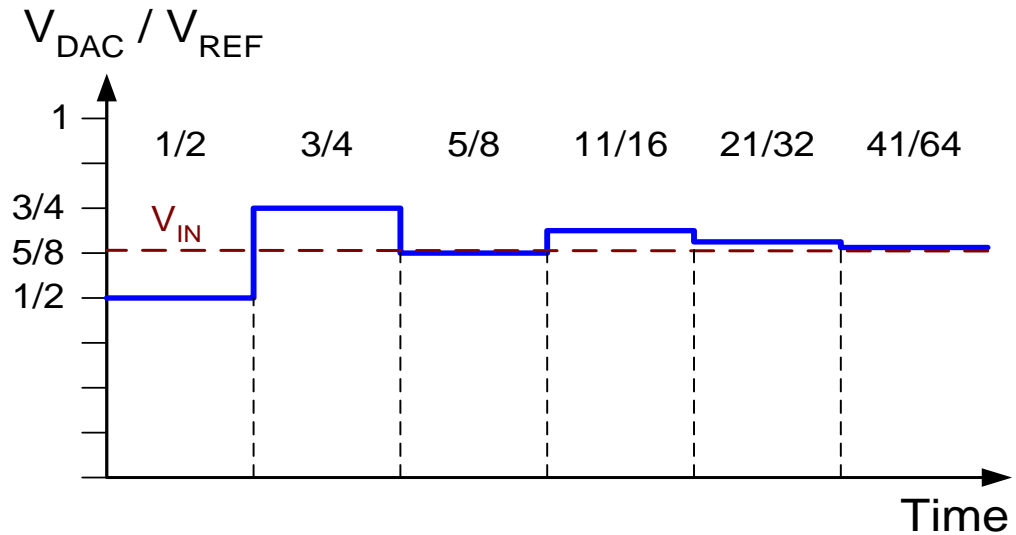
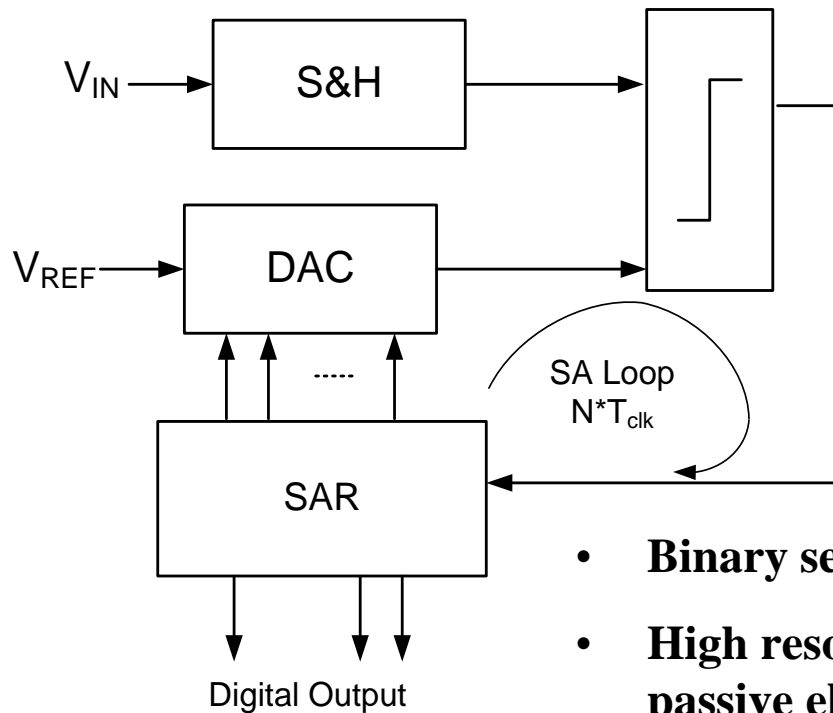
- Flash architecture → a single step conversion → large number of comparators and conversion power (area and power)
- In most ADC architectures it is possible to trade bandwidth for performance, either in the form of power or area.
- We will study three ADC architectures that provide trade-off of this kind ordered by complexity (not by bandwidth):
 - **The SAR ADC** uses a DAC and a feedback configuration to approximate to the input signal in several steps.
 - **The pipeline ADC** (medium bandwidth) is similar to the SAR but with a pipeline configuration
 - **The Sigma-Delta ADC** is based on a minimal error approximation to the input signal by integration and feedback

B. Murmann, "ADC Performance Survey 1997-2015," [Online].

Available: <http://web.stanford.edu/~murmman/adcsurvey.html>.



Successive Approximation Register (SAR) ADC



- **Binary search over DAC output**
- **High resolution is achievable but usually limited to <10bit due to passive elements size scaling**
- **Moderate speed $\sim 1\text{Ms/s}$**
 - Derived from maximum T_{clk} frequency divided by N steps.
- **Binary search algorithm $\rightarrow N * T_{\text{clk}}$ to complete N bits**
- **Conversion speed is limited by comparator, DAC, and digital logic**



SAR Advantages and drawbacks

Advantages:

- **No analog stages → only comparator and DAC, there is no need for gain**
 - **No OpAmp needed**
 - **Only power is consumed by DAC, logic, comparator → Very low power consumption**

Drawbacks:

- **Every step introduces the same error**
 - **Need to operate at maximum accuracy at every step**
 - **The maximum error step gives the accuracy performance**
- **We will readily see in next slides that this requirement results in a large scaling penalty**
- **The accuracy requirement also extends to the Sample and Hold**



SAR Resolution limits

- **DAC:**
 - **The DAC is the main limit to high resolution SARs**
 - **As seen in our previous lecture, the DAC resolution is limited by mismatch and parasitic elements.**
 - **Usually high resolution SAR (>10b) requires DAC calibration**
- **Comparator:**
 - **Little effect on the resolution**
 - **The comparator offset appears at the transfer characteristic, but this is a constant offset so it can be cancelled or calibrated**
 - **Common mode non-linearity can introduce INL/DNL**
 - **Comparator input noise must be kept low. As noise varies between successive SAR steps it may introduce an error in the successive approximation algorithm**
- **Sample and hold:**
 - **Non linearity and distortion at the S&H will be reflected in the ADC.**



Successive Approximation Example

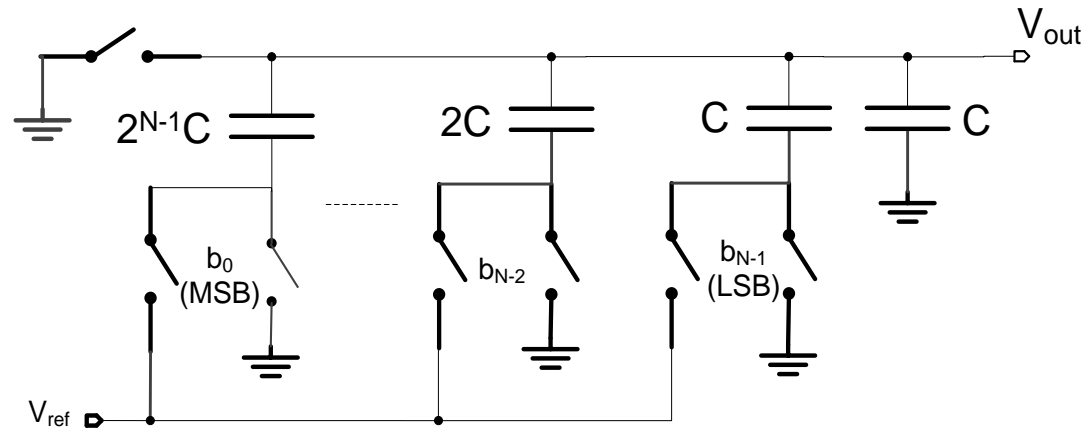
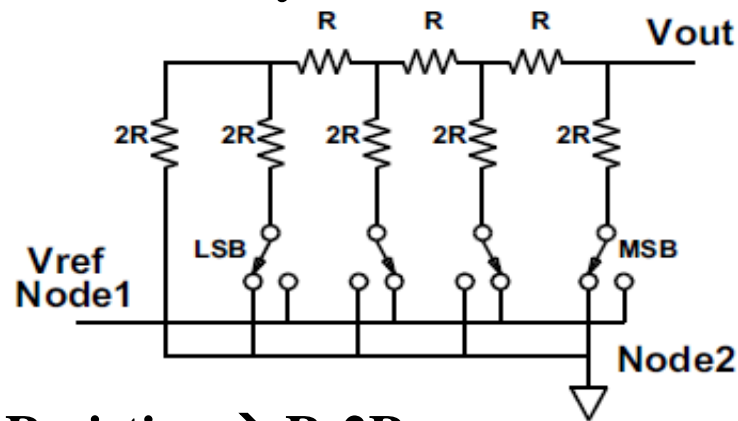
- 10 bit resolution or 0.0009765625V of V_{ref}
- $V_{in} = .6$ volts
- $V_{ref} = 1$ volts
- Find the digital value of V_{in}
- First bit: MSB (bit 9)
 - Divided V_{ref} by 2
 - Compare $V_{ref}/2$ with V_{in}
 - If V_{in} is greater than $V_{ref}/2$, turn MSB on (1)
 - If V_{in} is less than $V_{ref}/2$, turn MSB off (0)
 - $V_{in} = 0.6V$ and $V = 0.5$
 - Since $V_{in} > V$, MSB = 1 (on)

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625



SAR Implementation

- SAR implementation mainly differ on the DAC coding and implementation.
- We have already studied the two main DAC structures used in SAR

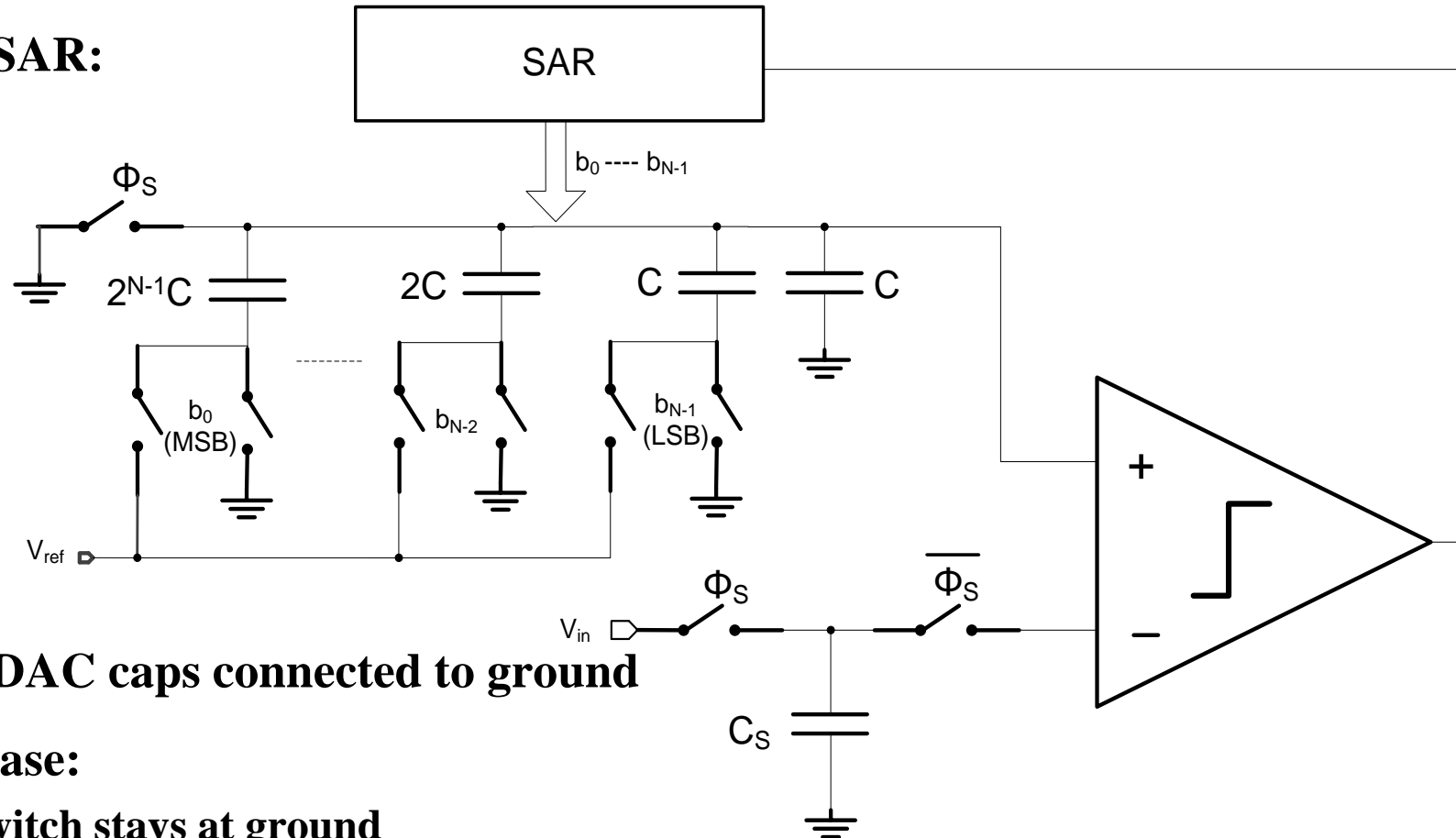


- **Resistive \rightarrow R-2R**
 - Consumes static power
 - Requires additional S&H for sampling because cannot sample at a resistor
- **Capacitive \rightarrow Charge redistribution**
 - Only Dynamic power consumption
 - Capacitor may function as Sample and hold
 - Usually binary weighted DAC, but also thermometer or C-2C are possible



SAR Implementation – Charge Redistribution

- Binary weighted DAC
- The S&H may or may not be included in the DAC.
- Separate S&H SAR:

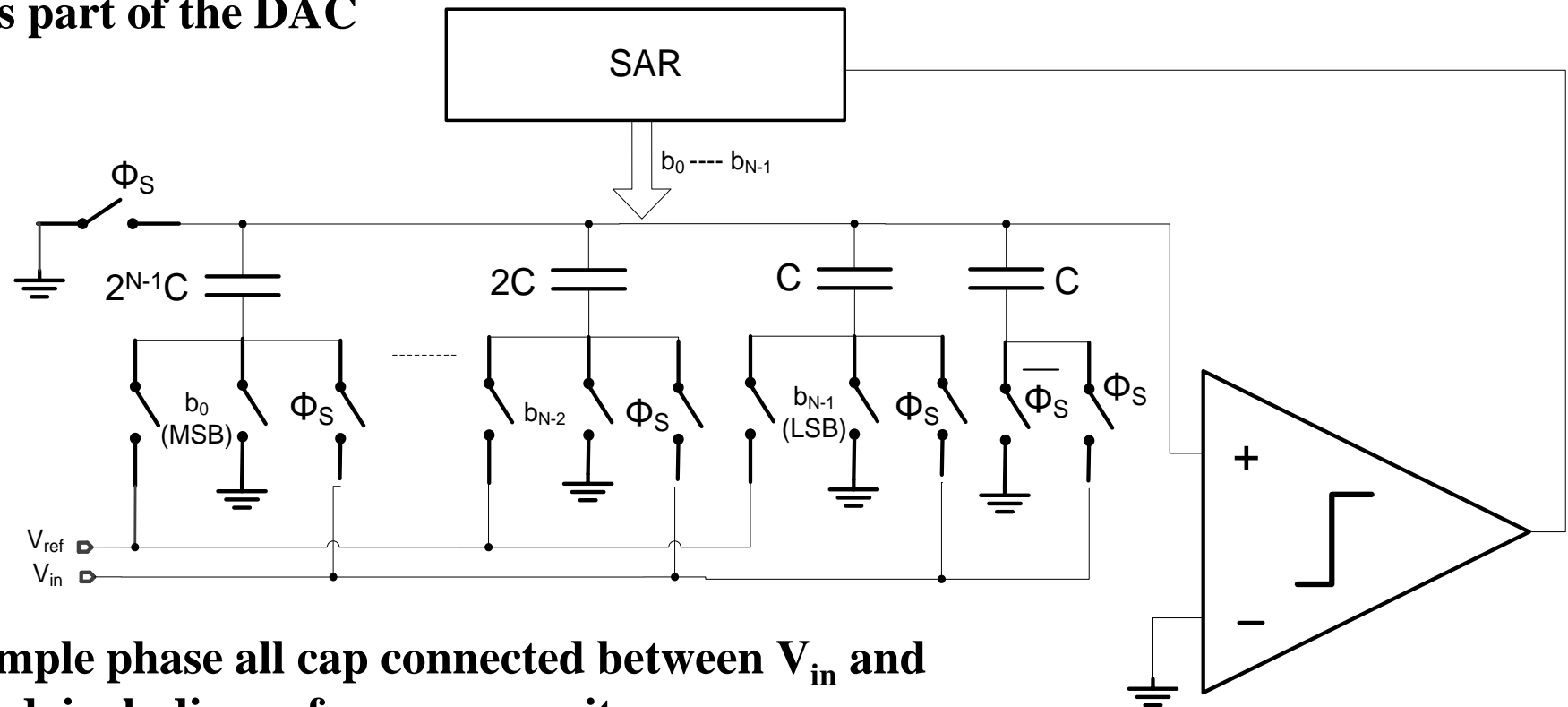


- Sample phase: DAC caps connected to ground
- Comparison phase:
 - $B=0 \rightarrow$ the switch stays at ground
 - $B=1 \rightarrow$ the switch connects to V_{ref}



SAR Implementation – Charge Redistribution

- S&H as part of the DAC



- At sample phase all cap connected between V_{in} and ground, including reference capacitor.
- Comparison phase
 - $B=0 \rightarrow$ the switch connects to ground
 - $B=1 \rightarrow$ the switch connects to V_{ref}



SAR Implementation – Charge Redistribution

S&H and DAC implemented separately

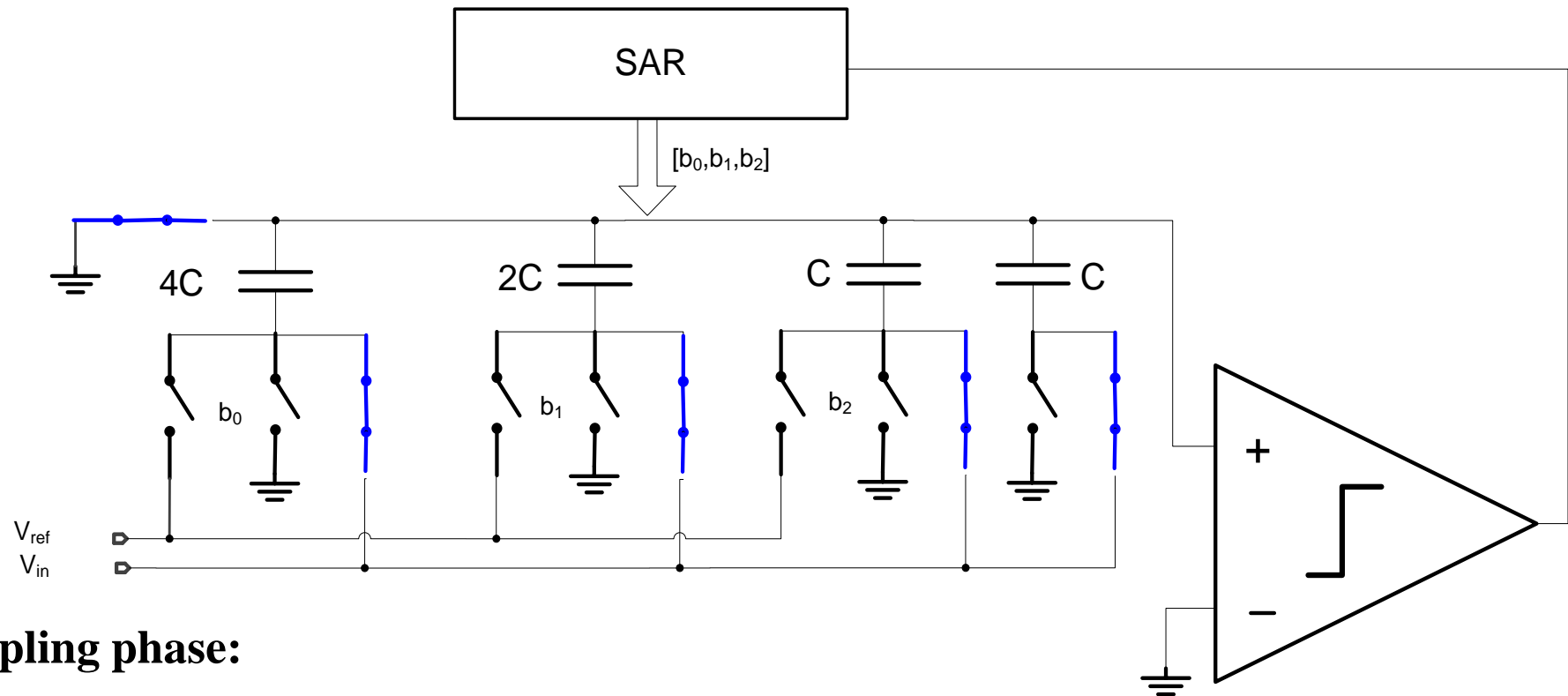
- + S&H can be optimized for noise, charge injection, clock-feedthrough
- + Easy to implement improved switch techniques like bottom-plate or bootstrap
- + V_{in} load is C_s which is not related to the DAC
- Larger area: requires both DAC caps and C_s
- Comparator common depends upon signal

Sampling at DAC caps

- + Compact solution, S&H and DAC shares the same array
- + Comparator operates at constant zero cross
- More difficult to optimize for clock feedthrough or charge injection
- Bottom-plate difficult to implement
- If bootstrapped, large number of switches
- V_{in} load is the DAC caps array



SAR Implementation example: 3 bit - Sampling

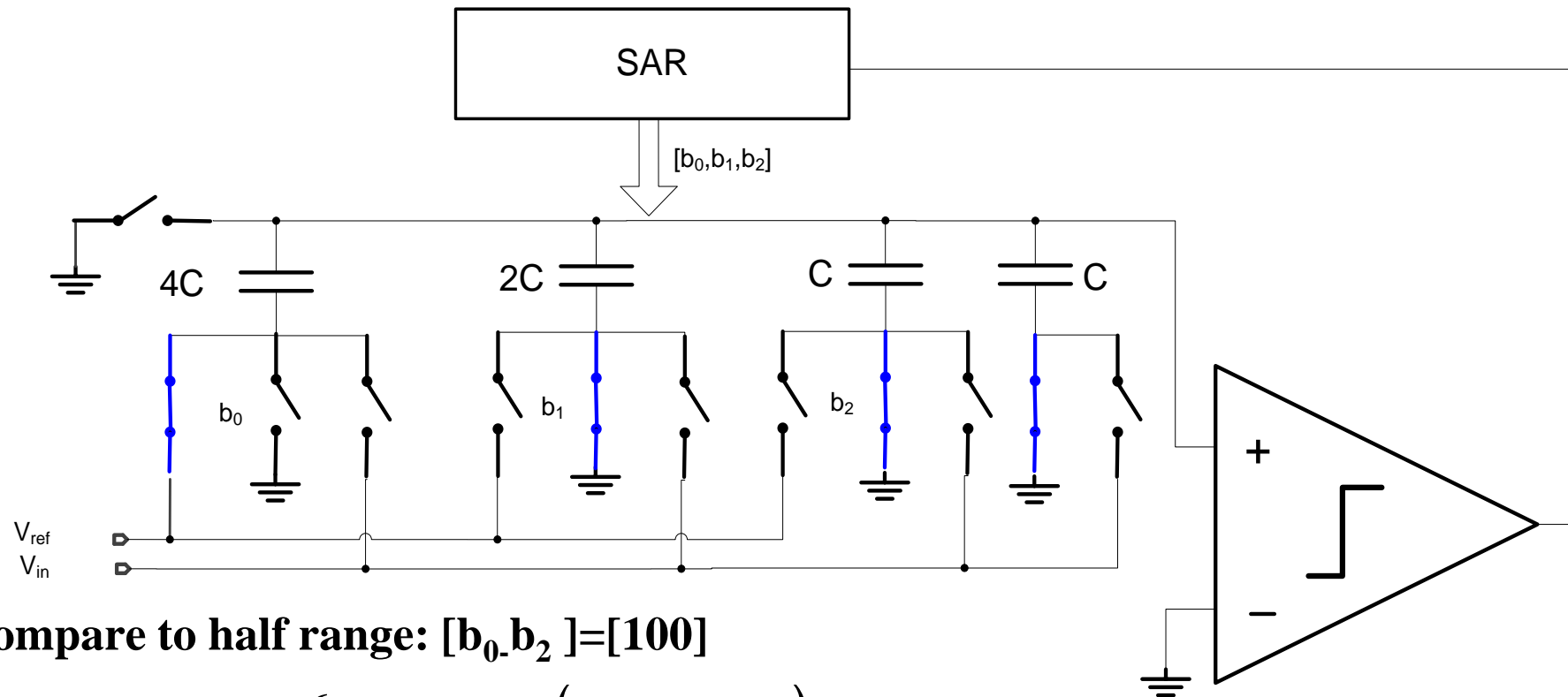


Sampling phase:

- All capacitors connected between V_{in} and ground
- Total charge is $Q_{tot} = 8CV_{in}$
- The total charge remains unchanged during the full conversion process



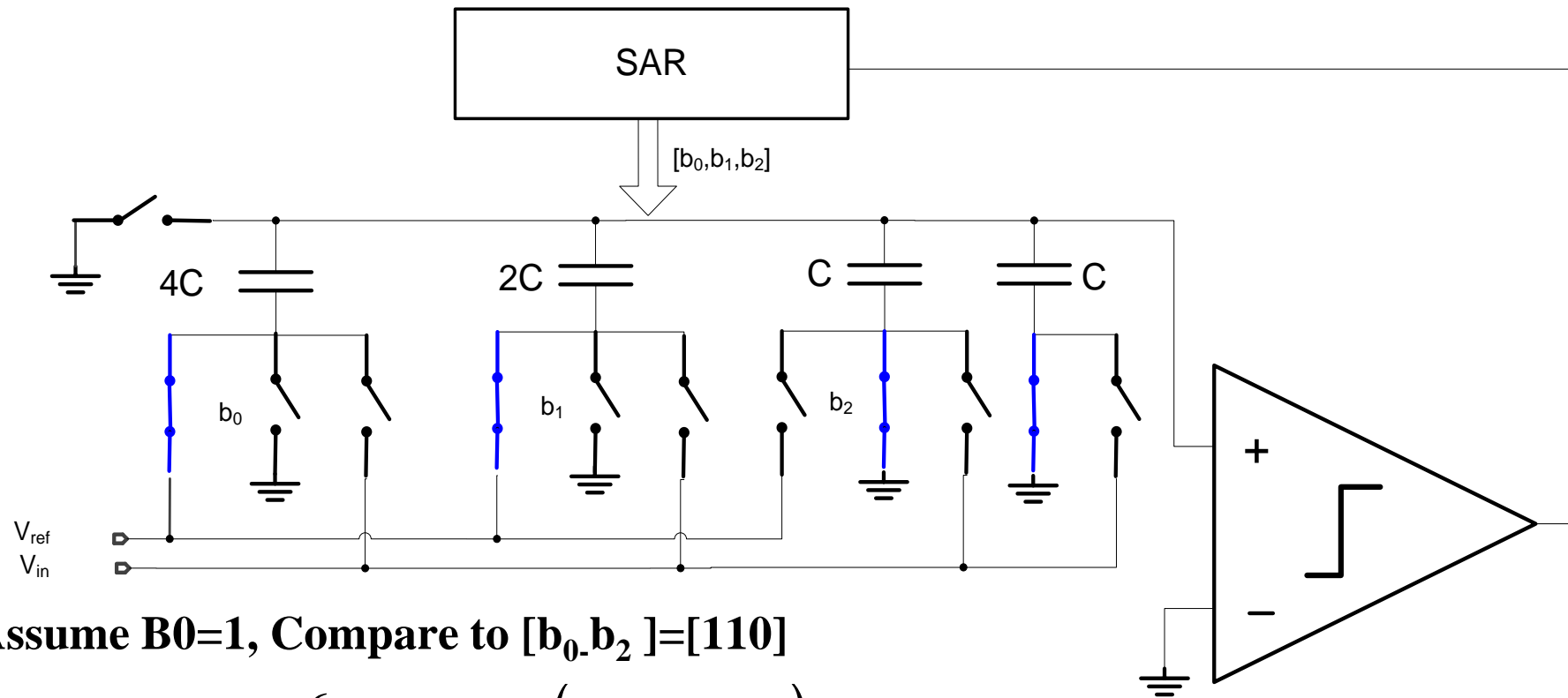
SAR Implementation example: 3 bit – B0 (MSB)



- Compare to half range: $[b_0.b_2] = [100]$
- Comparison
$$\begin{cases} Q_{tot} = 4C(V_{Ref} - V_+) - 4CV_+ \\ Q_{tot} = 8CV_{in} \end{cases} \Rightarrow V_+ = \frac{V_{Ref}}{2} - V_{in}$$
- If comparison < 0 B0=0 and b_0 is inverted, otherwise B0=1 and b_0 unchanged



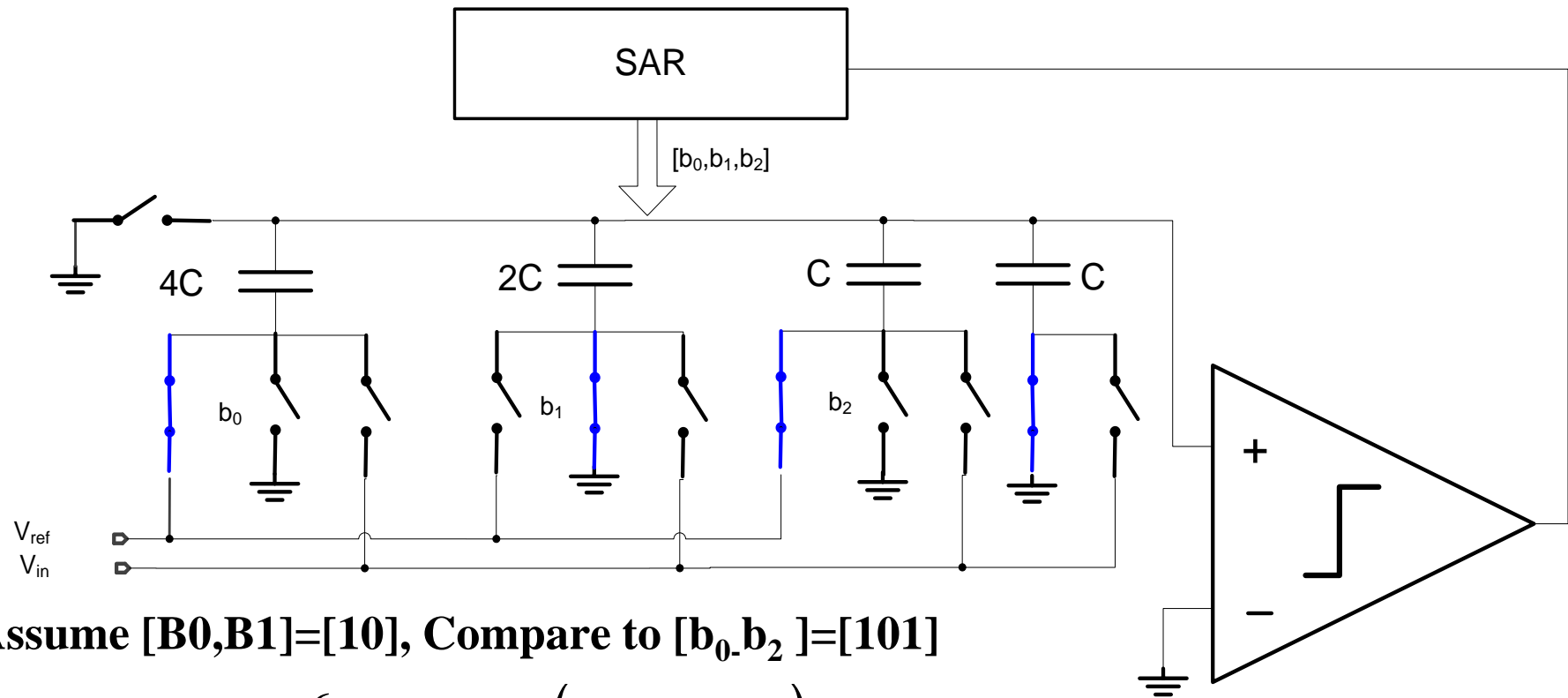
SAR Implementation example: 3 bit – B1



- Assume B0=1, Compare to $[b_0, b_2] = [110]$
- Comparison
$$\begin{cases} Q_{tot} = 6C(V_{Ref} - V_+) - 2CV_+ \\ Q_{tot} = 8CV_{in} \end{cases} \Rightarrow V_+ = \frac{3}{4}V_{Ref} - V_{in}$$
- If comparison < 0 B1=0 and b_1 is inverted, otherwise B1=1 and no change



SAR Implementation example: 3 bit – B2

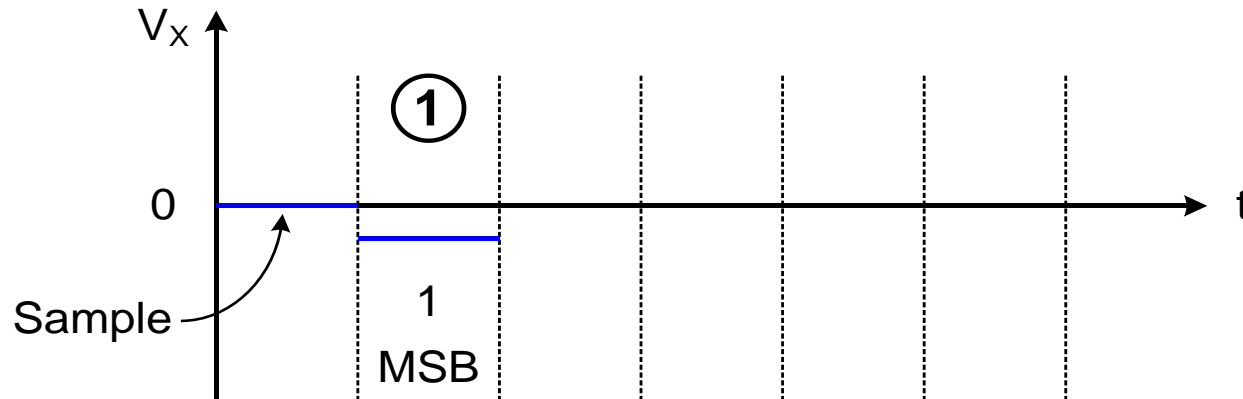


- Assume $[B_0, B_1] = [10]$, Compare to $[b_0, b_2] = [101]$
- Comparison
$$\begin{cases} Q_{tot} = 5C(V_{Ref} - V_+) - 3CV_+ \\ Q_{tot} = 8CV_{in} \end{cases} \Rightarrow V_+ = \frac{5}{8}V_{Ref} - V_{in}$$
- If comparison < 0 $B_1 = 0$ and b_1 is inverted, otherwise $B_1 = 1$ and no change

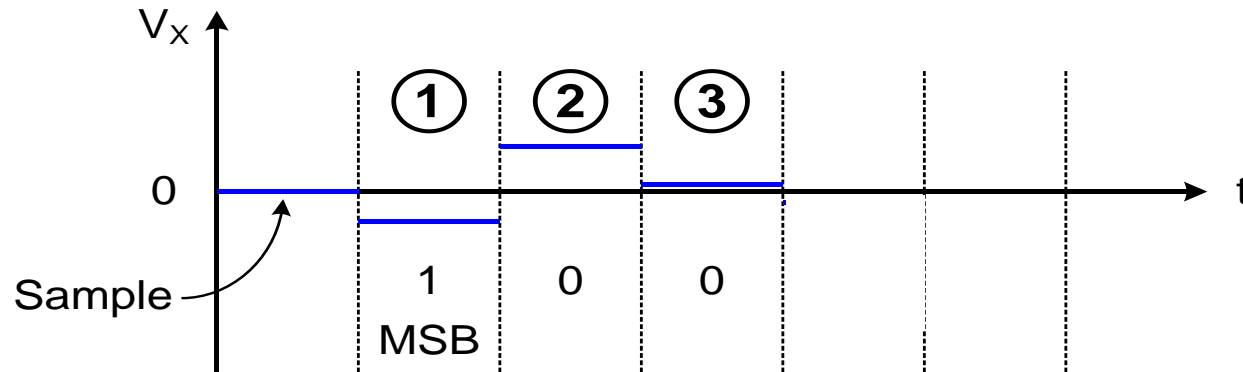


Conversion time

After two clock cycles



After 4 clock cycles



Sampling: Does not need to be single clock – Usually 2-3 clocks

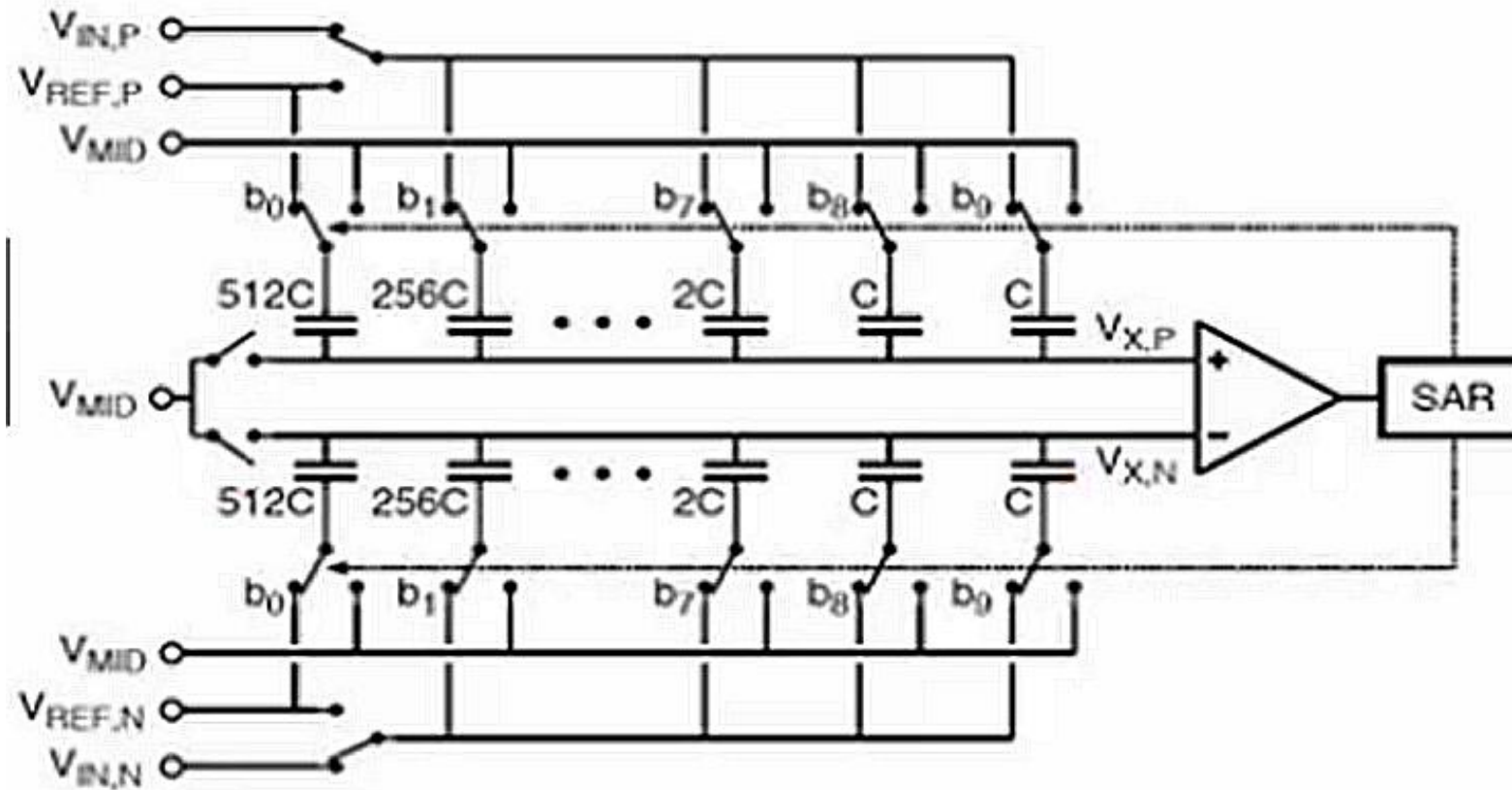
Comparison: Number of cycles equals the number of bits

$$T_{conv} = T_{samp} + N_B \cdot T_{clk} = (N_{samp} + N_B) \cdot T_{clk}$$



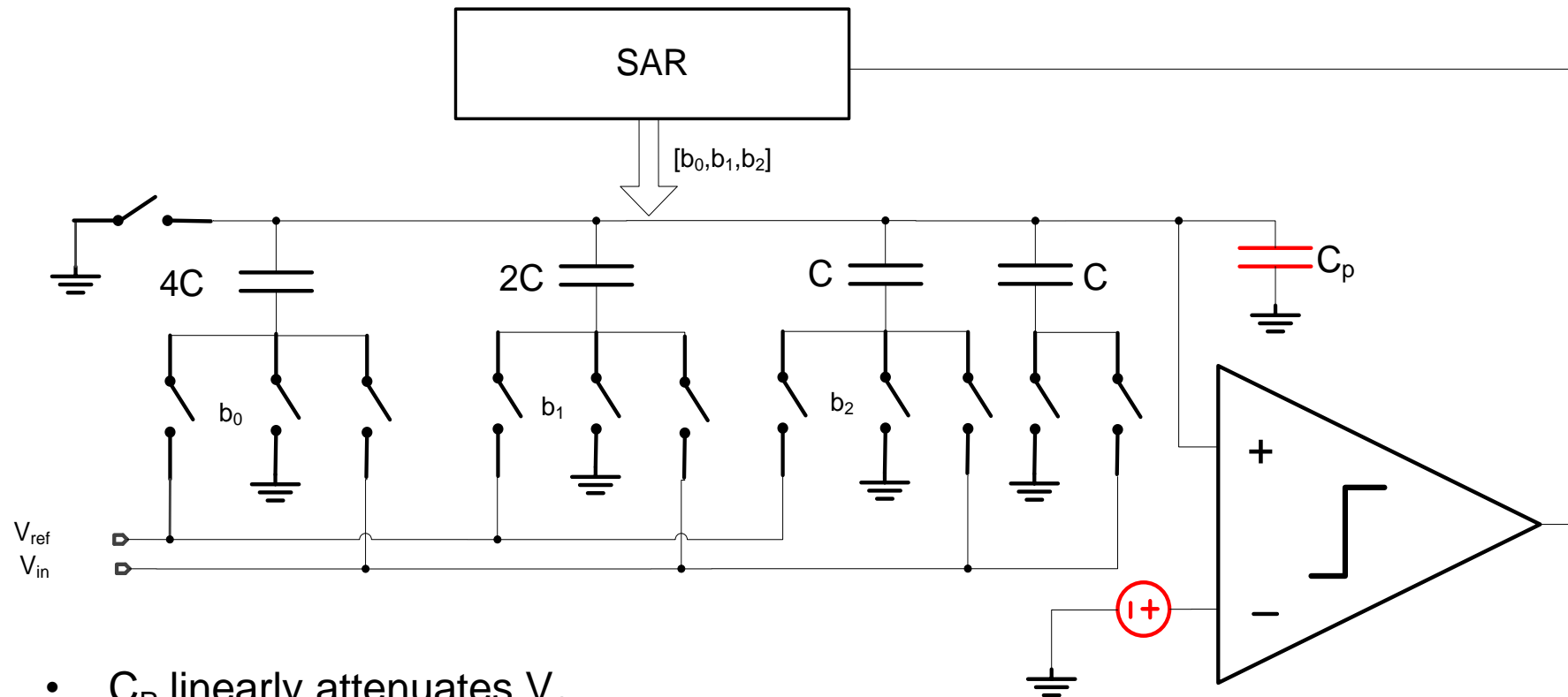
SAR Implementation: Ch. Redistribution – Fully Differential

- An additional advantage of the shared SAR is that it can be turned to fully differential \rightarrow double dynamic range





SAR parasitic capacitance and offset



- C_p linearly attenuates V_+
- In order to reduce C_p , the bottom plate of the capacitor is usually at V_{in}
- With V_{os} the comparator does not compares to zero \rightarrow requires calibration
- Alternatively, auto-zeroing can be applied to the comparator to reduce offset



SAR parasitic capacitance effect

- Without parasitic capacitance any X conversion follows the equation:

$$NCV_{in} = (N - X)C(V_{Ref} - V_{+}) - XCV_{+}$$

$$NCV_{in} = NCV_{ref} - XCV_{ref} - NCV_{+}$$

$$V_{+} = \frac{N - X}{N} V_{ref} - V_{in}$$

N : Number of Bits

X : Bits that set in a given conversion

- With parasitic capacitance:

$$NCV_{in} = (N - X)C(V_{Ref} - V_{+}) - X(C + C_p)V_{+}$$

$$NCV_{in} = NCV_{ref} - XCV_{ref} - N(C + C_p)V_{+}$$

$$V_{+} = \left(\frac{N - X}{N} V_{ref} - V_{in} \right) / \left(1 - \frac{X}{N} \frac{C_p}{C} \right)$$



Speed limit and solutions

- **Conversion rate typically limited by finite bandwidth of RC network during sampling and bit-tests**
- **For high resolution, the binary weighted capacitor array can become quite large**
 - **E.g. 16-bit resolution, $C_{\text{total}} \sim 100\text{pF}$ for reasonable kT/C noise contribution**
- **If matching is an issue, an even larger value may be needed**
 - **E.g. if matching dictates $C_{\text{min}} = 10\text{fF}$, then $2^{16}C_{\text{min}} = 655\text{pF}$**
- **Commonly used techniques**
 - **Implement "two-stage" or "multi-stage" capacitor network to reduce array size [Yee, JSSC 8/79]**
 - **Calibrate capacitor array to obtain precision beyond raw technology matching [Lee, JSSC 12/84]**
 - **Go down to the parasitic limit to reduce capacitor size**

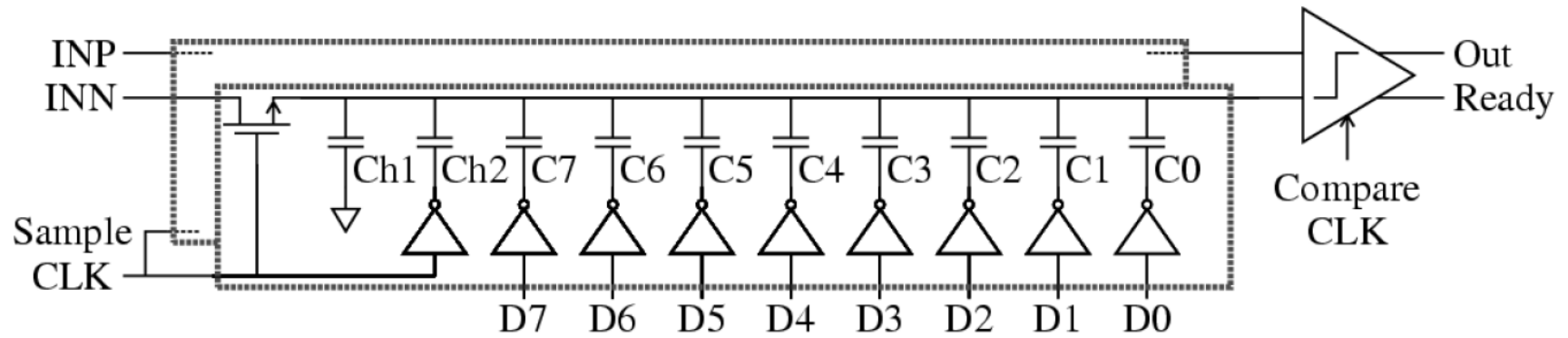


Parallel Structures

- **Due to the low power requirement and the digital circuitry advances SARs have made a “come-back” in latest years, particularly, there is large development in the communication area**
- **As each SAR uses relatively small area and number of elements paralleling the structure results in an efficient solution**
- **Many implementations are based on paralleling several ADCs**
 1. **Sub-ranging:**
 - **Divide the input range in sub-ranges**
 - **Use several low-resolution ADC for each sub-range and combine the output bits.**
 - **Not very efficient due to common differences, and mismatch**
 2. **Time Interleaving:**
 - **Use multiple samples intercalated in time, converting each time with low resolution**
 - **Very attractive solution compete with pipeline ADC**

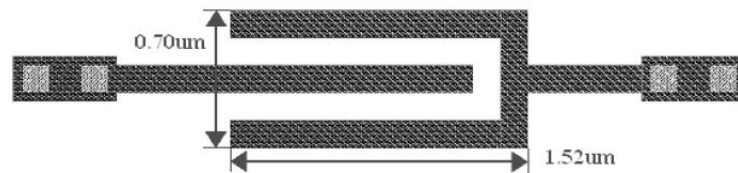


Architecture Examples



(a)

1fF unit element

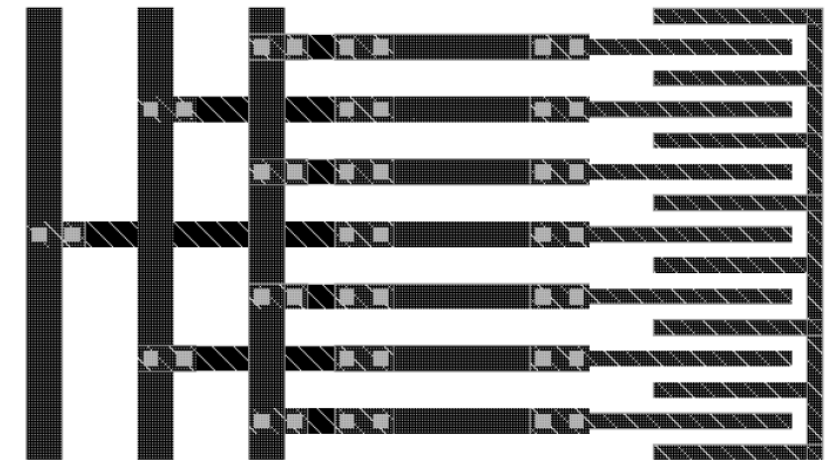


(b)

ISSCC 2010 / SESSION 21 / SUCCESSIVE-APPROXIMATION

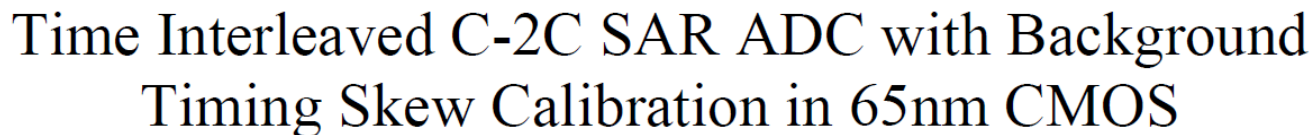
21.6 A 30fJ/Conversion-Step 8b 0-to-10MS/s
Asynchronous SAR ADC in 90nm CMOS

Pieter Harpe, Cui Zhou, Xiaoyan Wang, Guido Dolmans,
Harmke de Groot



1fF 2fF 4fF

(c)



European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014 - 40th, 2014



Architecture Examples

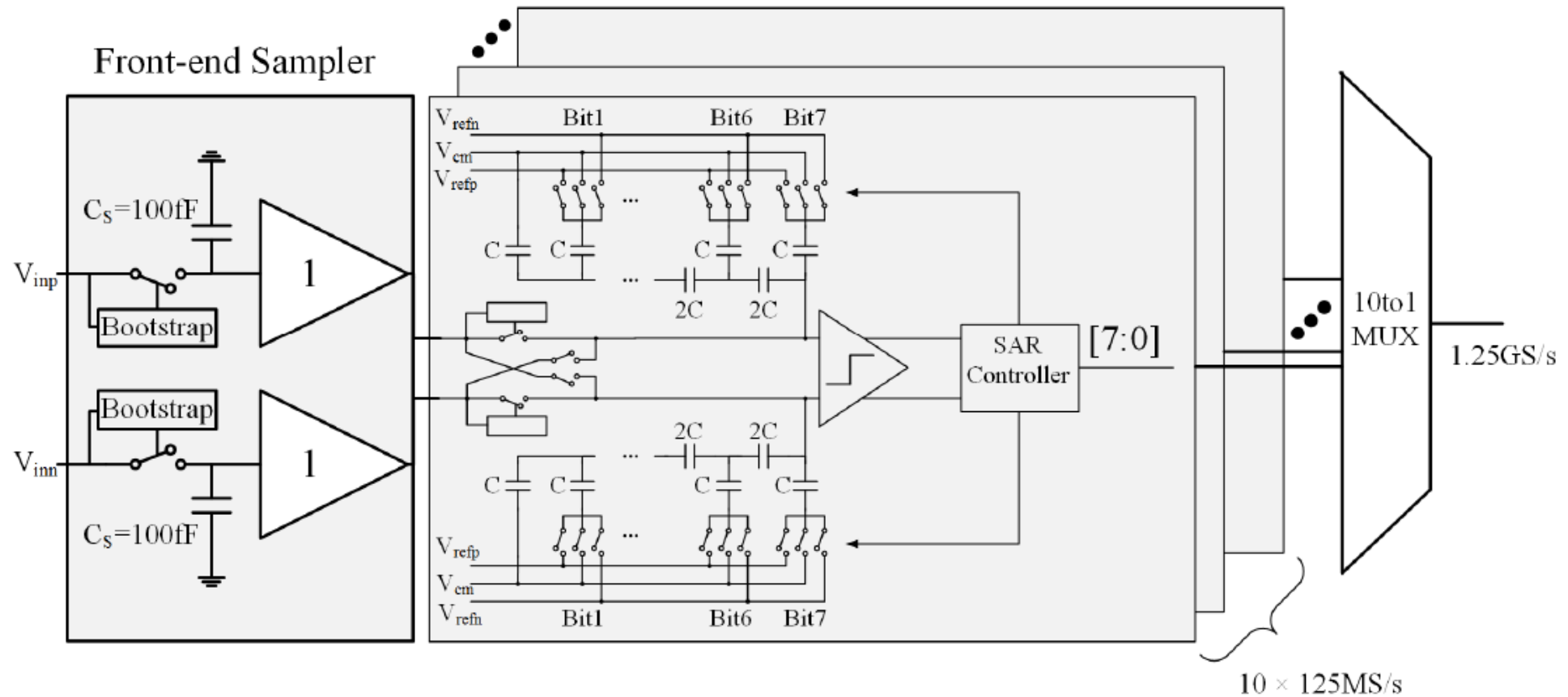
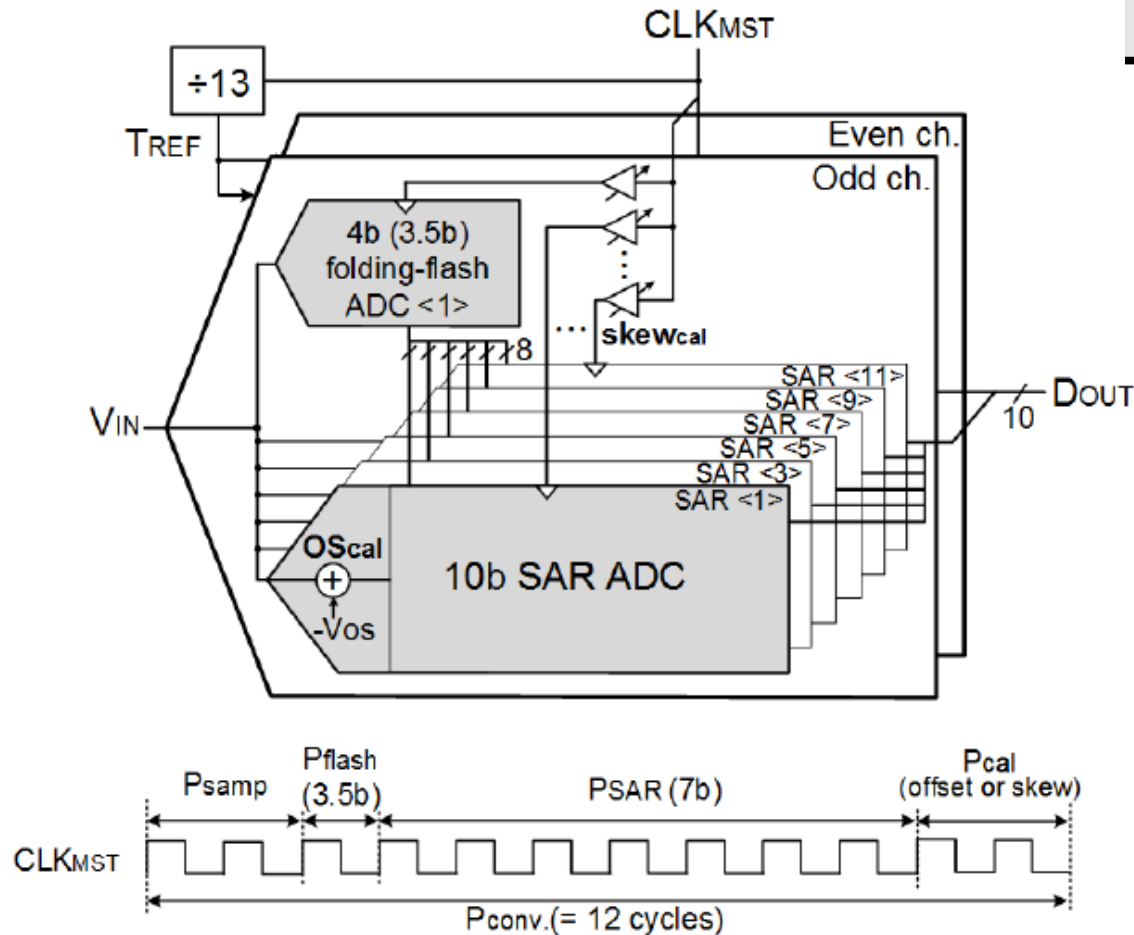


Fig. 1: 1.25GS/s 8-bit C-2C SAR sub-ADC block diagram



Architecture Examples

ISSCC 2015 / SESSION 26 / NYQUIST-RATE CONV



26.4 A 21fJ/conv-step 9 ENOB 1.6GS/s 2× Time-Interleaved FATI SAR ADC with Background Offset and Timing-Skew Calibration in 45nm CMOS

Ba-Ro-Saim Sung¹, Dong-Shin Jo¹, Il-Hoon Jang¹, Dong-Suk Lee², Yong-Sang You², Yong-Hee Lee², Ho-Jin Park², Seung-Tak Ryu¹

- **FATI: Flash-Assisted Time Interleaving**
 - Flash determines the first 4 (3.5) MSB
 - Time Interleaved SAR used to determine the remaining 7 LSB

Figure 26.4.1: Block diagram of the 2× time-interleaved 10b FATI SAR ADC and timing diagram of a single-channel 10b SAR ADC.



Architecture Examples

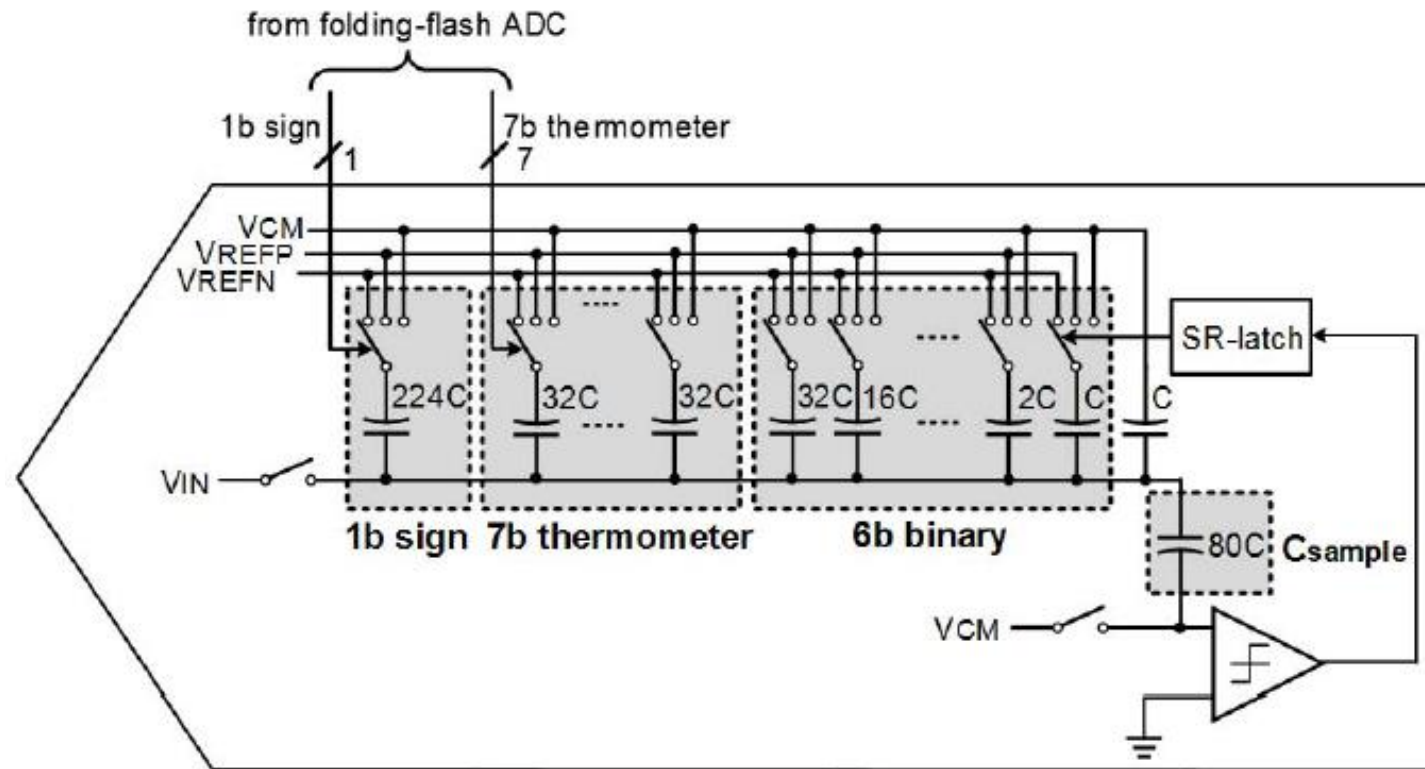


Figure 26.4.2: Single-channel 10b SAR ADC with a designated sampling capacitor (C_{sample}).