Investigation of a Class-J Power Amplifier with a Nonlinear $C_{\rm out}$ for Optimized Operation

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***Abstract*—This paper presents the operation principle of Class-J power amplifiers (PAs) with linear and nonlinear output capacitors ($C_{\rm out}$s). The efficiency of a Class-J amplifier is enhanced by the nonlinear capacitance because of the harmonic generation from the nonlinear $C_{\rm out}$, especially the second-harmonic voltage component. This harmonic voltage allows the reduction of the phase difference between the fundamental voltage and current components from 45° to less than 45° while maintaining a half-sinusoidal shape. Therefore, a Class-J amplifier with the nonlinear $C_{\rm out}$ can deliver larger output power and higher efficiency than with a linear $C_{\rm out}$. As a further optimized structure of the Class-J amplifier, the saturated PA, a recently-reported amplifier in our group, is presented. The phase difference of the proposed PA is zero. Like the Class-J amplifier, the PA uses a nonlinear $C_{\rm out}$ to shape the voltage waveform with a purely resistive fundamental load impedance at the current source, which enhances the output power and efficiency. The PA is favorably compared to the Class-J amplifier in terms of the waveform, load impedance, output power, and efficiency. These operations are described using both the ideal and real models of the transistor in Agilent Advanced Design System. A highly efficient amplifier based on the saturated PA is designed by using a Cree GaN HEMT CGH40010 device at 2.14 GHz. It provides a power-added efficiency of 77.3% at a saturated power of 40.6 dBm (11.5 W).**

***Index Terms*—Class-J, saturated amplifier, efficiency, nonlinear output capacitor, power amplifier.**

I. Introduction

HIGHLY efficient power amplifiers (PAs) are an essential RF component for wireless communication systems to achieve small, reliable, and low cost transmitters [1]– [3]. To date, a lot of topologies have been proposed to provide highly efficient operation. Among the various PAs, the Class-F delivers a good efficiency by controlling the odd-harmonic impedances to make a rectangular voltage waveform [3]– [6]. However, to get the proper third-harmonic voltage, the output capacitor ($C_{\rm out}$) should be accurately tuned out. Moreover, depending on the capacitance and the operating frequency, in some cases, the impedance of the capacitance might be a short-circuit for the third-harmonic frequency. Class-E amplifier provides excellent efficiency by acting as a ideal switch [7], [8]. However, the actual ideal switching operation of the power transistor might or might not be possible depending on the operating frequency and the power transistor. In addition, the high order frequency components of the drain voltage may be shorted and the switching time may not be negligible, making the zero-voltage switching and zero voltage derivative switching difficult. Such limitations degrade the efficiency of the Class-E PA at high frequency.

In 2006 [3] and 2009 [9], S. C. Cripps proposed Class-J amplifier that provides the same efficiency and linearity as Class-AB or Class-B amplifiers across a broad frequency range due to absence of the resonant impedance condition, such as short-circuit or open-circuit. The Class-J PA increases the fundamental voltage component assisted by the second-harmonic voltage by employing a capacitive harmonic load [10]– [12]. However, a complex load impedance at the fundamental frequency is required to shape the voltage waveform. As a result, the performance of the Class-J PA is degraded due to the phase mismatch, making it comparable to that of a harmonic tuned linear PA, such as a Class-AB or a Class-B, but the reported Class-J PA provides better efficiency than the theoretical expectation [13]– [15].

The highly efficient PAs have been extensively analyzed in the past, but most of these analyses have been carried out under the assumption of a linear $C_{\rm out}$ [3]– [15]. However, the $C_{\rm out}$ presents a heavily nonlinear behavior at the low voltage across the capacitor [16], [17], resulting in unexpected operation and the abstrusity of the analyses. Although some researchers have made an effort to describe PA operations accounting the nonlinear capacitor [18]– [23], they only focused on the class-E topology at low frequencies, below 400 MHz.

In this paper, the harmonic-generation property of the transistor's nonlinear $C_{\rm out}$ is explored, and the behaviors of the PAs with the linear and nonlinear $C_{\rm out}$ are investigated. Especially, Class-J amplifiers, which use the output capacitors as a second harmonic load, are further analyzed in terms of the time-domain voltage and current waveforms, load-lines, load impedances, and continuous wave (CW) performances. The Class-J amplifiers are compared with a saturated power amplifier, and it is shown that the amplifier is an optimized version of the Class-J PA to obtain better efficiency and output power. In [24] and [25], we explained the operation of the saturated PA. It uses the nonlinear $C_{\rm out}$ as a harmonic load, which is the same of the Class-J amplifier, and a purely resistive fundamental load, which is different from the Class-J PA. The resistive fundamental load impedance increases the power factor, resulting in better efficiency and output power than those of the Class-J amplifier.

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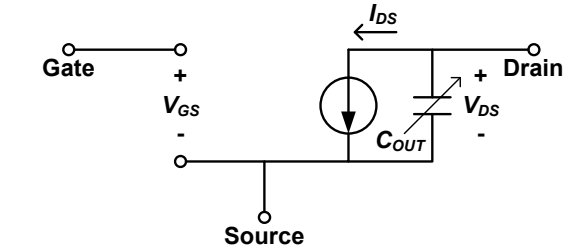

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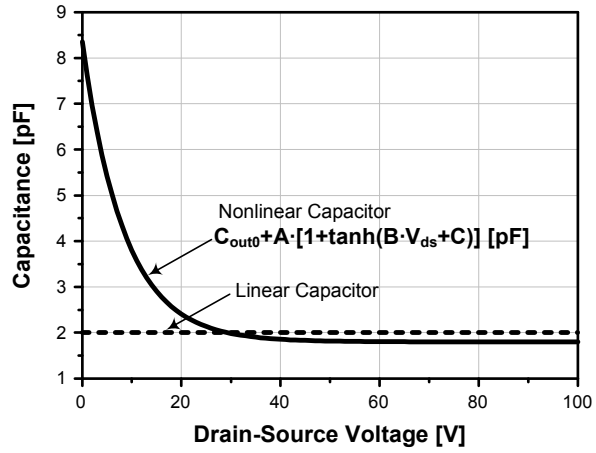

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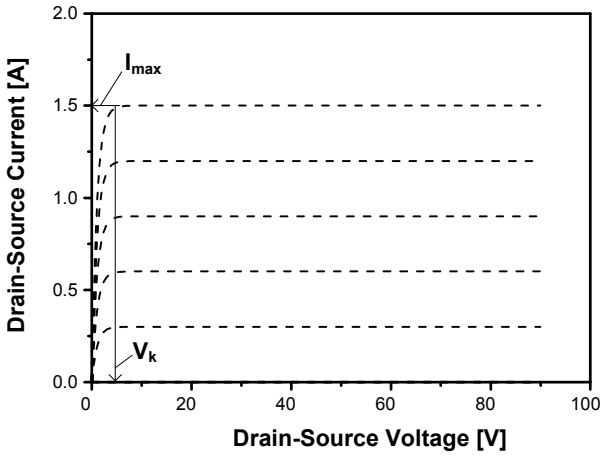


(c)

Fig. 1. (a) Simplified transistor equivalent circuit model. (b) Capacitances for the linear and nonlinear $C_{\rm out}$s. (c) DC-IV characteristic.

II. Analysis for Operation Characteristics of a Class-J Amplifier

A. Ideal Transistor Model for Simulations

To analyze the fundamental behaviors of the PAs, we have constructed a simplified transistor equivalent circuit model in the Agilent Advanced Design System (ADS) using the symbolically defined device, as shown in Fig. 1(a). To simplify the analysis, the transistor model contains two essential nonlinear parts: $C_{\rm out}$ and the drain current source. $C_{\rm out}$ represents all nonlinear capacitors of the transistor output, including the drain-source capacitor $C_{\rm ds}$ and gate-drain capacitor $C_{\rm gd}$. Even though $C_{\rm ds}$ and $C_{\rm gd}$ are modulated according to both the drain-source and the gate-source voltages, we assume only a dependence on the drain-source voltage in this model. Thus, $C_{\rm out}$ is given by

$$C_{\rm out}\left(V_{\rm ds}\right) = C_{\rm out0} + A\cdot\left[1+\tanh\left(B\cdot V_{\rm ds}+C\right)\right]\ \ [\rm pF]\,, \quad (1)$$

where $C_{\rm out0}$, A, B, and C are summarized in Table I. Fig. 1(b) illustrates the characteristic of the nonlinear $C_{\rm out}$ according to the drain-source voltage. The capacitance increases dramatically as the drain-source voltage becomes small. The drain-source current is given by

$$I_{\rm ds}\left(V_{\rm gs},V_{\rm ds}\right) = \begin{cases} 0, & V_{\rm gs}\le 0 \\ g_{\rm m}V_{\rm gs}\left(1-\exp\left(-\dfrac{V_{\rm ds}}{V_{\rm t}}\right)\right), & 0<V_{\rm gs}\le V_{\rm gs,max} \\ g_{\rm m}V_{\rm gs,max}\left(1-\exp\left(-\dfrac{V_{\rm ds}}{V_{\rm t}}\right)\right), & V_{\rm gs}\ge V_{\rm gs,max} \end{cases},$$

where $g_{\rm m}$ is the trans-conductance, and $V_{\rm gs,max}$ is the gate-source voltage when $I_{\rm ds}$ is equal to $I_{\rm max}$. For simplicity, we assume the pinch-off voltage is zero. As depicted in Fig. 1(c), the transistor model exhibits strongly nonlinear effects of cutoff and saturation. In the intermediate region between the cutoff and saturation, the transistor provides a highly linear operation. In particular, $g_{\rm m}$ and $I_{\rm max}$ are set to 1 S and 1.5 A, respectively, in this model, and $V_{\rm k}$ is about 4 V. These parameters are based on the model of the Cree GaN HEMT CGH60015 used for the implementation. It is well known that the input nonlinear capacitor $C_{\rm gs}$ has nonlinear characteristic, which results in the generation of harmonic components [10]–[12], [26], [27]. However, compared with the output nonlinear capacitor, $C_{\rm gs}$ has a minor effect on the performance, as will be described in Section III, so the effect of $C_{\rm gs}$ nonlinearity is eliminated in this model.

TABLE I
Summarized Parameters for Output Capacitor $C_{\rm out}$

$C_{\rm out0}$	A	B	C
1.9	1192.4	–0.0594714	–2.94696

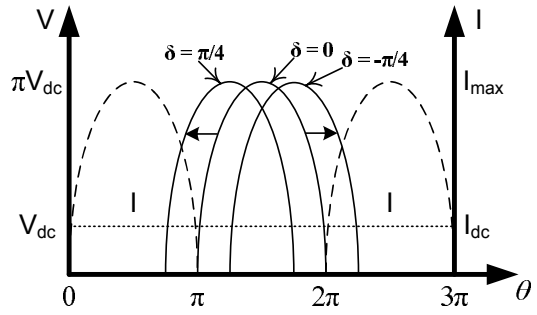
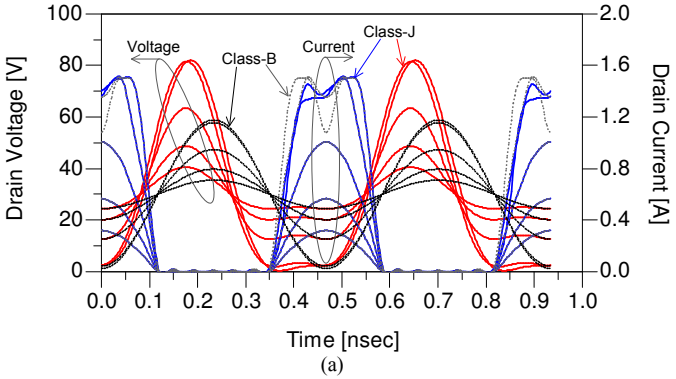


Fig. 2. Half-sinusoidal voltage and current waveforms for the various phase differences (In particular, $\delta = \pi/4$ represents the Class-J PA).

B. Class-J Amplifier with Linear Output Capacitor

First, we review the operation of Class-J amplifier with linear $C_{\rm out}$. Linear $C_{\rm out}$ refers to a constant capacitance, as shown in Fig. 1(b). Class-J amplifier can be characterized by



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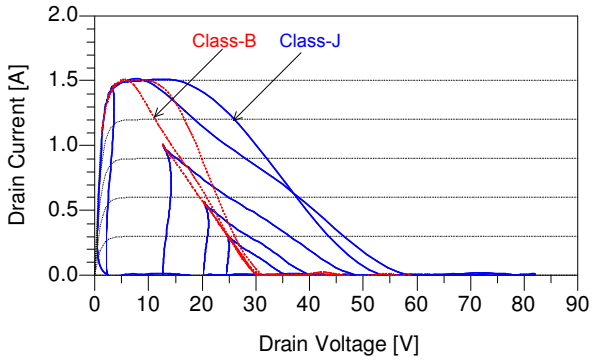


(b)

Fig. 3. Simulated (a) time-domain voltage and current waveforms and (b) load-lines for Class-B and Class-J amplifiers with linear $C_{\rm out}$.

half-sinusoidal voltage and current waveforms with a phase shift between them, as depicted in Fig. 2. These waveforms can be expressed by

$$I(\theta) = I_{\max} \cdot \left(\frac{1}{\pi} + \frac{1}{2}\sin\theta - \frac{2}{3\pi}\cos 2\theta - \cdots \right) \quad (2)$$

$$V(\theta) = \pi V_{\rm dc} \cdot \left(\frac{1}{\pi} - \frac{1}{2}\sin(\theta+\delta) - \frac{2}{3\pi}\cos(2(\theta+\delta)) - \cdots \right), \quad (3)$$

where δ is a phase difference between the voltage and current from the normal 180°. Thus, the load impedances of each harmonic frequencies can be calculated by

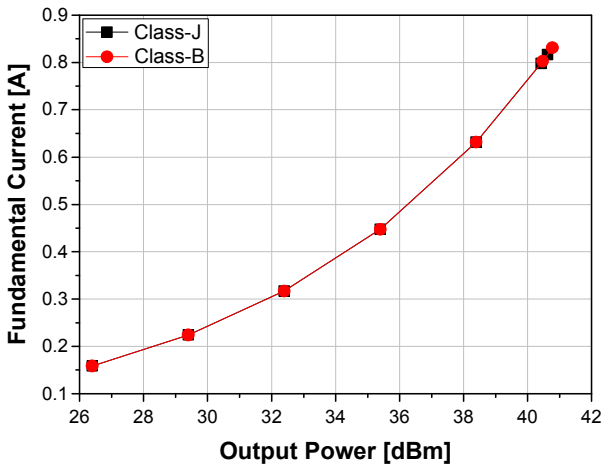
$$Z_{\rm n} = -\frac{V_{\rm n}}{I_{\rm n}}, \quad (4)$$

where n denotes the $n^{\rm th}$ frequency component. For $I_{\max} = 1$ and $V_{\rm dc} = 1/\pi$, the fundamental and second-harmonic loads are given by

$$Z_1 = 1\angle\delta, \quad Z_2 = 1\angle(2\delta - \pi) \quad (5)$$

For Class-J amplifier, δ is $\pi/4$ because the second harmonic loading is made by the capacitive component. Thus, to shape the half-sinusoidal voltage waveform, the fundamental load impedance is set to $1\angle(\pi/4)$. This leads to the degradation of the output power by a factor of $\cos(\pi/4)$.

The operation of the Class-J PA is further investigated by using the model described in Section II-A. Since the Class-J operation biased at the Class-B condition is assumed in this



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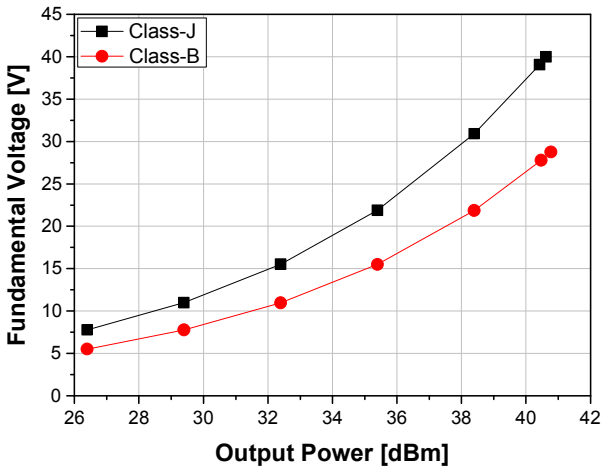


(b)

Fig. 4. Fundamental (a) current and (b) voltage components for the Class-B and Class-J amplifiers with the linear $C_{\rm out}$.

work, the Class-B amplifier is also simulated for comparison purpose. For the Class-B design, the optimum fundamental load impedance is chosen to obtain the maximum output power.

$$R_{\rm opt} = \frac{V_{\rm dc} - V_{\rm k}}{I_{\max}/2}. \quad (6)$$

In the simulation, $V_{\rm dc}$ is set to 30 V, so $R_{\rm opt}$ is chosen to be 34.6 Ω.

For the Class-J amplifier, the voltage waveform is half-sinusoidal. It consists of all even harmonic voltage components. However, the voltage components at the higher-order frequencies are assumed to be zero because of the device's large output capacitor. We believe that, in the real design environment, the half-sinusoidal voltage waveform is mainly made up the DC, fundamental, and second-harmonic voltage components. Among the various half-sinusoidal voltage waveforms manipulated by up to second-harmonic component, the "maximum-voltage gain" condition is assumed in this study [10]– [12]. Accordingly, the magnitude of the fundamental load impedance should be set to $\sqrt{2}R_{\rm opt}$ because the maximum value of the fundamental voltage extracted from

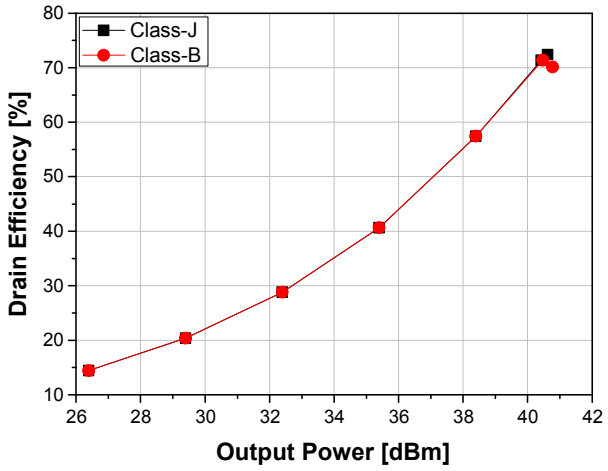


Fig. 5. Simulated efficiencies of the Class-B and Class-J amplifiers with the linear $C_{\rm out}$.

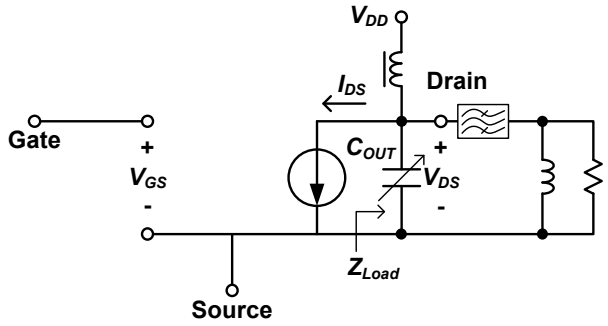


Fig. 6. Simulation setup to investigate the behavior of the amplifiers and the harmonic-generation property of the nonlinear $C_{\rm out}$.

the half-sinusoidal waveform is increased by a factor of $\sqrt{2}$ above that of Class-B amplifier. In addition, to properly shape the half-sinusoidal voltage waveform, the appropriate amount of the second-harmonic voltage is required. In particular, the "maximum-voltage gain" condition can be achieved when the ratio of the second-harmonic to the fundamental voltage is $-\sqrt{2}/4$. Thus, assuming the ideal half-sinusoidal current having the fundamental current of $I_{\max}/2$ and the second-harmonic current of $2I_{\max}/3\pi$, the required second-harmonic load impedance is given by

$$|Z_2| = \frac{3\pi}{8} R_{\rm opt}. \tag{7}$$

Consequently, the load condition for Class-J amplifier is represented by

$$Z_1 = \sqrt{2}R_{\rm opt}\angle 45^\circ, \quad Z_2 = \frac{3\pi}{8} R_{\rm opt}\angle -90^\circ. \tag{8}$$

In the simulation of the Class-J amplifier, the fundamental and second-harmonic load impedances are selected to be $34.6 + j34.6\ \Omega$ and $-j40.768\ \Omega$, respectively.

C. Class-J Amplifier with Nonlinear Output Capacitor

Fig. 3 depicts the simulated time-domain voltage and current waveforms and load-lines for the designed Class-J and Class-B amplifiers with linear $C_{\rm out}$. Because of the complex

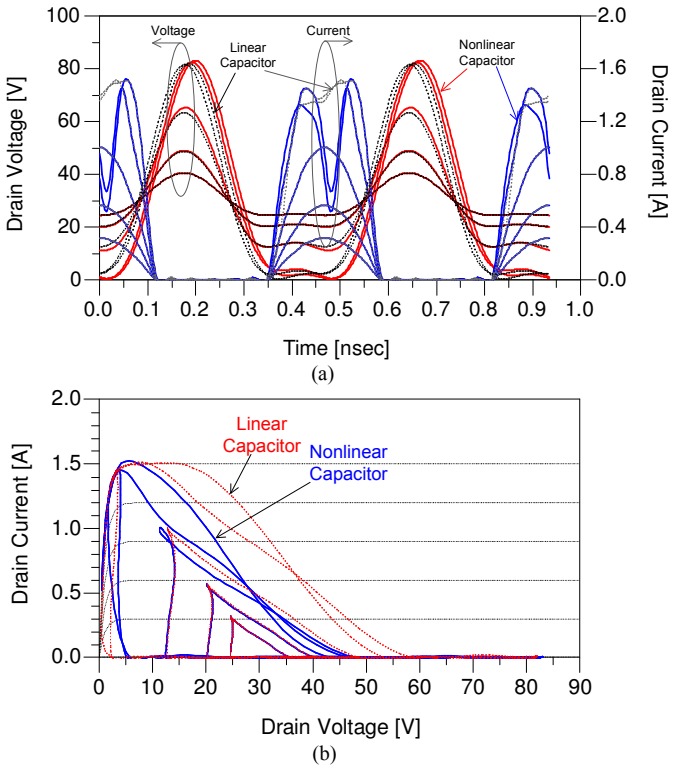


Fig. 7. Simulated (a) time-domain voltage and current waveforms and (b) load-lines for the Class-J amplifiers with the linear and nonlinear $C_{\rm out}$s.

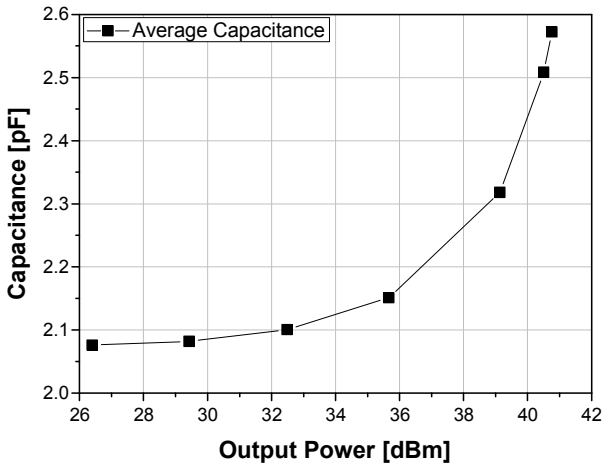


Fig. 8. Average capacitance for the Class-J with the nonlinear $C_{\rm out}$ according to the power level.

fundamental load impedance, the Class-J amplifier provides a loadline having "looping-characteristic". Fig. 4 shows the fundamental current and voltage components for the Class-B and Class-J amplifiers. In the saturated region, the fundamental current of the Class-B is slightly larger than that of the Class-J, because the Class-J has an asymmetric current waveform due to the complex fundamental load impedance, as shown in Fig. 3(a). However, the bifurcated current of the Class-B requires slightly larger DC current than the Class-J, and the efficiency of the Class-B at the highly saturated region is slightly lower than that of the Class-J amplifier, as depicted

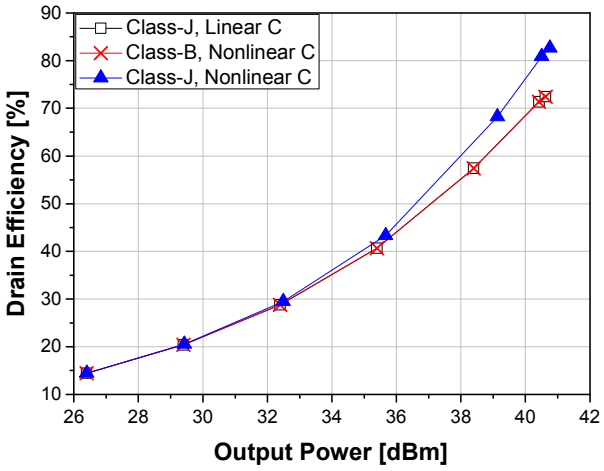


Fig. 9. Simulated efficiencies for the Class-J amplifier with a linear $C_{\rm out}$ and the Class-B and -J amplifiers with the nonlinear $C_{\rm out}$ according to the power level.

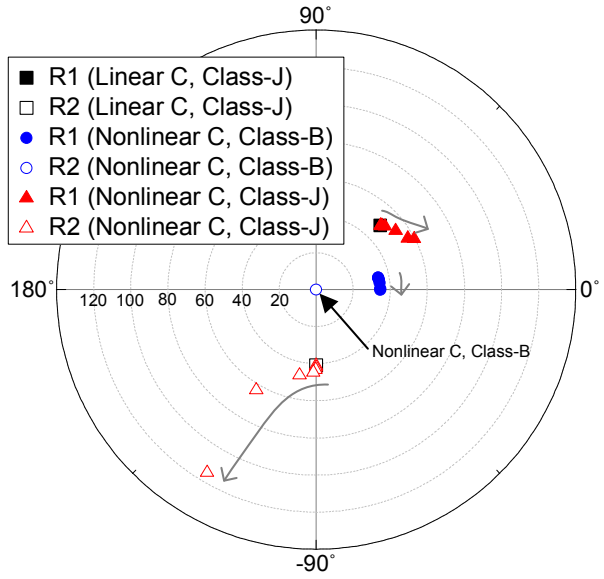


Fig. 10. Fundamental and second harmonic-load impedance trajectories according to the power level.

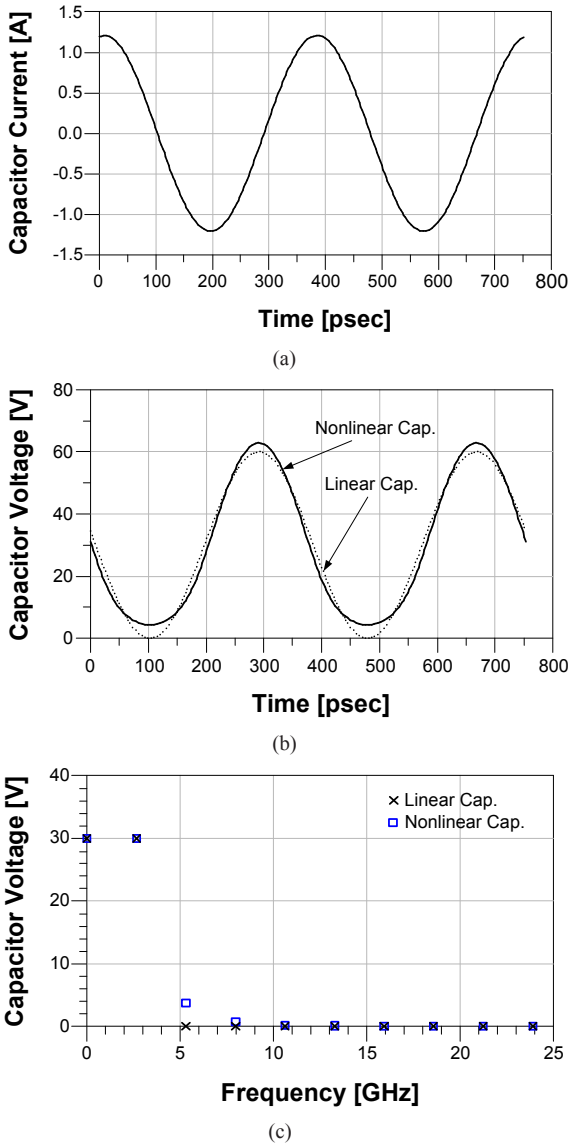


Fig. 11. Simulation results to demonstrate the harmonic generation of the nonlinear $C_{\rm out}$. (a) Current flowing from the linear and nonlinear $C_{\rm out}$s. The resultant capacitor voltage waveforms in the (b) time- and (c) frequency-domain.

in Fig. 5. Although the fundamental voltage of the Class-J amplifier is increased by a factor of $\sqrt{2}$ compared to the Class-B, as shown in Fig. 4(b), the output power and efficiency of the Class-J are equal to those of the Class-B amplifier due to the phase mismatch between the current and voltage waveforms by $45°$. In short, although the Class-B and Class-J amplifiers with linear $C_{\rm out}$ have different fundamental loads and harmonic terminations, the performances of the two PAs are nearly the same except at the highly saturated condition. However, even at the highly saturated condition, the difference is very small.

Although Section II-B explains clearly the fundamental operation of the Class-J amplifier and provides the proper load conditions, it does not describe the real behavior of the amplifier because $C_{\rm out}$ is not a linear element but a nonlinear element, as shown in Fig. 1(b). In this section, the basic operation of a Class-J amplifier with the nonlinear $C_{\rm out}$ is investigated using the setup shown in Fig. 6. Here, we define the load impedance at the current source $Z_{\rm Load}$ and the capacitance is tuned for the fundamental frequency at low power level. Fig. 7 represents the simulated time-domain voltage and current waveforms and load-lines of the Class-J amplifiers with linear and nonlinear $C_{\rm out}$s, and Fig. 8 describes the average capacitance according to the output power level for the Class-J amplifier with the nonlinear $C_{\rm out}$. In the low-power region, below 32 dBm (1.6 W) of the output power, the swing of the drain voltage is within the range where the nonlinear $C_{\rm out}$ could be regarded as a linear capacitance, as shown in Fig. 7 and Fig. 1. At the output power of 32 dBm (1.6 W), the voltage is varied from 20 V to 50 V so that the average capacitance remains around 2.1 pF. Therefore, the waveforms and load-lines with the nonlinear $C_{\rm out}$ case are the same as those with the linear $C_{\rm out}$ case. This results in nearly the same performances for the output

power and efficiency, as shown in Fig. 9. In addition, the output fundamental and second-harmonic load impedances for both the linear and nonlinear $C_{\rm out}$s are the same, properly shaping the half-sinusoidal voltage waveforms, as described in Fig. 10. However, as the output power increases above 32 dBm (1.6 W), the average capacitance also enlarges with a large capacitance at a low voltage. Thus, as shown in Fig. 7(a), the current waveform has a large dip at the middle, generating a large third-harmonic current and enhancing the efficiency. Moreover, the magnitude of the fundamental load impedance increases, but the phase decreases as depicted in Fig. 10. As a result, unlike the Class-J amplifier with the linear $C_{\rm out}$, the voltage waveform moves toward the direction to reduce the phase difference between the current and voltage waveforms while maintaining the half-sinusoidal shape of the voltage. This results in enhanced output power and efficiency performances compared to the Class-J amplifier with the linear $C_{\rm out}$. What is interesting here is that these waveforms can be made with δ of less than 45°. However, from (5), δ less than 45° leads to a negative resistance value of the second harmonic impedance. This means that the nonlinear $C_{\rm out}$ generates the second-harmonic voltage component. This phenomenon cannot be expected from the operation of a Class-J amplifier with a linear $C_{\rm out}$.

Fig. 11 shows the simulation results to demonstrate the harmonic generation of the nonlinear $C_{\rm out}$. The simulation is carried out using the circuit in Fig. 6. The simulation results include the current flowing through the linear and nonlinear $C_{\rm out}$ and the resultant capacitor voltage waveforms in the time-domain and frequency-domain. Differently from the linear capacitor, the nonlinear capacitor generates a voltage waveform consisting of the fundamental and harmonic voltage components. Although only the fundamental current is injected to the capacitor, the voltage contains a large second-harmonic component with small higher-order frequency components. Since the transistor can be regarded as a voltage controlled current source, the current flowing through the capacitor is determined by the input voltage. The voltage across the capacitor is proportional to the integral of the current, the charge in the capacitor, scaled by the capacitance. It can be expressed by

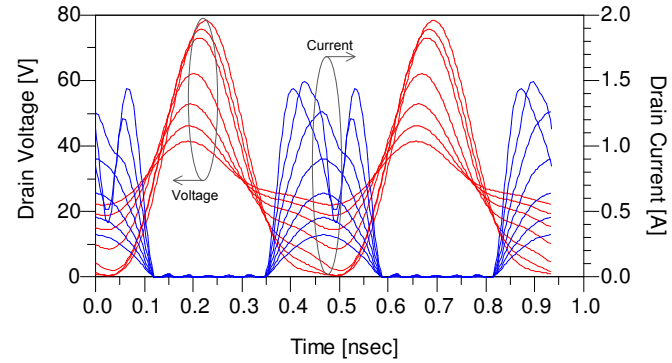
$$\begin{aligned} V_{\rm DS}(t_x) &= V_{\rm DD} + \frac{1}{C_{\rm out}(V_{\rm DS}(t_x))}\int_{-\infty}^{t_x} i(t)\,dt \\ &= V_{\rm DD} + \frac{Q(t_x)}{C_{\rm out}(V_{\rm DS}(t_x))}. \end{aligned} \quad (9)$$

$Q(t_x)$ indicates the charge on $C_{\rm out}$ until t_x. As $Q(t_x)$ decreases with negative $i(t)$, $C_{\rm out}$ increases rapidly. Around the bottom of the voltage, the output voltage $V_{\rm DS}(t_x)$ cannot change much because of the large variation of $C_{\rm out}$ with the limited current drive. That is, $Q(t_x)/C_{\rm out}(V_{\rm DS}(t_x))$ remains nearly constant, $V_{\rm DD}$, around the region. As a result, the voltage waveform has a flattened characteristic in the low voltage region, like the half-sinusoidal shape, as shown in Fig. 11(b). Thus, the second-harmonic impedance can be in the negative resistance region as shown in Fig. 10 because the second-harmonic component in the voltage waveform is generated not by the second-harmonic current and load but by the nonlinear $C_{\rm out}$. This second harmonic component allows the phase difference between the fundamental current and voltage less than 45°. Additionally, the harmonic components generated by the nonlinear capacitor can be varied according to the nonlinear $C_{\rm out}$ profile. The more the nonlinear capacitor changes, the more the second-harmonic is generated. If the second-harmonic load impedance attached parallel to the nonlinear $C_{\rm out}$ is larger than the impedance of the nonlinear $C_{\rm out}$, the half-sinusoidal voltage waveform can be maintained. The second-harmonic current component generated by the current source can assist this behavior, generating the half-sinusoidal voltage waveform. However, the saturated current with a large dip at the middle has a significant third-harmonic and rather small second-harmonic current. Together with the low harmonic impedance, the second-harmonic voltage is mainly built up by the harmonic voltage generation of the nonlinear capacitor. We will revisit this issue in the simulation using a real device model in Section III.

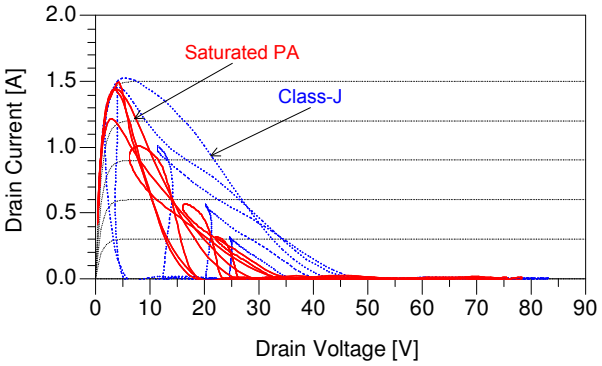
D. Optimization of Class-J Amplifier with Nonlinear Output Capacitor: Saturated Amplifier

The Class-J amplifier can be further optimized to achieve higher efficiency and output power by reducing the phase mismatch between the fundamental voltage and current components, adopting the resistive fundamental loading condition. This is possible due to the second-harmonic voltage generation by the nonlinear $C_{\rm out}$. To obtain the highly efficient operation, the voltage waveform should be shaped to minimize the dissipated power of the device by reducing the concurrent non-zero voltage and current. However, as mentioned in Section II-C, if the external second-harmonic loading is greater than the impedance level generated by the output capacitor, the half-sinusoidal voltage waveform can be generated by the nonlinear $C_{\rm out}$. In [24] and [25], we proposed a novel high efficiency PA, saturated power amplifier, taking advantage of the nonlinear $C_{\rm out}$ to shape the voltage waveform with the resistive fundamental load, and it is the optimized operation of the Class-J amplifier. Since its waveform is similar to that of the Class-F^{-1}, the fundamental load impedance is adjusted between $\sqrt{2}R_{\rm opt}$ to $2R_{\rm opt}$ to achieve the highest efficiency with an acceptable output power [6]. The harmonic load has large tolerance because the voltage waveform is mainly shaped by the nonlinear $C_{\rm out}$. It means that the half-sinusoidal voltage can be generated if the second harmonic load impedance is larger than the impedance level of the nonlinear $C_{\rm out}$. The harmonic load impedance comparable to or less than the nonlinear $C_{\rm out}$ disturbs the generation of the harmonic voltage. However, to achieve the maximum efficiency, the second harmonic should be carefully matched to a particular impedance.

Fig. 12 shows the simulated time-domain voltage and current waveforms and load-lines for the Class-J and saturated amplifiers with nonlinear $C_{\rm out}$. Unlike the waveforms of the Class-J amplifier depicted in Fig. 7(a), the phase difference between the current and voltage is nearly zero due to the resistive fundamental load impedance, as shown in Fig. 13. Moreover, since the second-harmonic voltage to shape the



(a)



(b)

Fig. 12. Simulated (a) time-domain voltage and current waveforms for the saturated amplifier and (b) load-lines for the Class-J and saturated amplifiers.

half-sinusoidal voltage waveform is generated mainly by the nonlinear C_{out}, the second-harmonic impedance remains in the negative resistance region. However, in the low-power region where the nonlinear C_{out} can be regarded as a linear capacitor, the phase of the fundamental-load impedance of the saturated amplifier is not $45°$ while the phase of the second-harmonic is $-90°$, so it does not provide the half-sinusoidal voltage waveform. Fig. 14 shows the simulated efficiencies for the Class-J and saturated amplifiers. Since the saturated amplifier has a smaller phase mismatch between the voltage and current compared to the Class-J amplifier, it produces a higher output power and efficiency than the Class-J amplifier.

In short, for the linear C_{out}, the Class-J amplifier does not have any merit compared to the Class-B amplifier with respect to the output power and efficiency because of the phase mismatch between the voltage and current waveforms. However, for the nonlinear C_{out} case, the Class-J amplifier has a chance to improve the performance because the nonlinear capacitor generates harmonic-voltage components, especially the second-harmonic voltage component. Thus, the phase difference can be reduced below $-45°$. A further improvement can be achieved by selecting a purely resistive load for the fundamental frequency to eliminate the phase mismatch between the voltage and current, while maintaining the half-sinusoidal voltage waveform. This can be carried out if the external second-harmonic impedance is greater than the level of the nonlinear C_{out}, which is a saturated PA, the further optimized version of the Class-J amplifier for highly efficient operation.

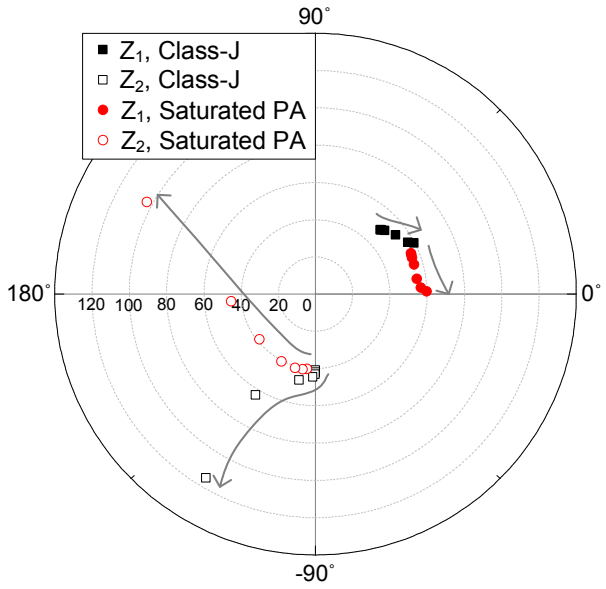


Fig. 13. Fundamental and second-harmonic load impedance trajectories for the Class-J and saturated amplifiers according to the power level.

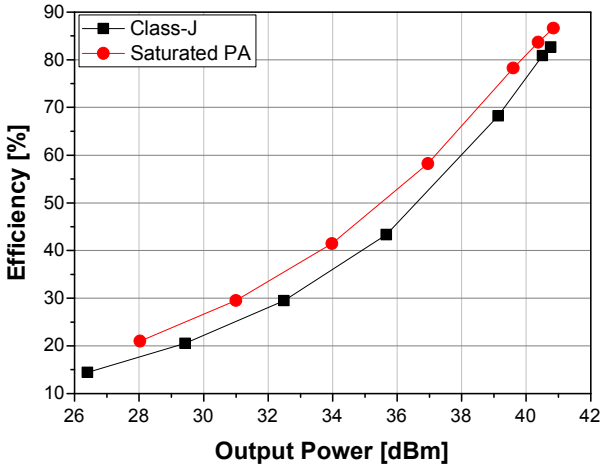


Fig. 14. Simulated efficiencies of the Class-J and saturated amplifiers.

III. Implementation and Experimental Results

To validate the voltage waveform shaping by the nonlinear C_{out} and the highly efficient operation, a saturated amplifier was designed and implemented at 2.14 GHz using a Cree GaN HEMT CGH40010 package device containing a CGH60015 bare chip. Since the commercial device model includes packaging effects, due to bonding wires, package leads, and parasitics, the simulation is conducted using a bare-chip model to show the inherent operation of the saturated PA. In addition, the simulation for the implementation is conducted using the model of the packaged-device. Fig. 15 shows the simulated second-harmonic load-pull contours of the output power and efficiency when the fundamental and third-harmonic impedances are set to $18.23 + j25.15\ \Omega$ and $0\ \Omega$, respectively, at the drain pad of the bare chip. The load-pull simulation was carried out using Agilent ADS 2008 Update 1. The device model, CGH60015 and package information, were

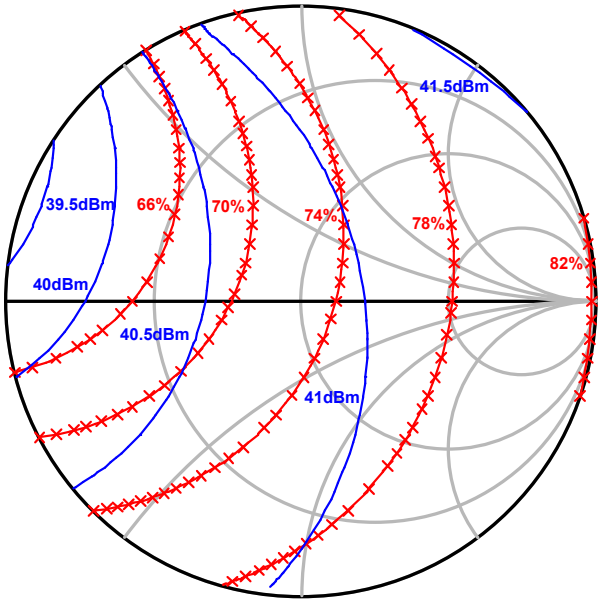


Fig. 15. Simulated second-harmonic load-pull contours of the output power and efficiency when the fundamental and third-harmonic impedance are set to $18.23 + j25.15\ \Omega$ and $0\ \Omega$, respectively, at the drain pad of the bare chip.

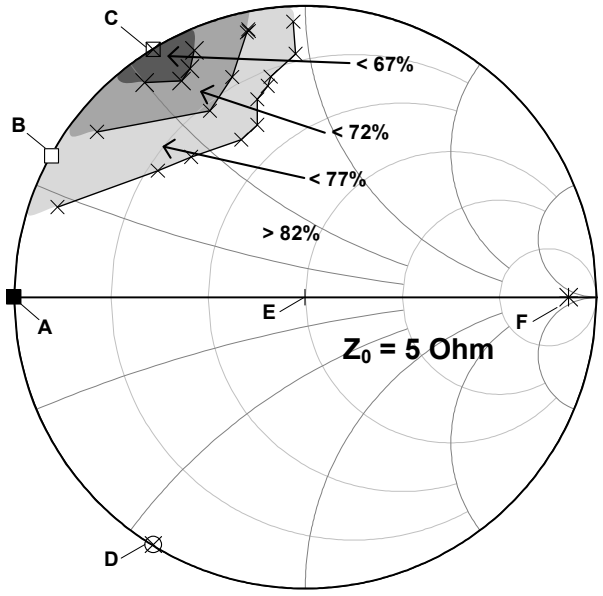
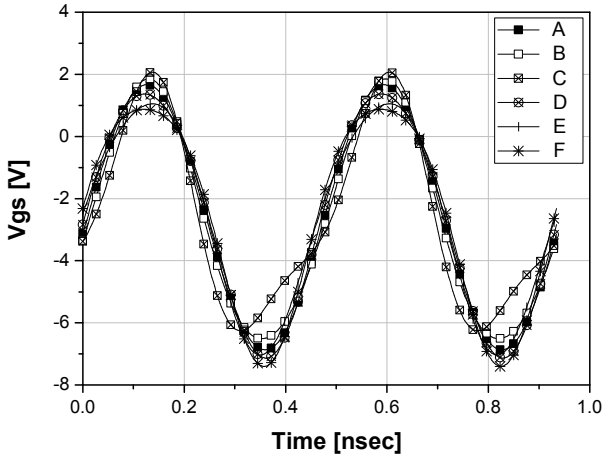
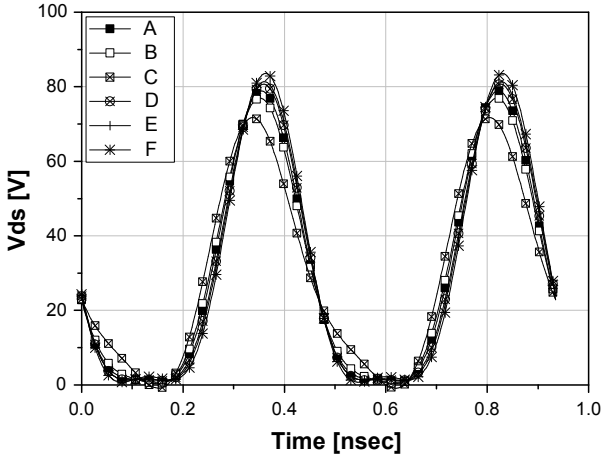


Fig. 16. Simulated second-harmonic source-pull contours of the efficiency when the fundamental source impedance is conjugate-match condition and the output load terminations are set to the condition of the saturated PA. The characteristic impedance of the smith chart is $5\ \Omega$.

provided by Cree Inc.. As mentioned in Section II, a high efficiency and output power can be achieved when the second-harmonic load impedance is large, proving that the nonlinear $C_{\rm out}$ is enough to shape the voltage to the half-sinusoidal. Since a large second-harmonic load impedance provides a high efficiency, it is set to $2 + j80\ \Omega$. For the high efficiency and output power operation, a fundamental-load impedance at the dependent current source is determined to be about $60\ \Omega$. Since the efficiency changes a little according to the third-harmonic matching impedance, the impedance is set to 0.



(a)



(b)

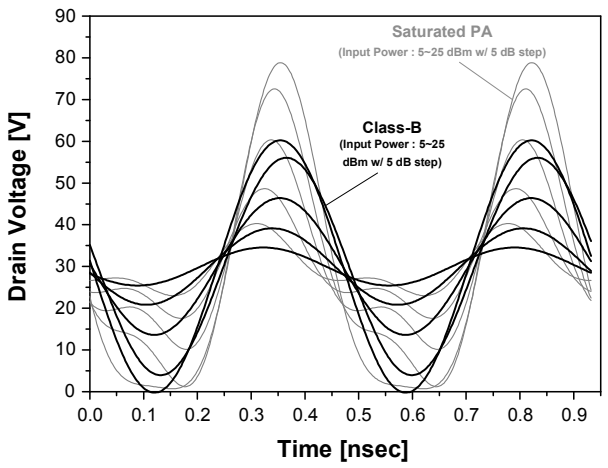
Fig. 17. Simulated (a) $V_{\rm gs}$ and (b) $V_{\rm ds}$ waveforms at the marked points on the Smith chart in Fig. 16 (A $= 0\ \Omega$, B $= 0.01 + {\rm j}1.3\ \Omega$, C $= 0.01 + {\rm j}2.8\ \Omega$, D $= 0.01 - {\rm j}2.8\ \Omega$, E $= 5\ \Omega$, and F $= 100\ \Omega$).

So far, the fundamental and harmonic-load impedances at the output have been considered to achieve high power and efficiency capabilities, and the fundamental input component is conjugately matched. However, it has been observed that the input harmonic terminations should be properly placed due to the nonlinear input capacitor $C_{\rm gs}$. In particular, to preserve the sinusoidal input drive at the gate, the input harmonic terminations are frequently set to be short-circuit [26], [27]. On the other hand, in [10]– [12], they make an effort to shape the output voltage waveform by using the nonlinear effect of $C_{\rm gs}$. To find the optimum input termination for the second harmonic, the source-pull simulation for the second harmonic is carried out, as shown in Fig. 16. During the simulation, the fundamental source impedance is conjugately matched, and the output load terminations are set to the condition of the saturated amplifier. A simulation of source-pull for the second-harmonic termination indicates only a minor effect on the efficiency if the termination is not in the gray colored region. This result supports that the output voltage waveform is mainly shaped by the nonlinear output capacitor. Fig. 17 shows the simulated $V_{\rm gs}$ and $V_{\rm ds}$ waveforms for second harmonic

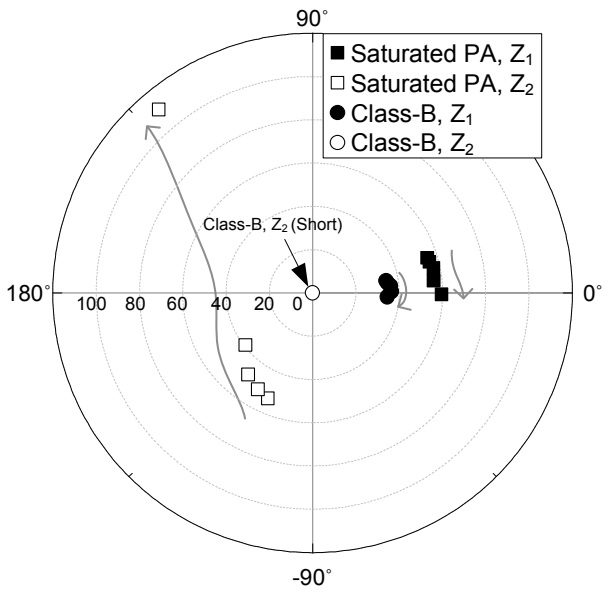
impedances at the marked points on the Smith chart in Fig. 16. Except for the points marked by A and C, the $V_{\rm gs}$ waveforms are very similar due to the harmonic voltage generation of $C_{\rm gs}$. Not just for these points, almost regions of the smith chart, except for the gray colored part, provide the analogous $V_{\rm gs}$ waveforms. For the point marked by A, due to the short-circuit for the second harmonic, the sinusoidal voltage is presented. In spite of the different $V_{\rm gs}$ waveforms, the output voltages at the drain are similar shapes. Those waveforms clearly show that the output voltage shape is not much affected by the harmonic generation of $C_{\rm gs}$ while considering the nonlinear $C_{\rm ds}$. However, even though most of regions provide the same performance, the output power and efficiency deteriorated when the source impedance for the second harmonic is located at the gray-colored region. In this region, the conduction angle of the drain current is reduced, resulting in low output power and efficiency. Therefore, in this work, the input termination for the second harmonic is set to the short-circuit.

Fig. 18 indicates the simulated time-domain voltage waveform and the fundamental and second-harmonic load impedance trajectories according to the power level. Like the simulation conducted in Section II-D, the half-sinusoidal voltage waveform is achieved at the high power level where a large amount of the second harmonic is generated by the nonlinear $C_{\rm out}$, so that the second-harmonic impedance remains in the negative resistance region. For comparison, the Class-B amplifier is also simulated using the same device. To provide the sinusoidal voltage waveform, all harmonics are short-circuited. In addition, the fundamental-load impedance of the Class-B PA is set to 36.5 Ω at the maximum power level to provide the full swings of the voltage and current waveforms. Fig. 19 shows the simulated gain and efficiency comparisons between the saturated PA and Class-B amplifier. Because the load impedance of the saturated PA is larger than that of the Class-B amplifier, the saturated PA provides higher gain than the Class-B's one in the low power region. At the high power level, compared with the Class-B amplifier, the saturated PA delivers the better efficiency performance with comparable output power, resulting from the second-harmonic manipulation caused by the nonlinear $C_{\rm out}$. In particular, the maximum efficiency of the saturated PA is 81.5%, which is an improvement of 9.3%.

Fig. 20(a) shows a photograph of the designed PA implemented on a Taconic TLY-5 substrate with $\varepsilon_r = 2.2$ and thickness of 31 mil. The detailed microstrip dimensions are shown in Fig. 20(b). In the experiment, the gate bias is set to –3.1 V ($I_{\rm DSQ} = 94$ mA) at a supplied drain voltage of 30 V. Unlike the conventional high efficiency PAs, any special harmonic-loading circuit is not used in the output matching. The simulated and measured output power, efficiency, and gain characteristics for a CW signal are well matched, as shown in Fig. 21. In particular, the implemented PA provides a maximum PAE of 77.3% at a saturated output power of 40.6 dBm (11.5 W). Fig. 22 depicts the measured adjacent channel leakage ratio (ACLR) and PAE for LTE signal with 6.6 dB PAPR and 10 MHz signal bandwidth. The proposed PA delivers a PAE of 42.3% and a power gain of 21 dB at an average output power of 34.2 dBm (2.6 W). To val-



(a)



(b)

Fig. 18. (a) Simulated time-domain voltage waveforms of the saturated amplifier and Class-B PA. (b) Fundamental and second-harmonic load impedance trajectories of the saturated amplifier and Class-B PA according to the power levels.

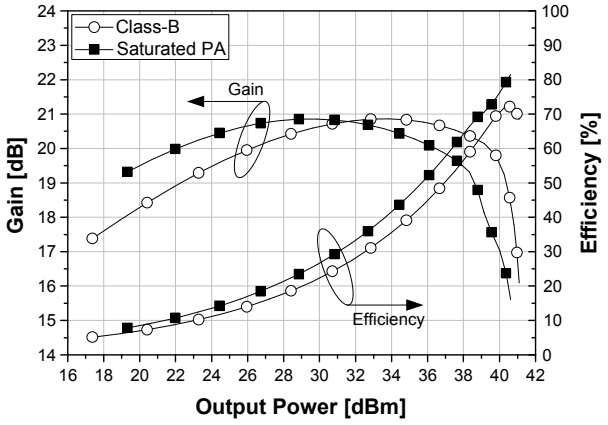
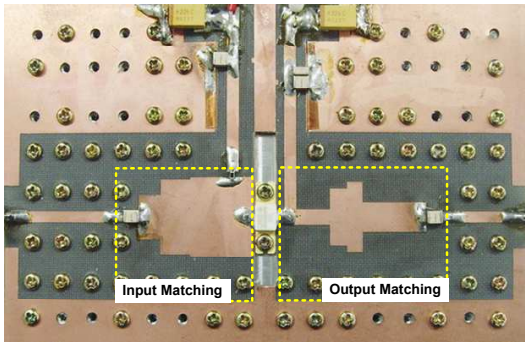
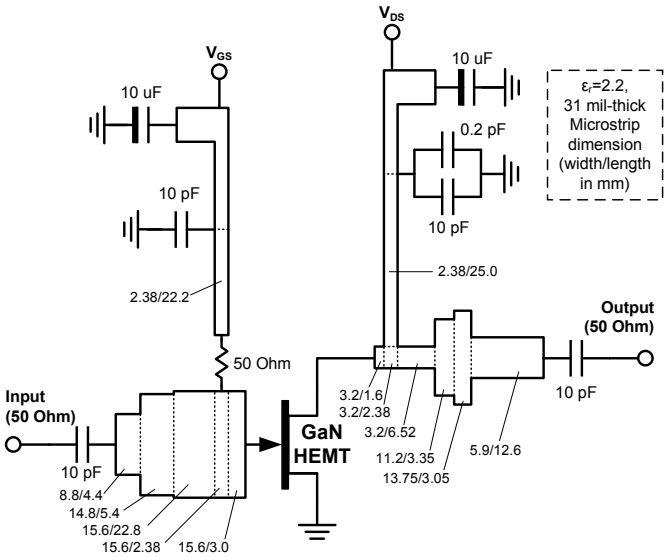


Fig. 19. Simulated gain and efficiency comparison between the saturated PA and Class-B amplifier.



(a)



(b)

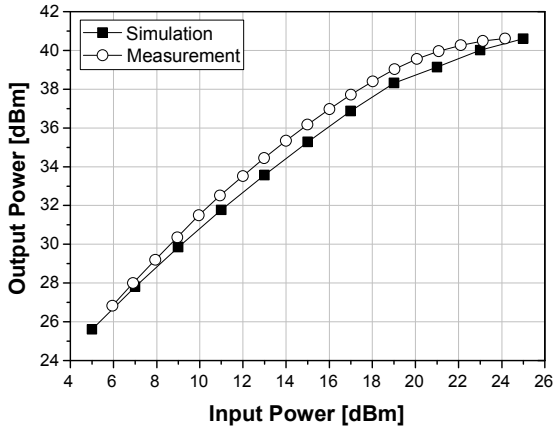
Fig. 20. (a) Photograph and (b) circuit schematic of the implemented PA.

idate potential of the proposed PA as a main block of a linear power amplifier (LPA), the linearization of the PA is carried out by employing the digital feedback predistortion technique (DPBPD) [28]. Fig. 23 shows the measured output spectra before and after the linearization. The ACLR at an offset of 7.5 MHz is –45.1 dBc, which is an improvement of 23 dB at an average output power of 34.2 dBm (2.6 W). The linearization results are summarized in Table II. These experimental results clearly show that the proposed saturated amplifier can provide excellent efficiency without any special harmonic loading circuit. Moreover, by applying the linearization technique, it is well suited to be a highly efficient main amplifier of a LPA for use in a LTE transmitter.

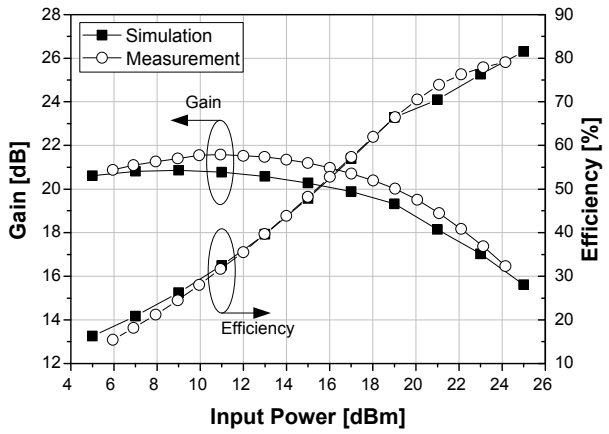
Comparison of the performance among the designed PA with state-of-the-art results for high-efficiency is summarized in Table III. The comparison shows the excellent performance of the saturated PA, the optimized Class-J PA, without any harmonic control circuitry.

IV. Conclusion

The operation principles of Class-J amplifiers with linear and nonlinear C_{out}s are analyzed using a simple transistor model in an ADS simulator. The performance of the Class-J



(a)



(b)

Fig. 21. Simulated and measured (a) output power, (b) efficiency and gain characteristics for a CW signal.

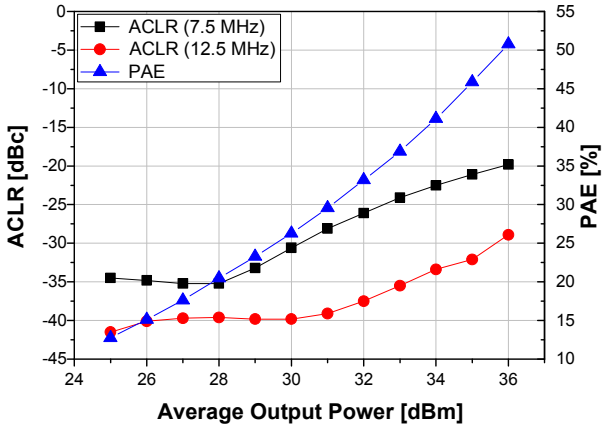


Fig. 22. Measured ACLR and PAE characteristics for an LTE signal.

TABLE II
Linearization Performance at an Average Output Power of 34.2 dBm (2.6 W) for LTE Signal

	ACLR [dBc] at 7.5-MHz	ACLR [dBc] at 12.5-MHz	PAE [%]
Before Linearization	–22.3	–33.1	42.3
After Linearization	–45.1	–47.9	43.8

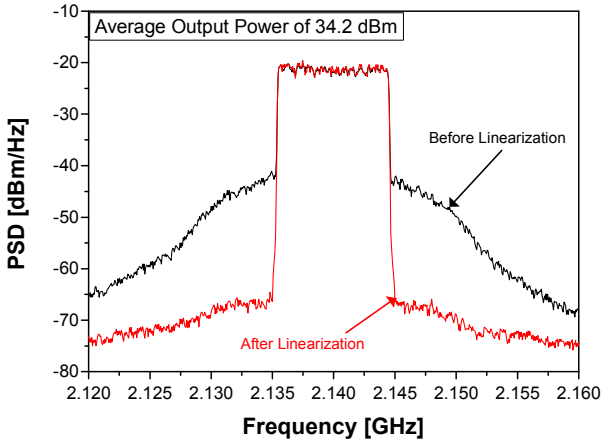


Fig. 23. Output spectra before and after the linearization using DFBPD.

TABLE III
STATE-OF-THE-ART HIGH EFFICIENCY PAS USING GAN HEMT DEVICE ABOVE 2 GHz

Reference	f_o* [GHz]	P_{sat} [W]	V_{DC} [V]	PAE [%]	Topoplgy
[29]♯	2.10	11.2	50.0	79.7	Class-E
[30]	2.00	11.5	50.0	74.3	Class-E
[31]†	2.00	16.5	42.5	85.5	Class-F
[32]‡	2.10	12.0	28.0	79.6	Class-F^{-1}
[33]	2.14	7.2	28.0	68.0	H·T PA⋆
[34]†	2.14	12.0	40.0	74.0	Class-E
This work	2.14	11.5	30.0	77.3	Saturated PA

*f_o denotes the operating frequency.
⋆H·T PA denotes the harmonically tuned PA.
♯Internal matching circuitry is optimized for the class-E.
†PA is fabricated using bare-chip.
‡Performance is measured on the load-pull measurement setup.

PA with linear C_{out} is comparable to that of the conventional Class-B amplifier. However, due to the harmonic generation property of the nonlinear C_{out}, the half-sinusoidal voltage waveform can be properly shaped while the phase overlap between the voltage and current components are reduced below $45°$. This allows the improvement of the efficiency beyond that of a Class-J amplifier with a linear C_{out}. The further optimization of the amplifier can be carried out by adopting the phase difference to zero degree using the purely resistive fundamental load impedance. It minimizes the dissipated power caused by the concurrent non-zero voltage and current while maintaining the half-sinusoidal voltage waveform. Since the voltage shaping is achieved by the nonlinear C_{out}, efforts to control the harmonic components are unnecessary. If the external harmonic load impedances are larger than the level of the capacitor, a highly efficient voltage waveform is obtained. This is supported by the ADS simulation using both ideal and real models of the transistor. This is the optimized version of Class-J PA, which is the saturated PA we have reported. A highly efficient saturated PA is implemented by using a Cree GaN HEMT CGH40010 device at 2.14 GHz. It provides a PAE of 77.3% and a saturated output power of 40.6 dBm (11.5 W) without any special harmonic loading network.

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