6.2 INTRODUCTION TO OP AMPS

INTRODUCTION

Objective

The objective of this presentation is:

1.) Characterize the operational amplifier

2.) Illustrate the analysis of both BJT and MOS op amps

3.) Illustrate the design of both BJT and MOS op amps

Outline

- Introduction and Characterization of Op Amps
- Compensation of Op Amps
  - General principles
  - Miller, Nulling Miller
  - Self-compensation
  - Feedforward
- Simple Op Amps
  - Two-stage
  - Folded-cascode
- Design of Op Amps
- Summary

INTRODUCTION AND CHARACTERIZATION OF OP AMPS

High-Level Viewpoint of an Op Amp

Block diagram of a general, two-stage op amp:

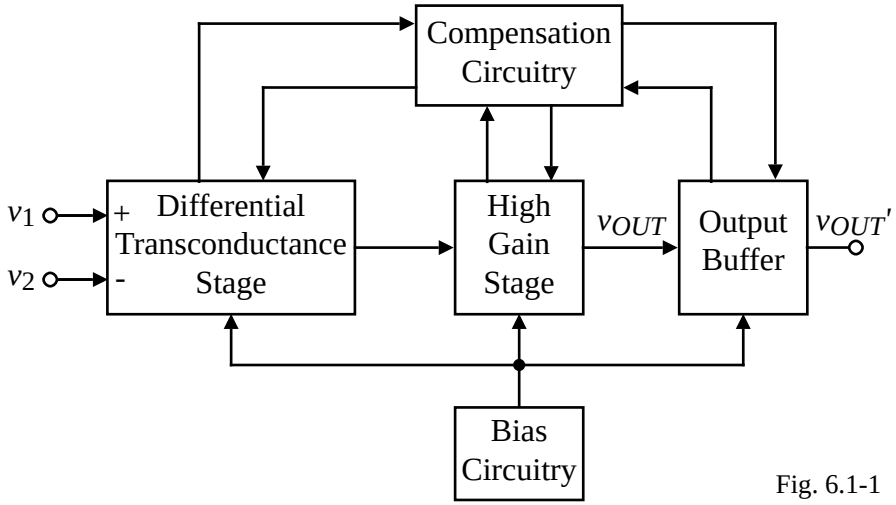


Fig. 6.1-1

- Differential transconductance stage:

Forms the input and sometimes provides the differential-to-single ended conversion.

- High gain stage:

Provides the voltage gain required by the op amp together with the input stage.

- Output buffer:

Used if the op amp must drive a low resistance.

- Compensation:

Necessary to keep the op amp stable when resistive negative feedback is applied.

Ideal Op Amp

Symbol:

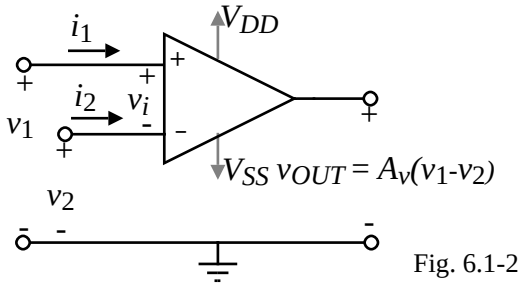


Fig. 6.1-2

Null port:

If the differential gain of the op amp is large enough then input terminal pair becomes a null port.

A null port is a pair of terminals where the voltage is zero and the current is zero.

I.e.,

$$v_1 - v_2 = v_i = 0$$

and

$$i_1 = 0 \text{ and } i_2 = 0$$

Therefore, ideal op amps can be analyzed by assuming the differential input voltage is zero and that no current flows into or out of the differential inputs.

General Configuration of the Op Amp as a Voltage Amplifier

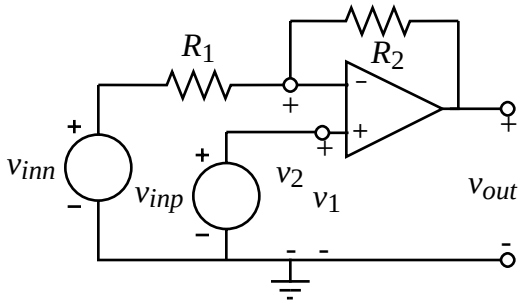


Fig. 6.1-3

Noniverting voltage amplifier:

$$v_{inn} = 0 \quad \Rightarrow \quad v_{out} = \left(\frac{R_1+R_2}{R_1}\right) v_{inp}$$

Inverting voltage amplifier:

$$v_{inp} = 0 \quad \Rightarrow \quad v_{out} = -\left(\frac{R_2}{R_1}\right) v_{inn}$$

Example 1 - Simplified Analysis of an Op Amp Circuit

The circuit shown below is an inverting voltage amplifier using an op amp. Find the voltage transfer function, v_{out}/v_{in}.

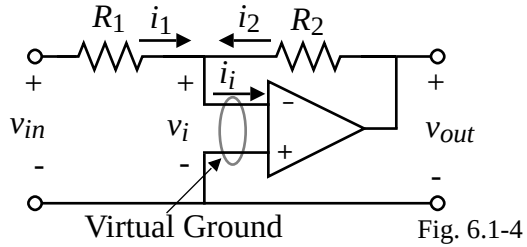


Fig. 6.1-4

Solution

If the differential voltage gain, A_v, is large enough, then the negative feedback path through R_2 will cause the voltage v_i and the current i_i shown on Fig. 6.1-4 to both be zero. Note that the null port becomes the familiar *virtual ground* if one of the op amp input terminals is on ground. If this is the case, then we can write that

$$i_1 = \frac{v_{in}}{R_1}$$

and

$$i_2 = \frac{v_{out}}{R_2}$$

Since, $i_i = 0$, then $i_1 + i_2 = 0$ giving the desired result as

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}.$$

Linear and Static Characterization of the Op Amp

A model for a nonideal op amp that includes some of the linear, static nonidealities:

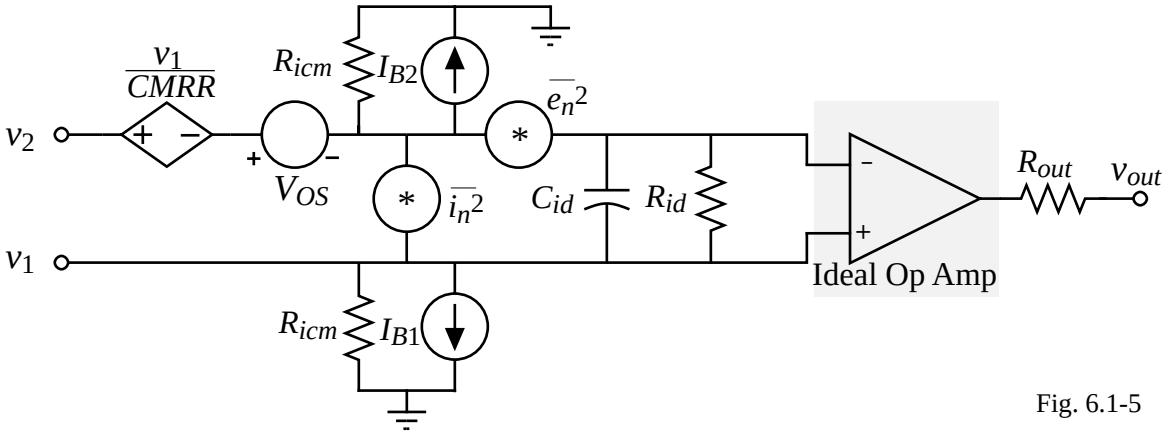


Fig. 6.1-5

where

R_{id} = differential input resistance

C_{id} = differential input capacitance

R_{icm} = common mode input resistance

V_{OS} = input-offset voltage

I_{B1} and I_{B2} = differential input-bias currents

I_{OS} = input-offset current ($I_{OS} = I_{B1}$-I_{B2})

$CMRR$ = common-mode rejection ratio

$\overline{e}_n^2$ = voltage-noise spectral density (mean-square volts/Hertz)

$\overline{i}_n^2$ = current-noise spectral density (mean-square amps/Hertz)

Linear and Dynamic Characteristics of the Op Amp

Differential and common-mode frequency response:

$$V_{out}(s) = A_v(s)[V_1(s) - V_2(s)] \pm A_c(s)\left(\frac{V_1(s)+V_2(s)}{2}\right)$$

Differential-frequency response:

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\cdots} = \frac{A_{v0}\, p_1 p_2 p_3 \cdots}{(s - p_1)(s - p_2)(s - p_3)\cdots}$$

where $p_1, p_2, p_3, \cdots$ are the poles of the differential-frequency response.

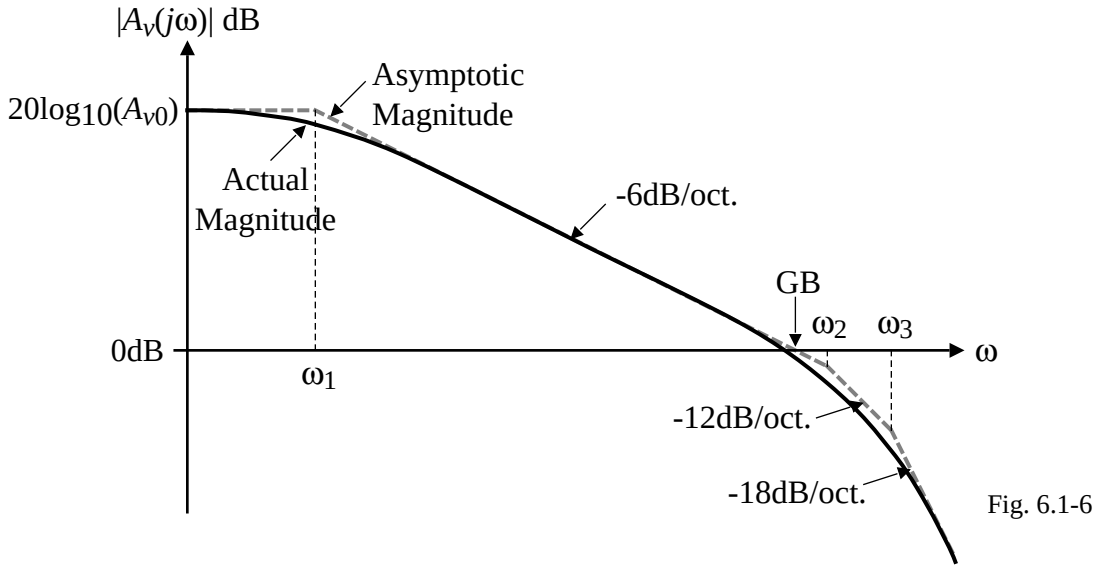


Fig. 6.1-6

Other Characteristics of the Op Amp

Power supply rejection ratio (*PSRR*):

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{\text{OUT}}} A_v(s) = \frac{V_o/V_{\text{in}}\,(V_{dd}=0)}{V_o/V_{dd}\,(V_{\text{in}}=0)}$$

Input common mode range (*ICMR*):

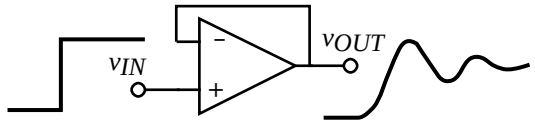
ICMR = the voltage range over which the input common-mode signal can vary without influence the differential performance

Slew rate (*SR*):

SR = output voltage rate limit of the op amp

Settling time (T_s):

T_s = time needed for the output of the op amp to reach a final value to with a predetermined tolerance when excited by a small signal. (SR is large signal excitation)



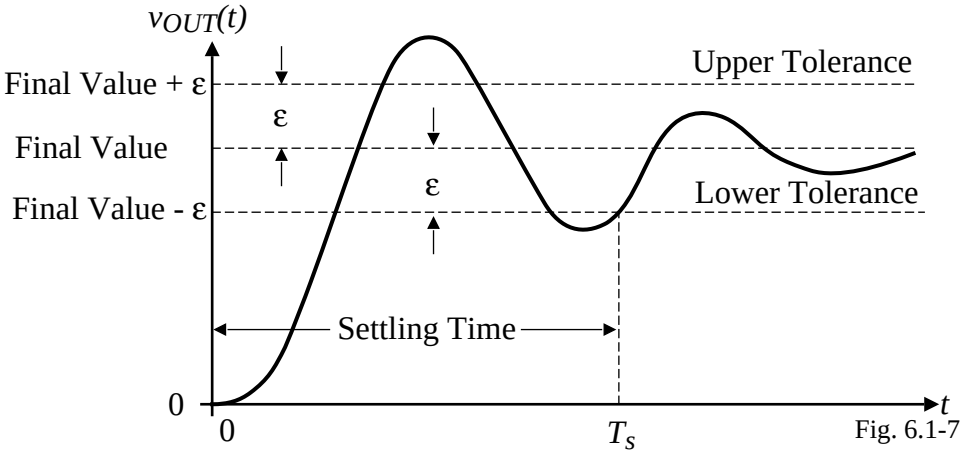


Fig. 6.1-7

Classification of CMOS Op Amps

Categorization of op amps:

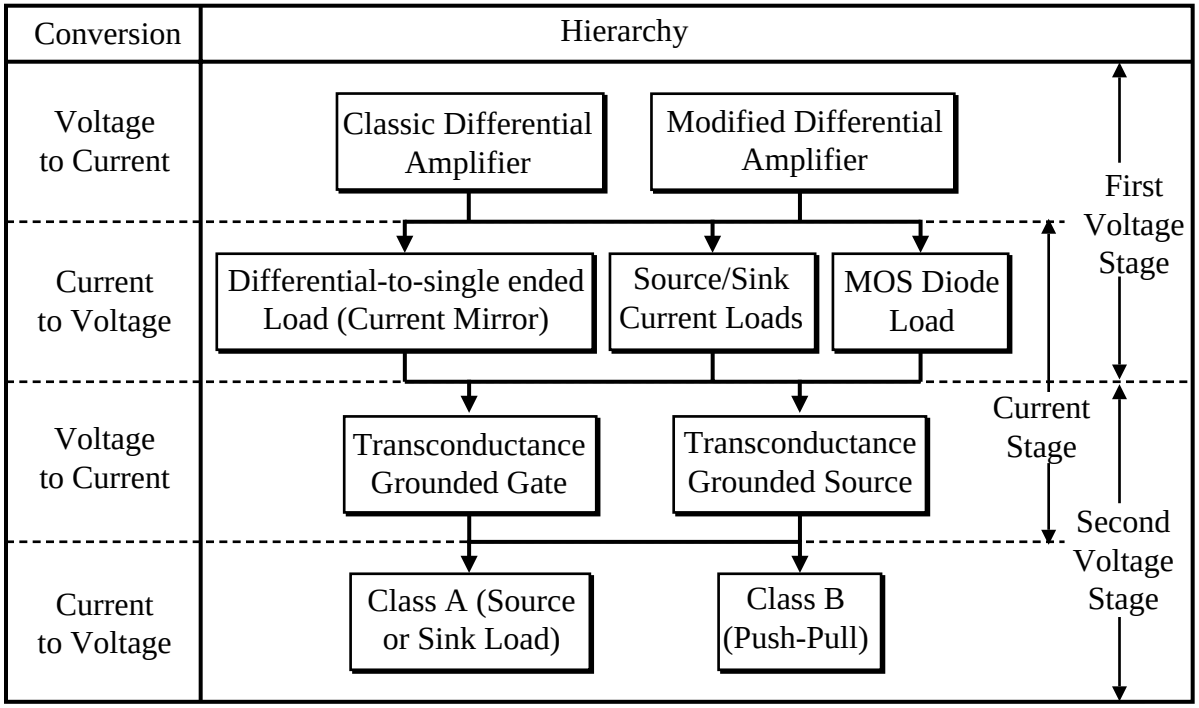
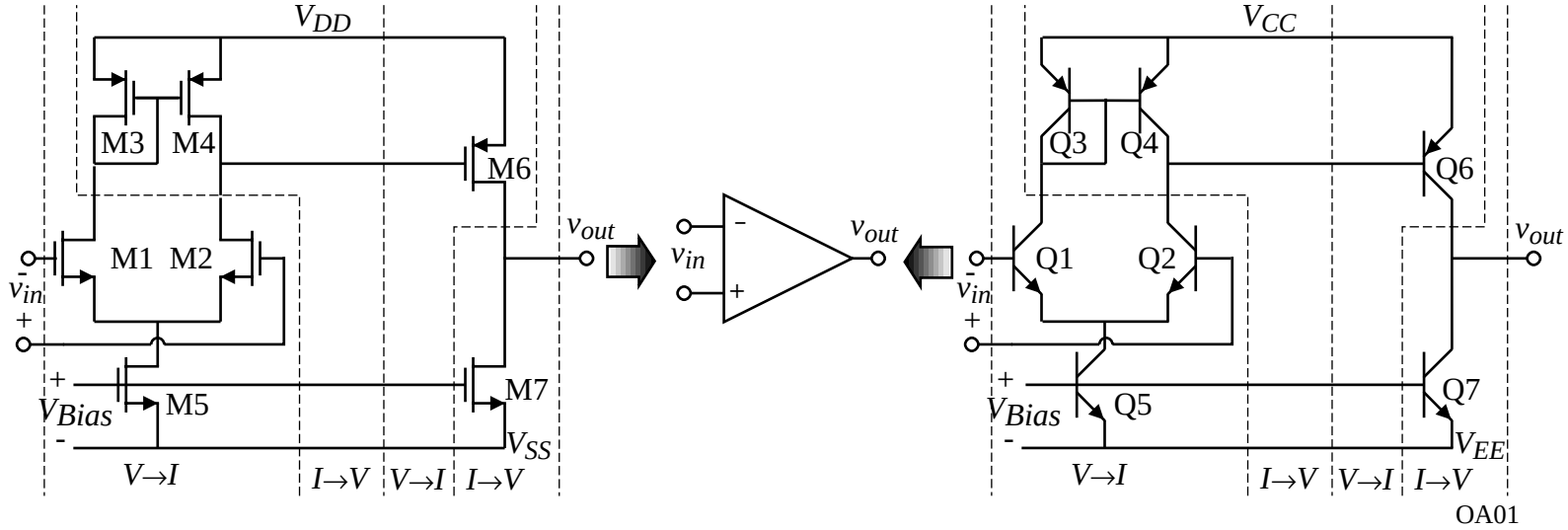


Table 6.1-1

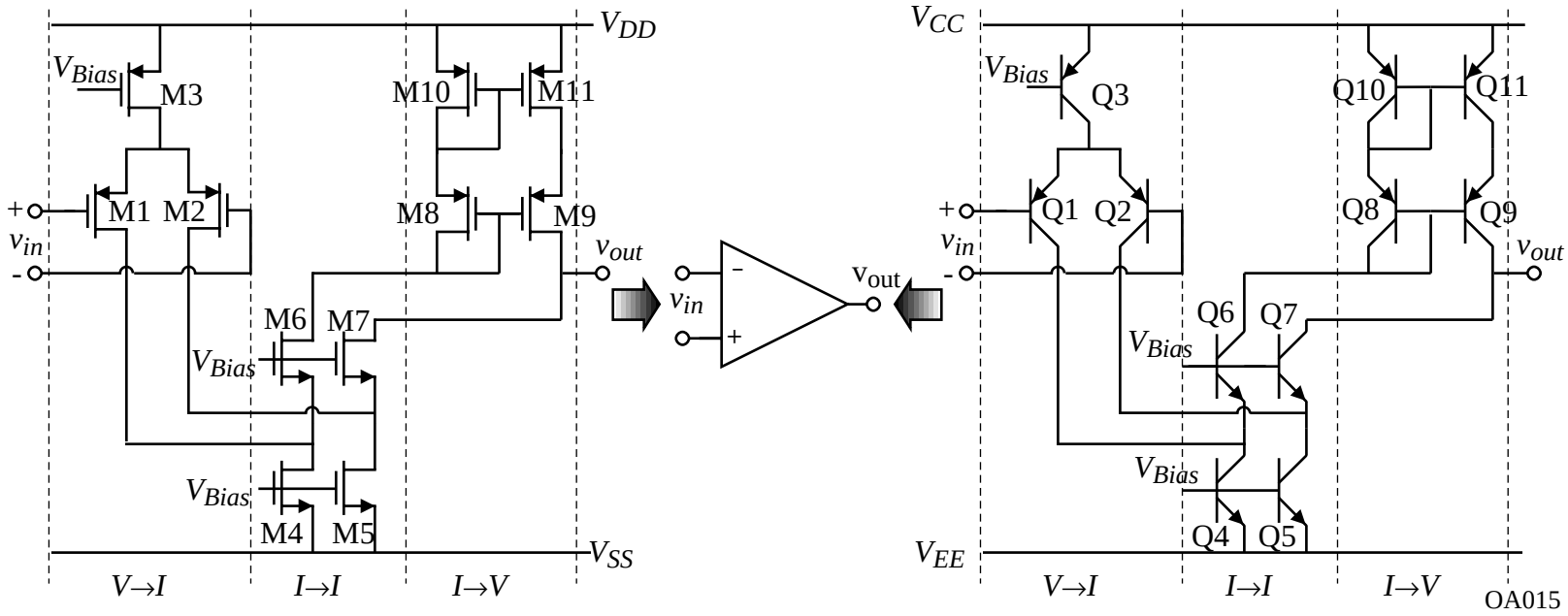
Two-Stage Op Amp Architecture

Simple two-stage op amp broken into voltage-to-current and current-to-voltage stages:



Folded-Cascode Op Amp Architecture

Simple folded-cascode op amp broken into voltage-to-current and current-to-voltage stages:



COMPENSATION OF OP AMPS

GENERAL PRINCIPLES

Objective

Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
   - Miller capacitor only
   - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
   - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.
2. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.
3. Self compensating - Load capacitor compensates the op amp.

Single-Loop, Negative Feedback Systems

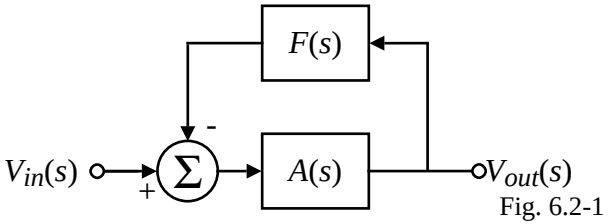


Fig. 6.2-1

$A(s)$ = amplifier gain (normally the differential-mode voltage gain of the op amp)

$F(s)$ = transfer function of the external feedback from the output of the op amp back to the input.

Definitions:

- Open-loop gain = $L(s) = -A(s)F(s)$
- Closed-loop gain = $\dfrac{V_{out}(s)}{V_{in}(s)} = \dfrac{A(s)}{1+A(s)F(s)}$

Stability Requirements:

The requirements for stability for a single-loop, negative feedback system is,

$$|A(j\omega_{0^\circ})F(j\omega_{0^\circ})| = |L(j\omega_{0^\circ})| < 1$$

where ω_{0° is defined as

$$\text{Arg}[-A(j\omega_{0^\circ})F(j\omega_{0^\circ})] = \text{Arg}[L(j\omega_{0^\circ})] = 0^\circ$$

Another convenient way to express this requirement is

$$\text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})] > 0^\circ$$

where ω_{0dB} is defined as

$$|A(j\omega_{0dB})F(j\omega_{0dB})| = |L(j\omega_{0dB})| = 1$$

Illustration of the Stability Requirement using Bode Plots

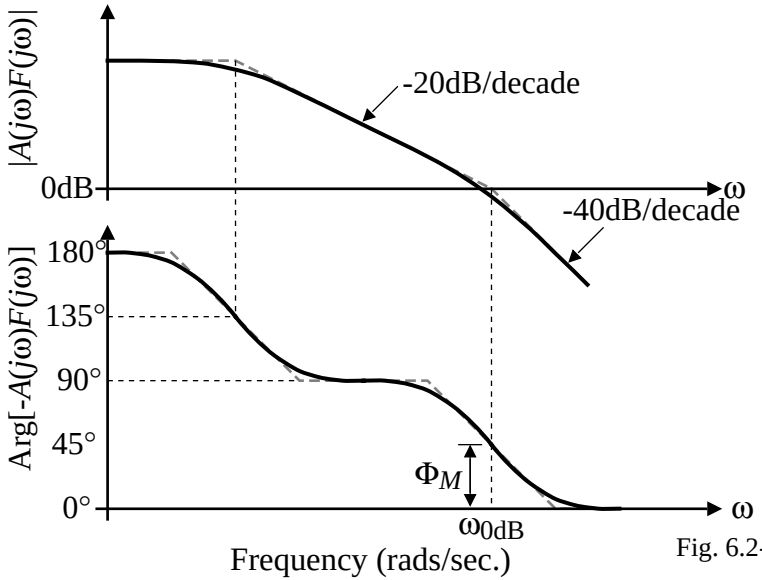


Fig. 6.2-2

A measure of stability is given by the phase when $|A(j\omega)F(j\omega)| = 1$. This phase is called *phase margin*.

Phase margin = $\Phi_M = \text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})]$

Why Do We Want Good Stability?

Consider the step response of second-order system which closely models the closed-loop gain of the op amp.

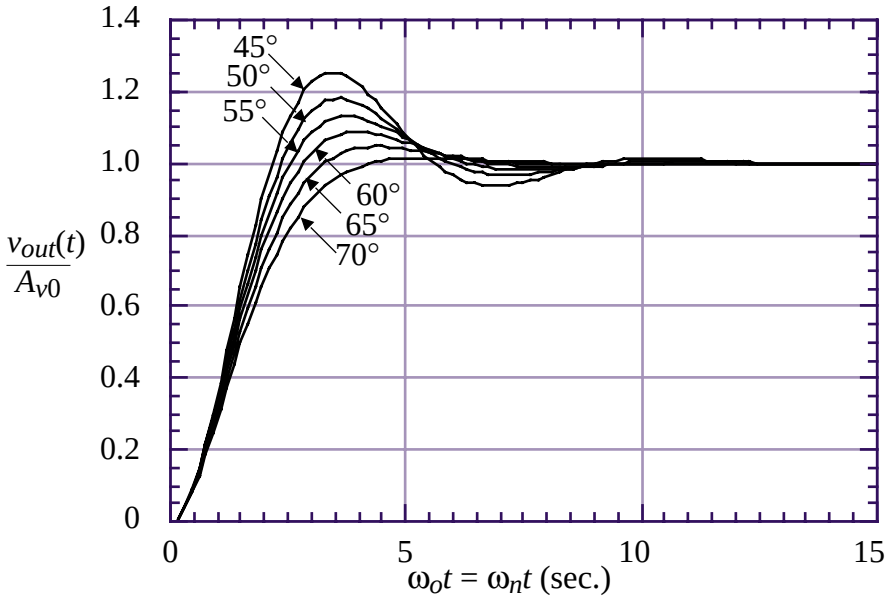


Fig. 6.2-3

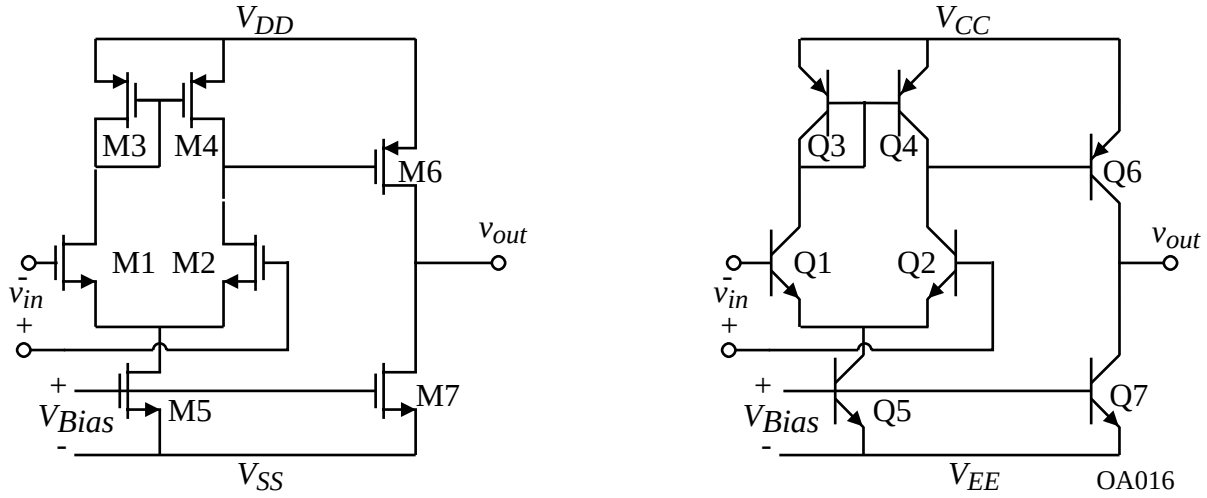
A "good" step response is one that quickly reaches its final value.

Therefore, we see that phase margin should be at least 45° and preferably 60° or larger.

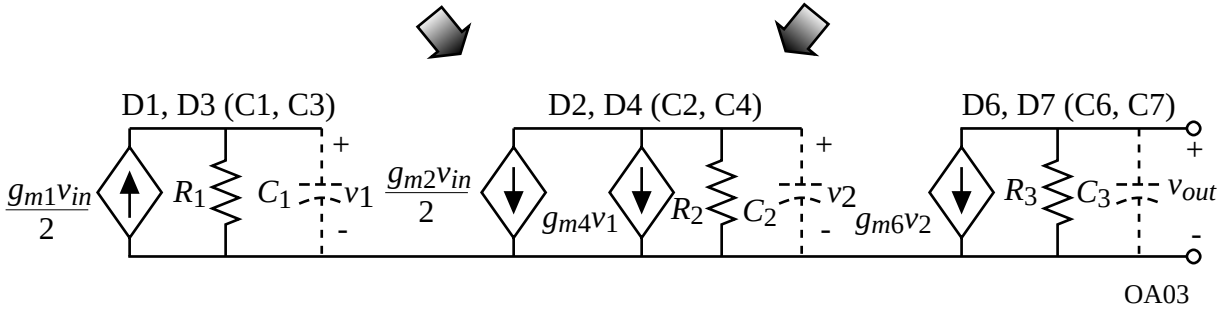
(A good rule of thumb for satisfactory stability is that there should be less than three rings.)

Uncompensated Frequency Response of Two-Stage Op Amps

Two-Stage Op Amps:



Small-Signal Model:



Note that this model neglects the base-collector and gate-drain capacitances for purposes of simplification.

Uncompensated Frequency Response of Two-Stage Op Amps - Continued

For the MOS two-stage op amp:

$$R_1 \approx \frac{1}{g_{m3}} \| r_{ds3} \| r_{ds1} \approx \frac{1}{g_{m3}} \qquad R_2 = r_{ds2} \| r_{ds4} \qquad \text{and} \qquad R_3 = r_{ds6} \| r_{ds7}$$

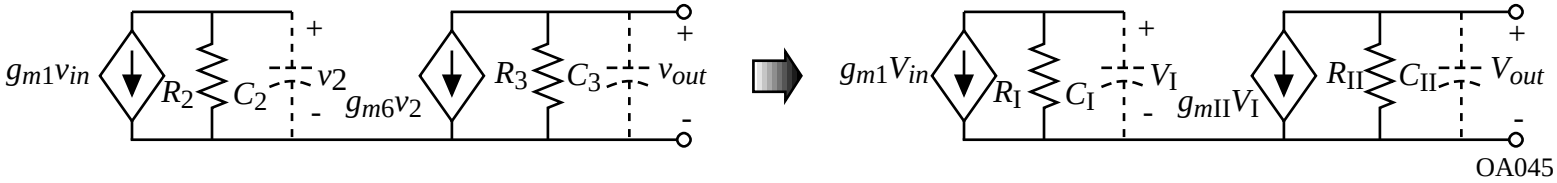
$$C_1 = C_{gs3} + C_{gs4} + C_{bd1} + C_{bd3} \qquad C_2 = C_{gs6} + C_{bd2} + C_{bd4} \qquad \text{and} \qquad C_3 = C_L + C_{bd6} + C_{bd7}$$

For the BJT two-stage op amp:

$$R_1 = \frac{1}{g_{m3}} \| r_{\pi 3} \| r_{\pi 4} \| r_{o3} \approx \frac{1}{g_{m3}} \qquad R_2 = r_{\pi 6} \| r_{o2} \| r_{o4} \approx r_{\pi 6} \qquad \text{and} \qquad R_3 = r_{o6} \| r_{o7}$$

$$C_1 = C_{\pi 3} + C_{\pi 4} + C_{cs1} + C_{cs3} \qquad C_2 = C_{\pi 6} + C_{cs2} + C_{cs4} \qquad \text{and} \qquad C_3 = C_L + C_{cs6} + C_{cs7}$$

Assuming the pole due to C_1 is much greater than the poles due to C_2 and C_3 gives,



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The locations for the two poles are given by the following equations

$$p'_1 = \frac{-1}{R_I C_I} \quad \text{and} \quad p'_2 = \frac{-1}{R_{II} C_{II}}$$

where R_I (R_{II}) is the resistance to ground seen from the output of the first (second) stage and C_I (C_{II}) is the capacitance to ground seen from the output of the first (second) stage.

Uncompensated Frequency Response of an Op Amp

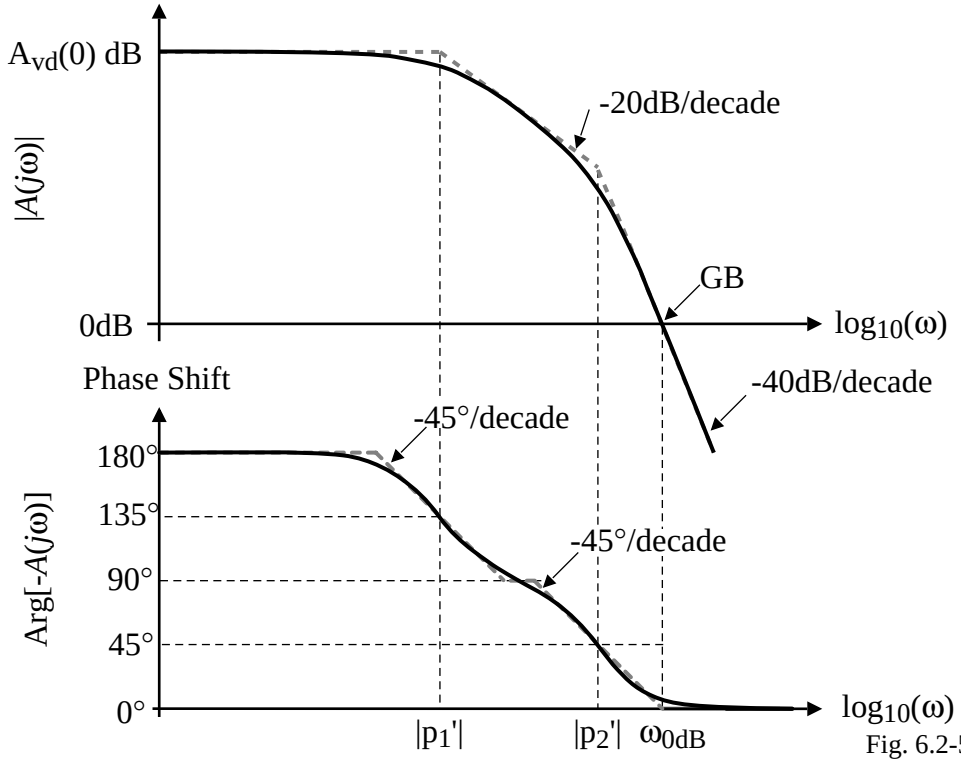


Fig. 6.2-5

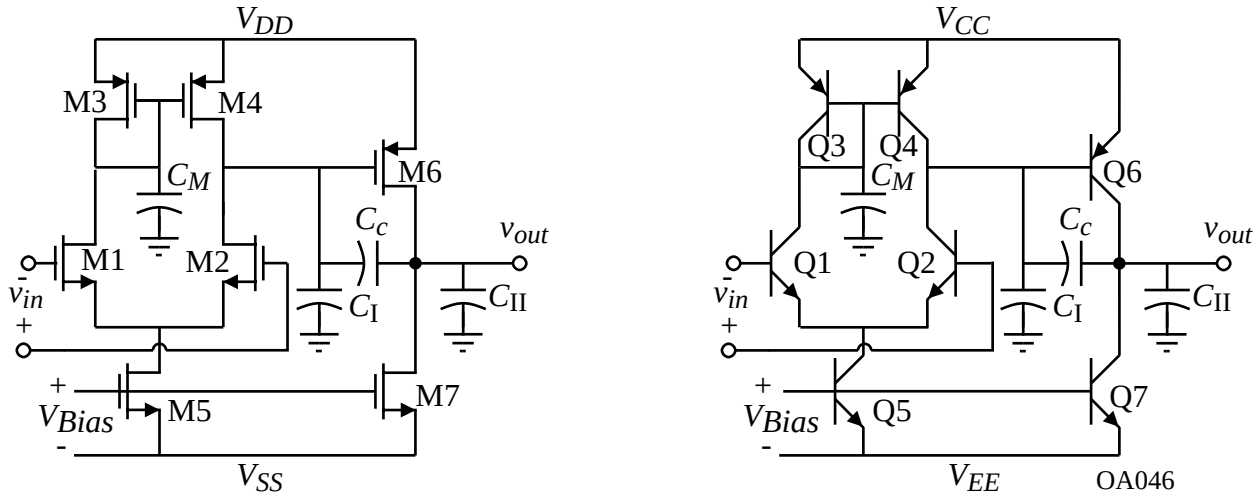
If we assume that $F(s) = 1$ (this is the worst case for stability considerations), then the above plot is the same as the loop gain.

Note that the phase margin is much less than 45°.

Therefore, the op amp must be compensated before using it in a closed-loop configuration.

MILLER COMPENSATION

Two-Stage Op Amp



The various capacitors are:

C_c = accomplishes the Miller compensation

C_M = capacitance associated with the first-stage mirror (mirror pole)

C_I = output capacitance to ground of the first-stage

C_{II} = output capacitance to ground of the second-stage

Simplification of the Compensated Two-Stage, Small-Signal Frequency Response Model

Use the CMOS op amp to illustrate:

1.) Assume that $g_{m3} >> g_{ds3} + g_{ds1}$

2.) Assume that $\frac{g_{m3}}{C_M} >> GB$

Therefore,

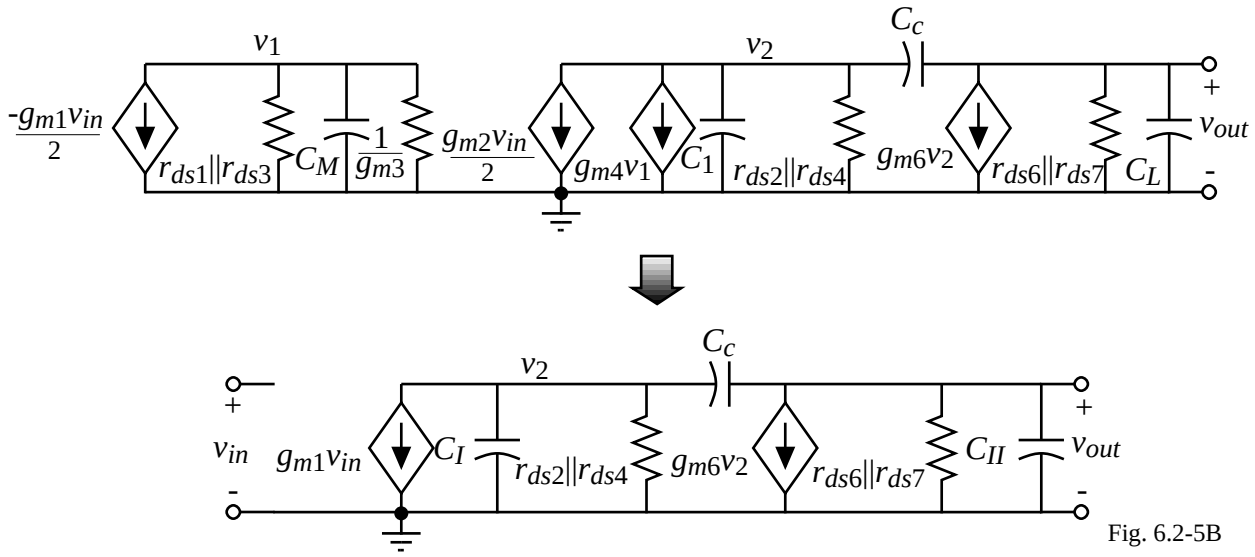


Fig. 6.2-5B

Same circuit holds for the BJT op amp with different component relationships.

General Two-Stage Frequency Response Analysis

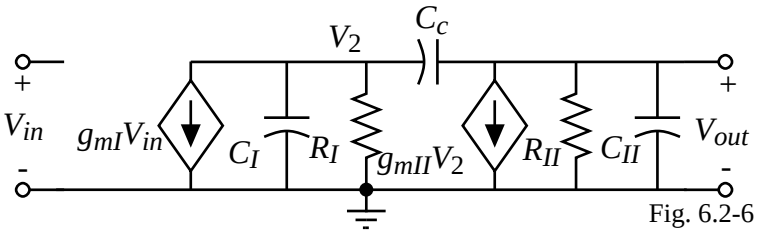


Fig. 6.2-6

where

$g_{mI} = g_{m1} = g_{m2}$, $R_I = r_{ds2}||r_{ds4}$, $C_I = C_1$

and

$g_{mII} = g_{m6}$, $R_{II} = r_{ds6}||r_{ds7}$, $C_{II} = C_2 = C_L$

Nodal Equations:

$$-g_{mI}V_{in} = [G_I + s(C_I + C_c)]V_2 - [sC_c]V_{out} \quad \text{and} \quad 0 = [g_{mII} - sC_c]V_2 + [G_{II} + sC_{II} + sC_c]V_{out}$$

Solving using Cramer's rule gives,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}(g_{mII} - sC_c)}{G_IG_{II} + s\,[G_{II}(C_I+C_{II}) + G_I(C_{II}+C_c) + g_{mII}C_c] + s^2[C_IC_{II} + C_cC_I + C_cC_{II}]}$$

$$= \frac{A_o[1 - s\,(C_c/g_{mII})]}{1 + s\,[R_I(C_I+C_{II}) + R_{II}(C_2+C_c) + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II})]}$$

where, $A_o = g_{mI}g_{mII}R_IR_{II}$

In general, $D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2} \quad \rightarrow \quad D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2}$, if $|p_2| >> |p_1|$

$$\therefore \quad \boxed{p_1 = \frac{-1}{R_I(C_I+C_{II}) + R_{II}(C_{II}+C_c) + g_{mII}R_IR_{II}C_c} \approx \frac{-1}{g_{mII}R_IR_{II}C_c}}, \quad \boxed{z = \frac{g_{mII}}{C_c}}$$

$$\boxed{p_2 = \frac{-[R_I(C_I+C_{II}) + R_{II}(C_{II}+C_c) + g_{mII}R_IR_{II}C_c]}{R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II})} \approx \frac{-g_{mII}C_c}{C_IC_{II} + C_cC_I + C_cC_{II}} \approx \frac{-g_{mII}}{C_{II}}} \text{ where } C_{II} > C_c > C_I.$$

Summary of Results for Miller Compensation of the Two-Stage Op Amp

There are three roots of importance:

1.) Right-half plane zero:

This root is very undesirable because it boosts the loop magnitude while decreasing the phase.

2.) Dominant left-half plane pole (the Miller pole):

$$z_1 = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

$$p_1 \spadesuit \frac{-1}{g_{mII}R_I R_{II}C_c} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}C_c}$$

This root accomplishes the desired compensation.

3.) Left-half plane output pole:

$$p_2 \spadesuit \frac{-g_{mII}}{C_{II}} \spadesuit \frac{-g_{m6}}{C_L}$$

This pole must be beyond the unity-gainbandwidth or the phase margin will not be satisfied.

Root locus plot of the Miller compensation:

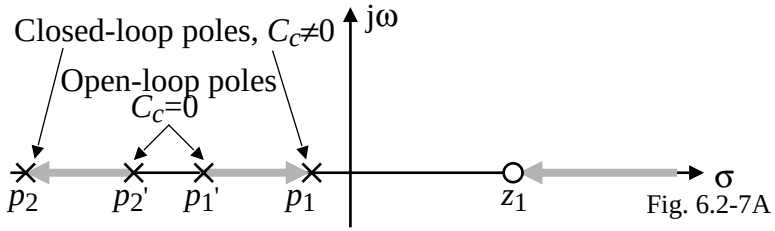


Fig. 6.2-7A

Compensated Open-Loop Frequency Response of the Two-Stage Op Amp

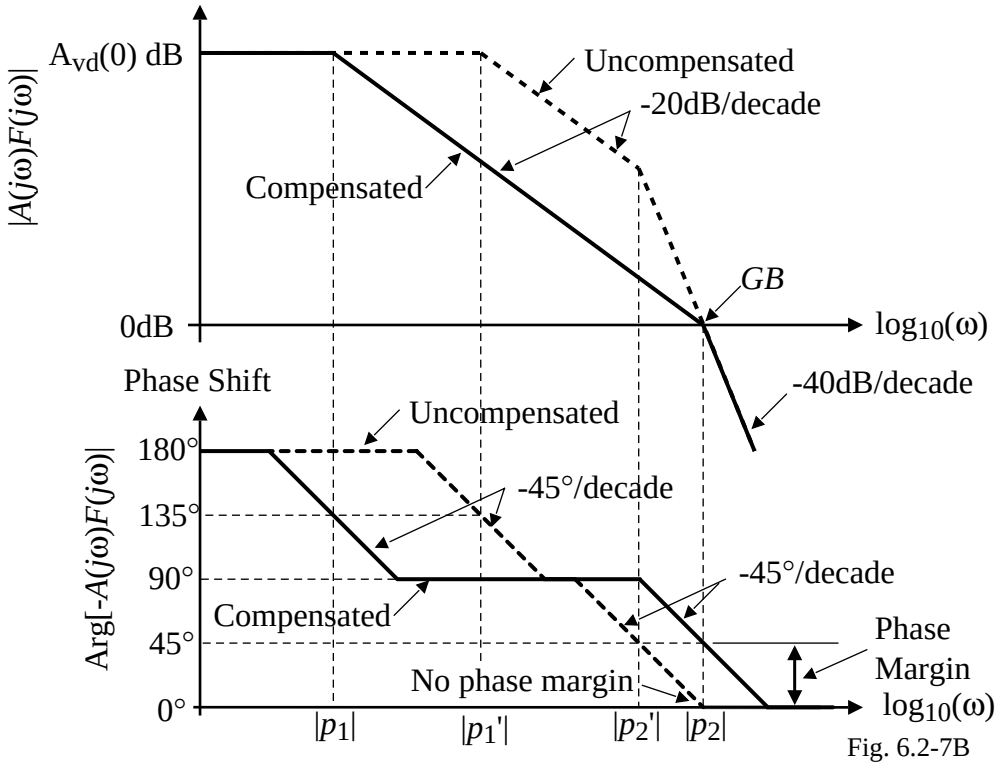


Fig. 6.2-7B

Note that the unity-gainbandwidth, *GB*, is

$$GB = A_{vd}(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\frac{1}{g_{mII}R_IR_{II}C_c} = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{g_{m2}}{C_c}$$

Conceptually, where do these roots come from?

1.) The Miller pole:

$$|p_1| \spadesuit \frac{1}{R_I(g_{m6}R_{II}C_c)}$$

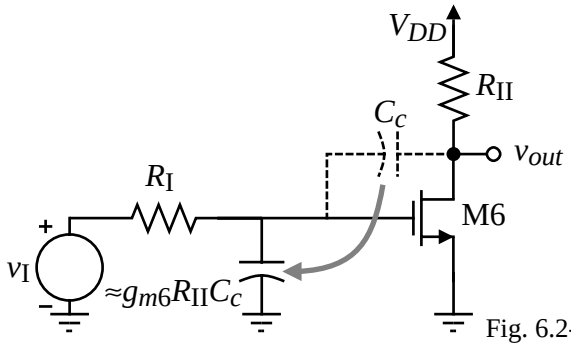


Fig. 6.2-9

2.) The left-half plane output pole:

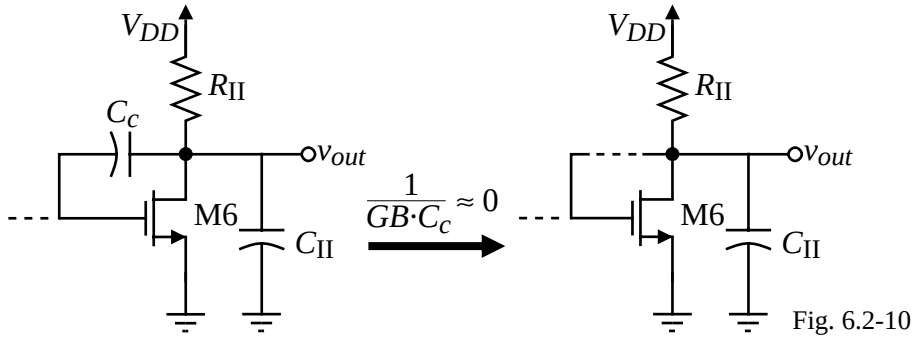


Fig. 6.2-10

$$|p_2| \spadesuit \frac{g_{m6}}{C_{II}}$$

3.) Right-half plane zero (*Zeros always arise from multiple paths from the input to output*):

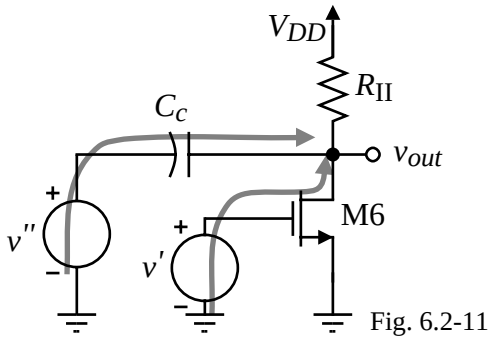


Fig. 6.2-11

$$v_{out} = \left(\frac{-g_{m6}R_{II}(1/sC_c)}{R_{II} + 1/sC_c}\right)v' + \left(\frac{R_{II}}{R_{II} + 1/sC_c}\right)v'' = \frac{-R_{II}\left(\frac{g_{m6}}{sC_c} - 1\right)}{R_{II} + 1/sC_c}v$$

where $v = v' = v''$.

Influence of the Mirror Pole

Up to this point, we have neglected the influence of the pole, p_3, associated with the current mirror of the input stage. If $|p_2| \approx |p_3|$, we have problems in compensation. This pole is given approximately as

$$p_3 \spadesuit \frac{-g_{m3}}{C_M}$$

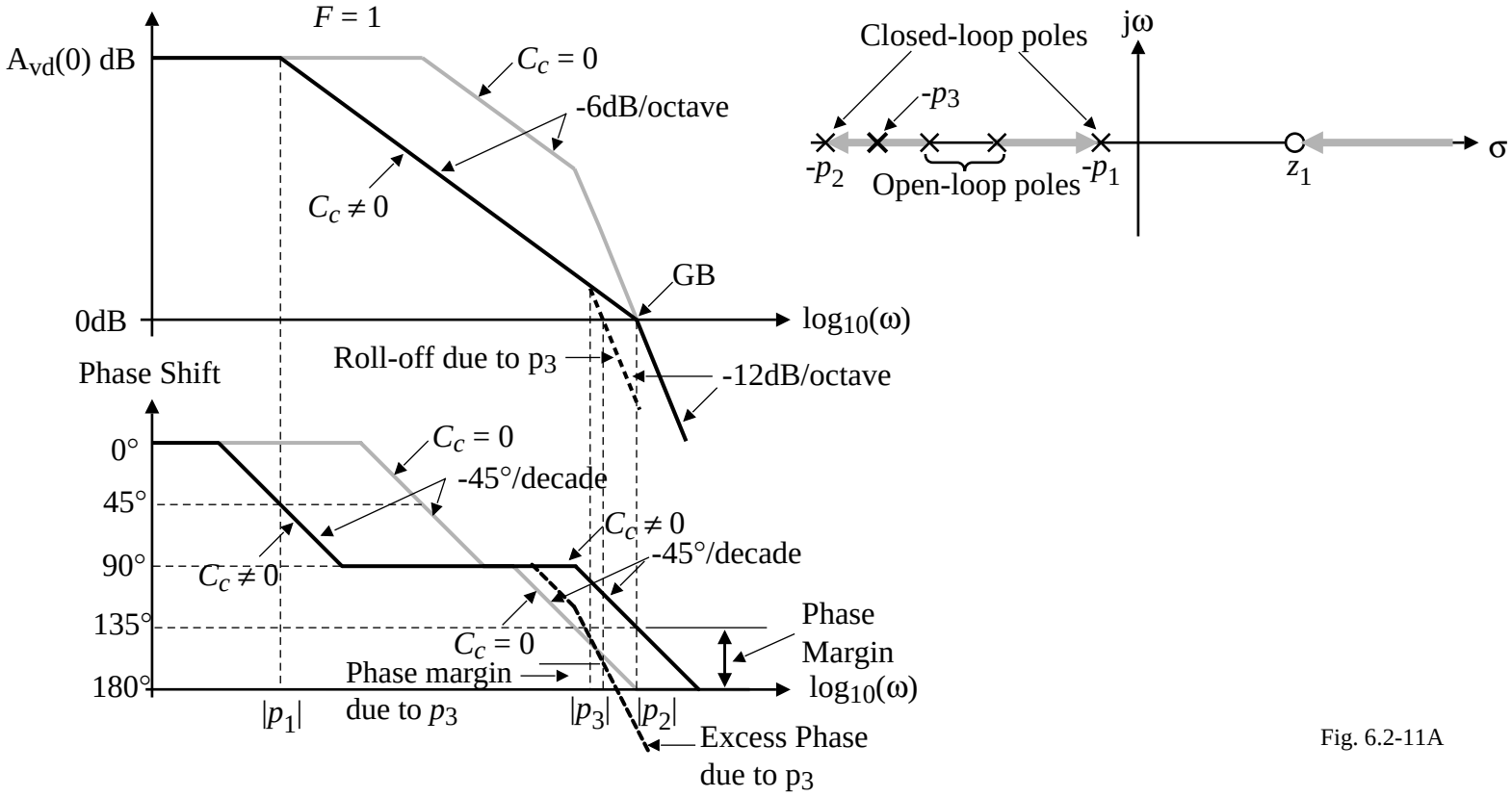


Fig. 6.2-11A

Summary of the Conditions for Stability of the Two-Stage Op Amp (Assuming $p_3 \geq GB$)

• Unity-gainbandwith is given as:

$$GB = A_v(0)\cdot|p_1| = \left(g_{mI}g_{mII}R_IR_{II}\right)\cdot\left(\frac{1}{g_{mII}R_IR_{II}C_c}\right) = \frac{g_{mI}}{C_c} = \left(g_{m1}g_{m2}R_1R_2\right)\cdot\left(\frac{1}{g_{m2}R_1R_2C_c}\right) = \frac{g_{m1}}{C_c}$$

• The requirement for 45° phase margin is:

$$\pm 180° - \text{Arg}[AF] = \pm 180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45°$$

$$135° \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1) = 90° + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + 5.7°$$

$$39.3° \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow \boxed{|p_2| \text{ ε } 1.22GB}$$

• The requirement for 60° phase margin:

$$\boxed{|p_2| \text{ ε } 2.2GB \text{ if } z \text{ ε } 10GB}$$

• If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{m6}}{C_c} > \frac{10g_{m1}}{C_c} \Rightarrow \boxed{g_{m6} > 10g_{m1}} \quad \text{and} \quad \frac{g_{m6}}{C_2} > \frac{2.2g_{m1}}{C_c} \Rightarrow \boxed{C_c > 0.22C_2}$$

Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.

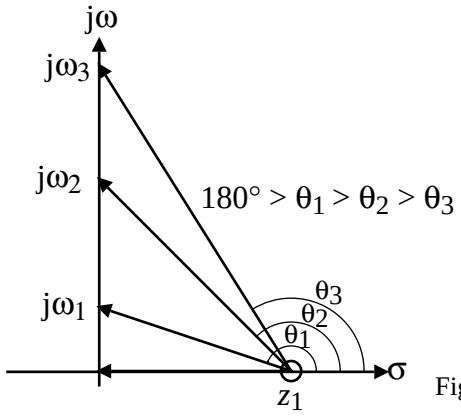


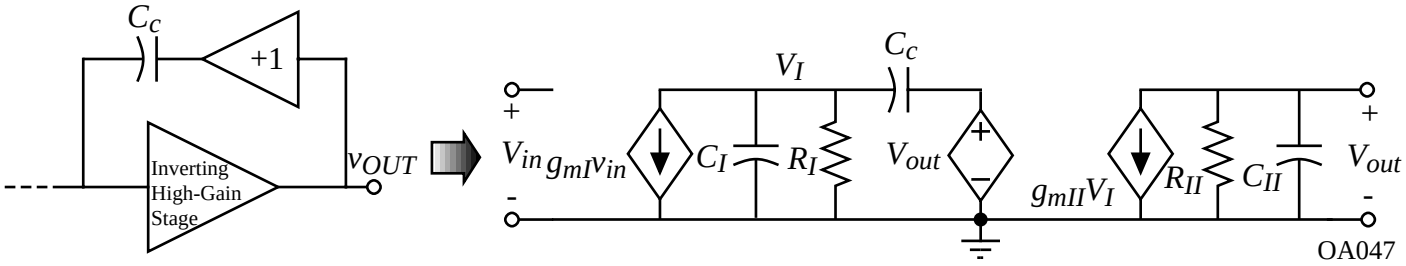
Fig. 6.2-11B

Solution of the problem:

If zeros are caused by two paths to the output, then eliminate one of the paths.

Use of Buffer to Eliminate the Feedforward Path through the Miller Capacitor

Model:



The transfer function is given by the following equation,

$$\frac{V_o(s)}{V_{\text{in}}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})}{1 + s[R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}C_{II}(C_I + C_c)]}$$

Using the technique as before to approximate p_1 and p_2 results in the following

$$p_1 \cong \frac{-1}{R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c} \cong \frac{-1}{g_{mII}R_IR_{II}C_c}$$

and

$$p_2 \cong \frac{-g_{mII}C_c}{C_{II}(C_I + C_c)}$$

Comments:

Poles are approximately what they were before with the zero removed.

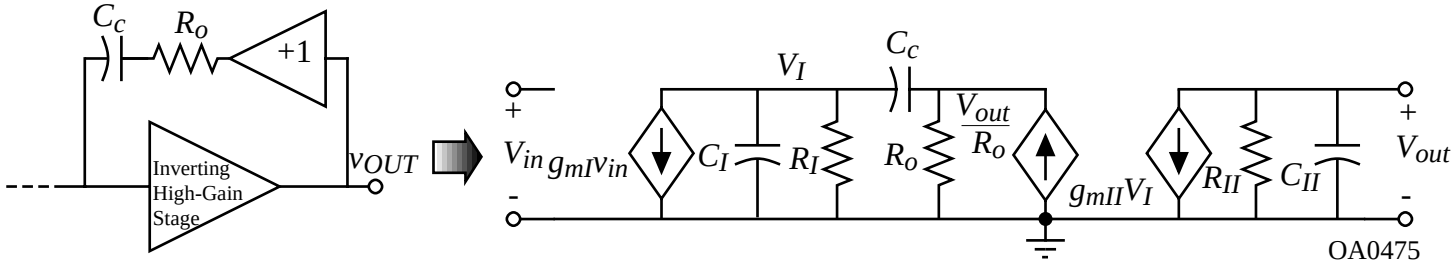
For 45° phase margin, $|p_2|$ must be greater than GB

For 60° phase margin, $|p_2|$ must be greater than $1.73GB$

Use of Buffer with Finite Output Resistance to Eliminate the RHP Zero

Assume that the unity-gain buffer has an output resistance of R_o.

Model:



It can be shown that if the output resistance of the buffer amplifier, R_o, is not neglected that another pole occurs at,

$$p_4 \cong \frac{-1}{R_o[C_I C_c/(C_I + C_c)]}$$

and a LHP zero at

$$z_2 \cong \frac{-1}{R_o C_c}$$

Closer examination shows that if a resistor, called a *nulling resistor*, is placed in series with C_c that the RHP zero can be eliminated or moved to the LHP.

Use of Nulling Resistor to Eliminate the RHP Zero (or turn it into a LHP zero)†

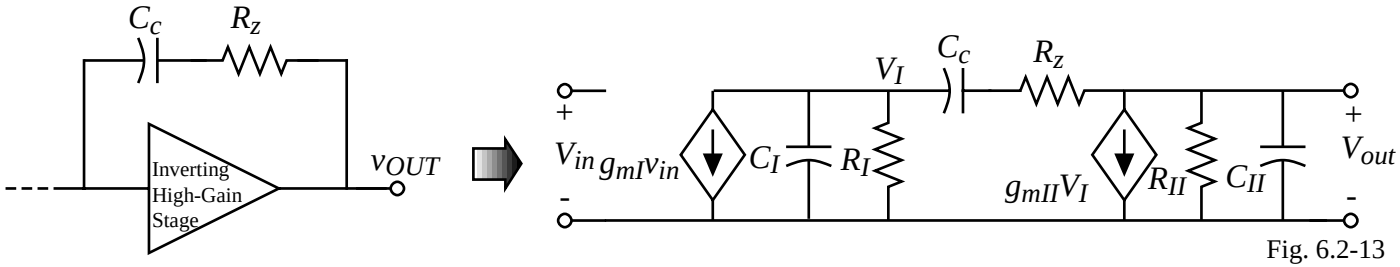


Fig. 6.2-13

Nodal equations:

$$g_{mI}V_{\text{in}} + \frac{V_I}{R_I} + sC_IV_I + \left(\frac{sC_c}{1+sC_cR_z}\right)(V_I - V_{out}) = 0 \qquad g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_{out} + \left(\frac{sC_c}{1+sC_cR_z}\right)(V_{out} - V_I) = 0$$

Solution:

$$\frac{V_{out}(s)}{V_{\text{in}}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_zC_c]\}}{1 + bs + cs^2 + ds^3}$$

where

$$a = g_{mI}g_{mII}R_IR_{II}$$
$$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_IR_{II}C_c + R_zC_c$$
$$c = [R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II}) + R_zC_c(R_IC_I + R_{II}C_{II})]$$
$$d = R_IR_{II}R_zC_IC_{II}C_c$$

† William J. Parrish, "An Ion Implanted CMOS Amplifier for High Performance Active Filters", Ph.D. Dissertation, 1976, Univ. of Calif., Santa Barbara, CA.

Use of Nulling Resistor to Eliminate the RHP - Continued

If R_z is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots of the above transfer function can be approximated as

$$p_1 \cong \frac{-1}{(1+g_{mII}R_{II})R_IC_c} \cong \frac{-1}{g_{mII}R_{II}R_IC_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_IC_{II}+C_cC_I+C_cC_{II}} \cong \frac{-g_{mII}}{C_{II}}$$

$$p_4 = \frac{-1}{R_zC_I}$$

and

$$z_1 = \frac{1}{C_c(1/g_{mII}-R_z)}$$

Note that the zero can be placed anywhere on the real axis.

Conceptual Illustration of the Nulling Resistor Approach

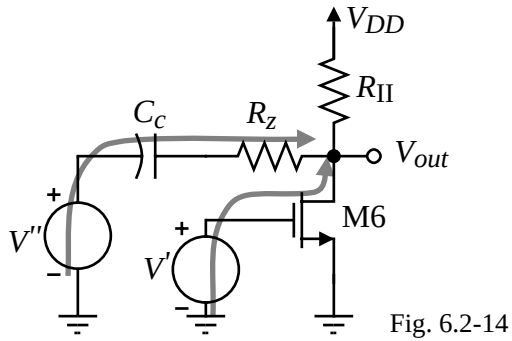


Fig. 6.2-14

The output voltage, V_{out}, can be written as

$$V_{out} = \frac{-g_{m6}R_{II}\left(R_z + \frac{1}{sC_c}\right)}{R_{II} + R_z + \frac{1}{sC_c}} V' + \frac{R_{II}}{R_{II} + R_z + \frac{1}{sC_c}} V'' = \frac{-R_{II}\left[g_{m6}R_z + \frac{g_{m6}}{sC_c} - 1\right]}{R_{II} + R_z + \frac{1}{sC_c}} V$$

when $V = V' = V''$.

Setting the numerator equal to zero and assuming $g_{m6} = g_{mII}$ gives,

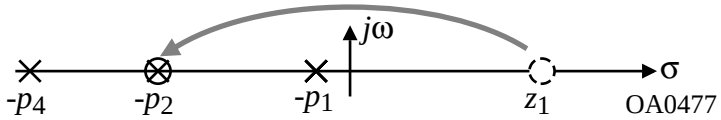
$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, p_2

We desire that $z_1 = p_2$ in terms of the previous notation.

Therefore,

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$



The value of R_z can be found as

$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)(1/g_{mII})$$

With p_2 canceled, the remaining roots are p_1 and p_4(the pole due to R_z) . For unity-gain stability, all that is required is that

$$|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_IC_c} = \frac{g_{mI}}{C_c}$$

and

$$(1/R_zC_I) > (g_{mI}/C_c) = GB$$

Substituting R_z into the above inequality and assuming $C_{II} >> C_c$ results in

$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}} C_IC_{II}}$$

This procedure gives excellent stability for a fixed value of C_{II} ($\approx C_L$).

Unfortunately, as C_L changes, p_2 changes and the zero must be readjusted to cancel p_2.

Increasing the Magnitude of the Output Pole[†]

The magnitude of the output pole , p_2, can be increased by introducing gain in the Miller capacitor feedback path. For example,

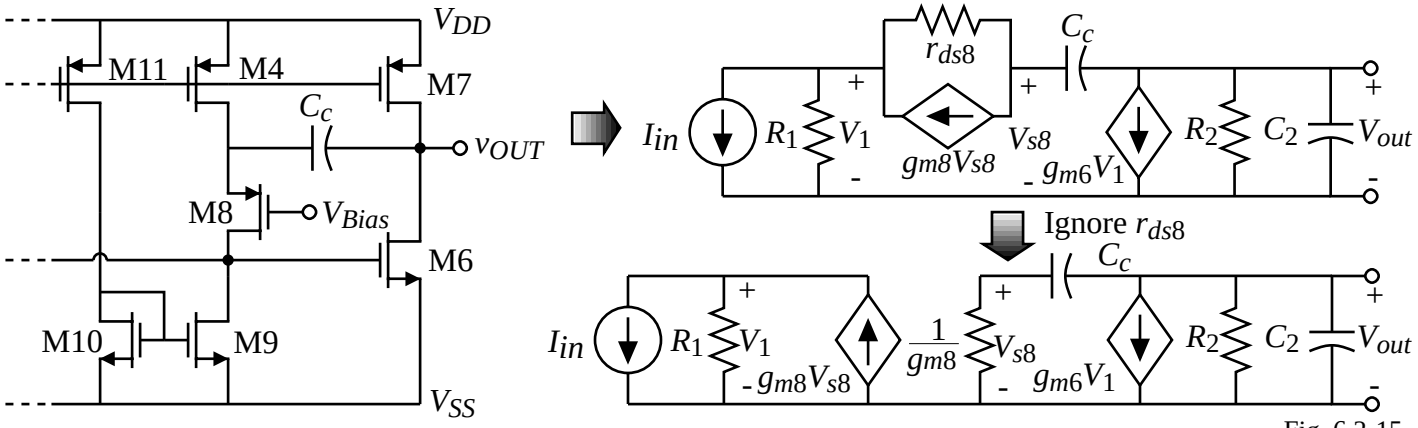


Fig. 6.2-15

The resistors R_1 and R_2 are defined as

$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \quad \text{and} \quad R_2 = \frac{1}{g_{ds6} + g_{ds7}}$$

where transistors M2 and M4 are the output transistors of the first stage.

Nodal equations:

$$I_{in} = G_1 V_1 - g_{m8} V_{s8} = G_1 V_1 - \left(\frac{g_{m8} s C_c}{g_{m8} + s C_c} \right) V_{out} \qquad \text{and} \quad 0 = g_{m6} V_1 + \left[G_2 + s C_2 + \frac{g_{m8} s C_c}{g_{m8} + s C_c} \right] V_{out}$$

[†] B.K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. of Solid-State Circuits*, Vol. SC-18, No. 6 (Dec. 1983) pp. 629-633.

Increasing the Magnitude of the Output Pole - Continued

Solving for the transfer function V_{out}/I_{in} gives,

$$\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_1 G_2}\right)\left[\frac{\left(1+\frac{sC_c}{g_{m8}}\right)}{1+s\left[\frac{C_c}{g_{m8}}+\frac{C_2}{G_2}+\frac{C_c}{G_2}+\frac{g_{m6}C_c}{G_1G_2}\right]+s^2\left(\frac{C_cC_2}{g_{m8}G_2}\right)}\right]$$

Using the approximate method of solving for the roots of the denominator illustrated earlier gives

$$p_1 = \frac{-1}{\frac{C_c}{g_{m8}}+\frac{C_c}{G_2}+\frac{C_2}{G_2}+\frac{g_{m6}C_c}{G_1G_2}} \approx \frac{-6}{g_{m6}r_{ds}{}^2C_c}$$

and

$$p_2 \approx \frac{-\frac{g_{m6}r_{ds}{}^2C_c}{6}}{\frac{C_cC_2}{g_{m8}G_2}} = \frac{g_{m8}r_{ds}{}^2G_2}{6}\left(\frac{g_{m6}}{C_2}\right) = \left(\frac{g_{m8}r_{ds}}{3}\right)|p_2'|$$

where all the various channel resistance have been assumed to equal r_{ds} and p_2' is the output pole for normal Miller compensation.

Result:

Dominant pole is approximately the same and the output pole is increased by roughly $g_m r_{ds}$.

Concept Behind the Increasing of the Magnitude of the Output Pole

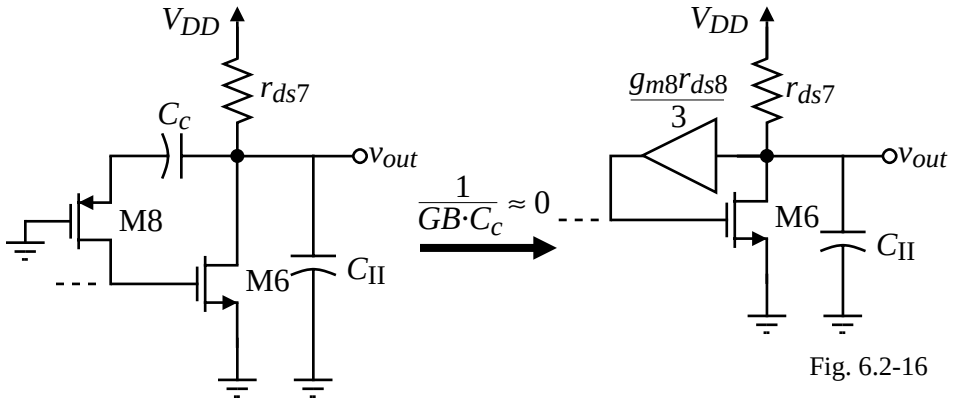


Fig. 6.2-16

$$R_{out} = r_{ds7} \| \left(\frac{3}{g_{m6} g_{m8} r_{ds8}} \right) \spadesuit \frac{3}{g_{m6} g_{m8} r_{ds8}}$$

Therefore, the output pole is approximately,

$$|p_2| \spadesuit \frac{g_{m6} g_{m8} r_{ds8}}{3 C_{II}}$$

FEEDFORWARD COMPENSATION

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

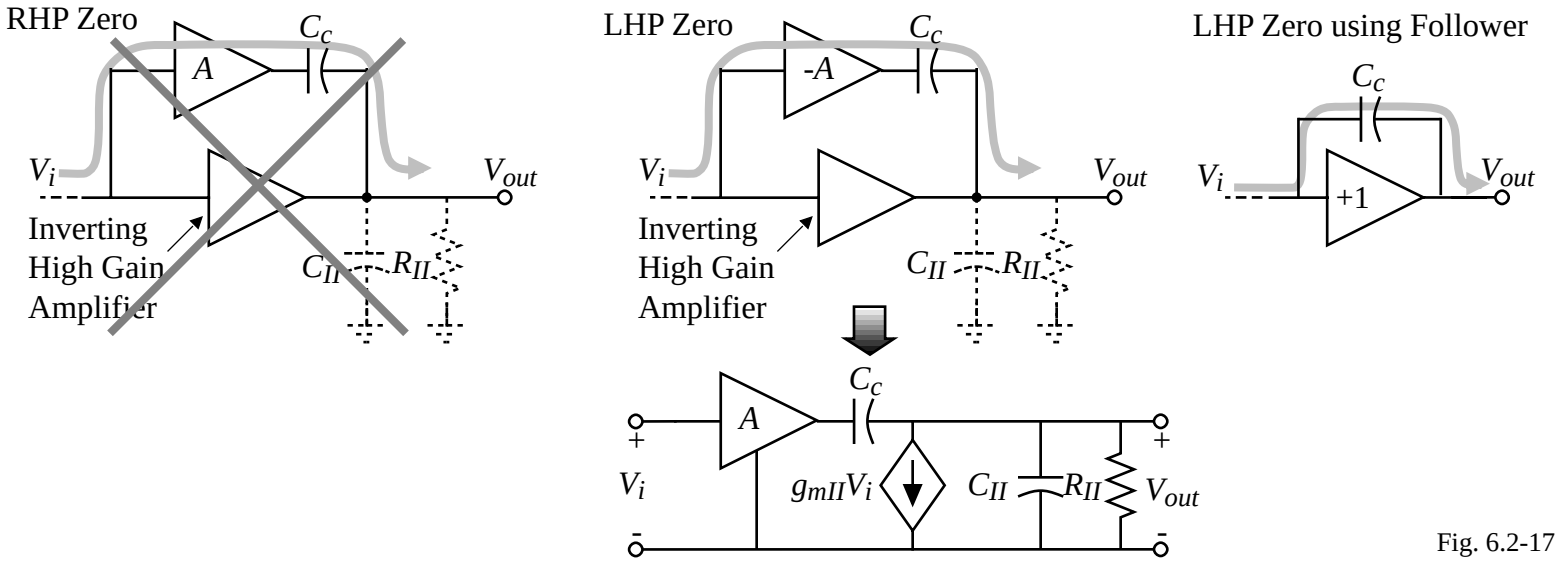


Fig. 6.2-17

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}}\left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]}\right)$$

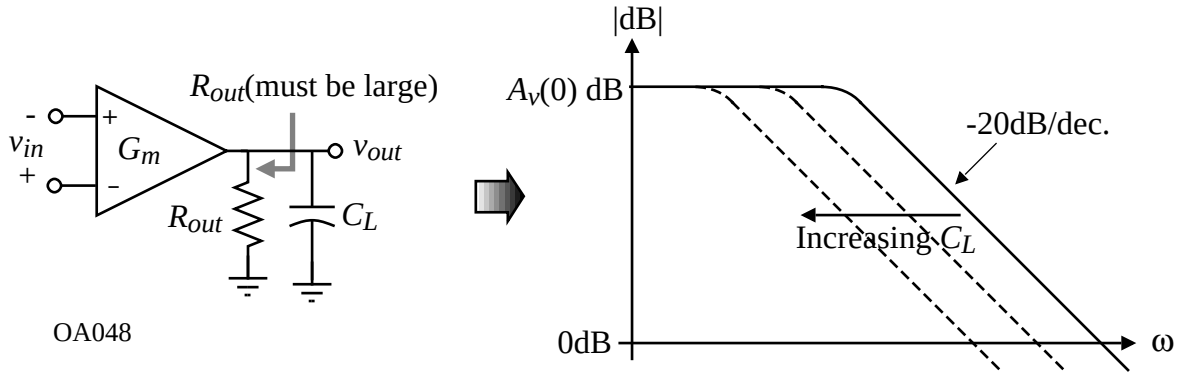
To use the LHP zero for compensation, a compromise must be observed.

- Placing the zero below *GB* will lead to boosting of the loop gain which could deteriorate the phase margin.
- Placing the zero above *GB* will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward compensation.

SELF-COMPENSATED OP AMPS

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback)



Voltage gain:

$$\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}$$

Dominant pole:

$$p_1 = \frac{-1}{R_{out}C_L}$$

Unity-gainbandwidth:

$$GB = A_v(0)\cdot|p_1| = \frac{G_m}{C_L}$$

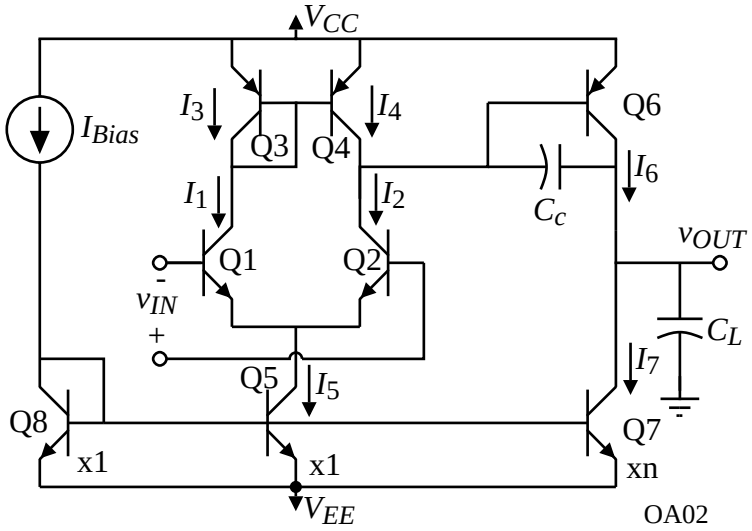
Stability:

Large load capacitors simply reduce the *GB* and the phase is 90° at the unity gain frequency

SIMPLE TWO-STAGE OP AMPS

BJT Two-Stage Op Amp

Circuit:



DC Conditions:

$I_5 = I_{bias}$, $I_1 = I_2 = 0.5I_5 = 0.5I_{bias}$, $I_7 = I_6 = nI_{Bias}$

$V_{icm}(\text{max}) = V_{CC} - V_{EB3} - V_{CE1}(\text{sat}) + V_{BE1}$

$V_{icm}(\text{min}) = V_{EE} + V_{CE5}(\text{sat}) + V_{BE1}$

$V_{out}(\text{max}) = V_{CC} - V_{EC6}(\text{sat})$

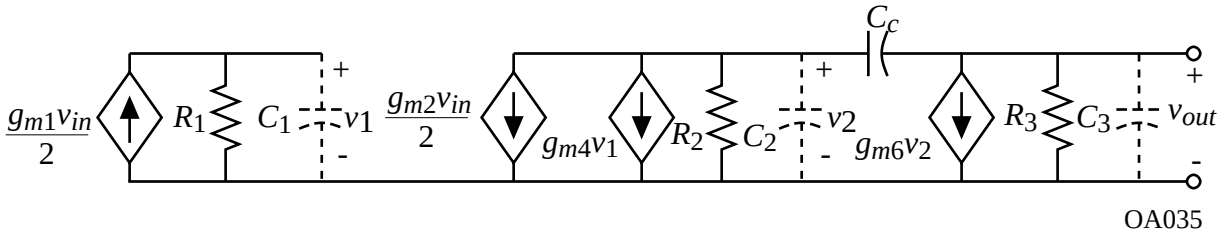
$V_{out}(\text{min}) = V_{EE} + V_{CE7}(\text{sat})$

Notice that the output stage is class A $\Rightarrow$ $I_{sink} = I_7$ and $I_{source} = \beta_F I_5 - I_7$

Two-Stage BJT Op Amp - Continued

Small Signal Performance:

Assuming differential mode operation, we can write the small-signal model as,



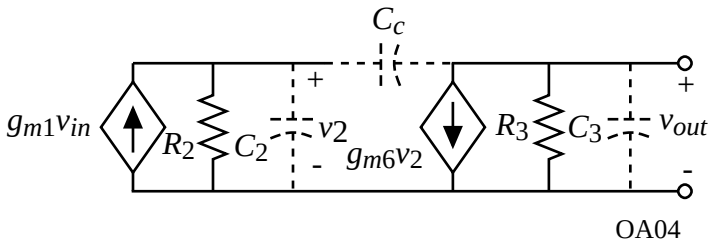
where,

$$R_1 = \frac{1}{g_{m3}} \| r_{\pi 3} \| r_{\pi 4} \| r_{o3} \approx \frac{1}{g_{m3}} \qquad R_2 = r_{\pi 6} \| r_{o2} \| r_{o4} \approx r_{\pi 6} \qquad \text{and} \qquad R_3 = r_{o6} \| r_{o7}$$

$$C_1 = C_{\pi 3} + C_{\pi 4} + C_{cs1} + C_{cs3} \qquad C_2 = C_{\pi 6} + C_{cs2} + C_{cs4} \qquad \text{and} \quad C_3 = C_L + C_{cs6} + C_{cs7}$$

Note that we have ignored the base-collector capacitors, C_μ, except for M6, which is called C_c.

Assuming the pole due to C_1 is much greater than the poles due to C_2 and C_3 gives



Two-Stage BJT Op Amp - Continued

Summary of the small signal performance:

Midband performance-

$A_o = g_{mI}g_{mII}R_IR_{II} \approx g_{m1}g_{m6}r_{\pi 6}(r_{o6}||r_{o7}) = g_{m1}\beta_{F6}(r_{o6}||r_{o7}), \quad R_{out} = r_{o6}||r_{o7}, \quad R_{in} = 2r_{\pi 1}$

Roots-

$$\text{Zero} = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

Poles at $p_1 \approx \dfrac{-1}{g_{mII}R_IR_{II}C_c} = \dfrac{-1}{g_{m6}r_{\pi 6}(r_{o6}||r_{o7})C_c} = \dfrac{-g_{m1}}{A_oC_c}$ and $p_2 \spadesuit \dfrac{-g_{mII}}{C_{II}} \spadesuit \dfrac{-g_{m6}}{C_L}$

Assume that β_F =100, g_{m1} = 1mS, g_{m6} = 10mS, $r_{o6} = r_{o7}$ = 0.5MΩ, C_c = 5pF and C_L = 10pF:

A_o = (1mS)(100)(250kΩ) = 25,000V/V, $R_{in} = 2(\beta_F/g_{m1})$ 2(100kΩ) = 200kΩ, R_{out} = 250kΩ

$$\text{Zero} = \frac{10\text{mS}}{5\text{pF}} = 2\text{x}10^9 \text{ rads/sec or } 318.3\text{MHz},$$

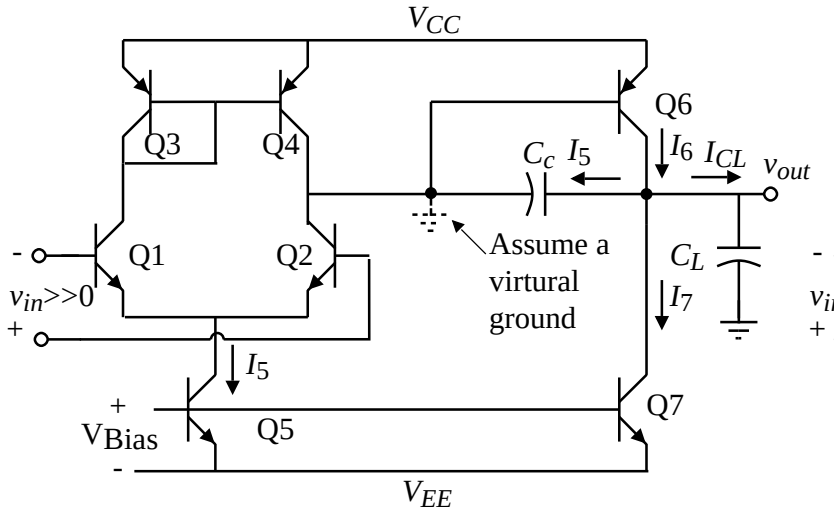
$$p_1 = \frac{-1\text{mS}}{(25{,}000)5\text{pF}} = \frac{-2\text{x}10^8}{25{,}000} = -8000 \text{ rads/sec or } 1273\text{Hz},$$

and $$p_2 = \frac{-10\text{mS}}{10\text{pF}} = 10^9 \text{ rads/sec or } 159.15\text{MHz}$$

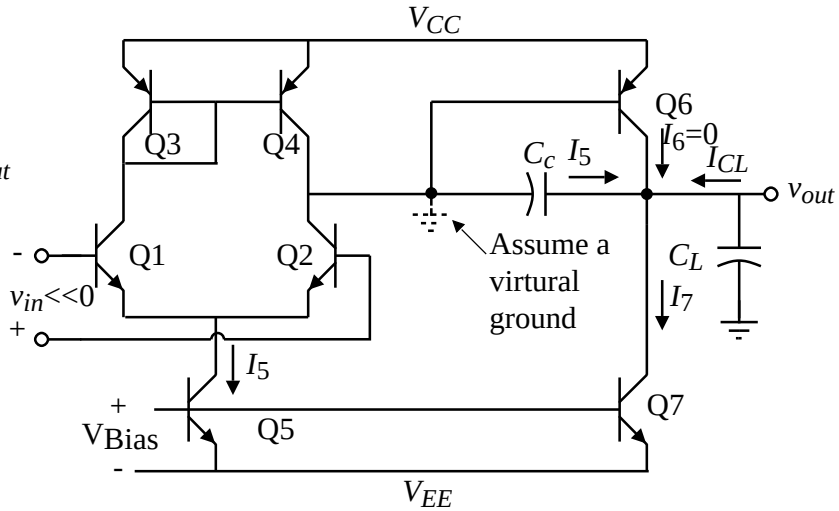
Slew Rate of the Two-Stage BJT Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{lim} = C\frac{dv_C}{dt}$$ where v_C is the voltage across the capacitor C.



Positive Slew Rate



Negative Slew Rate OA07

$$SR^+ = \min\left[\frac{I_5}{C_c}, \frac{I_6\text{-}I_5\text{-}I_7}{C_L}\right] = \frac{I_5}{C_c} \text{ because } I_6 >> I_5$$

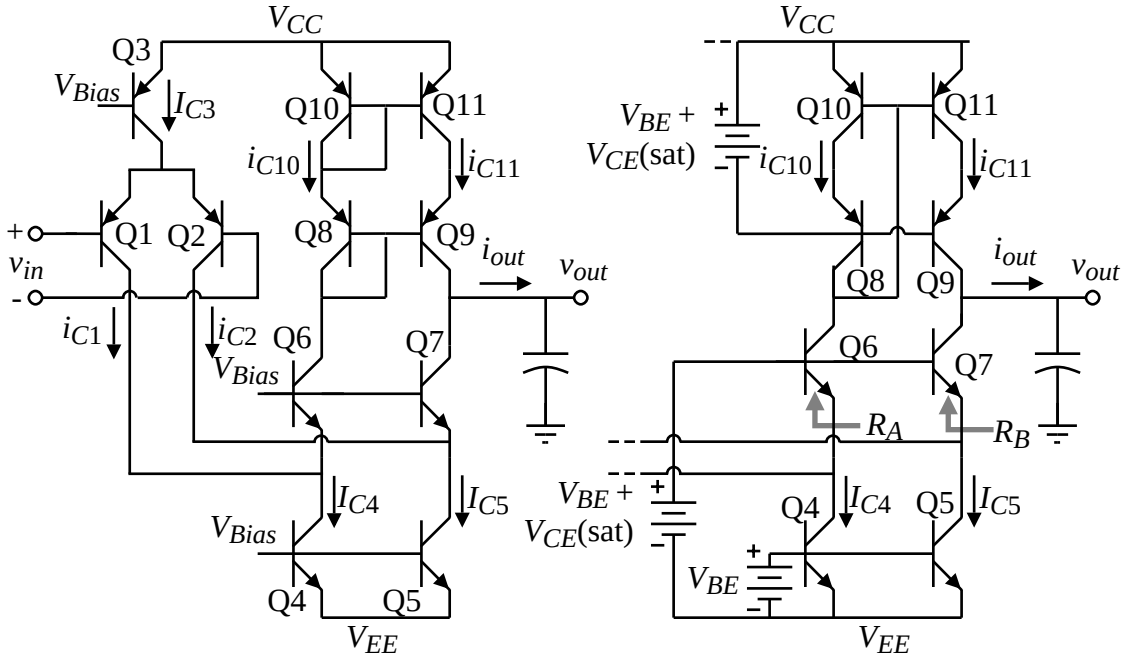
$$SR^- = \min\left[\frac{I_5}{C_c}, \frac{I_7\text{-}I_5}{C_L}\right] = \frac{I_5}{C_c} \text{ if } I_7 >> I_5.$$

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5, then the slew rate of the two-stage op amp should be,

$$SR = \frac{I_5}{C_c}$$

Folded-Cascode BJT Op Amp

Circuit



Simplified circuit Biasing details of the output OA08

DC Conditions:

$I_3 = I_{bias}$, $I_1 = I_2 = 0.5I_5 = 0.5I_{bias}$, $I_4 = I_5 = kI_{Bias}$ $I_{10} = I_{11} = kI_{Bias} - 0.5I_{bias}$ (k>1)

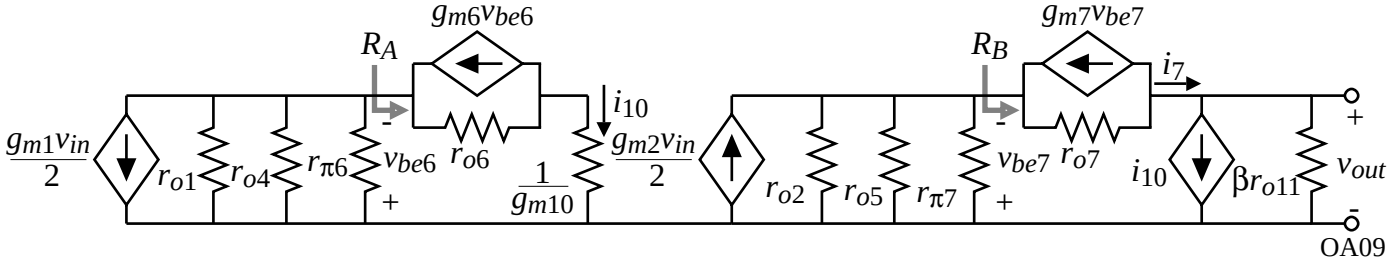
$V_{icm}(\max) = V_{CC} - V_{CE3}(\text{sat}) + V_{EB1}$ $V_{icm}(\min) = V_{EE} + V_{CE4}(\text{sat}) + V_{EC1}(\text{sat}) - V_{BE1}$

$V_{out}(\max) = V_{CC} - V_{EC9}(\text{sat}) - V_{EC11}(\text{sat})$ $V_{out}(\min) = V_{EE} + V_{CE5}(\text{sat}) + V_{CE7}(\text{sat})$

Notice that the output stage is push-pull $\Rightarrow$ I_{sink} and I_{source} are limited by the base current.

Folded-Cascode BJT Op Amp - Continued

Small-Signal Analysis:



where $R_A \approx 1/g_{m6}$ and $R_B \approx \dfrac{r_{o7}+\beta_P r_{o11}/2}{1+g_{m7}r_{o7}} \spadesuit \dfrac{r_{\pi 7}}{2}$ if $r_{o7} \approx r_{o11}$

$$i_{10} \approx \frac{-g_{m1}r_{\pi 6}v_{in}}{2(r_{\pi 6}+R_A)} \spadesuit \frac{-g_{m1}v_{in}}{2} \qquad i_7 \approx \frac{g_{m2}r_{\pi 7}v_{in}}{2(r_{\pi 7}+R_B)} \spadesuit \frac{g_{m2}r_{\pi 7}v_{in}}{2(r_{\pi 7}+0.5r_{\pi 7})} = \frac{g_{m2}v_{in}}{3}$$

$$\therefore \quad v_{out} = (i_7 - i_{10})\beta_P R_{out} v_{in} = \frac{5}{6}(g_{m1}\beta_P R_{out})v_{in} \quad \text{if } g_{m1} = g_{m2} \Rightarrow \quad \frac{v_{out}}{v_{in}} = \frac{5}{6}(g_{m1}\beta_P R_{out})$$

$R_{out} = \beta_P r_{o11} \| [\beta_N (r_{o5} \| r_{o2})]$ and $R_{in} = 2r_{\pi 1}$

Assume that β_{FN} =100, β_{FP} =50, $g_{m1} = g_{m2}$ =1mS, r_{oN} = 1MΩ, and r_{oP} = 0. 5MΩ:

$$\frac{v_{out}}{v_{in}} = 14{,}285\text{V/V} \qquad R_{out} = 14.285\ \text{MΩ} \qquad \text{and} \quad R_{in} = 100\text{kΩ}$$

Folded-Cascode BJT Op Amp - Continued

Frequency response includes only 1 dominant pole at the output (self-compensation),

$$p_1 = \frac{-1}{R_{out} C_L}$$

There are other poles but we shall assume that they are less than *GB*

If C_L = 25pF, then $|p_1|$ = 2800 rads/sec. or 446Hz $\Rightarrow$ *GB* = 6.371 MHz

Checking some of the nondominant poles gives:

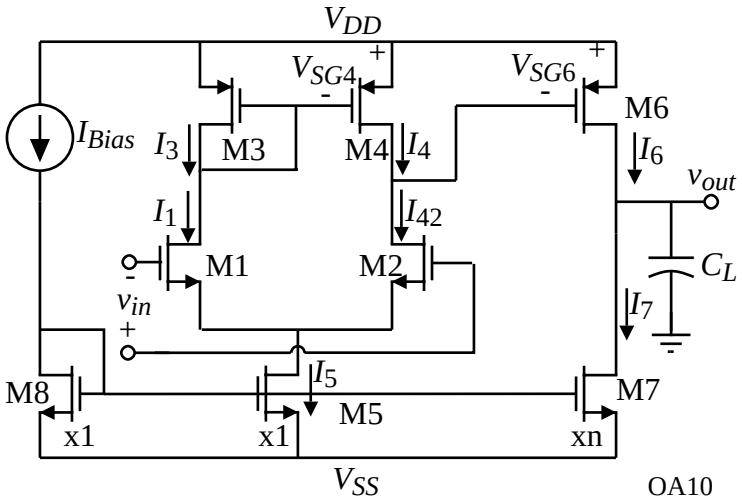
$$|p_A| = \frac{1}{R_A C_A} = \frac{g_{m6}}{C_A} \Rightarrow \text{159MHz if } C_A = \text{1pf (the capacitance to ac ground at the emitter of Q6)}$$

$$|p_B| = \frac{1}{R_B C_B} = \frac{2}{r_{\pi 7} C_B} \Rightarrow \text{6.37MHz if } C_B = \text{1pf (the capacitance to ac ground at the emitter of Q7)}$$

This indicates that for small capacitive loads, this op amp will suffer from higher poles with respect to phase margin. Capacitive loads greater than 25pF, will have better stability (and less *GB*).

Two-Stage CMOS Op Amp

Circuit:



DC Conditions:

$I_5 = I_{bias}$, $I_1 = I_2 = 0.5I_5 = 0.5I_{bias}$, $I_7 = I_6 = nI_{Bias}$

$V_{icm}(\max) = V_{DD} - V_{SG3} + V_{T1}$

$V_{icm}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1}$

$V_{out}(\max) = V_{DD} - V_{SD6}(\text{sat})$

$V_{out}(\min) = V_{SS} + V_{DS7}(\text{sat})$

Notice that the output stage is class A $\Rightarrow$ $I_{sink} = I_7$ and $I_{source} = \frac{K_N' W_6}{2L_6}(V_{DD}-V_{SS}-V_T)^2 - I_7$

DC Balance Conditions for the Two-Stage Op Amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

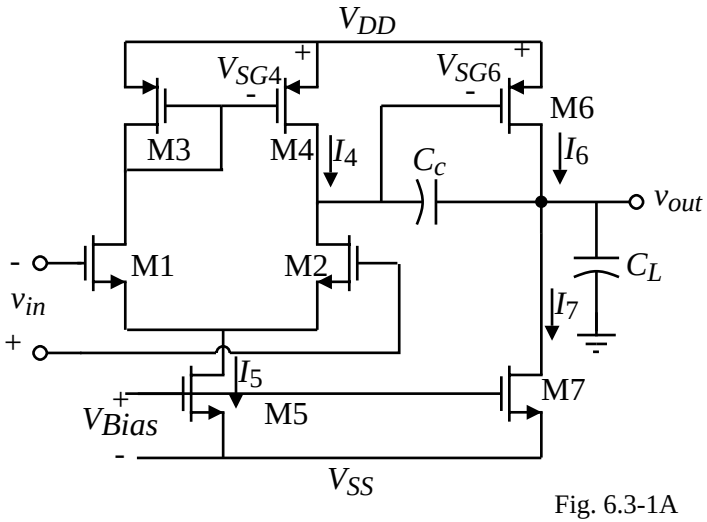


Fig. 6.3-1A

1.) First *assume* that $V_{SG4} = V_{SG6}$. This will cause "proper mirroring" in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is "guaranteed" to be in saturation.

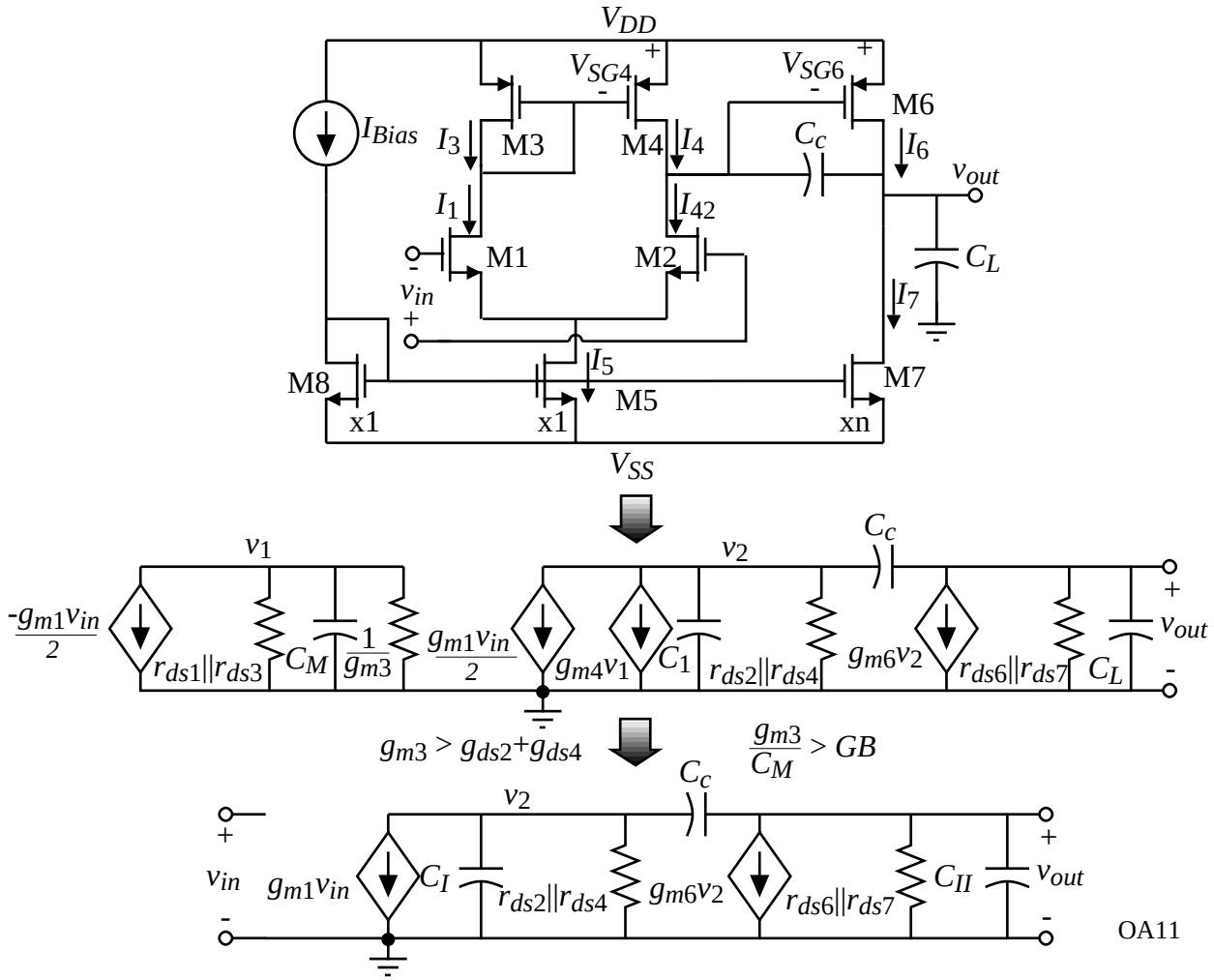
2.) Let $S_i \equiv \frac{W_i}{L_i}$, *if* $V_{SG4} = V_{SG6}$, then $I_6 = \left(\frac{S_6}{S_4}\right) I_4$

3.) However, $I_7 = \left(\frac{S_7}{S_5}\right) I_5 = \left(\frac{S_7}{S_5}\right)(2I_4)$

4.) For balance, I_6 must equal $I_7 \Rightarrow \boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}}$ which is called the "balance conditions"

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.

Small-Signal Performance of the Two-Stage CMOS Op Amp



Small-Signal Performance of the Two-Stage CMOS Op Amp

Summary of the small signal performance:

Midband performance-

$$A_o = g_{mI}g_{mII}R_IR_{II} \approx g_{m1}g_{m6}(r_{ds2}||r_{ds4})(r_{ds6}||r_{ds7}), \quad R_{out} = r_{ds6}||r_{ds7}, \quad R_{in} = \infty$$

Roots-

$$\text{Zero} = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

$$\text{Poles at} \quad p_1 \spadesuit \frac{-1}{g_{mII}R_IR_{II}C_c} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}C_c} \qquad \text{and} \qquad p_2 \spadesuit \frac{-g_{mII}}{C_{II}} \spadesuit \frac{-g_{m6}}{C_L}$$

Assume that $g_{m1} = 100\mu S$, $g_{m6} = 1mS$, $r_{ds2} = r_{ds4} = 2M\Omega$ $r_{ds6} = r_{ds7} = 0.5M\Omega$, $C_c = 5pF$ and $C_L = 10pF$:

$$A_o = (100\mu S)(1M\Omega)(1000\mu S)(0.25M\Omega) = 25{,}000V/V, \quad R_{in} = \infty, \quad R_{out} = 250k\Omega$$

$$\text{Zero} = \frac{1000\mu S}{5pF} = 2x10^8 \text{ rads/sec or } 31.83MHz,$$

$$p_1 = \frac{-1}{(1mS)(1M\Omega)(0.25M\Omega)(5pF)} = -800 \text{ rads/sec or } 127.3Hz, \qquad GB = 3.178MHz$$

$$\text{and} \qquad p_2 = \frac{-1000\mu S}{10pF} = 10^8 \text{ rads/sec or } 15.915MHz$$

Slew Rate of a Two-Stage CMOS Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{lim} = C\frac{dv_C}{dt}$$ where v_C is the voltage across the capacitor C.

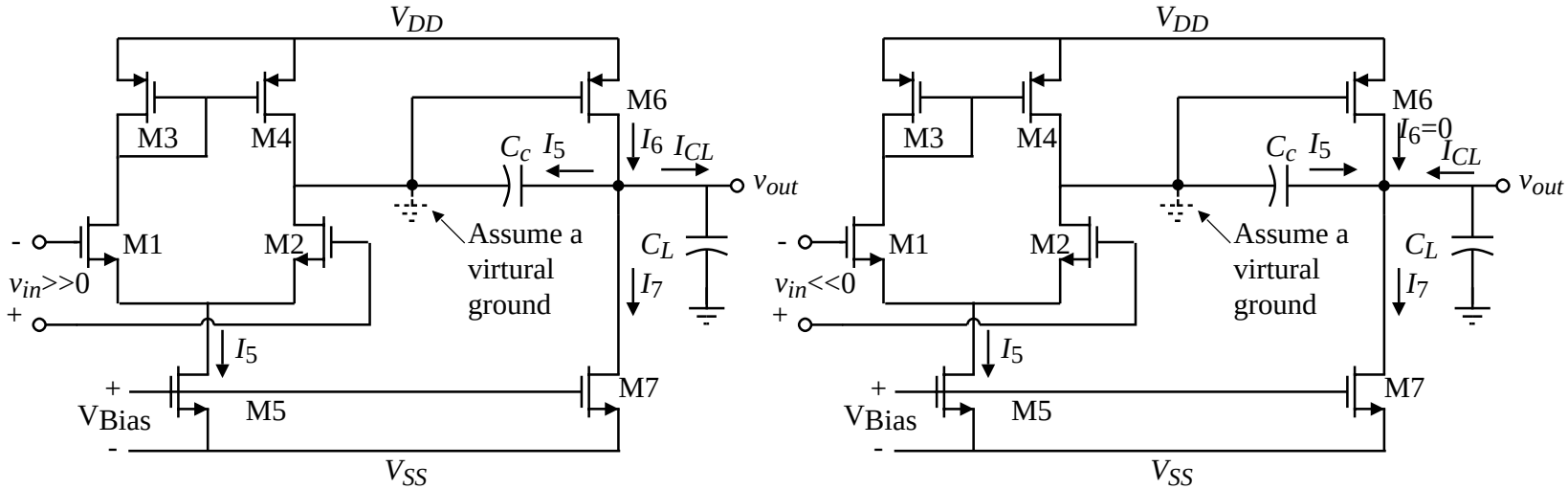


Fig. 6.2-18

$$SR^+ = \min\left[\frac{I_5}{C_c}, \frac{I_6\text{-}I_5\text{-}I_7}{C_L}\right] = \frac{I_5}{C_c} \text{ because } I_6 >> I_5$$

$$SR^- = \min\left[\frac{I_5}{C_c}, \frac{I_7\text{-}I_5}{C_L}\right] = \frac{I_5}{C_c} \text{ if } I_7 >> I_5.$$

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5, then the slew rate of the two-stage op amp should be,

$$SR = \frac{I_5}{C_c}$$

Folded Cascode, CMOS Op Amp

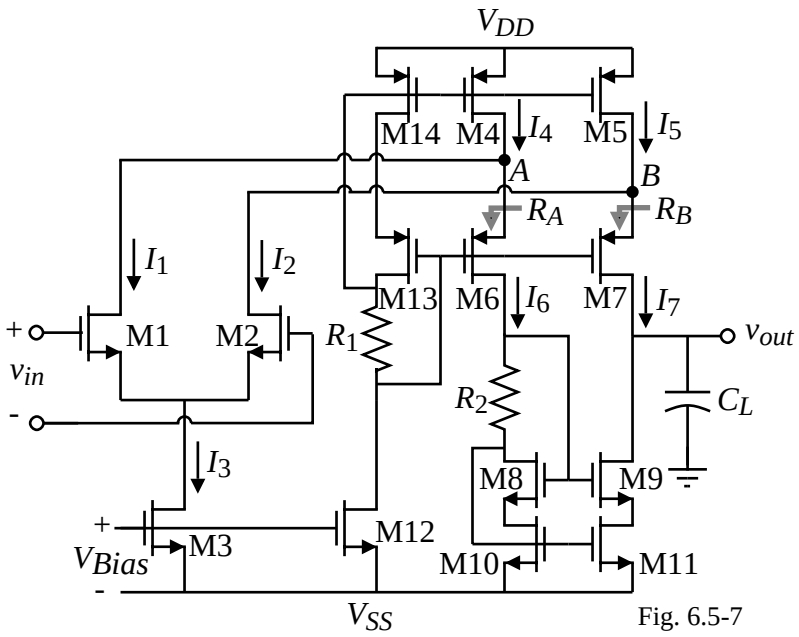


Fig. 6.5-7

Comments:

- The bias currents, I_4 and I_5, should be designed so that I_6 and I_7 never become zero (i.e. I_5=I_6=1.5I_3)
- This amplifier is nearly balanced (would be exactly if R_A was equal to R_B)
- Self compensating
- Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if R_A and R_B are greater than g_{m1} or g_{m2}.

Small-Signal Analysis of the Folded Cascode Op Amp

Model:

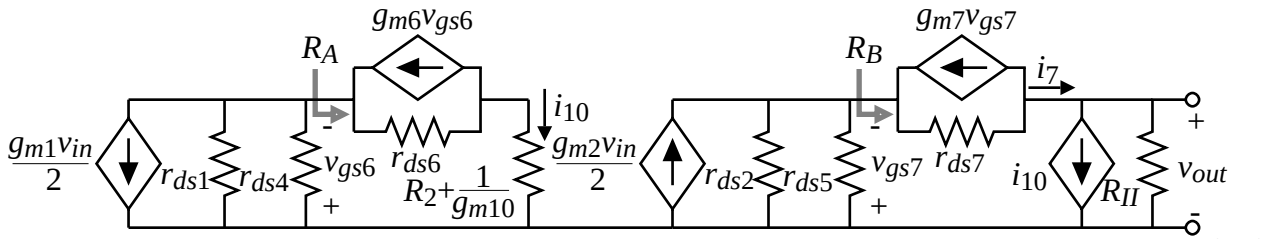


Fig. 6.5-8

Recalling what we learned about the resistance looking into the source of the cascode transistor,

$$R_A = \frac{r_{ds6}+R_2+(1/g_{m10})}{1+g_{m6}r_{gs6}} \spadesuit \frac{1}{g_{m6}} \quad \text{and} \quad R_B = \frac{r_{ds7}+R_{II}}{1+g_{m7}r_{ds7}} \spadesuit \frac{R_{II}}{g_{m7}r_{ds7}} \quad \text{where} \quad R_{II} \approx g_{m9}r_{ds9}r_{ds11}$$

The small-signal voltage transfer function can be found as follows. The current i_{10} is written as

$$i_{10} = \frac{-g_{m1}(r_{ds1}\|r_{ds4})v_{in}}{2[R_A+(r_{ds1}\|r_{ds4})]} \spadesuit \frac{-g_{m1}v_{in}}{2}$$

and the current i_7 can be expressed as

$$i_7 = \frac{g_{m2}(r_{ds2}\|r_{ds5})v_{in}}{2\left[\frac{R_{II}}{g_{m7}r_{ds7}}+(r_{ds2}\|r_{ds5})\right]} = \frac{g_{m2}v_{in}}{2\left(1+\frac{R_{II}(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}}\right)} = \frac{g_{m2}v_{in}}{2(1+k)} \qquad \text{where} \qquad k = \frac{R_{II}(g_{ds2}+g_{ds4})}{g_{m7}r_{ds7}}$$

The output voltage, v_{out}, is equal to the sum of i_7 and i_{10} flowing through R_{out}. Thus,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)g_{mI}R_{out}$$

Frequency Response of the Folded Cascode Op Amp

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

$$p_{out} = \frac{-1}{R_{out}C_{out}}$$

where C_{out} is all the capacitance connected from the output of the op amp to ground.

All other poles must be greater than $GB = g_{m1}/C_{out}$. The approximate expressions for each pole is

1.) Pole at node A: $p_A \spadesuit \frac{-1}{R_A C_A}$

2.) Pole at node B: $p_B \spadesuit \frac{-1}{R_B C_B}$

3.) Pole at drain of M6: $p_6 \spadesuit \frac{-1}{(R_2+1/g_{m10})C_6}$

4.) Pole at source of M8: $p_8 \spadesuit \frac{-g_{m8}}{C_8}$

5.) Pole at source of M9: $p_9 \spadesuit \frac{-g_{m9}}{C_9}$

6.) Pole at gate of M10: $p_{10} \spadesuit \frac{-g_{m10}}{C_{10}}$

where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because R_B is approximately r_{ds} that this pole might be too small. However, at frequencies where this pole has influence, C_{out}, causes R_{out} to be much smaller making p_B also non-dominant.

Folded Cascode, CMOS Op Amp - Example

Assume that all $g_{mN} = g_{mP} = 100\mu S$, $r_{dsN} = 2M\Omega$, $r_{dsP} = 1M\Omega$, and $C_L = 10pF$. Find all of the small-signal performance values for the folded-cascode op amp.

$R_{II} = 0.4G\Omega$, $R_A = 10k\Omega$, and $R_B = 4M\Omega$ $\quad \therefore \quad k = \dfrac{0.4x10^9(0.3x10^{-6})}{100} = 1.2$

$$\frac{v_{out}}{v_{in}} = \left(\frac{2+1.2}{2+2.2}\right)(100)(57.143) = 4{,}354V/V$$

$$R_{out} = R_{II} \| [g_{m7} r_{ds7} (r_{ds5} \| r_{ds2})] = 400M\Omega \| [(100)(0.667M\Omega)] = 57.143M\Omega$$

$$|p_{out}| = \frac{1}{R_{out} C_{out}} = \frac{1}{57.143M\Omega \cdot 10pF} = 1{,}750 \text{ rads/sec.} \Rightarrow \quad 278Hz \quad \Rightarrow \quad GB = 1.21MHz$$

Comments on the Folded Cascode, CMOS Op Amp:

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required

OP AMP DESIGN

Unbuffered, Two-Stage CMOS Op Amp

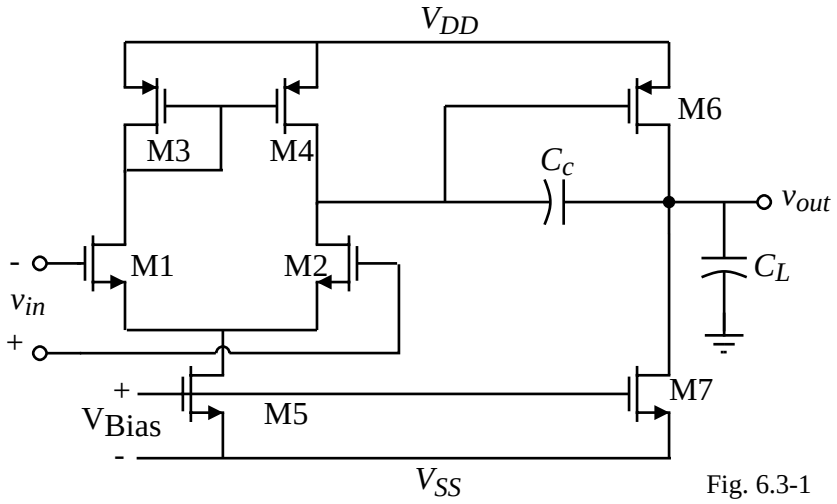


Fig. 6.3-1

Notation:

$$S_i = \frac{W_i}{L_i} = W/L \text{ of the ith transistor}$$

Design Relationships for the Two-Stage Op Amp

Slew rate $SR = \frac{I_5}{C_c}$ (Assuming $I_7 >> I_5$ and $C_L > C_c$)

First-stage gain $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$

Second-stage gain $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$

Gain-bandwidth $GB = \frac{g_{m1}}{C_c}$

Output pole $p_2 = \frac{-g_{m6}}{C_L}$

RHP zero $z_1 = \frac{g_{m6}}{C_c}$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are ≥ $10GB$.

Positive ICMR $V_{\text{in(max)}} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{(\max)} + V_{T1(\min)})$

Negative ICMR $V_{\text{in(min)}} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(\max)} + V_{DS5}(\text{sat})$

Saturation voltage $V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}}$

It is assumed that all transistors are in saturation for the above relationships.

Op Amp Specifications

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, *GB*
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, C_L
6. Slew-rate, *SR*
7. Output voltage swing
8. Power dissipation, P_{diss}

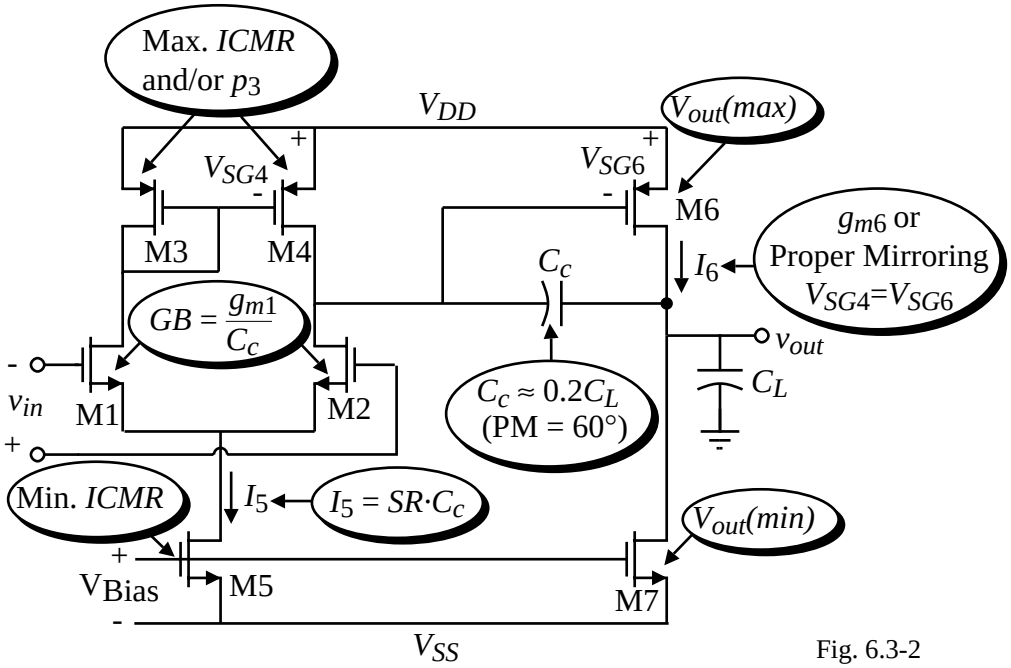


Fig. 6.3-2

Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22C_L$$

2. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

$$I_5 = SR \cdot C_c \qquad \text{or} \qquad I_5 \cong 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

3. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2} \geq 1$$

4. Verify that the pole of M3 due to C_{gs3} and C_{gs4} (=$0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 GB

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

5. Design for S_1 (S_2) to achieve the desired GB.

$$g_{m1} = GB \cdot C_c \Rightarrow S_2 = \frac{g_{m2}}{K'_2 I_5}$$

Unbuffered Op Amp Design Procedure - Continued

6. Design for S_5 from the minimum input voltage. First calculate $V_{DS5}(\text{sat})$ then find S_5.

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100 \text{ mV} \rightarrow \qquad S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$g_{m6} = 2.2g_{m2}(C_L/C_c) \qquad \rightarrow \qquad S_6 = S_4\frac{g_{m6}}{g_{m4}}$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2K'_6S_6}$$

Check to make sure that S_6 satisfies the $V_{out}(\text{max})$ requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$S_7 = (I_6/I_5)S_5$ (Check the minimum output voltage requirements)

10. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)} \qquad P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.

Example 6.3-1 - Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1μm.

$A_V > 3000$V/V $V_{DD} = 2.5$V $V_{SS} = -2.5$V 60° phase margin
$GB = 5$MHz $C_L = 10$pF $SR > 10$V/μs
V_{out} range = ±2V $ICMR = -1$ to 2V $P_{diss} \leq 2$mW

Solution

1.) The first step is to calculate the minimum value of the compensation capacitor C_c, which is

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

2.) Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3\text{x}10^{-12})(10 \times 10^6) = 30\ \mu\text{A}$$

3.) Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30 \times 10^{-6}}{(50\text{x}10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 3 \qquad \rightarrow \qquad \boxed{(W/L)_3 = (W/\text{L})_4 = 3}$$

4.) Now we can check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 0.4$fF/μm^2. The mirror pole can be found as

$$p_3 \spadesuit \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = 6.79\text{x}10^9(\text{rads/sec})$$

or 1.08 GHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

Example 6.3-1 - Continued

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5\text{x}10^{6})(2\pi)(3\text{x}10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}{}^2}{2K'_N I_1} = \frac{(94.25)^2}{2\cdot 110\cdot 15} = 2.79 \approx 3.0 \Rightarrow \qquad \boxed{(W/L)_1 = (W/L)_2 = 3}$$

6.) Next calculate V_{DS5},

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30\text{x}10^{-6}}{110\text{x}10^{-6}\cdot 3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30\times 10\text{-}6)}{(110\times 10\text{-}6)(0.35)^2} = 4.49 \approx 4.5 \qquad \rightarrow \qquad \boxed{(W/L)_5 = 4.5}$$

7.) For 60° phase margin, we know that

$$g_{m6} \geq 10 g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu\text{S}$ and knowing that $g_{m4} = 67\mu\text{S}$, we calculate $(W/L)_6$ as

$$(W/L)_6 = 3\,\frac{942.5\times 10\text{-}6}{(67\times 10\text{-}6)} = 42.2 \approx 40$$

Example 6.3-1 - Continued

8.) Calculate I_6 using the small-signal g_m expression: $I_6 = \frac{(942.5 \times 10\text{-}6)^2}{(2)(50 \times 10\text{-}6)(42)} = 211.5\mu A \approx 212\mu A$

If we calculate $(W/L)_6$ based on V_{out}(max), the value is approximately 38. Since 42 exceeds the specification and maintains better phase margin, we will stay with $(W/L)_6 = 42$ and $I_6 = 212\mu A$.

With $I_6 = 212\mu A$ the power dissipation is

$$P_{diss} = 5V \cdot (30\mu A + 212\mu A) = 1.21mW.$$

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5\left(\frac{234 \times 10\text{-}6}{30 \times 10\text{-}6}\right) = 35.1 \approx 35 \quad \rightarrow \quad \boxed{(W/L)_7 = 35}$$

Let us check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{out}(\text{min}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2 \cdot 234}{110 \cdot 35}} = 0.349V$$

which is less than required. At this point, the first-cut design is complete.

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(92.45 \times 10\text{-}6)(942.5 \times 10\text{-}6)}{15 \times 10\text{-}6(.04 + .05)212 \times 10\text{-}6(.04 + .05)} = 3{,}383V/V$$

which barely meets specifications. We might want to consider decreasing the output current back to 190μA to increase the second-stage gain by a factor of 1.1 or better yet, increase the channel length to 2μm causing a gain increase of 20.

Incorporating the Nulling Resistor into the Miller Compensated Two-Stage Op Amp

Circuit:

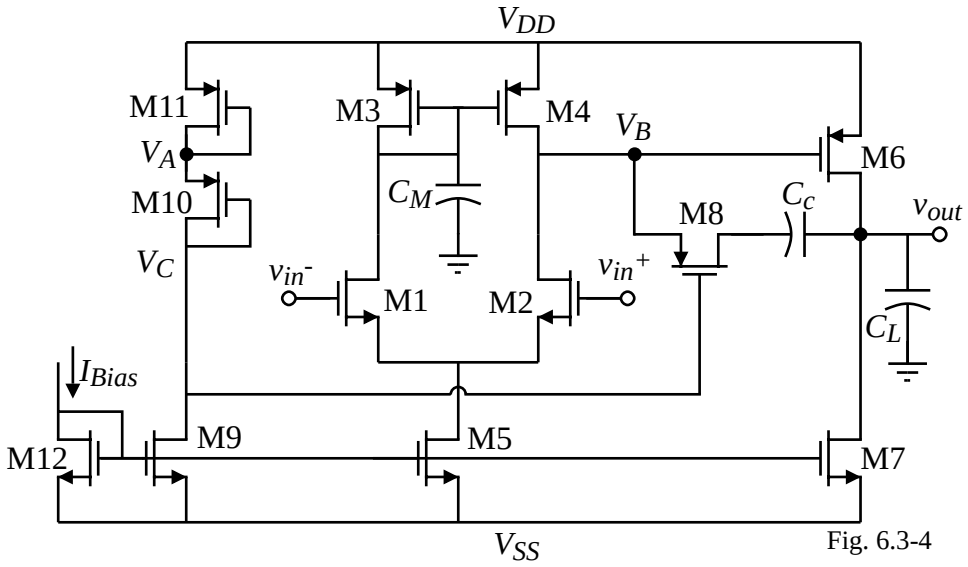


Fig. 6.3-4

We saw earlier that the roots were:

$$p_1 = -\frac{g_{m2}}{A_v C_c} = -\frac{g_{m1}}{A_v C_c} \qquad p_2 = -\frac{g_{m6}}{C_L}$$

$$p_3 = -\frac{1}{R_z C_I} \qquad z_1 = \frac{-1}{R_z C_c - C_c/g_{m6}}$$

where $A_v = g_{m1} g_{m6} R_I R_{II}$. (Note that p_3 is the pole resulting from the nulling resistor compensation technique.)

Design of the Nulling Resistor (M8)

In order to place the zero on top of the second pole (p_2), the following relationship must hold

$$R_z = \frac{1}{g_{m6}}\left(\frac{C_L + C_c}{C_c}\right) = \left(\frac{C_c + C_L}{C_c}\right)\frac{1}{\sqrt{2K'_P S_6 I_6}}$$

The resistor, R_z, is realized by the transistor M8 which is operating in the active region because the dc current through it is zero. Therefore, R_z, can be written as

$$R_z = \frac{v_{DS8}}{i_{D8}}\underset{V_{DS8}=0}{\subseteq} = \frac{1}{K'_P S_8 (V_{SG8} - |V_{TP}|)}$$

The bias circuit is designed so that voltage V_A is equal to V_B.

$$\therefore \quad |V_{GS10}| - |V_T| = |V_{GS8}| - |V_T| \quad \Rightarrow \quad V_{SG11} = V_{SG6} \quad \Rightarrow \quad \left(\frac{W_{11}}{L_{11}}\right) = \left(\frac{I_{10}}{I_6}\right)\left(\frac{W_6}{L_6}\right)$$

In the saturation region

$$|V_{GS10}| - |V_T| = \sqrt{\frac{2(I_{10})}{K'_P(W_{10}/L_{10})}} = |V_{GS8}| - |V_T|$$

$$\therefore \quad R_z = \frac{1}{K'_P S_8}\sqrt{\frac{K'_P S_{10}}{2I_{10}}} = \frac{1}{S_8}\sqrt{\frac{S_{10}}{2K'_P I_{10}}}$$

Equating the two expressions for R_z gives

$$\left(\frac{W_8}{L_8}\right) = \left(\frac{C_c}{C_L + C_c}\right)\sqrt{\frac{S_{10} S_6 I_6}{I_{10}}}$$

Example 6.3-2 - RHP Zero Compensation

Use results of Ex. 6.3-1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2. Use device data given in Ex. 6.3-1.

Solution

The task at hand is the design of transistors M8, M9, M10, M11, and bias current I_{10}. The first step in this design is to establish the bias components. In order to set V_A equal to V_B, then V_{SG10} must equal V_{SG6}. Therefore,

$$S_{11} = (I_{11}/I_6)S_6$$

Choose $I_{11} = I_{10} = I_9 = 30\mu A$ which gives $S_{11} = (30A/212\mu A)42 = 5.94 \approx 6$.

$$W_{11} = 6\mu m$$

The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of V_{SG11}, V_{SG10}, and V_{DS9}. The ratio of I_{10}/I_5 determines the (W/L) of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (30/30)(4.5) = 4.5$$

$$W_9 = 4.5\mu m$$

Now $(W/L)_8$ is determined to be

$$(W/L)_8 = \left(\frac{3pF}{3pF+10pF}\right)\sqrt{\frac{1\cdot 42\cdot 212\mu A}{30\mu A}} = 3.98$$

$$W_8 = 3.98\mu m \approx 4\mu m$$

Example 6.3-2 - Continued

It is worthwhile to check that the RHP zero has been moved on top of p_2. To do this, first calculate the value of R_z. V_{SG8} must first be determined. It is equal to V_{SG10}, which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K'_P S_{10}}} + |V_{TP}| = \sqrt{\frac{2 \cdot 30}{50 \cdot 1}} + 0.7 = 1.795\text{V}$$

Next determine R_z.

$$R_z = \frac{1}{K'_P S_8 (V_{SG10} - |V_{TP}|)} = \frac{10^6}{50 \cdot 3.97(1.795 - .7)} = 4.601\text{k}\Omega$$

The location of z_1 is calculated as

$$z_1 = \frac{-1}{(4.601 \times 10^3)(3\text{x}10^{-12}) - \frac{3\text{x}10^{-12}}{942.5\text{x}10^{-6}}} = -94.16\text{x}10^6 \text{ rads/sec}$$

The output pole, p_2, is

$$p_2 = \frac{942.5\text{x}10^{-6}}{10\text{x}10^{-12}} = -94.25\text{x}10^6 \text{ rads/sec}$$

Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below.

$W_8 = 4\mu\text{m}$ $W_9 = 4.5\mu\text{m}$ $W_{10} = 1\mu\text{m}$ $W_{11} = 6\mu\text{m}$

An Alternate Form of Nulling Resistor

To cancel p_2,

$$z_1 = p_2 \rightarrow \quad R_z = \frac{C_c + C_L}{g_{m6A} C_C} = \frac{1}{g_{m6B}}$$

Which gives

$$g_{m6B} = g_{m6A}\left(\frac{C_c}{C_c + C_L}\right)$$

In the previous example,

$g_{m6A} = 942.5\mu S$, $C_c = 3pF$ and $C_L = 10pF$.

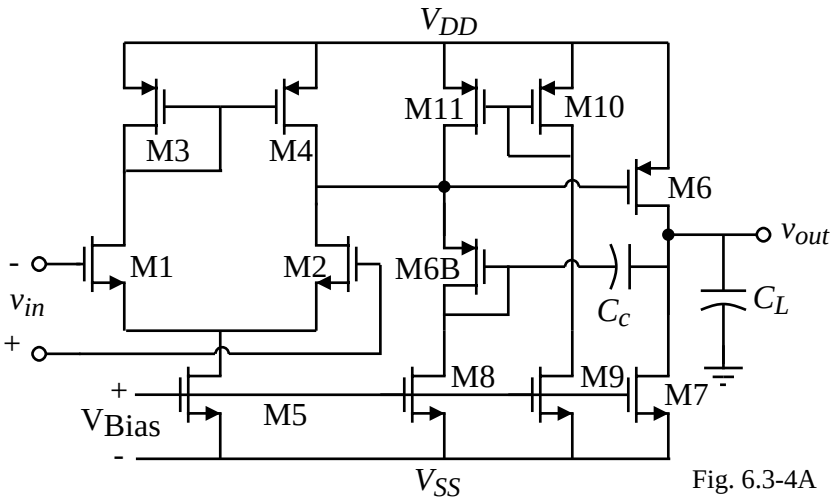


Fig. 6.3-4A

Choose $I_{6B} = 10\mu A$ to get

$$g_{m6B} = \frac{g_{m6A} C_c}{C_c + C_L} \rightarrow \sqrt{\frac{2K_P W_{6B} I_{6B}}{L_{6B}}} = \left(\frac{C_c}{C_c + C_L}\right)\sqrt{\frac{2K_P W_{6A} I_{D6}}{L_{6A}}}$$

or

$$\frac{W_{6B}}{L_{6B}} = \left(\frac{3}{13}\right)^2 \frac{I_{6A}}{I_{6B}} \frac{W_{6A}}{L_{6A}} = \left(\frac{3}{13}\right)^2 \left(\frac{234}{10}\right)(23) = 28.7 \rightarrow W_{6B} = 29\mu m$$

Implementation of C_c using a MOS Transistor

Two Approaches:

1.) Have to keep $V_{GS} \geq V_T$

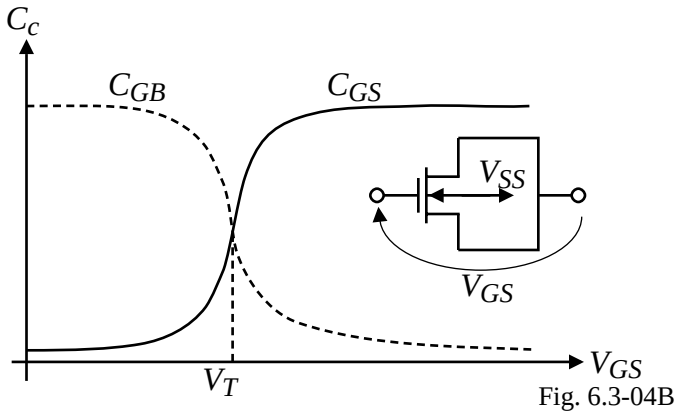


Fig. 6.3-04B

2.) Better - V_{GS} not restricted

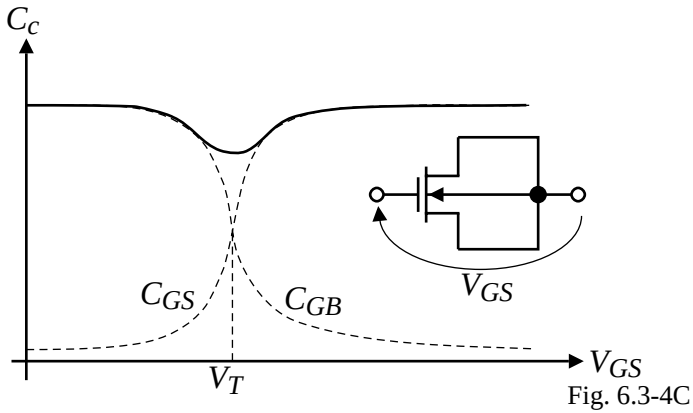


Fig. 6.3-4C

Programmability of the Two-Stage Op Amp

The following relationships depend on the bias current, I_{bias}, in the following manner and allow for programmability after fabrication.

$$A_v(0) = g_{mI}g_{mII}R_IR_{II} \propto \frac{1}{I_{Bias}}$$

$$GB = \frac{g_{mI}}{C_c} \propto \sqrt{I_{Bias}}$$

$$P_{diss} = (V_{DD}+|V_{SS}|)(1+K_1+K_2)I_{Bias} \quad \propto I_{bias}$$

$$SR = \frac{K_1 I_{Bias}}{C_c} \propto I_{Bias}$$

$$R_{out} = \frac{1}{2\lambda K_2 I_{Bias}} \propto \frac{1}{I_{Bias}}$$

$$|p_1| = \frac{1}{g_{mII}R_IR_{II}C_c} \propto \frac{I_{Bias}^2}{\sqrt{I_{Bias}}} \propto I_{Bias}^{1.5}$$

$$|z| = \frac{g_{mII}}{C_c} \propto \sqrt{I_{Bias}}$$

Illustration of the I_{bias} dependence →

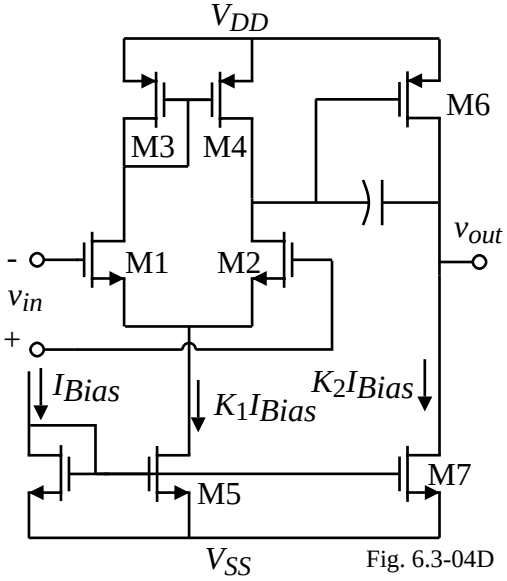


Fig. 6.3-04D

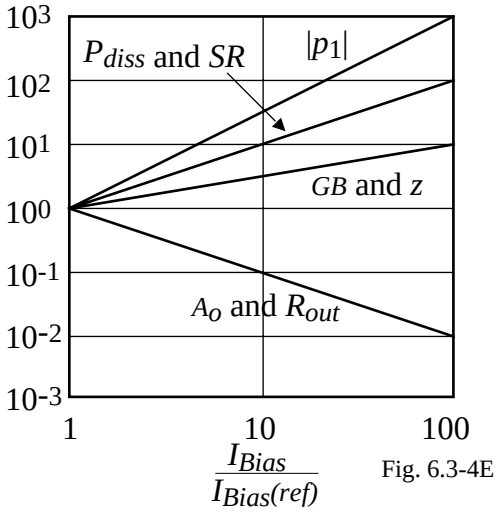


Fig. 6.3-4E

Simulation of the Electrical Design

Area of source or drain = AS = AD = W[L1 + L2 + L3]

where

L1 = Minimum allowable distance between the contact in the S/D and the polysilicon (5μm)

L2 = Width of a minimum size contact (5μm)

L3 = Minimum allowable distance from the contact in S/D to the edge of the S/D (5μm)

∴ AS = AD = Wx15μm

Perimeter of the source or drain = PD = PS = 2W + 2(L1+L2+L3)

∴ PD = PS = 2W + 30μm

Illustration:

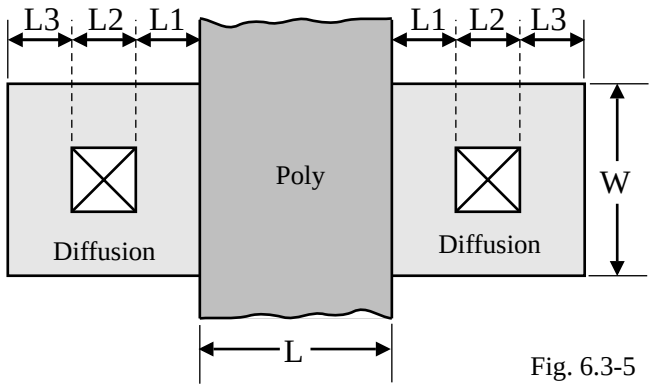


Fig. 6.3-5

Reduction of Parasitics

The major objective of good layout is to minimize the parasitics that influence the design.

Typical parasitics include:

Capacitors to ac ground

Series resistance

Capacitive parasitics is minimized by minimizing area and maximizing the distance between the conductor and ac ground.

Resistance parasitics are minimized by using wide busses and keeping the bus length short.

For example:

At 2mΩ/square, a metal run of 1000μm and 2μm wide will have 1Ω of resistance.

At 1 mA this amounts to a 1 mV drop which could easily be greater than the least significant bit of an analog-digital converter. (For example, a 10 bit ADC with V_{REF} = 1V has an LSB of 1mV)

SUMMARY

Introduction and Characterization

- Ideal op amp, virtual ground at input when gain approaches infinity
- Characteristics are static and dynamic and time-independent and time-dependent

Op Amp Architectures

- Two stage
- Folded
- Many others

Compensation

- Designed so that the op amp with unity gain feedback (buffer) is stable
- Types
  - Miller
  - Miller with nulling resistors
  - Self Compensating
  - Feedforward

Simple Op Amps

- CMOS - two-stage and folded cascode
- BJT - two-stage and folded cascode

Op Amp Design

- CMOS only